VLSI LAB Digital Assignment 1

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School of Electrical Engineering

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Course: **EEE-4028**

Course Name: **VLSI Lab**

Lab Slot: **L43 + L44**

This work is submitted in partial fulfilment of the requirement of the award of the degree of Bachelor of Technology in EEE

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4-BIT RIPPLE CARRY ADDER

Objectives

1. To provide students with the background needed to design, develop, and test digital arithmetic circuits using IEEE standard Verilog HDL.
2. To provide an understanding complex arithmetic circuit design principles and its architecture design.

Outcomes

1. After completion of this course the students will be familiar with design and implementation of Digital Arithmetic building blocks using Verilog HDL and Modelsim Software.

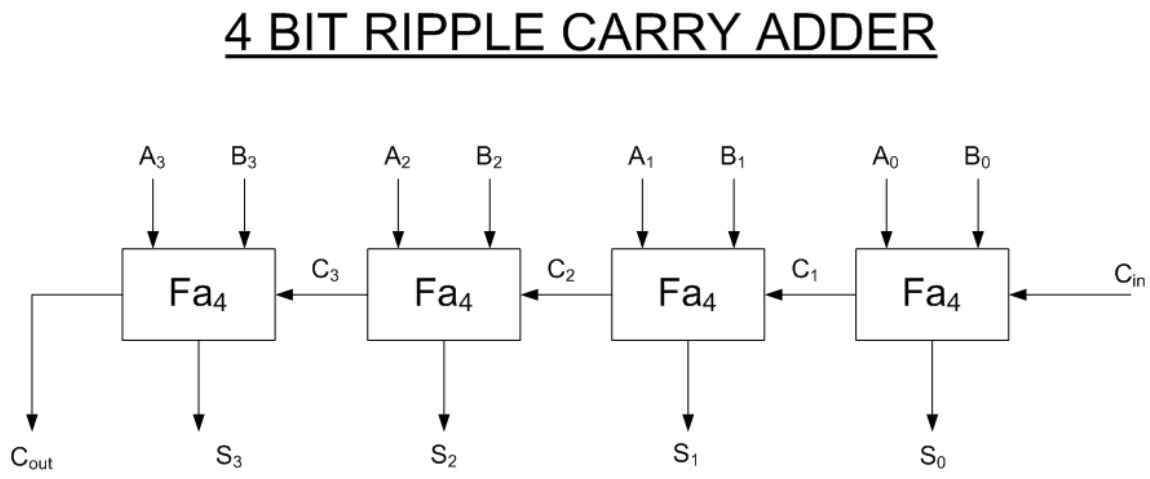
AIM

1. Design a 4 bit ripple carry adder using four full adder circuit.

REQUIRED SOFTWARE

1. Model sim software for simulation
2. Microsoft Visio for making flowchart
3. Documentation to be done using LaTeX

CIRCUIT DIAGRAM



Design Code

1. **Verilog Module** — rippleAdder.v

```
//Ripple Carry Adder
module rca_4bit_19BEE0167(input [3:0]a,b, input cin, output [4:0]sum);
wire w1,w2,w3;
fa_df fa1(a[0],b[0],cin,sum[0],w1);
fa_df fa2(a[1],b[1],w1,sum[1],w2);
fa_df fa3(a[2],b[2],w2,sum[2],w3);
fa_df fa4(a[3],b[3],w3,sum[3],sum[4]);
endmodule
```

2. **Fulladder.v**

```
//Full adder using Dataflow
module fa_df(input a,b,cin, output sum,cout);
assign sum = a^b^cin;
assign cout = (a&b) | cin&(a^b);
endmodule
```

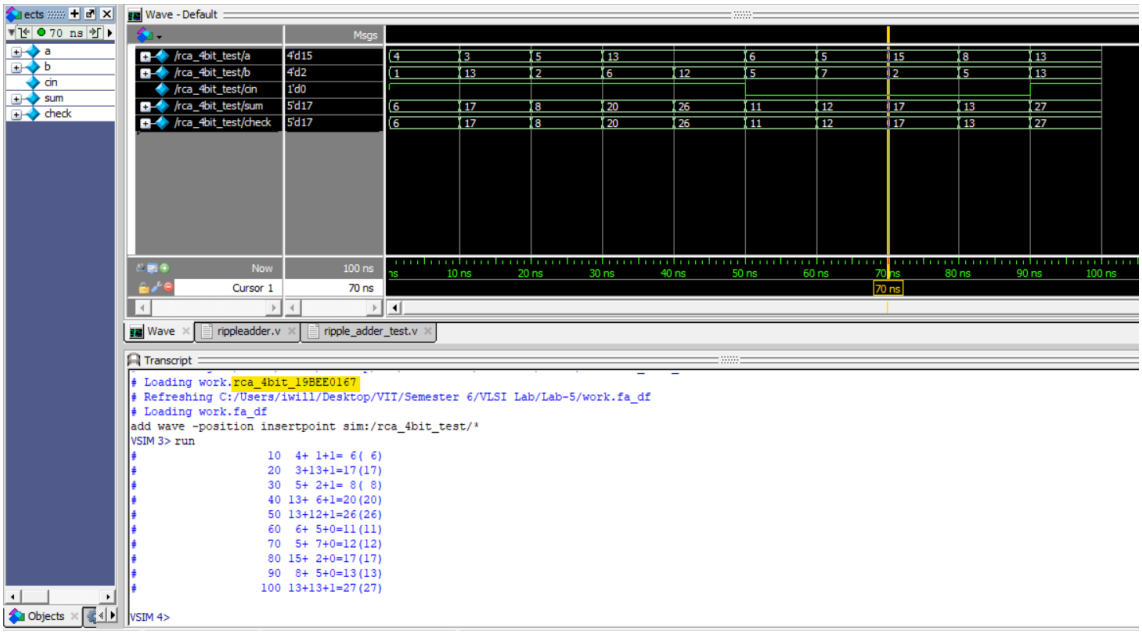
3. **Test Fixture** — rippleAdderTest.v

```
//Creating the testbench
module rca_4bit_test();
reg [3:0]a,b;
reg cin;
wire[4:0]sum;
reg[4:0]check;

rca_4bit_19BEE0167 UUT(a,b,cin,sum);

initial repeat(10) begin
a= $random;
b= $random;
cin= $random;
check = a+b+cin;
#10
$display($time, " %d+%d+%d=%d(%d)",a,b,cin,sum,check);
end
endmodule
```

4. **Output**



5. **Console Output**

```
#                  10  4+ 1+1= 6( 6)
#                  20  3+13+1=17(17)
#                  30  5+ 2+1= 8( 8)
#                  40 13+ 6+1=20(20)
#                  50 13+12+1=26(26)
#                  60  6+ 5+0=11(11)
#                  70  5+ 7+0=12(12)
#                  80 15+ 2+0=17(17)
#                  90  8+ 5+0=13(13)
#                 100 13+13+1=27(27)
```

Result

1. Successfully the 4-bit ripple carry adder has been designed and the output was verified.

Inference

1. In this experiment learnt about how to construct multiple-bit adders.