VLSI LAB Digital Assignment 9

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School of Electrical Engineering

Faculty: **Professor Balamurugan S**

Course: **EEE-4028**

Course Name: **VLSI Lab**

Lab Slot: **L43 + L44**

This work is submitted in partial fulfilment of the requirement of the award of the degree of Bachelor of Technology in EEE

April 21, 2022

FIR FILTER

Objectives

1. To provide students with the background needed to design, develop, and test digital arithmetic circuits using IEEE standard Verilog HDL.
2. To provide an understanding complex arithmetic circuit design principles and its architecture design.

Outcomes

1. After completion of this course the students will be familiar with design and implementation of Digital Arithmetic building blocks using Verilog HDL and Modelsim Software.

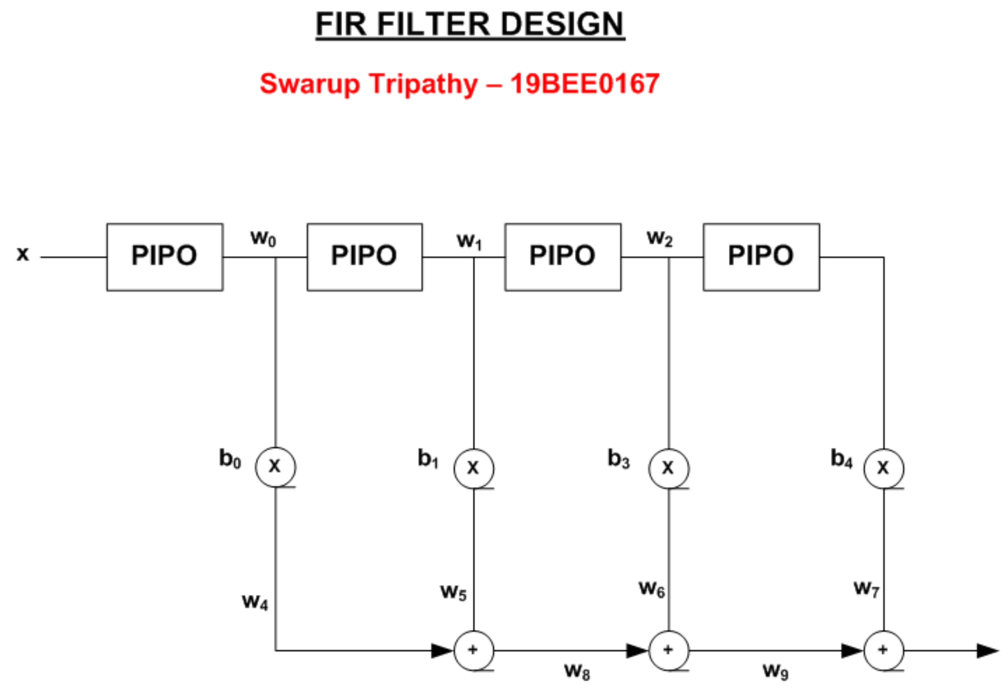
AIM

1. Design a FIR Filter.

REQUIRED SOFTWARE

1. Model sim software for simulation
2. Microsoft Visio for making flowchart
3. Documentation to be done using LaTeX

CIRCUIT DIAGRAM



Design Code

1. **Verilog Module** — designcode.v

```
module fir_filter(input[3:0]x,input clk,rst,
output[9:0]y);
wire[3:0]w1,w2,w3;
wire[7:0]w4,w5,w6;
wire[9:0]w8,w9;

parameter b0=4'b0000;
parameter b1=4'b0010;
parameter b2=4'b0011;
parameter b3=4'b0100;

assign w4=w0*b0;
assign w5=w1*b1;
assign w6=w2*b2;
assign w7=w3*b3;
assign w8=w4+b5;
assign w9=w6*b8;

pipo4bit p1(x,clk,rst,w1);
```

```
pipo4bit p2(x,clk,rst,w2);
pipo4bit p3(x,clk,rst,w3);
pipo4bit p4(x,clk,rst,w4);

assign y=w7+w9;
endmodule
```

2. **pipo4bit.v**

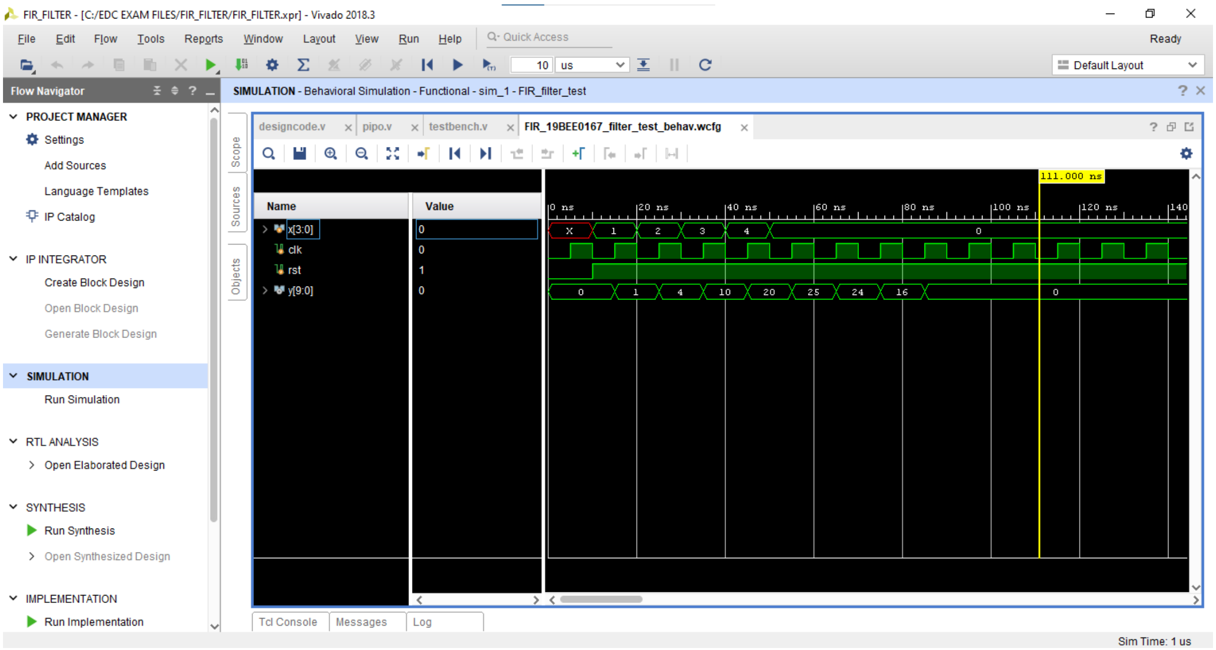
```
module pipo_4b(input clk, rst, input[3:0]d, output reg[3:0]q);
always@(posedge clk, negedge rst)
begin
if(!rst)
q<=’b0;
else
q<=d;
end
endmodule
```

3. **Test Fixture** — Test.v

```
module fir_filter_test;
reg[3:0]x;
reg clk,rst;
wire[9:0]y;

FIR_filter(.x(x),.clk(clk),.rst(rst),.y(y));

initial begin
    rst=1’b0;
    clk=1’b0;

#5
    rst=1’b1;
    clk=1’b0;
#10
    x=4’b0011;
#10
    x=4’b0100;
#10
    x=4’b0000;
#10
    end
    always #5 clk=~clk;
```

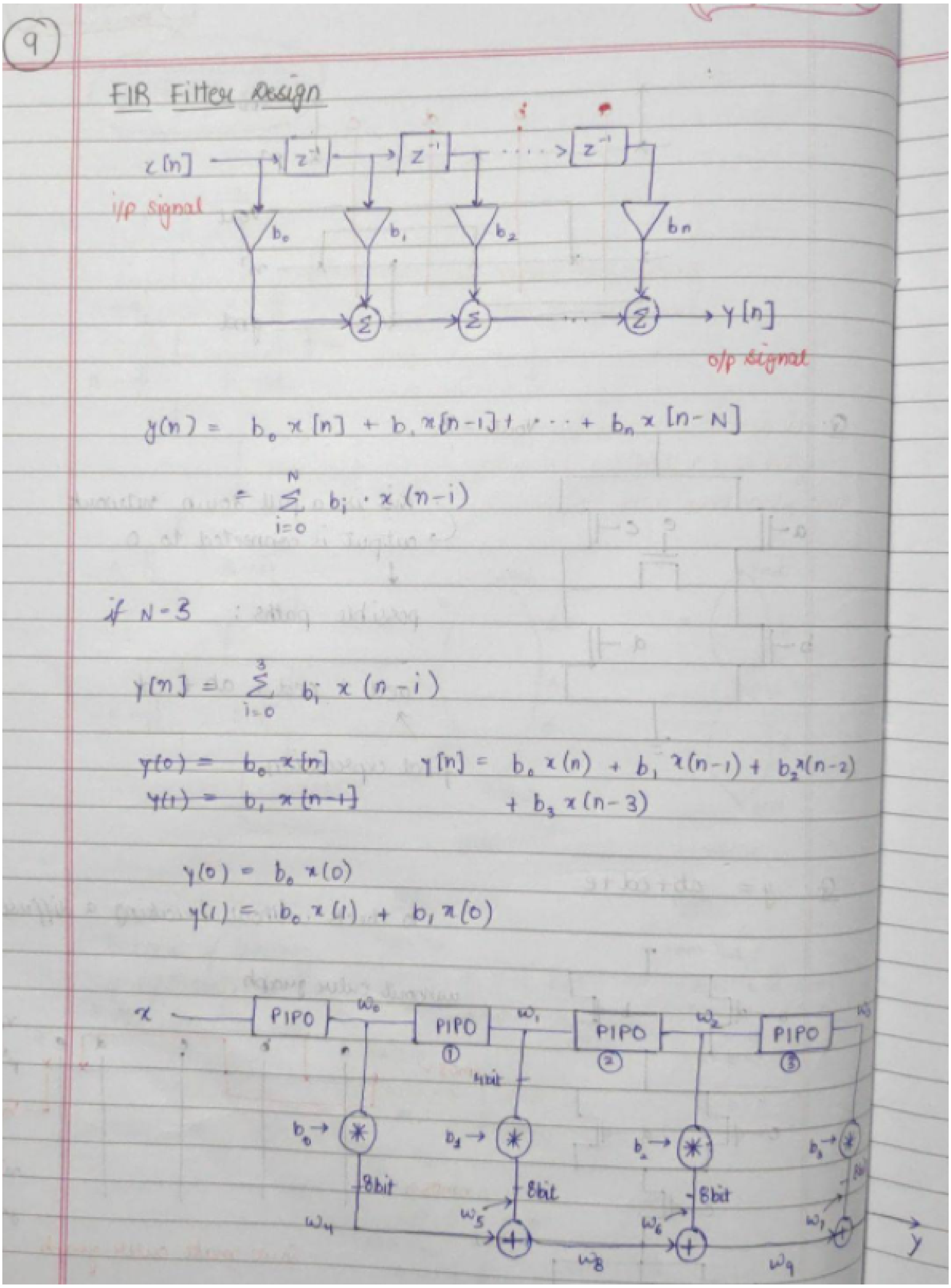
```
endmodule
```

4. **Output**



Result

1. Successfully the FIR filter has been designed and the output was verified.



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FIR Filter Design

x[n]
i/p signal
z^{-1}
z^{-1}
z^{-1}
b_0
b_1
b_2
b_n
Σ
Σ
Σ
y[n]
o/p signal

$$y(n) = b_0 x[n] + b_1 x[n-1] + \cdots + b_n x[n-N]$$

$$= \sum_{i=0}^{N} b_i \cdot x(n-i)$$

if N = 3

$$y[n] = \sum_{i=0}^{3} b_i \, x(n-i)$$

~~$y(0) = b_0 x[n]$~~

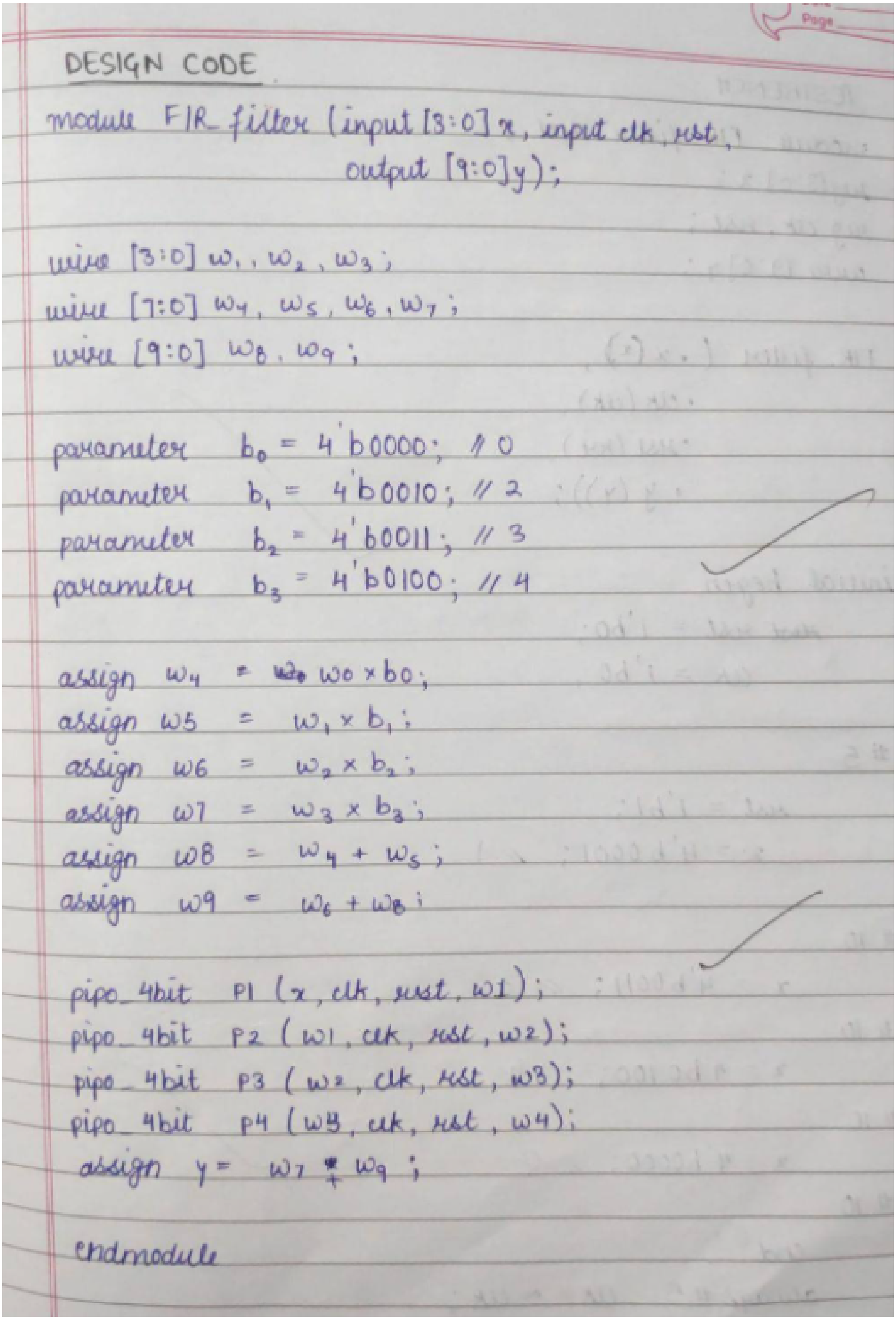
~~$y(1) = b_1 x[n-1]$~~

$$y[n] = b_0 x(n) + b_1 x(n-1) + b_2 x(n-2) + b_3 x(n-3)$$

$$y(0) = b_0 x(0)$$

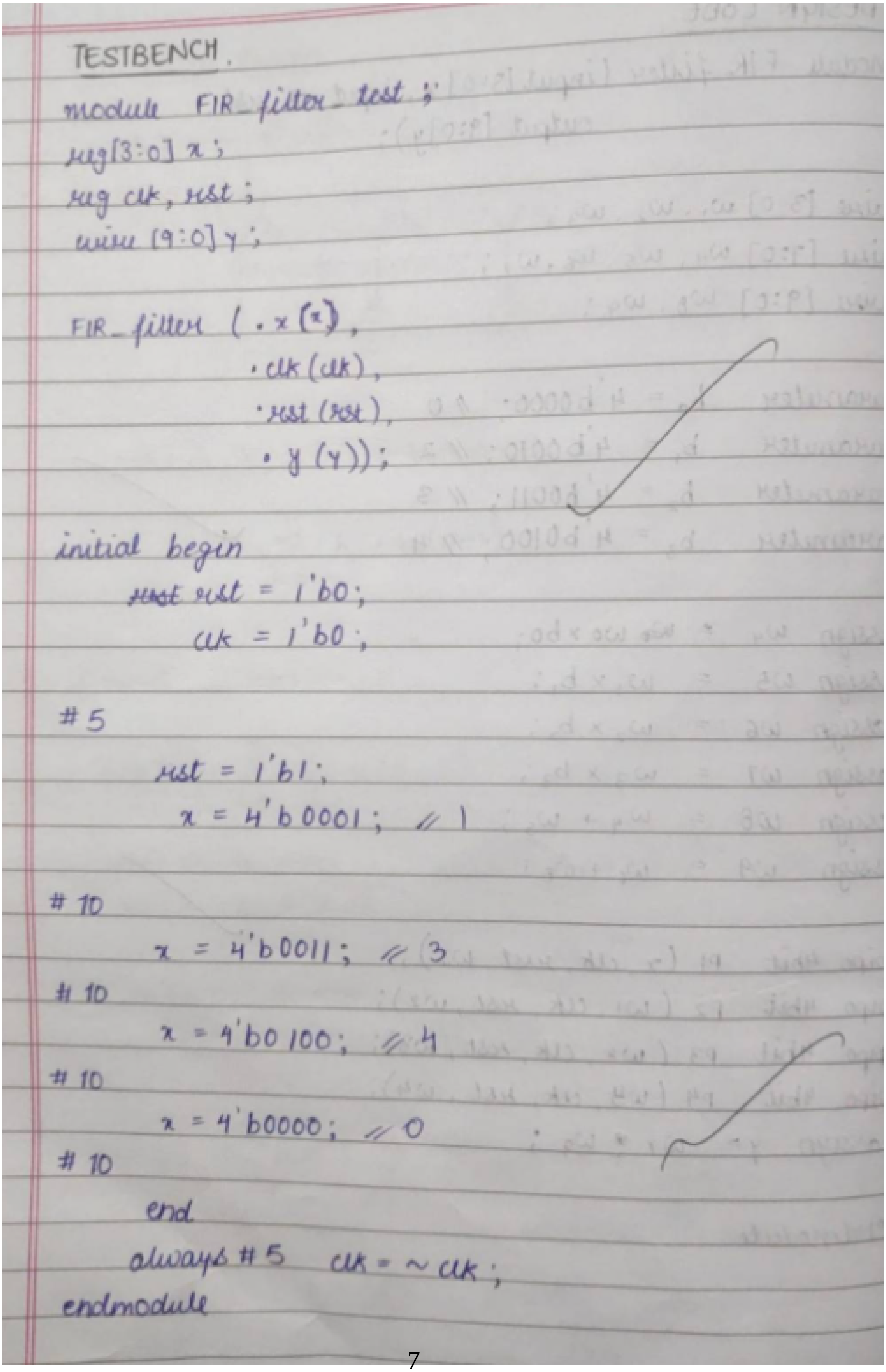
$$y(1) = b_0 x(1) + b_1 x(0)$$

x
PIPO
w_0
PIPO ①
w_1
PIPO ②
w_2
PIPO ③
w_3
4bit
b_0 →
b_1 →
b_2 →
b_3 →
✱
8bit
8bit
8bit
8bit
w_4
w_5
w_6
w_7
⊕
w_8
w_9
y



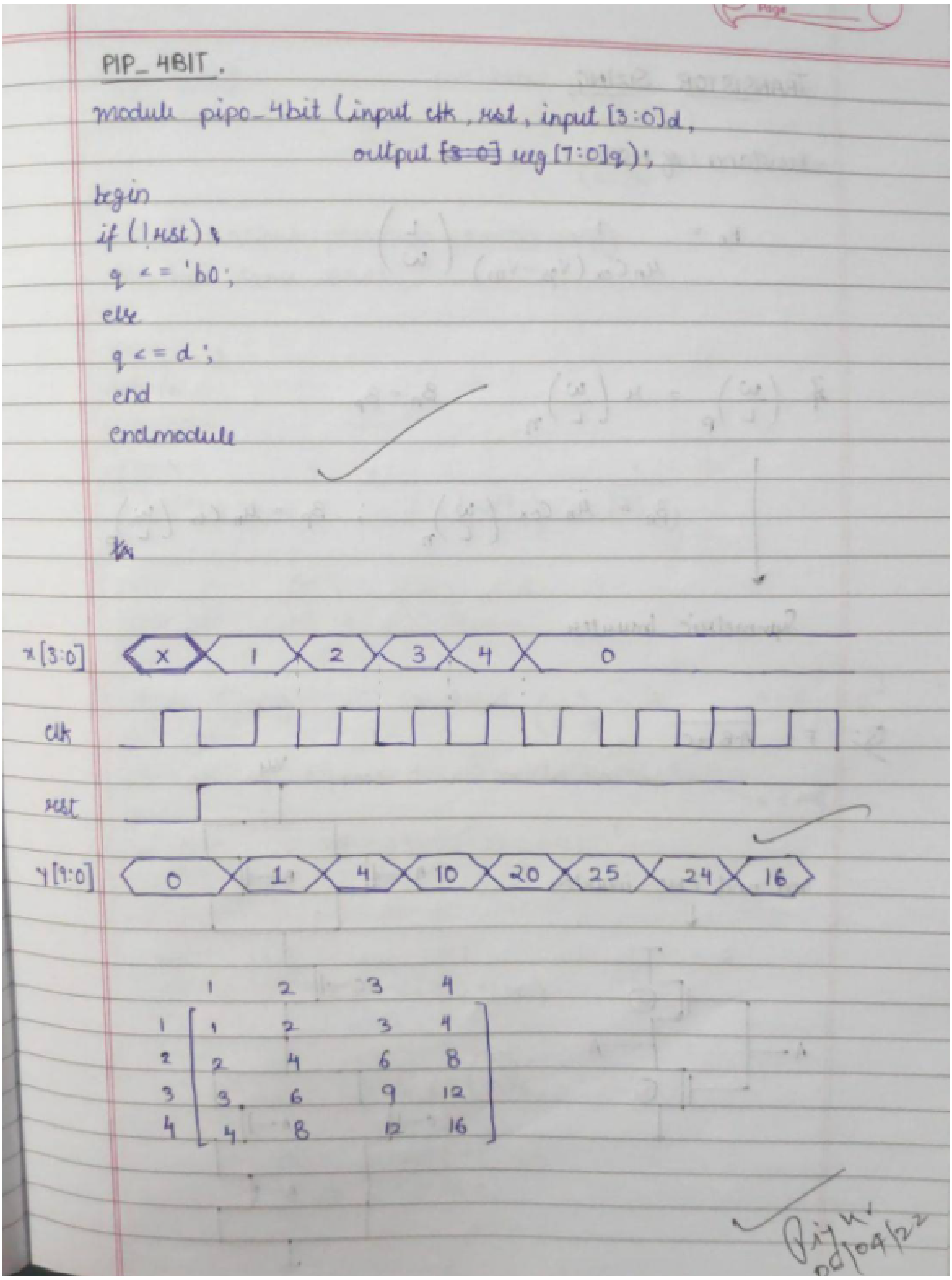
DESIGN CODE

```
module FIR_filter (input [3:0] x, input clk, rst,
                   output [9:0]y);

wire [3:0] w1, w2, w3;
wire [7:0] w4, w5, w6, w7;
wire [9:0] w8, w9;

parameter  b0 = 4'b0000; // 0
parameter  b1 = 4'b0010; // 2
parameter  b2 = 4'b0011; // 3
parameter  b3 = 4'b0100; // 4

assign w4  =  w0 x b0;
assign w5  =  w1 x b1;
assign w6  =  w2 x b2;
assign w7  =  w3 x b3;
assign w8  =  w4 + w5;
assign w9  =  w6 + w8;

pipo_4bit  P1 (x, clk, rst, w1);
pipo_4bit  P2 (w1, clk, rst, w2);
pipo_4bit  P3 (w2, clk, rst, w3);
pipo_4bit  P4 (w3, clk, rst, w4);
assign y =  w7 + w9 ;

endmodule
```



TESTBENCH.

```
module FIR_filter_test ;
reg[3:0] x ;
reg clk, rst ;
 wire [9:0] y ;

FIR_filter ( .x(x),
             .clk(clk),
             .rst(rst),
             .y(y));

initial begin
      ~~rst~~ rst = 1'b0;
           clk = 1'b0;

#5

       rst = 1'b1;
        x = 4'b0001; // 1

#10
       x = 4'b0011; // 3
#10
       x = 4'b0100; // 4
#10
       x = 4'b0000; // 0
#10
      end
    always #5  clk = ~clk;
endmodule
```



PIP_4BIT.

```
module pipo-4bit (input clk , rst , input [3:0]d ,
                  output ~~[3:0]~~ reg [7:0]q);
begin
if (!rst) ;
 q <= 'b0;
else
 q <= d ;
 end
 endmodule
```

~~ta~~

x[3:0]
x
1
2
3
4
0
clk
rst
y[9:0]
0
1
4
10
20
25
24
16

$$
\begin{array}{c|cccc}
 & 1 & 2 & 3 & 4 \\
\hline
1 & 1 & 2 & 3 & 4 \\
2 & 2 & 4 & 6 & 8 \\
3 & 3 & 6 & 9 & 12 \\
4 & 4 & 8 & 12 & 16
\end{array}
$$

Piyu
20/04/22

Inference

1. In this experiment learnt about how to construct FIR filter.