VLSI LAB Digital Assignment 10

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School of Electrical Engineering

Faculty: **Professor Balamurugan S**

Course: **EEE-4028**

Course Name: **VLSI Lab**

Lab Slot: **L43 + L44**

This work is submitted in partial fulfilment of the requirement of the award of the degree of Bachelor of Technology in EEE

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DCT DESIGN

Objectives

1. To provide students with the background needed to design, develop, and test digital arithmetic circuits using IEEE standard Verilog HDL.
2. To provide an understanding complex arithmetic circuit design principles and its architecture design.

Outcomes

1. After completion of this course the students will be familiar with design and implementation of Digital Arithmetic building blocks using Verilog HDL and Modelsim Software.

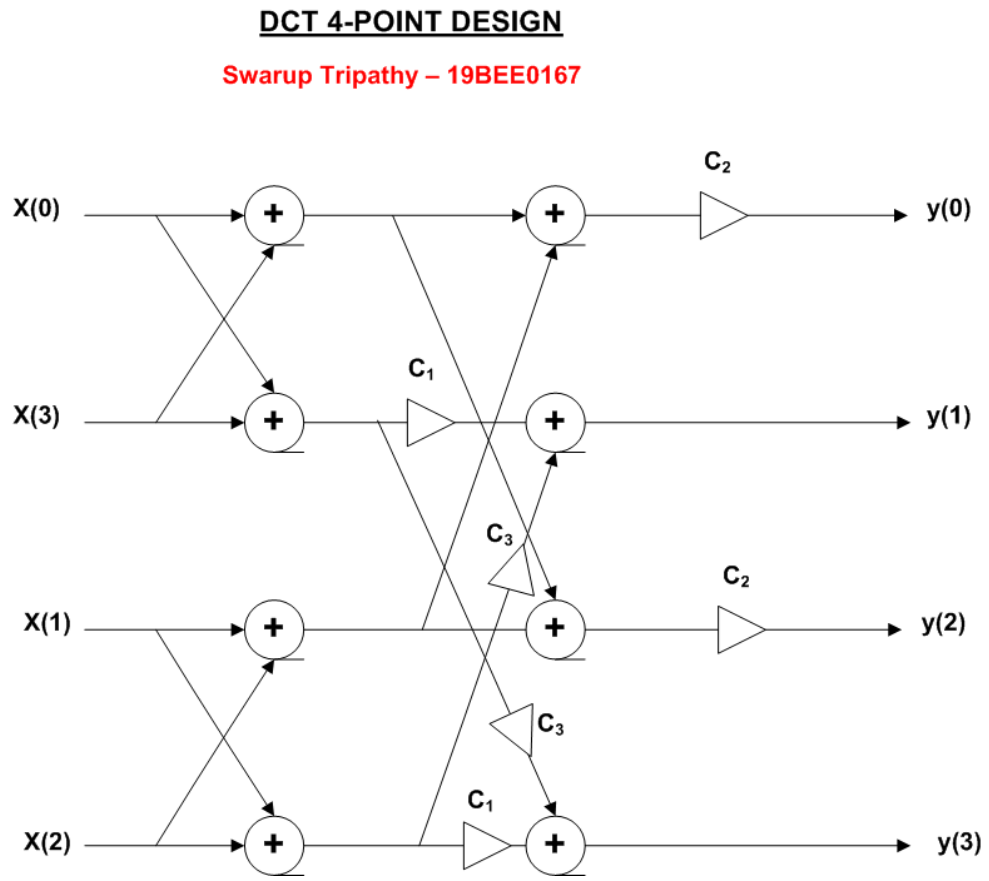
AIM

1. To design a DCT.

REQUIRED SOFTWARE

1. Model sim software for simulation
2. Microsoft Visio for making flowchart
3. Documentation to be done using LaTeX

CIRCUIT DIAGRAM



Design Code

1. **Verilog Module** — designcode.v

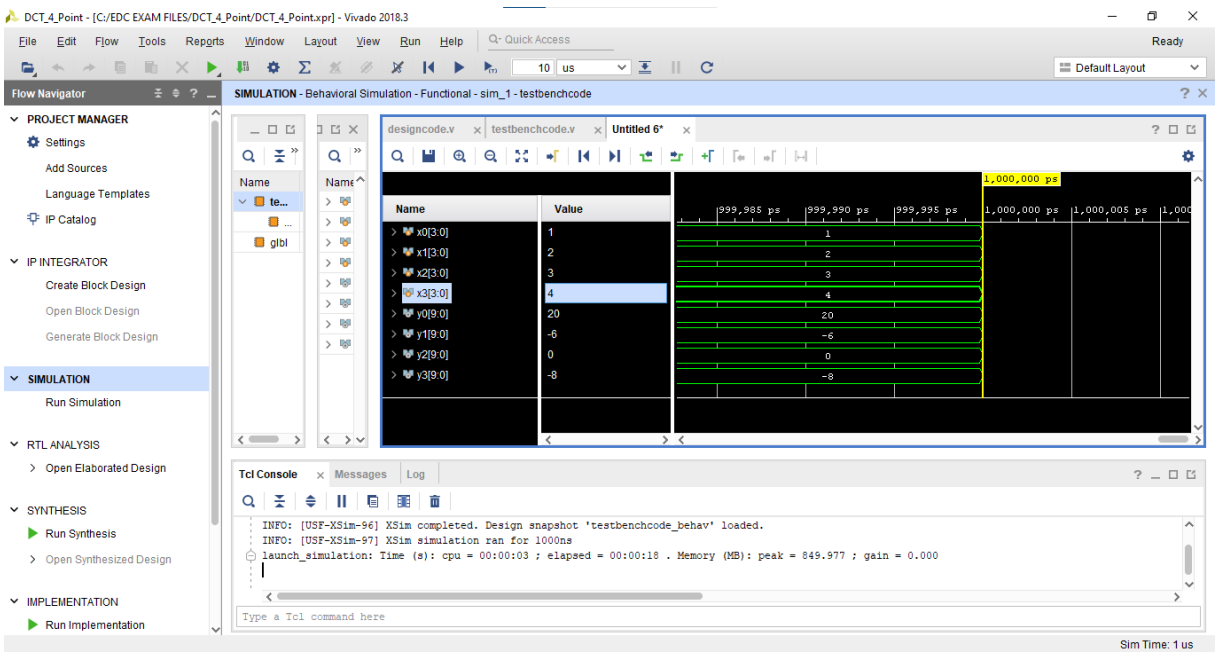
```
module DCT_4point(input signed[3:0]x0,x1,x2,x3,
        output signed[9:0]y0,y1,y2,y3);
wire signed[4:0]p0,m0,p1,m1;
assign p0=x0+x3;
assign m0=x0+x3;
assign p1=x1+x2;
assign m1=x1-x2;

parameter c1=1;
parameter c2=2;
parameter c3=3;

assign y0=(p0+p1)*c2;
assign y1=(m0*c1)+(m1*c3);
assign y2=(p0-p1)*c2;
assign y3=(m0*c3)-(m1*c1);
```

```
endmodule
```

2. **Test Fixture** — Test.v

```
module test;
reg signed[3:0]x0,x1,x2,x3;
wire signed[9:0]y0,y1,y2,y3;
DCT_4point UUT(x0,x1,x2,x3,y0,y1,y2,y3);
initial begin
x0=1;
x1=2;
x2=3;
x3=4;
#10;
end
endmodule
```

3. **Output**



Result

1. Successfully the 4-point DCT has been designed and the output was verified.

DCT → 4 POINT

» DesignCode.V

```
module DCT_4point (input signed [3:0] x0, x1, x2, x3,
                   output signed [9:0] y0, y1, y2, y3);

wire signed [4:0] p0, m0, p1, m1;
assign p0 = x0 + x3;
assign m0 = x0 - x3;
assign p1 = x1 + x2;
assign m1 = x1 - x2;

parameter c1 = 1;
parameter c2 = 2;
parameter c3 = 3;

assign y0 = (p0 + p1) * c2;
assign y1 = (m0 * c1) + (m1 * c3);
assign y2 = (p0 - p1) * c2;
assign y3 = (m0 * c3) - (m1 * c1);

endmodule
```

» TestBenchcode.V

```
module testbenchcode();
reg signed [3:0] x0, x1, x2, x3;
wire signed [9:0] y0, y1, y2, y3;
DCT_4point UUT (x0, x1, x2, x3, y0, y1, y2, y3);
```

```
initial begin
x0 = 1;
x1 = 2;
x2 = 3;
x3 = 4;
#10;
end
endmodule
```

>> OUTPUT.

x0	1
x1	2
x2	3
x3	4
y0	20
y1	-6
y2	0
y3	-8

MANUAL CAL.

$x(0) = 1 ; x(1) = 2 ; x(2) = 3 ; x(3) = 4$

$c1 = 1 ; c2 = 2 ; c3 = 3$

$x(0) = [P_0 + P_1] \times C_2$

$P_0 = x_0 + x_3$

$P_1 = x_1 + x_2$

$P_0 = 5 ; P_1 = 5$

$x(0) = (5+5) \times 2 = 20$

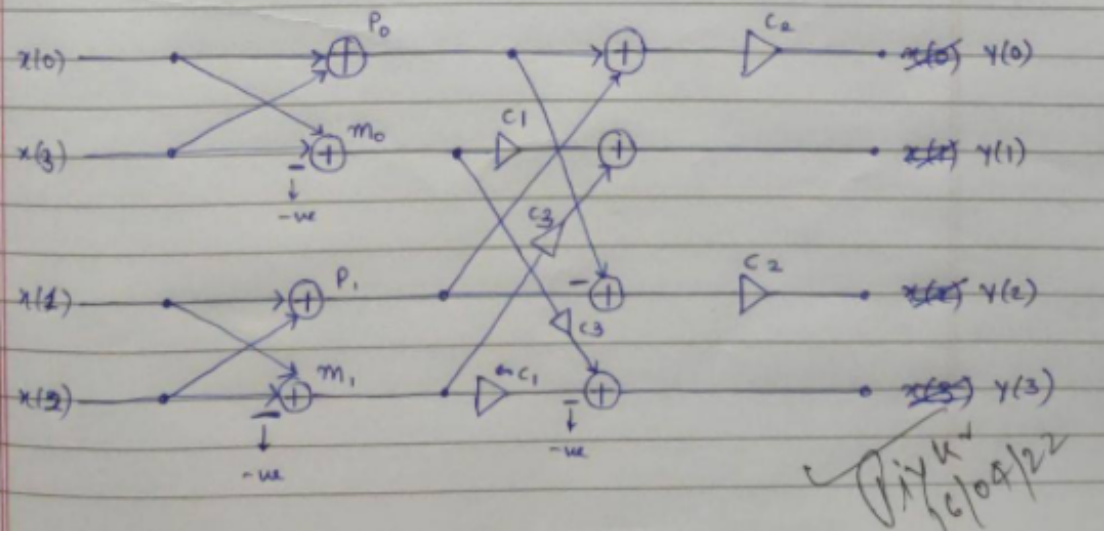
$x(1) = m_0 C_1 + m_1 C_3$

$= -6$

$x(2) = (P_0 - P_1) C_2 = 0$

$x(3) = m_0 C_3 - m_1 C_1$

$= -8$



Inference

1. In this experiment learnt about how to construct a 4point DCT.