VLSI LAB Digital Assignment 2

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School of Electrical Engineering

Faculty: **Professor Balamurugan S**

Course: **EEE-4028**

Course Name: **VLSI Lab**

Lab Slot: **L43 + L44**

This work is submitted in partial fulfilment of the requirement of the award of the degree of Bachelor of Technology in EEE

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4-BIT CARRY LOOK AHEAD ADDER

Objectives

1. To provide students with the background needed to design, develop, and test digital arithmetic circuits using IEEE standard Verilog HDL.
2. To provide an understanding complex arithmetic circuit design principles and its architecture design.

Outcomes

1. After completion of this course the students will be familiar with design and implementation of Digital Arithmetic building blocks using Verilog HDL and Modelsim Software.

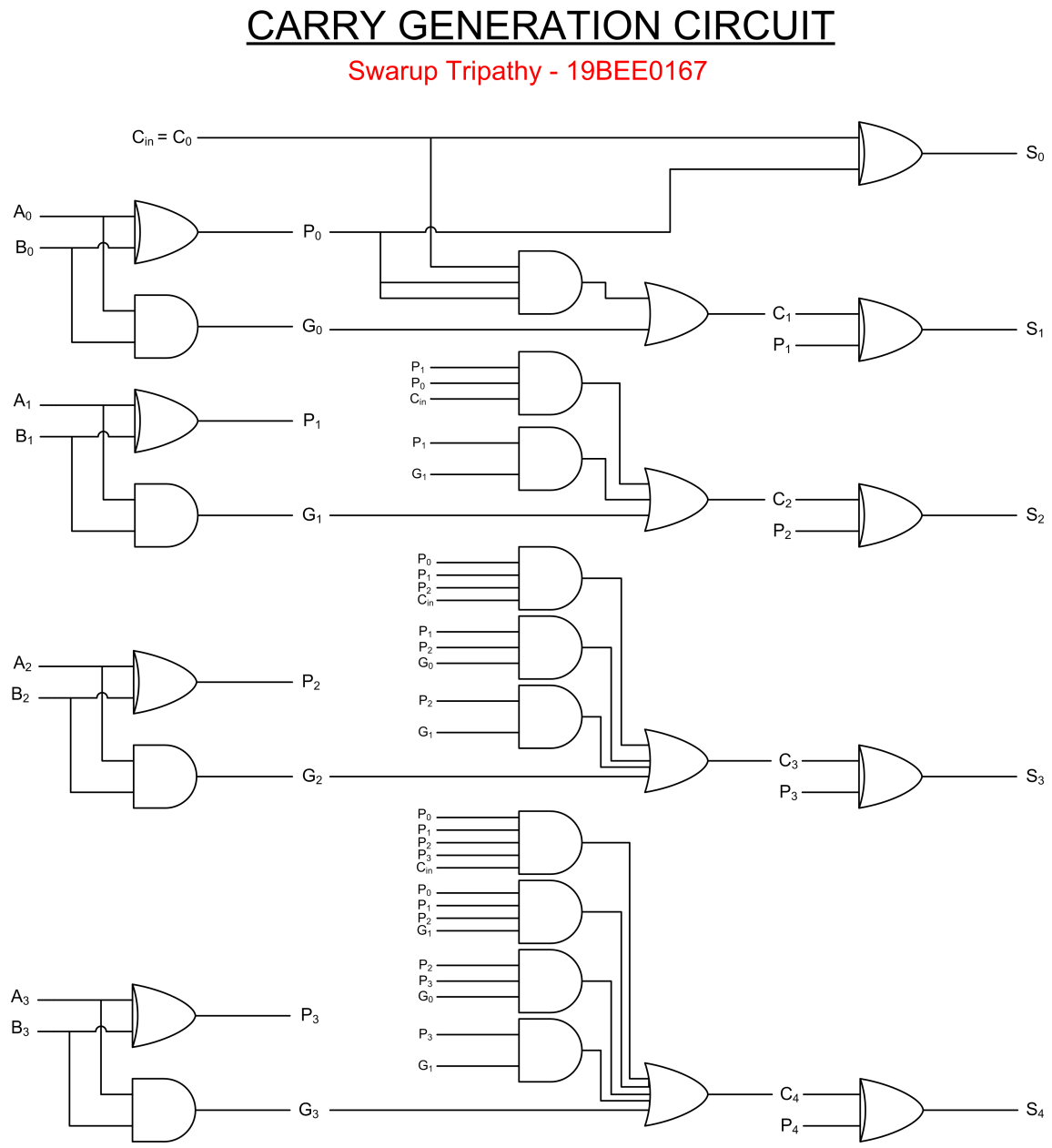
AIM

1. Design a 4 bit carry look ahead adder using four full adder circuit.

REQUIRED SOFTWARE

1. Model sim software for simulation
2. Microsoft Visio for making flowchart
3. Documentation to be done using LaTeX

CIRCUIT DIAGRAM



Design Code

1. **Verilog Module** — cla.v

```
module cla_4bit_19bee0167(input[3:0]a,b,input cin,output[4:0]s);
wire[3:0]p,g;
wire[4:0]c;
assign p=a^b;
assign g=a&b;
assign c[0] = cin;
```

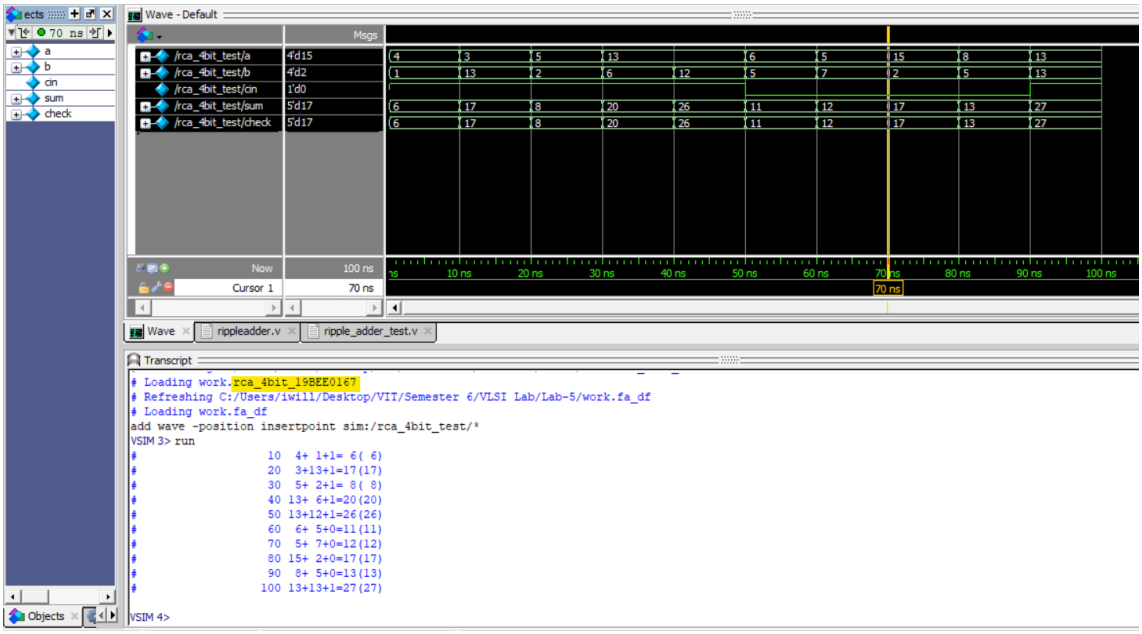
```
assign c[1] = p[0]&c[0]|g[0];
assign c[2] = ((p[1]&p[0]&c[0])|(p[1]&g[0])|g[1]);
assign c[3] = ((p[2]&p[1]&p[0]&c[0])|(p[2]&p[1]&g[0])|(p[2]&g[1])|g[2]);
assign c[4] = ((p[3]&p[2]&p[1]&p[0]&c[0])|(p[3]&p[2]&p[1]&g[0])|
(p[3]&p[2]&g[1])|(p[3]&g[2])|g[3]);
assign s[3:0] = p^c[3:0];
assign s[4] = c[4];
endmodule
```

2. **Test Fixture** — claTest.v

```
module cla_test_4bit_19bee0167;
reg [3:0]a,b;
reg cin;
reg [4:0]check;
wire [4:0]s;

cla_4bit_19bee0167 uut(a,b,cin,s);
initial repeat(10)
begin
a = $random;
b = $random;
cin = $random;
check = a+b+cin;
#10 $display($time,"%d +%d+%d=%d(%d)",a,b,cin,s,check);
end
endmodule
```

3. **Output**



4. **Console Output**

```
#                  10  4 +  1+1= 6( 6)
#                  20  3 +13+1=17(17)
#                  30  5 +  2+1= 8( 8)
#                  4013 +  6+1=20(20)
#                  5013 +12+1=26(26)
#                  60  6 +  5+0=11(11)
#                  70  5 +  7+0=12(12)
#                  8015 +  2+0=17(17)
#                  90  8 +  5+0=13(13)
#                 10013 +13+1=27(27)
```

Result

1. Successfully the 4-bit carry look ahead adder has been designed and the output was verified.

Inference

1. In this experiment learnt about how to construct multiple-bit adders.