VLSI LAB Digital Assignment 4

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School of Electrical Engineering

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Course: **EEE-4028**

Course Name: **VLSI Lab**

Lab Slot: **L43 + L44**

This work is submitted in partial fulfilment of the requirement of the award of the degree of Bachelor of Technology in EEE

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4-BIT BOUGH WOOLEY ARRAY MULTIPLIER

Objectives

1. To provide students with the background needed to design, develop, and test digital arithmetic circuits using IEEE standard Verilog HDL.
2. To provide an understanding complex arithmetic circuit design principles and its architecture design.

Outcomes

1. After completion of this course the students will be familiar with design and implementation of Digital Arithmetic building blocks using Verilog HDL and Modelsim Software.

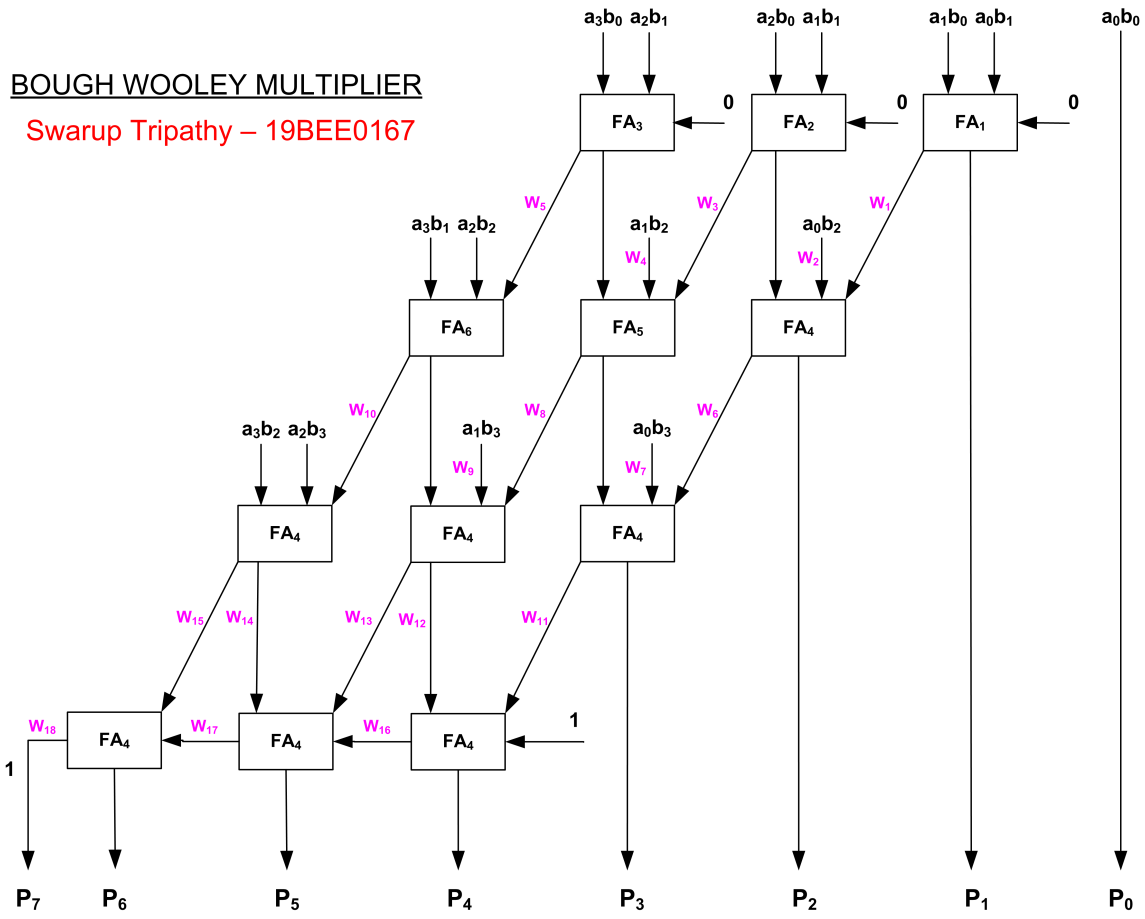
AIM

1. Design a 4 bit bough wooley array multiplier using 12 full adders.

REQUIRED SOFTWARE

1. Model sim software for simulation
2. Microsoft Visio for making flowchart
3. Documentation to be done using LaTeX

CIRCUIT DIAGRAM



Design Code

1. **Verilog Module** — bw.v

```
module bw_4b_19BEE0167(input signed[3:0]a,b, output signed[7:0]p);
wire[18:1]w;
supply0 zero;
supply1 one;
assign p[0] = a[0]&b[0];

fulladder_19BEE067 fa1((a[1]&b[0]),(a[0]&b[1]),zero,p[1],w[1]);
fulladder_19BEE067 fa2((a[2]&b[0]),(a[1]&b[1]),zero,w[2],w[3]);
fulladder_19BEE067 fa3(~(a[3]&b[0]),(a[2]&b[1]),zero,w[4],w[5]);

fulladder_19BEE067 fa4(w[2],(a[0]&b[2]),w[1],p[2],w[6]);
fulladder_19BEE067 fa5(w[4],(a[1]&b[2]),w[3],w[7],w[8]);
fulladder_19BEE067 fa6(~(a[3]&b[1]),(a[2]&b[2]),w[5],w[9],w[10]);
```

```
fulladder_19BEE067 fa7(w[7],~(a[0]&b[3]),w[6],p[3],w[11]);
fulladder_19BEE067 fa8(w[9],~(a[1]&b[3]),w[8],w[12],w[13]);
fulladder_19BEE067 fa9(~(a[3]&b[2]),~(a[2]&b[3]),w[10],w[14],w[15]);

fulladder_19BEE067 fa10(w[12],one,w[11],p[4],w[16]);
fulladder_19BEE067 fa11(w[14],w[16],w[13],p[5],w[17]);
fulladder_19BEE067 fa12((a[3]&b[3]),w[17],w[15],p[6],w[18]);
assign p[7] = ~(w[18]);
endmodule
```

2. **Fulladder.v**

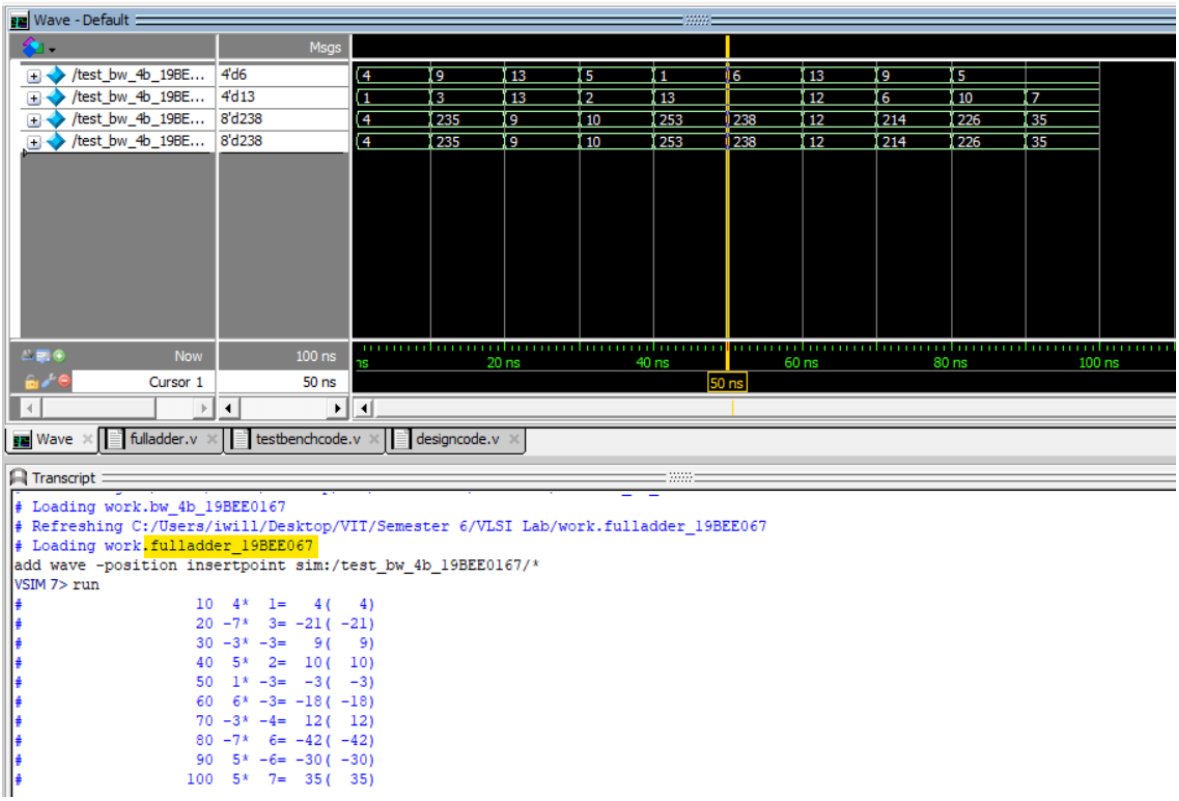
```
//Full adder using Dataflow
module fa_df_19BEE0167(input a,b,cin,output sum,cout);
assign sum=a^b^cin;
assign cout=(a^b)&cin|(a&b);
endmodule
```

3. **Test Fixture** — bwTest.v

```
module test_bw_4b_19BEE0167;
reg signed[3:0]A,B;
wire signed[7:0]Sum;
reg signed[7:0]check;

bw_4b_19BEE0167 uut(A,B,Sum);
initial repeat(10) begin
A = $random;
B = $random;
check = A*B;
#10 $display($time,"%d*%d=%d(%d)",A,B,Sum,check);
end
endmodule
```

4. **Output**



5. **Console Output**

```
#                  10  4*  1=   4(   4)
#                  20 -7*  3= -21( -21)
#                  30 -3* -3=   9(   9)
#                  40  5*  2=  10(  10)
#                  50  1* -3=  -3(  -3)
#                  60  6* -3= -18( -18)
#                  70 -3* -4=  12(  12)
#                  80 -7*  6= -42( -42)
#                  90  5* -6= -30( -30)
#                 100  5*  7=  35(  35)
```

Result

1. Successfully the 4-bit bough wooley array multiplier has been designed and the output was verified.

Inference

1. In this experiment learnt about how to construct multiple-bit adders.