



HLW8012 Datasheet

REV 1.3

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History Revision Record

Date	Revision Record	Version
2013-1-2	Initial Version	REV 1.0
2014-6-20	Change Company Address	REV 1.1
2014-8-01	Change Pin Nam: VIN To V1N, VIP To V1P	REV 1.2
2015-11-11	Change Digital Characteristic: DCLK To MCLK Add description of current channel and voltage channel: V_{peak}	REV 1.3

1 Function Description

HLW8012 is single phase multifunction metering chip. The high frequency pulse CF is provided for the energy measurement and the high frequency CF1 for indicating the effective value of the current or the effective value of the voltage. The chip uses SOP8 package.

1.1 Main Features

- High frequency pulse CF, indicating active power, meet the accuracy of 50/60Hz IEC 687/1036 standards, in the range of 1000:1 to reach 0.2% accuracy.
- High frequency pulse CF1 can be configured to output current or voltage RMS, in the range of 500:1 to reach of 0.5% accuracy.
- Built-in power supply monitoring circuit, when the power supply voltage is low to 4V, the chip will be reset.
- Built-in 2.43V voltage reference source; 5V power supply, operating current is less than 3mA.
- Application areas: The occasion of measuring the voltage, current and power, such as single-phase multi-function meter, smart socket, digital meter, smart street lamps, small appliances, etc.

1.2 Structure Description

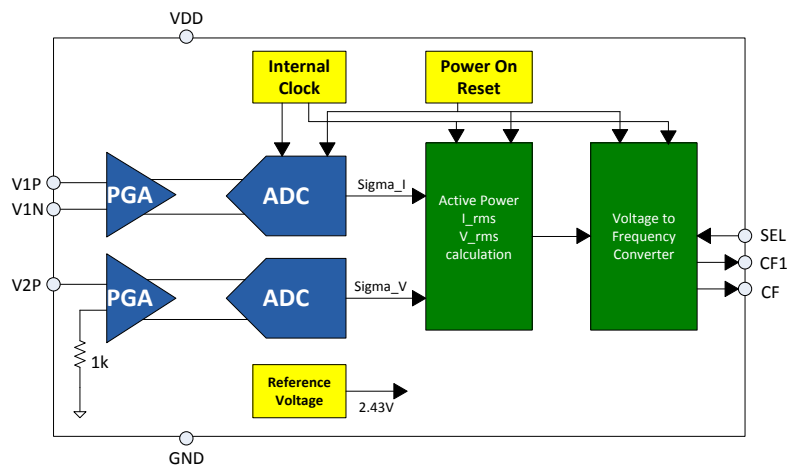


Figure 1 Function block diagram

1.3 PIN CONFIGURATION

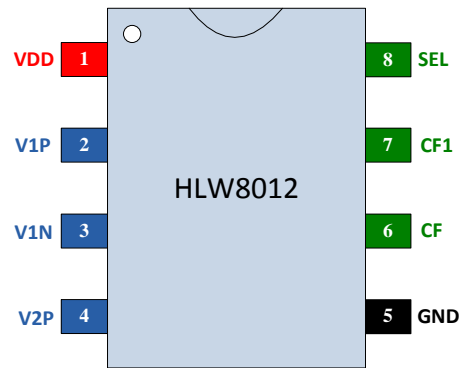


Figure 2 Pin Configuration

Table 1: PIN FUNCTION DESCRIPTIONS

Pin No.	Pin Name	Input/Output	Description
1	VDD	Power Supply	Power Supply
2, 3	V1P, V1N	Input	Analog Inputs for Channel 1(Current Channel) with maximum differential signal level of $\pm 43.75\text{mV}(V_{\text{peak}})$.
4	V2P	Input	Analog Input for Channel 2(Voltage Channel) with maximum single signal level of $\pm 700\text{mV}(V_{\text{peak}})$.
5	GND	Ground	Ground
6	CF	Output	Output active high frequency pulse, duty cycle 50%
7,	CF1	Output	SEL=0, Output current effective, duty cycle 50%; SEL=1, Output voltage RMS, duty cycle 50%;
8	SEL	Input	Configure RMS output type, with drop resistor

2 Feature Description

2.1 Recommended Operating Conditions

Parameter	Symbol	Min	Type	Max	Unit
Positive Power Supply	VDD	4.5	5.0	5.5	V
Operation Temperature Range	T _A	-40	-	+85	°C

2.2 Analog Characteristic

VDD = 5 V ± 10%; GND = 0 V

Parameter	Symbol	Min	Type	Max	Unit
ACCURACY					
Active Power Full Gain Range Input Range 0.1%~100%	P _{Active}	-	±0.2	-	%
Current RMS Full Gain Range Input Range 0.2%~100%	I _{RMS}	-	±0.5	-	%
Voltage RMS Full Gain Range Input Range 0.2%~100%	V _{RMS}	-	±0.5	-	%
Analog Input (All Channel)					
Common-mode Range		-1	-	1	V
Crosstalk in voltage channel When full range in current channel(50, 60Hz)		-	-100	-	dB
Input Capacitance	IC	-	6.4	-	pF
Input Impedance Current Channel Voltage Channel	EII		500 6	-	kΩ MΩ
Input-Referred Noise Current Channel Voltage Channel	N _I	- -	- -	2 20	μVrms μVrms
Power Supply					
Supply Current IA+ID			3	-	mA
Power Consumption (VDD = 5 V)	PC	-	15		mW

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Low Threshold of Power-Down Voltage	PMLO	-	4	-	V
High Threshold of Power-Down Voltage	PMHI	-	4.3	-	V

2.3 Built-In Reference

Parameter	Symbol	Min	Type	Max	Unit
Reference Voltage	VREF	+2.3	+2.43	+2.55	V
Temperature Coefficient	TC _{VREF}	-	25	-	ppm/°C

2.4 Digital Characteristic

VDD = 5 V, GND = 0 V

Parameter	Symbol	Min	Type	Max	Unit
BUILT-IN CLOCK					
Frequency	MCLK	3.04	3.579	4.12	MHz
Duty Cycle		30	50	70	%
FILTER					
Sampling Rate (DCLK=MCLK/4)		-	MCLK/4	-	Hz
Digital Filter Output Rate	OWR	-	MCLK/128	-	Hz
High-Pass Filter Bandwidth (-3dB)		-	0.543	-	Hz
INPUT					
Input High Voltage (VDD=5V)	V _{IH}	0.8VDD	-	-	V
Input Low Voltage (VDD=5V)	V _{IL}	-	-	0.8	V
Input Leakage	I _{in}	-	±10	-	μA
OUTPUT					
Output High Voltage (I _{out} = +5 mA)	V _{OH}	VDD-0.5	-	-	V
Output Low Voltage (I _{out} =-5 mA)	V _{OL}	-	-	0.5	V
Capacitance Of Digital Output Pin	C _{OUT}	-	5	-	pF

2.5 Switching Characteristic

Pin SEL is digital input port, the duty cycle of CF and CF1 pluses are 50%.

2.6 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Type	Max	Unit
Digital Supply	VDD	-0.3	-	+6.0	V
Analog Supply	VDD	-0.3	-	+6.0	V
VDD to GND		-0.3	-	+6.0	V
V1P, V1N, V2P to GND		-2		+2	V
Analog Input Voltage	V _{INA}	-0.3	-	VDD+0.3	V
Digital Input Voltage	V _{IND}	-0.3	-	VDD+0.3	V
Digital Output Voltage	V _{OUTD}	-0.3	-	VDD+0.3	V
Operating Temperature Range	T _A	-40	-	85	°C
Storage Temperature Range	T _{stg}	-65	-	150	°C

3 Application

3.1 HLW8012 Typical application

As shown in Figure 3, the power supply the HLW8012 should be in parallel with two small capacitors to filter out the noise from the grid. The signal of current channel is provided by the current diverter. The signal of voltage channel is provided by the resistor network. CF, CF1, SEL connect to the input port of the MCU. MCU measure the pulse periods of CF and CF1, then calculate the active power, current RMS and voltage RMS.

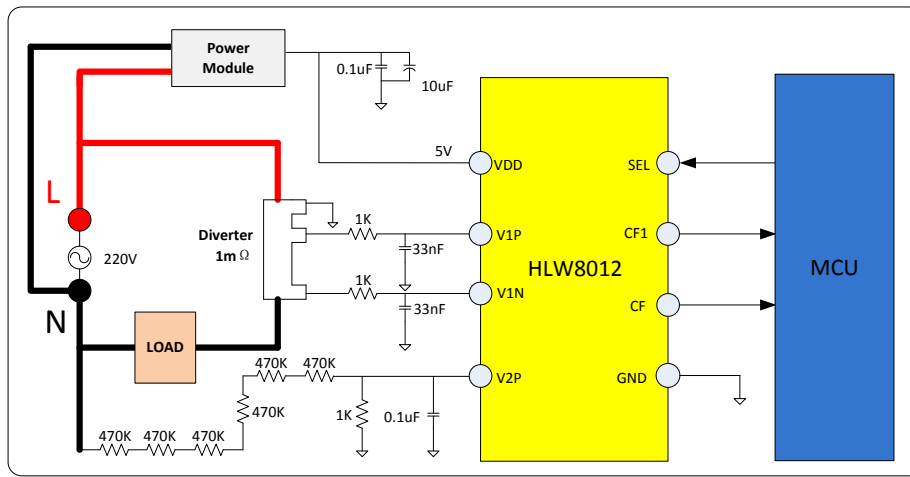


Figure 3 Typical application

3.2 Frequency of CF、CF1

The internal DSP of HLW8012 Integrates the PGA. After frequency conversion, the output frequency of active power, current RMS and voltage RMS can be calculated by the following formula:

$$(1) \text{ Active Power: } F_{CF} = \frac{V1 \times V2 \times 48}{V_{REF}^2} \times \frac{f_{osc}}{128}$$

$$(2) \text{ Current RMS: } F_{CFI} = \frac{V1 \times 24}{V_{REF}} \times \frac{f_{osc}}{512}$$

$$(3) \text{ Voltage RMS: } F_{CFU} = \frac{V2 \times 2}{V_{REF}} \times \frac{f_{osc}}{512}$$

V1: Voltage of the current channel

V2: Voltage of the voltage channel

f_{osc} : Frequency of built-in oscillator is 3.579MHz

V_{REF} : Voltage of the built-in reference is 2.43V

3.3 Threshold and Creeping Prevention

HLW8012 uses the anti-creep new algorithm, as long as the input signal is greater than the noise, the module to normal measurement.

3.4 Built-In Oscillator

The frequency of the built-in oscillator is 3.579MHz, the power supply rejection ratio is less than <0.01/V.

3.5 Built-In Reference

HLW8012 Integrated high precision band-gap reference source, the voltage of the reference is 2.43V.

4 HLW8012 Package

HLW8012 uses SOP8 package, the information is shown in Figure 4:

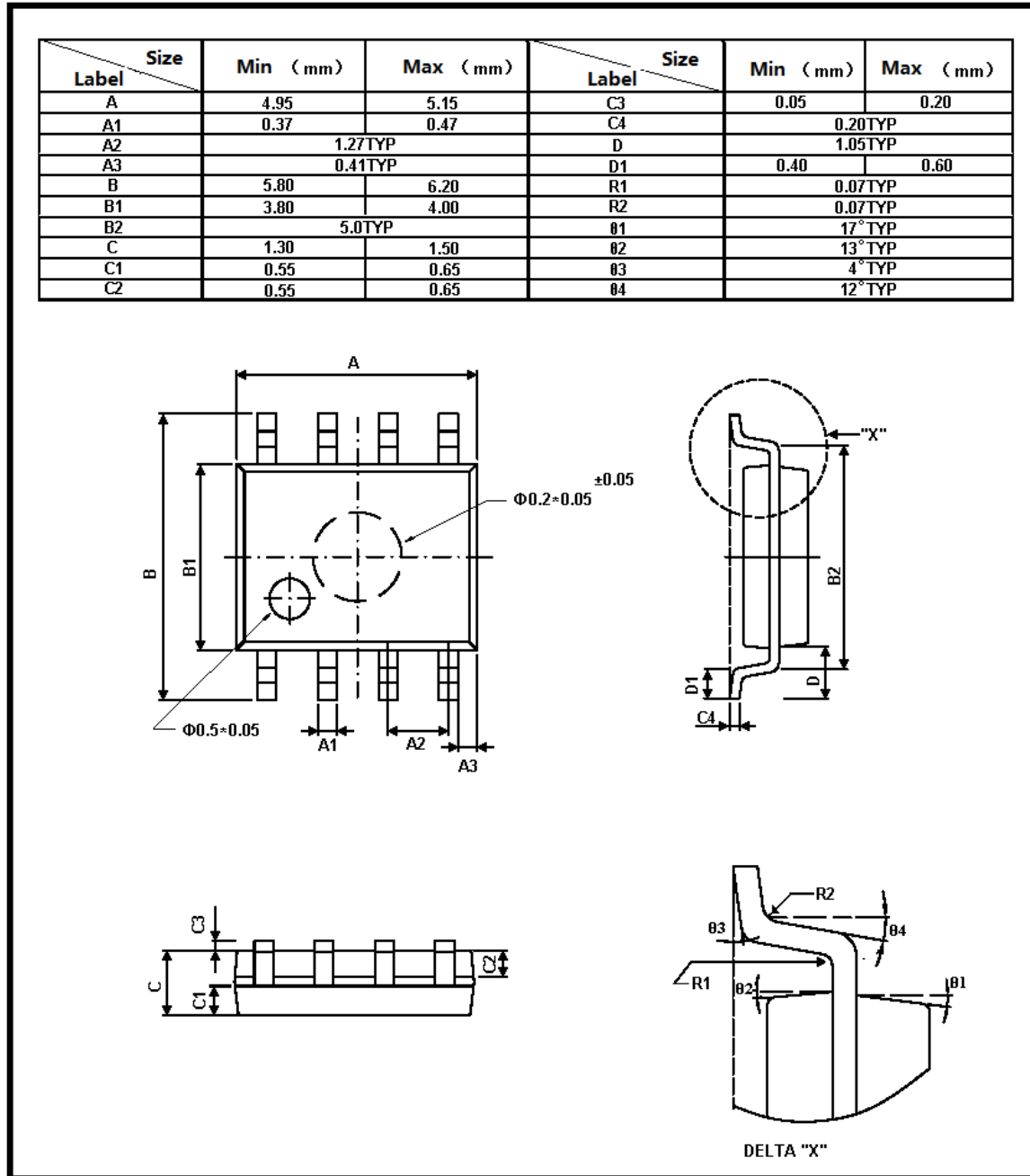


Figure 4 Package