

[illegible]

```

;-----;
MAIN:
    out PORTB, r21                ;Use Register 21 on Port B

    lsl r21                       ;Shift r21's LEDs to the Left
    call DELAY                   ;Call DELAY

    cp r21, r23                   ;Compare register 21 with 23
    breq SHIFT_LEFT              ;If 21 = 23 go to "SHIFT_LEFT" branch.

rjmp MAIN

```

```

;-----;
; SHIFT_LEFT                      ;
;-----;
SHIFT_LEFT:
    out PORTB, r23                ;Use Register 23 on Port B
    call DELAY                   ;Call DELAY
    ldi r21, 0b10000000

    ;-----;
    ; SHIFT_RIGHT                  ;
    ;-----;
SHIFT_RIGHT:
    out PORTB, r21
    asr r21                       ;Swap direction (Arithmetic Shift Right)
    call DELAY                   ;Call DELAY

    cp r21, r22                   ;Compare r21 = r22
    breq MAIN                     ;if 21 = 23 go to "MAIN" Branch

    rjmp SHIFT_RIGHT

;-----;

rjmp SHIFT_LEFT

```

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;-----;
;DELAY                            ;
;-----;
DELAY:
    ; Generated by delay loop calculator
    ; at http://www.bretmulvey.com/avrdelay.html
    ;
    ; Delay 500 000 cycles
    ; 500ms at 1 MHz

    ldi r18, 4
    ldi r19, 138
    ldi r20, 86

```

```
L1: dec r20
    brne L1
    dec r19
    brne L1
    dec r18
    brne L1
    rjmp PC+1
ret
;-----
```