

[illegible]

```
out DDRA, r16                                ;Set A Port as output Port.
```

```
ldi r17, 0b00000001  
mov r21, r17  
ldi r25, 0b11111111
```

```
ldi r22, 0  
ldi r23, 0  
.def FIRSTTIME = r22  
.def SECONDTIME = r23
```

```
ldi r29, 0b00001111  
ldi r30, 0b11110000
```

```
;-----;  
;INFINITE LOOP                               ;  
;-----;  
INFINITE:
```

```
FIRST:  
    call DELAY  
    in r16, PINA  
    ldi r26, 0b11111110  
    cp r26, r16  
    brne NOREACT
```

```
REACT:  
    com SECONDTIME  
    ldi r17, 0b00000001
```

```
NOREACT:  
    mov r16, r17  
    com r16  
    out PORTB, r16  
    cpi SECONDTIME, 0  
    brne JOHNSON
```

```
RING:  
    lsl r17  
    cpi SECONDTIME, 0  
    breq JOHNSON_END
```

```
JOHNSON:  
    cpi FIRSTTIME, 0xFF  
    breq SHIFT_RIGHT
```

```
SHIFT_LEFT:  
    lsl r17  
    add r17, r21
```

```
    cpi FIRSTTIME, 0xFF
    brne BEGIN_COMPARE
```

```
SHIFT_RIGHT:
    lsr r17
```

```
BEGIN_COMPARE:
    cp r17, r25
    breq EQUAL
```

```
JOHANSSON_END:
    cpi SECONDTIME, 0
    brne RING_END_CONDITION_1
    cpi r17, 0
    brne RING_END_CONDITION_1
    ldi r17, 1
```

```
RING_END_CONDITION_1:
```

```
    rjmp FIRST
```

```
EQUAL:
    com r25
    com FIRSTTIME
```

```
    rjmp INFINITE
```

```
;-----;
;DELAY          ;
;-----;
```

```
DELAY:
; Generated by delay loop calculator
; at http://www.bretmulvey.com/avrdelay.html
;
; Delay 500 000 cycles
; 500ms at 1 MHz
```

```
    ldi r18, 4
    ldi r19, 138
    ldi r20, 86
L1: dec r20
    brne L1
    dec r19
    brne L1
    dec r18
    brne L1
    rjmp PC+1
ret
```

;

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