### 计算机系统结构第二次作业

Consider the unpipelined processor. Assume that it has a 1ns clock cycle and that it uses 4 cycles for branches and stores and 5 cycles for other operations. Assume that the relative frequencies of branch and store operations are 15% and 10%, respectively.

Consider a pipelined processor. Assume the slowest stage takes 1ns and clock skew and register setup add 0.2 ns to the clock period.

How much speedup in the instruction execution rate will we gain from an ideal pipeline?

非流水线处理器：

流水线处理器：

所以