

RALINK TECHNOLOGY, CORP.

RALINK Auto-Frequency and Power Save

Application Note

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Ralink Technology Corporation (Taiwan)

5F, No.5, Tai-Yuen 1st Street,

Jhubei City

HsinChu Country 30265, Taiwan, ROC

Tel +886-3-560-0868

Fax +886-3-560-0818

Sales Taiwan: Sales@ralinktech.com.tw

Technical Support Taiwan: FAE@ralinktech.com.tw

http://www.ralinktech.com/



Content

1.	Introduction4	2.3 How to turn on DDR Self Refresh Power Save 5	
2.	Setup 5	3.	Check Function 7
2.1 How to turn on CPU Auto-Frequency 5			
2.2 How to turn on SDP Pre-charge Power Down 5			



1. Introduction

The RT3352/RT5350 SOC has the capability of auto-frequency and power saving.

- CPU Auto-Frequency (RT3352/RT5350)
- SDR Power Pre-charge Power Down (RT3352/RT5350)
- DDR self Refresh Power Save (RT3352)

Notice: Those new features are supported by SDK 3.5.2.0 or following version.





2. Setup

2.1 How to turn on CPU Auto-Frequency

For RT3352/RT5350, We can turn on CPU auto frequency function by

1. Modifying config.mk in Uboot and rebuild uboot firmware

```
RALINK DDR CONTROLLER OPTIMIZATION = OFF
RALINK CPU AUTO FREQUENCY = ON
RALINK_SDR_PRECHARGE_POWER_DOWN = OFF
RALINK DDR SELF REFRESH POWER SAVE MODE = OFF
```

\$make

2. Set Linux Kernel Configuration and then rebuild linux firmware \$make menuconfig --->

```
Machine selection ---> [*] Ralink External Timer
.....
$make dep; make
```

2.2 How to turn on SDR Pre-charge Power Down

For RT3352/RT5350, We can turn on SDR power save by

1. Modifying config.mk in Uboot and rebuild uboot firmware

```
RALINK_DDR_CONTROLLER_OPTIMIZATION = OFF
RALINK_CPU_AUTO_FREQUENCY = OFF
RALINK_SDR_PRECHARGE_POWER_DOWN = ON
RALINK DDR SELF REFRESH POWER SAVE MODE = OFF
```

\$make

2.3 How to turn on DDR Self Refresh Power Save

For RT3352, We can turn on DDR power save by

1. Modifying config.mk in Uboot and rebuild uboot firmware



RALINK_DDR_CONTROLLER_OPTIMIZATION = OFF

RALINK_CPU_AUTO_FREQUENCY = OFF

RALINK_SDR_PRECHARGE_POWER_DOWN = OFF

RALINK_DDR_SELF_REFRESH_POWER_SAVE_MODE = ON

\$make





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3. Check Function

You can check if those functions are enabled or disabled by register.

CPU Auto-Frequency

Turn off:

```
#
# reg s b00000000
switch register base addr to 0xb00000000
# reg r 40
0x34501
#
```

Turn on:

```
# reg s b00000000
switch register base addr to 0xb0000000
# reg r 40
0x80035f41
#
```

SDR Pre-charge Power Save

Turn off:

```
# reg s b0000300
switch register base addr to 0xb0000300
# reg r 1c
0x3ffff
# reg r 4
0xe1110600
#
```

Turn on:

```
# reg s b0000300
switch register base addr to 0xb0000300
# reg r 1c
0x1
# reg r 4
0xf1110600
#
```

DDR Self Refresh Power Save

Turn off:

```
# reg s b0000300
switch register base addr to 0xb0000300
# reg r 1c
0x3ffff
# reg r 18
0x3
#
```

Turn on:

```
# reg s b0000300
switch register base addr to 0xb0000300
# reg r 1c
0x6d000001
# reg r 18
0x13
#
```