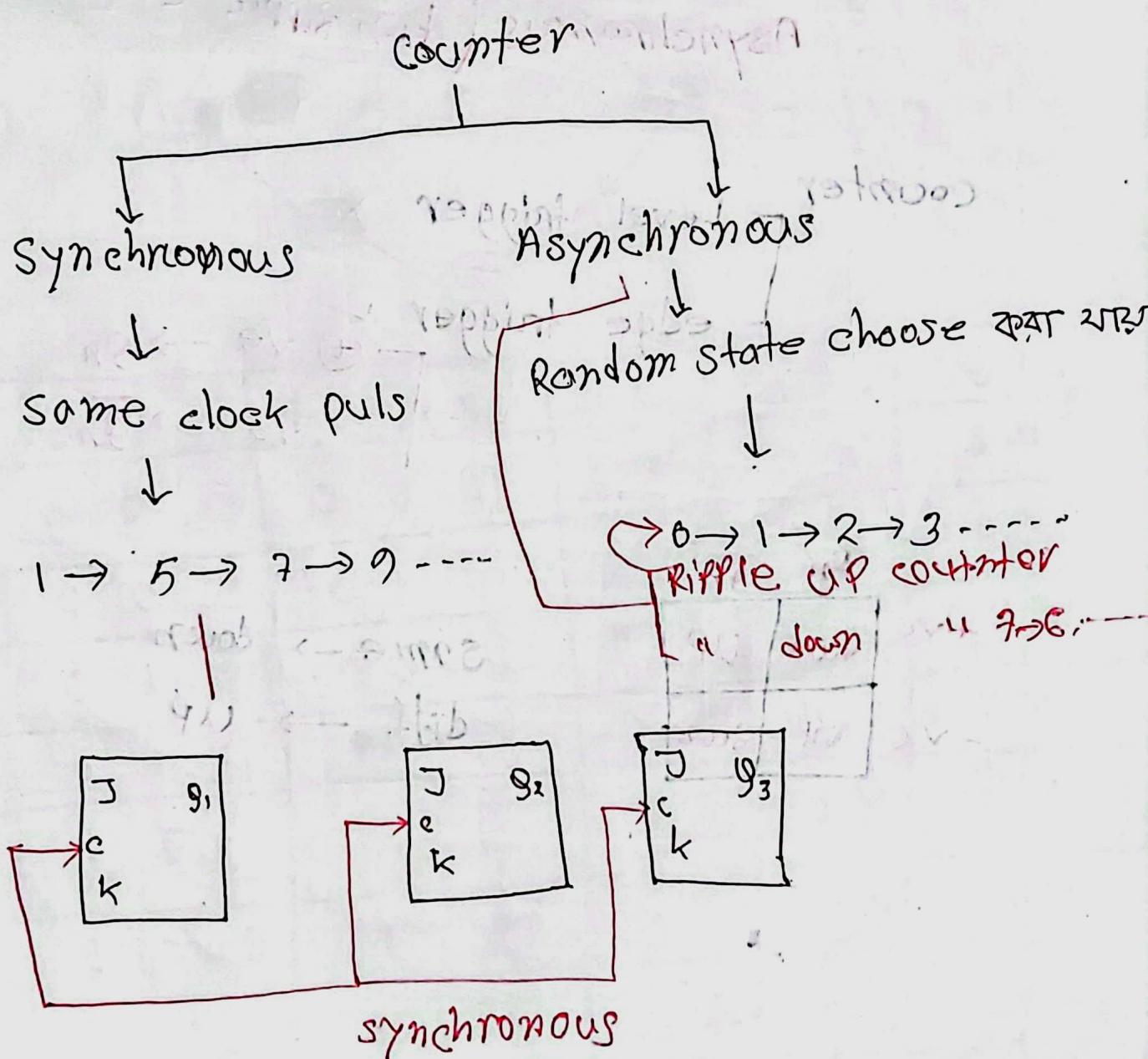
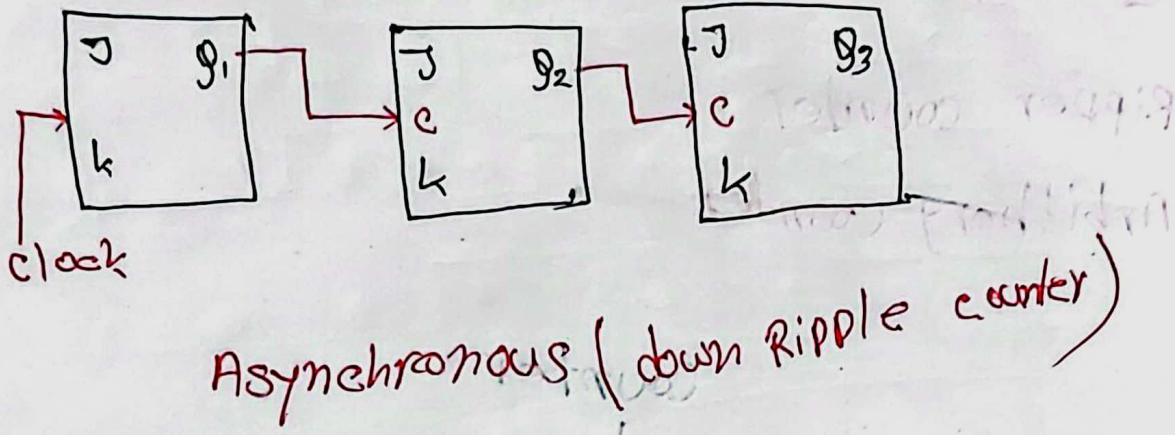
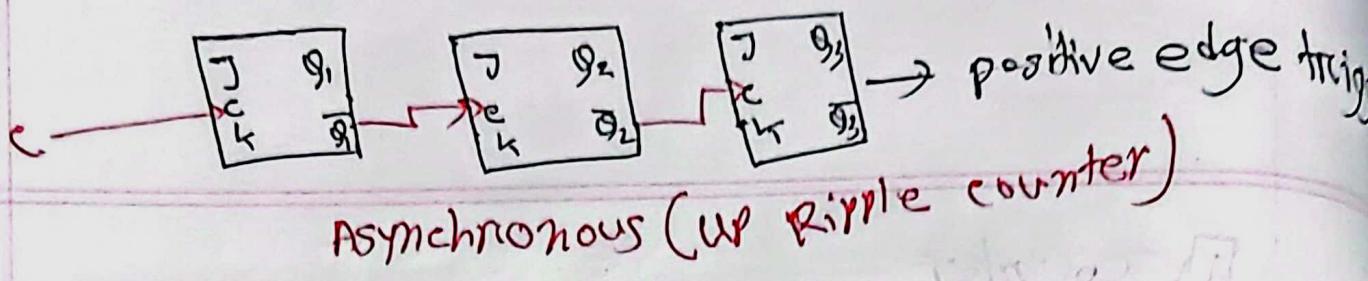


 counter

Ripper counter

Arbitrary Counter





counter

Level trigger X

edge trigger ✓

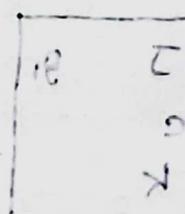
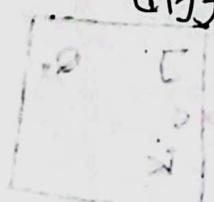
+ve → Q_n

-ve → \bar{Q}_n

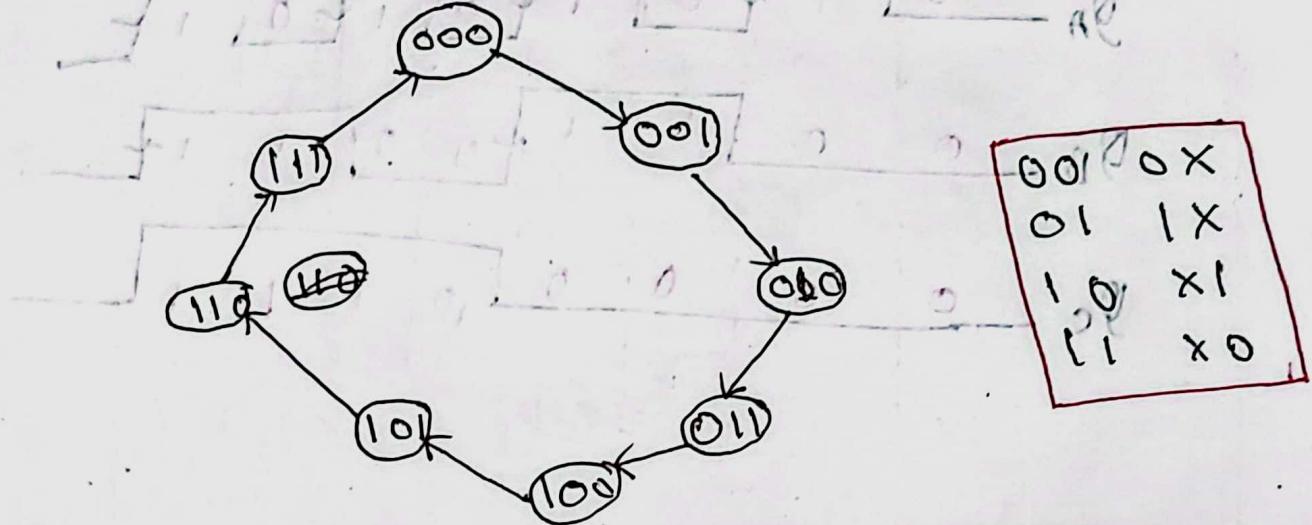
+ve	down	UP
-ve	UP	down

same → down

diff → up

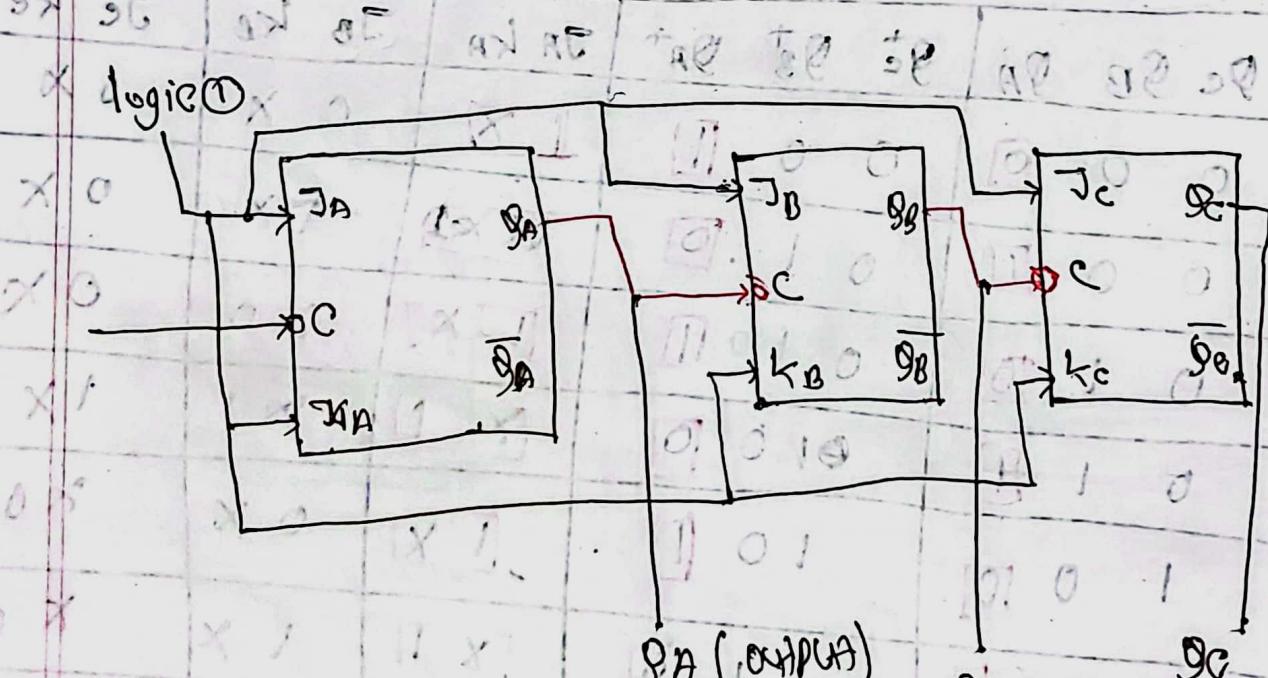
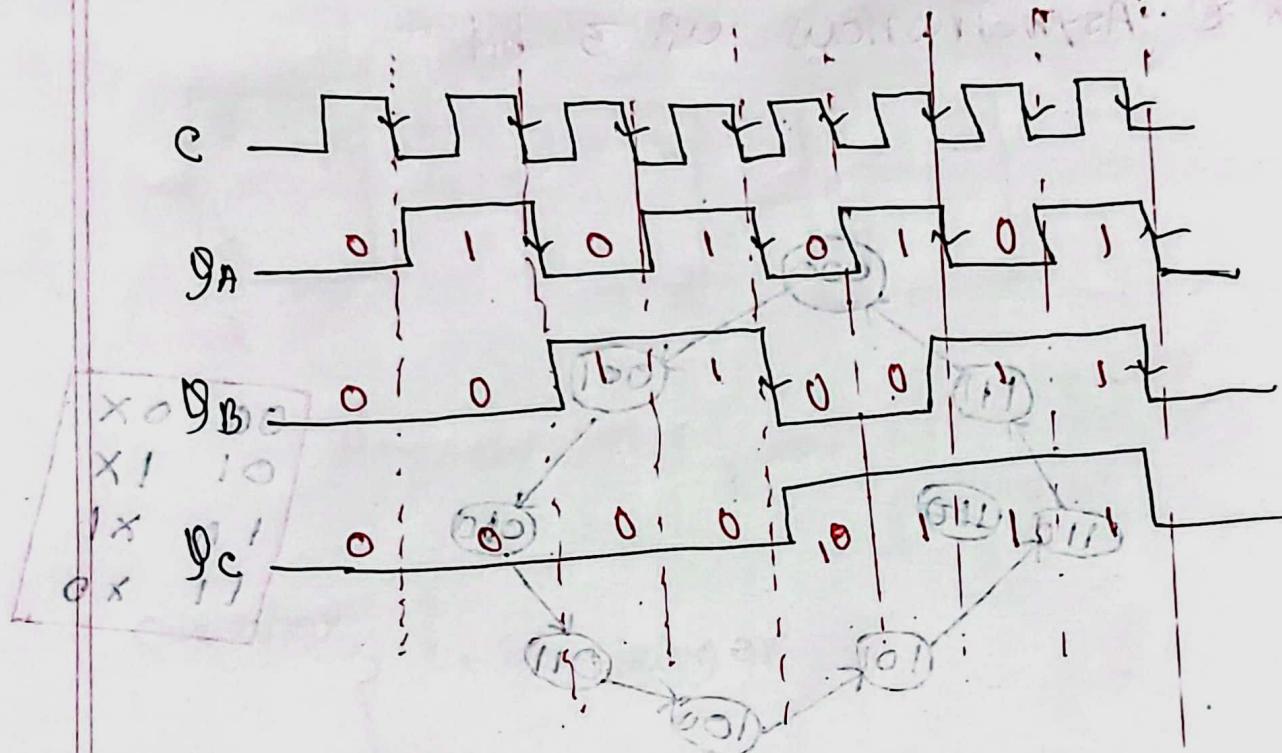


Asynchronous up 3 bit

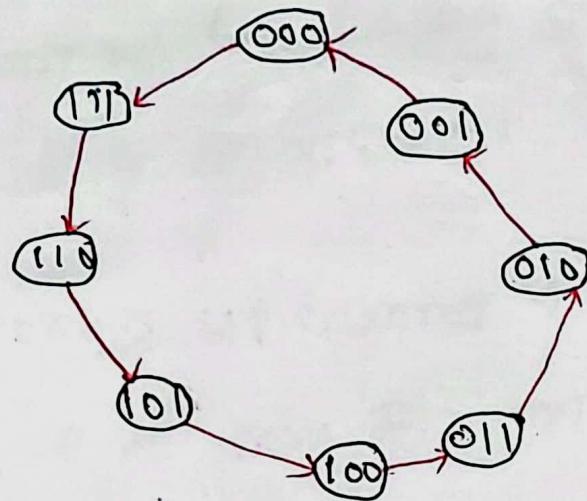


D_c	Q_B	Q_A	Q_c^+	Q_B^+	Q_A^+	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1		X	0	X	0	X
0	0	1	1	0			X	X		0	X
0	1	0	0	1	1		X		X	0	X
0	1	1	0	1	0		X	1	X	1	X
1	0	0	1	0	1		X	X	0	X	X
1	0	1	1	1	0		X	1	X	X	0
1	1	0	1	1	0		X	1	X	X	0
1	1	1	0	0	0		X	1	X	1	X

positive edge trigger

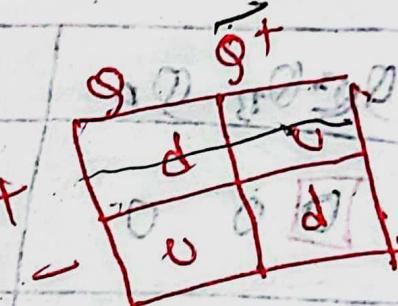


Asynchronous down counter 3-bit



$Q_C Q_B Q_A$	$Q_C^+ Q_B^+ Q_A^+$	$J_E K_E$	$J_B K_B$	$J_A K_A$
0 0 0	1 1 1	1 X	Q1 X	1 X / J1
0 0 1	0 0 0	0 X	0 X	X 1
0 1 0	0 0 1	0 X	X 1	1 X
0 1 1	0 1 0	0 X	X 0	X 1
1 0 0	0 1 1	X 1	1 X	1 X
1 0 1	1 0 0	X 0	0 X	X 1
1 1 0	1 0 1	X 0	K 1	1 X
1 1 1	1 1 0	X 0	X 0	X 1

~~Q~~ $\oplus \ominus \otimes$ up + down counter
(control bit)



	M	S	Y	Q1	Q2	Q3	Q4	Y	Q1	Q2	Q3	Q4
X	0	0	X 0 0	0 0 0	1 0 0	0 0 1	0 0 0	0 0 0 1	0 0 0 1	1 0 0	0 0 1	0 0 0
X	1	0	X 0 1	0 0 1	1 0 1	0 0 0	1 0 0	0 0 0 1	0 0 0 1	1 0 1	0 0 0	1 0 0
X	0	1	X 1 1	0 1 1	0 1 1	1 1 1	1 1 1	1 1 1 1	1 1 1 1	0 1 1	1 1 1	1 1 1
X	1	1	X 1 0	1 0 0	0 1 0	1 0 0	0 1 0	1 0 0 1	1 0 0 1	0 1 0	1 0 0	0 1 0
X	0	0	X 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0 0	0 0 0 0	0 0 0	0 0 0	0 0 0
X	1	0	X 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1 0	0 0 1 0	0 0 1	0 0 1	0 0 1
X	0	1	X 1 1	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1 1	1 1 1 1	1 1 1	1 1 1	1 1 1
X	1	1	X 1 0	1 0 0	0 1 0	1 0 0	0 1 0	1 0 0 1	1 0 0 1	0 1 0	1 0 0	0 1 0
X	0	0	X 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0 0	0 0 0 0	0 0 0	0 0 0	0 0 0
X	1	0	X 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1 0	0 0 1 0	0 0 1	0 0 1	0 0 1
X	0	1	X 1 1	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1 1	1 1 1 1	1 1 1	1 1 1	1 1 1
X	1	1	X 1 0	1 0 0	0 1 0	1 0 0	0 1 0	1 0 0 1	1 0 0 1	0 1 0	1 0 0	0 1 0

$$Y = M\bar{S} + \bar{M}S$$

$$Y = M \oplus S$$

Important note

7. Asynchronous counter

Asynchronous

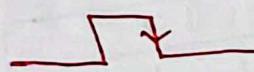
Asynchronous & diagram circuit diagram

K-map लागू ना करिए।

Asynchronous up counter & clock negative

क्रैमर (up to down क्रैमर वाले वाले)

1 (भयो 0 2 (क्लक्क वाले वाले)



100

101

110

111

101

110

111

100

101

110

111

100

101

110

111

100

101

110

111

100

101

110

111

Circuit & logic 1 करें।

प्रथम ff में 0 value 1 में 0 2 तक के पास

ff कास करें।

short state

77

state bin state binary

AT AT ST T after step NL QL RL RR

1	0	0	0	0 0 0 0	0	0	0 0
---	---	---	---	---------	---	---	-----

1	1	0	0	0 1 0 0	1	0	0 0
---	---	---	---	---------	---	---	-----

1	0	0	0	1 0 0 0	0	1	0 0
---	---	---	---	---------	---	---	-----

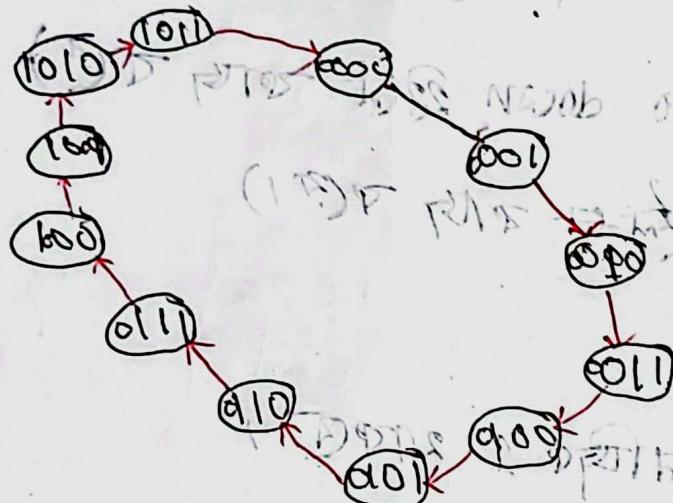
Asynchronous Mod-12 counter with T FF

মানে state table 6-12 এর মতো

যাকি গল্প don't care এর সমর্থন

কাউন্ট তা করা 90-এ

bit state diagram

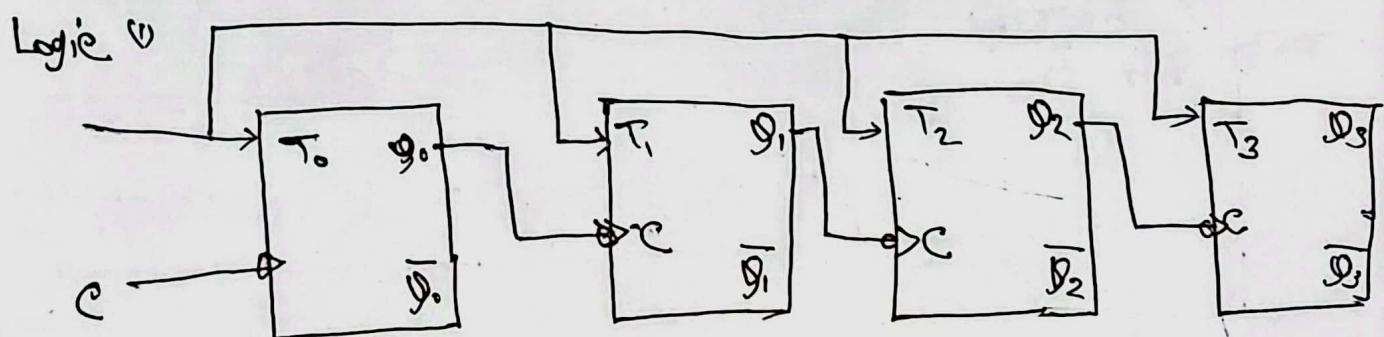


state table

present state	next state	FF
1010 1001 0001 0010 0100 0110 0111 0101 0011 0000 0101 1010	1010 1001 0001 0010 0100 0110 0111 0101 0011 0000 0101 1010	T _D T _L T _B T _A
00 0 0 0	0 0 0 0 1	0 0 0 1
00 0 0 1	0 0 1 0	0 0 1 1
00 1 0	0 0 1 1	0 0 0 1

0 0 1 1	0 1 0 0	0 1 1 . .
0 1 0 0	0 1 0 1	0 0 0 1
0 1 0 1	0 1 1 0	0 0 1 1
0 1 1 0	0 1 1 1	0 0 0 1
0 1 1 1	0 0 0 0	1 1 1 1
1 0 0 0	0 0 0 1	0 0 0 1
0 0 0 1	0 0 1 0	0 0 1 1
0 0 1 0	0 0 1 1	0 0 0 1
0 0 1 1	0 0 0 0	1 0 1 1
1 1 0 0	X X X X	X X X X
1 1 0 1	X X X X	X X X X
1 1 1 0	X X X X	X X X X
1 1 1 1	X X X X	X X X X

circuit



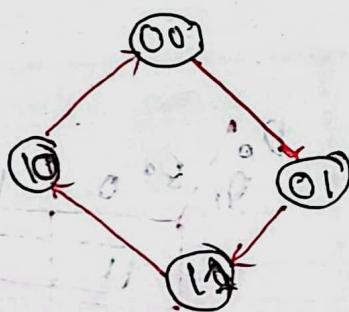
■ Synchronous counter

Follow no sequence

must have to use k-map

$\oplus \otimes \otimes 0 \rightarrow 1 \rightarrow 3 \rightarrow 2$ using D FF

state diagram



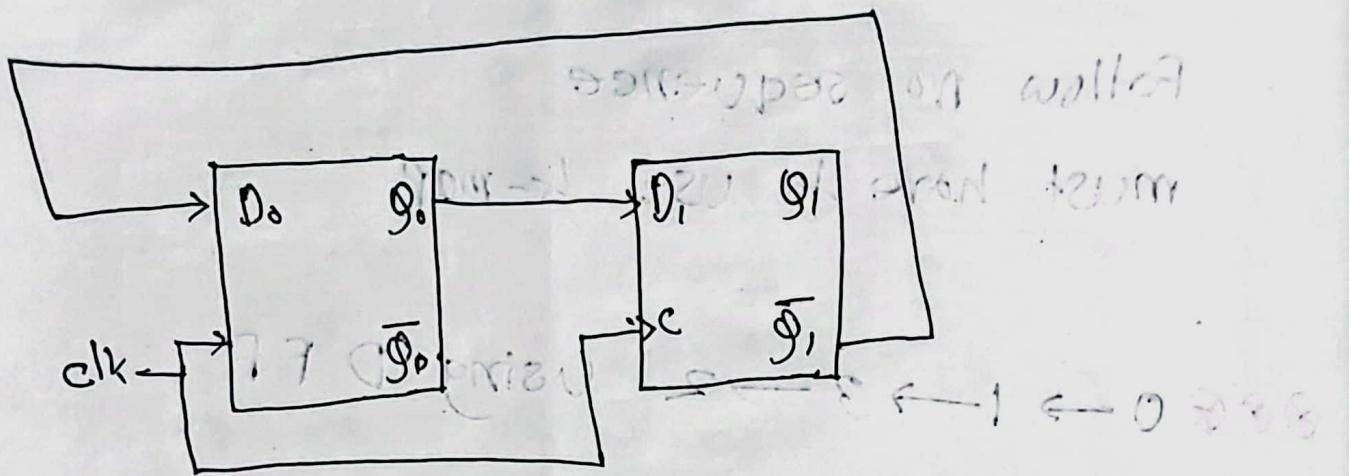
state table

present state	next state	FF
01	01	D ₁ D ₀
00	01	0 1
01	01	1 1
10	00	0 0
11	00	1 0

भासा नम्बर येते फल
प्रथम भासा द्वितीय FF
द्वितीय तीव्र तर
तीव्र तीव्र ।

0 येते 3 द्वितीय
द्वितीय तीव्र तीव्र तीव्र
तीव्र FF 2 तर

circuit



k-map

D_1	Q_0	1
0	0	1
1	1	1

D_0	Q_1	0	1
0	0	0	1
1	1	1	0

$$D_1 = Q_0$$

$$D_0 = \bar{Q}_1$$

state table Gt contd

$Q_2 Q_1 Q_0$

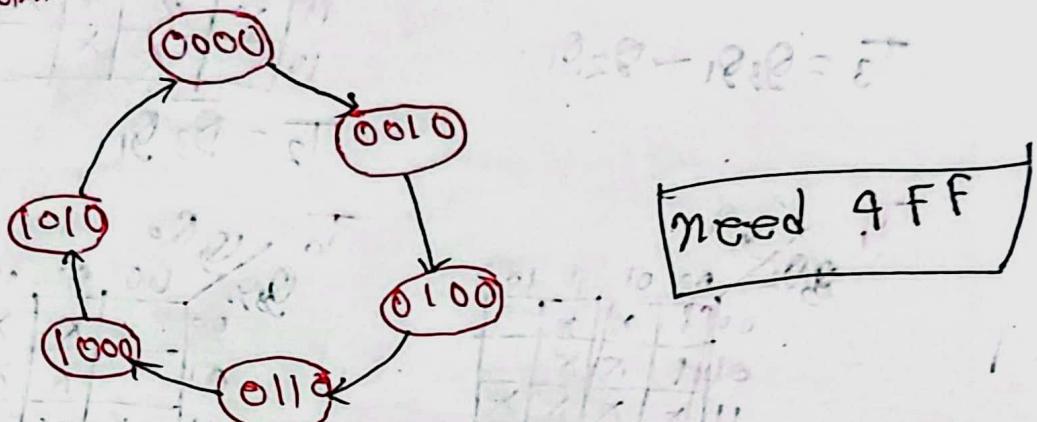
Circuit Gt contd

$Q_0 Q_1 Q_2 \dots$

Mod - 12 using T FF (synchronous)

(Among even number)

state diagram



State table

present state	next state	FF
q ₃ q ₂ q ₁ q ₀	q ₃ ⁺ q ₂ ⁺ q ₁ ⁺ q ₀ ⁺	T ₃ T ₂ T ₁ T ₀
0 0 0 0	0 0 0 0	0 0 1 0
0 0 0 1	0 0 1 0	X X X X
0 0 1 0	0 1 0 0	0 1 0 0
0 0 1 1	X X X X	X X X X
0 1 0 0	0 1 0 0	0 0 1 0
0 1 0 1	X X X X	X X X X
0 1 1 0	0 0 0 0	1 1 0 0
0 1 1 1	X X X X	X X X X
1 0 0 0	0 0 1 0	0 0 1 0
1 0 0 1	X X X X	X X X X
1 0 1 0	0 0 0 0	1 0 0 0
1 0 1 1	X X X X	X X X X
1 1 0 0	X X X X	X X X X
1 1 0 1	X X X X	X X X X
1 1 1 0	X X X X	X X X X

(7) K-map

		Q ₃ Q ₂	00	01	11	10
		Q ₁ Q ₀	00	X	X	X
T ₃		00	X	X	X	X
Q ₃ Q ₂	01	X	X	X	X	X
	11	X	X	X	X	X
Q ₁ Q ₀	00	X	X	X	X	X
	01	X	X	X	X	X

$$T_3 = Q_3 Q_1 + Q_2 Q_1$$

T₂

		Q ₃ Q ₂	00	01	11	10
		Q ₁ Q ₀	00	X	X	X
T ₂		00	X	X	X	X
Q ₃ Q ₂	01	X	X	X	X	X
	11	X	X	X	X	X
Q ₁ Q ₀	00	X	X	X	X	X
	01	X	X	X	X	X

$$T_2 = \overline{Q_3} Q_1$$

T₁

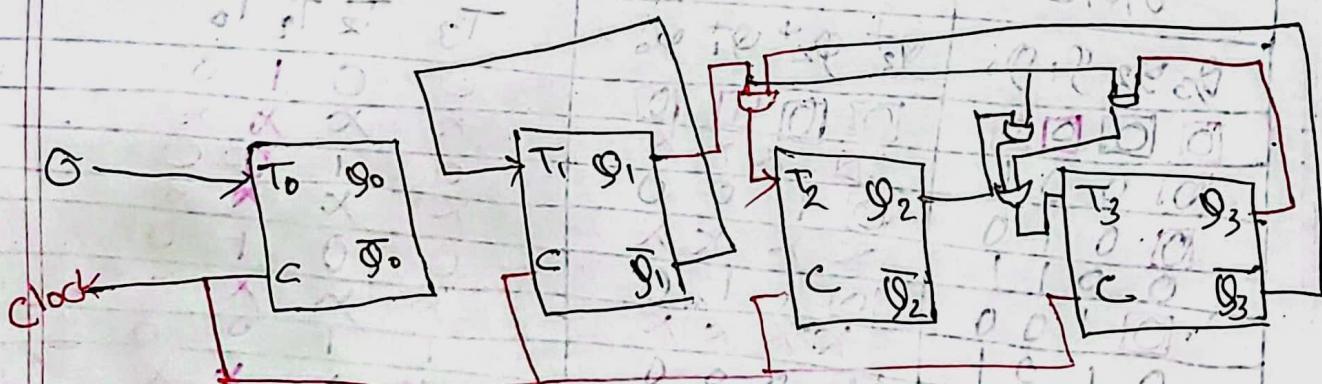
		Q ₃ Q ₂	00	01	11	10
		Q ₁ Q ₀	00	X	X	X
T ₁		00	X	X	X	X
Q ₃ Q ₂	01	X	X	X	X	X
	11	X	X	X	X	X
Q ₁ Q ₀	00	X	X	X	X	X
	01	X	X	X	X	X

$$T_1 = \overline{Q}_1$$

T₀

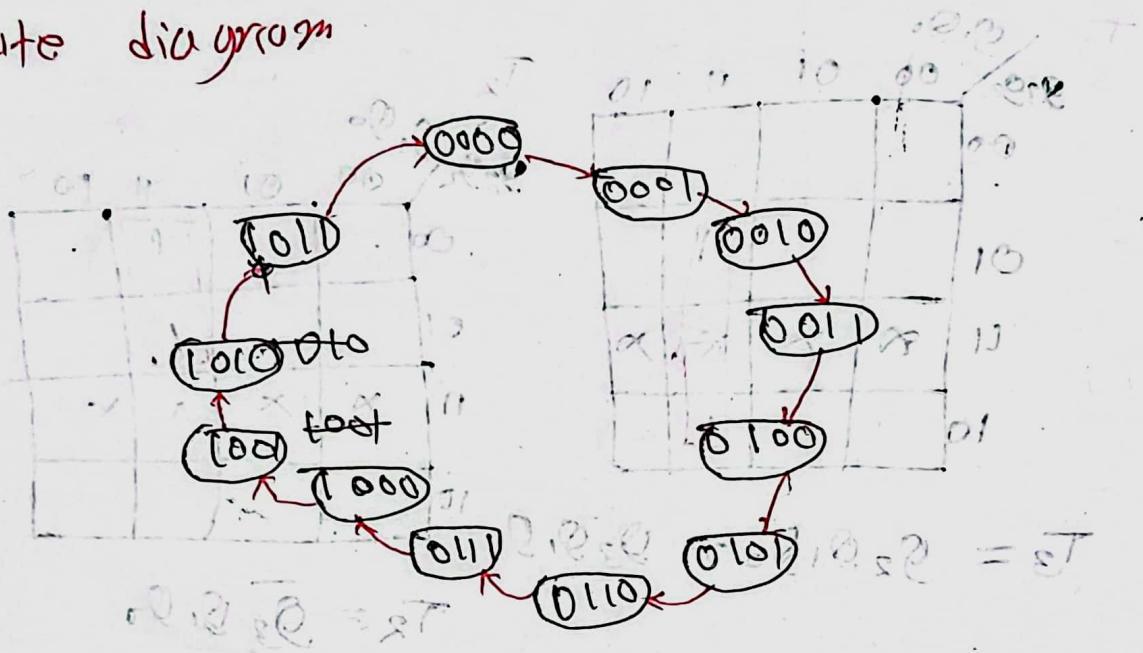
		Q ₃ Q ₂	00	01	11	10
		Q ₁ Q ₀	00	X	X	X
T ₀		00	X	X	X	X
Q ₃ Q ₂	01	X	X	X	X	X
	11	X	X	X	X	X
Q ₁ Q ₀	00	X	X	X	X	X
	01	X	X	X	X	X

$$T_0 = 0$$



⊗⊗⊗ Mod-12 Using T FF (synchronous)

state diagram



state table

present state	next state	FF
0,0,0,0	0,0,0,1	T ₃ T ₂ T ₁ T ₀
0,0,0,1	0,0,1,0	0,0,0,1
0,0,1,0	0,0,1,1	0,0,1,1
0,0,1,1	0,1,0,0	0,1,1,1
0,1,0,0	0,1,0,1	0,0,0,1
0,1,0,1	0,1,1,0	0,0,1,1
0,1,1,0	0,1,1,1	0,0,0,1
0,1,1,1	1,0,0,0	1,1,1,1
1,0,0,0	1,0,0,1	0,0,0,1
1,0,0,1	1,0,1,0	0,0,1,1
1,0,1,0	1,0,1,1	0,0,0,1
1,0,1,1	0,0,0,0	1,0,1,1
1,1,0,0	X X X X	X X X X
1,1,0,1	X X X X	X X X X
1,1,1,0	X X X X	X X X X
1,1,1,1	X X X X	X X X X

K-map

T_3

		Q ₁ Q ₀			
		00	01	11	10
Q ₃ Q ₂	00	0	0	0	0
	01	0	1	1	1
Q ₃ Q ₂	11	1	x	x	x
	10	0	0	1	0

T_2

		Q ₁ Q ₀			
		00	01	11	10
Q ₃ Q ₂	00	0	0	0	0
	01	0	1	1	1
Q ₃ Q ₂	11	x	x	x	x
	10	0	0	0	0

$$T_3 = Q_2 Q_1 Q_0 + Q_3 Q_1 Q_0$$

$$T_2 = \overline{Q}_3 Q_1 Q_0$$

T_1

		Q ₁ Q ₀			
		00	01	11	10
Q ₃ Q ₂	00	0	0	0	0
	01	0	1	1	1
Q ₃ Q ₂	11	x	x	x	x
	10	0	0	0	0

$$T_1 = Q_0$$

		Q ₁ Q ₀			
		00	01	11	10
Q ₃ Q ₂	00	0	0	0	0
	01	0	1	1	1
Q ₃ Q ₂	11	x	x	x	x
	10	0	0	0	0

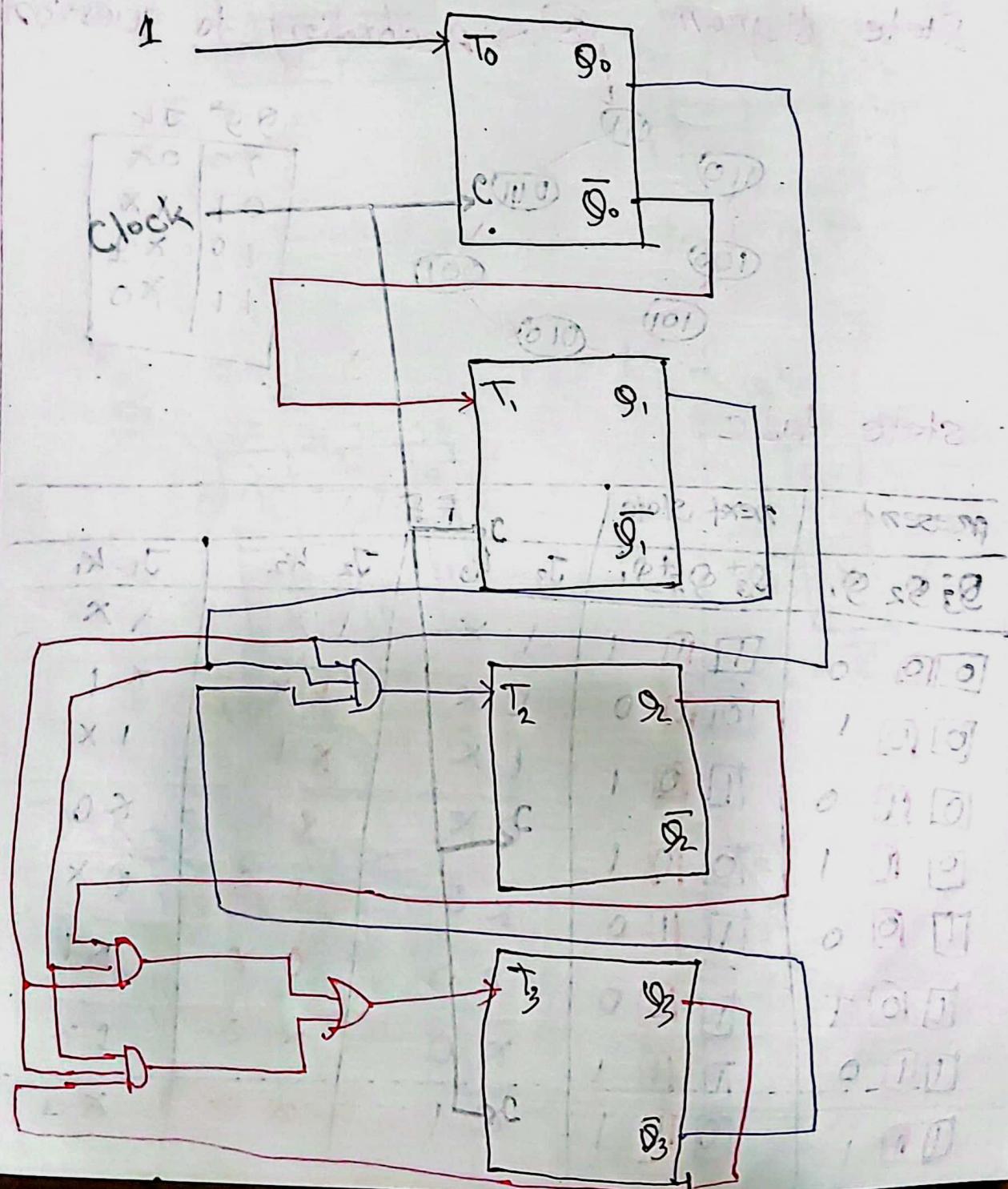
$$\overline{T_0} = 1$$

state table
circuit

$(Q_3 \rightarrow Q_2 \rightarrow Q_1 \rightarrow Q_0)$

$(T_0 \rightarrow T_1 \rightarrow T_2 \rightarrow T_3)$

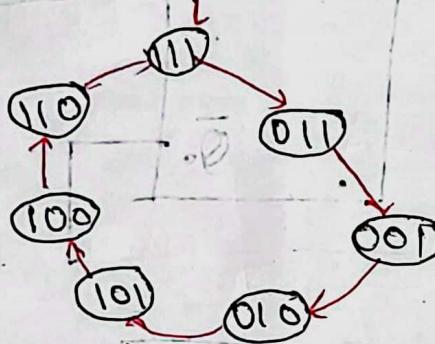
→ circuit diagram



Arbitrary counter (synchronous)

7, 2, 1, 2, 5, 4, 6, 7, ...

State diagram \Rightarrow According to question



Q_3^{gt}	Q_2^{gt}	Q_1^{gt}	J_K
0	0	0	0X
0	0	1	1X
0	1	0	X1
0	1	1	X0
1	0	0	0X
1	0	1	0X
1	1	0	X0
1	1	1	X0

state table

present	next state	FF					
$Q_3 Q_2 Q_1$	$Q_3^{gt} Q_2^{gt} Q_1^{gt}$	J_3	K_3	J_2	K_2	J_1	K_1
000	0	1	X	1	X	1	X
000	1	0	X	1	X	X1	
010	0	1	X	X1		1X	
010	1	0	X	X1		X0	
100	0	X0		1	X	0X	
100	1	0	X0	0	X	X1	
110	0	X1		X0		CX	
110	1	1	X1	X0		X0	

K-map

$J_3 \backslash Q_2 Q_1$	00	01	11	10
0	1	X	X	X
1	X	X	X	1

$$J_3 = \overline{Q}_1$$

$K_3 \backslash Q_2 Q_1$	00	01	11	10
0	X	X	X	1
1	1	X	X	X

$$K_3 = Q_2 Q_1$$

$J_2 \backslash Q_2 Q_1$	00	01	11	10
0	1	1	X	X
1	1	X	X	1

$$J_2 = \overline{Q}_1 + \overline{Q}_3$$

$K_2 \backslash Q_2 Q_1$	00	01	11	10
0	X	X	1	1
1	X	X	X	X

$$K_2 = \overline{Q}_3$$

$J_1 \backslash Q_2 Q_1$	00	01	11	10
0	1	X	X	1
1	X	X	1	1

$$J_1 = \overline{Q}_3 + Q_2$$

$K_1 \backslash Q_2 Q_1$	00	01	11	10
0	X	1	X	X
1	X	1	X	X

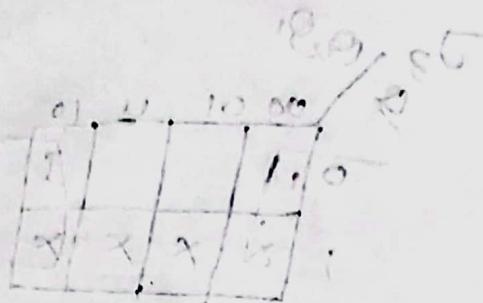
$$K_1 = \overline{Q}_2$$

Circuit diagram

$$J_3 = \bar{Q}_1 \quad K_3 = Q_2 \bar{Q}_1$$

$$J_2 = \bar{Q}_1 + \bar{Q}_2 \quad K_2 = \bar{Q}_3$$

$$J_1 = \bar{Q}_3 + Q_2 \quad K_1 = \bar{Q}_2$$



$$\bar{Q} = S5$$

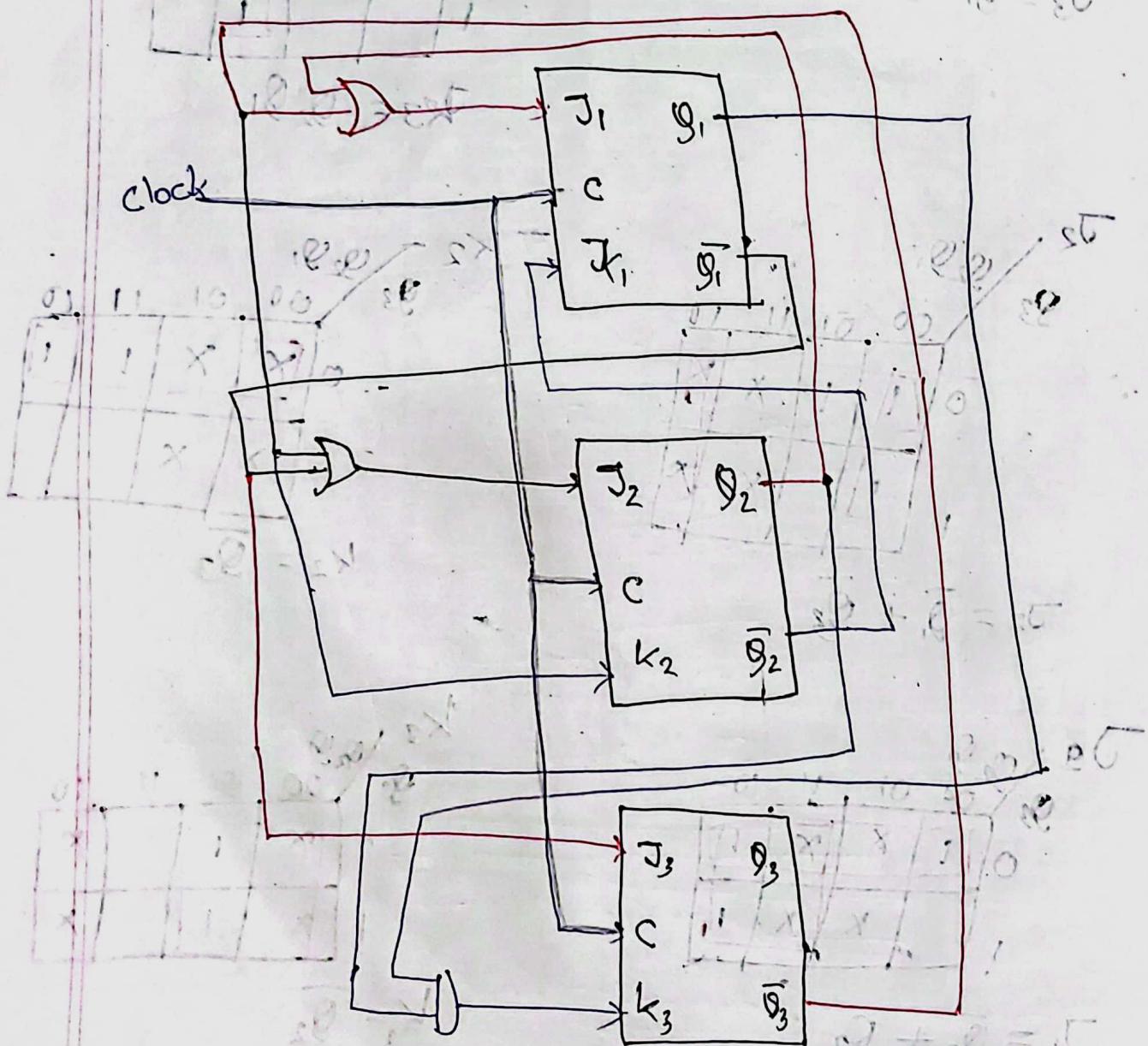
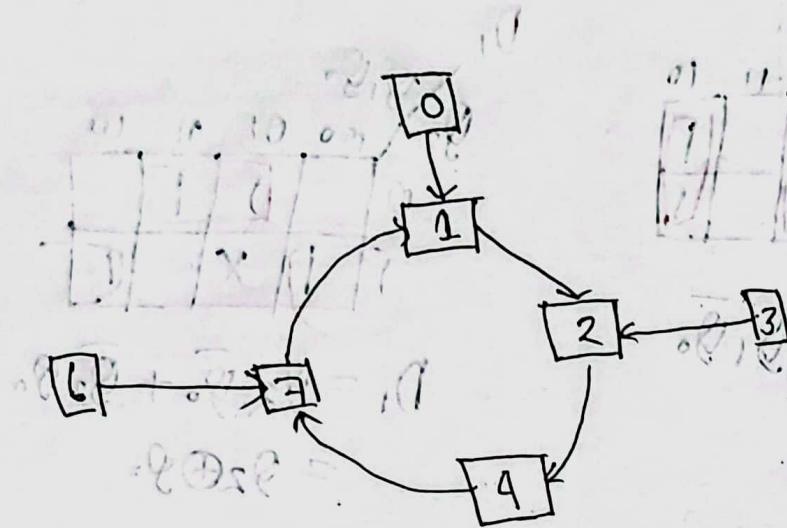


diagram to circuit (counter)



state table

present state	next state	FF assignments
$g_2\ g_1\ g_0$	$g_2^+\ g_1^+\ g_0^+$	$D_2\ D_1\ D_0$
0 0 0	0 0 1	0 0 1
0 0 1	0 1 0	0 1 0
0 1 0	0 1 0	1 0 0
0 1 1	0 1 0	0 1 0
1 0 0	1 1 1	1 1 1
1 0 1	x x x	x x x
1 1 0	1 1 1	1 1 1
1 1 1	0 0 1	0 0 1

- i) PIPD
- ii) SISO
- iii) PISO
- iv) SIPO

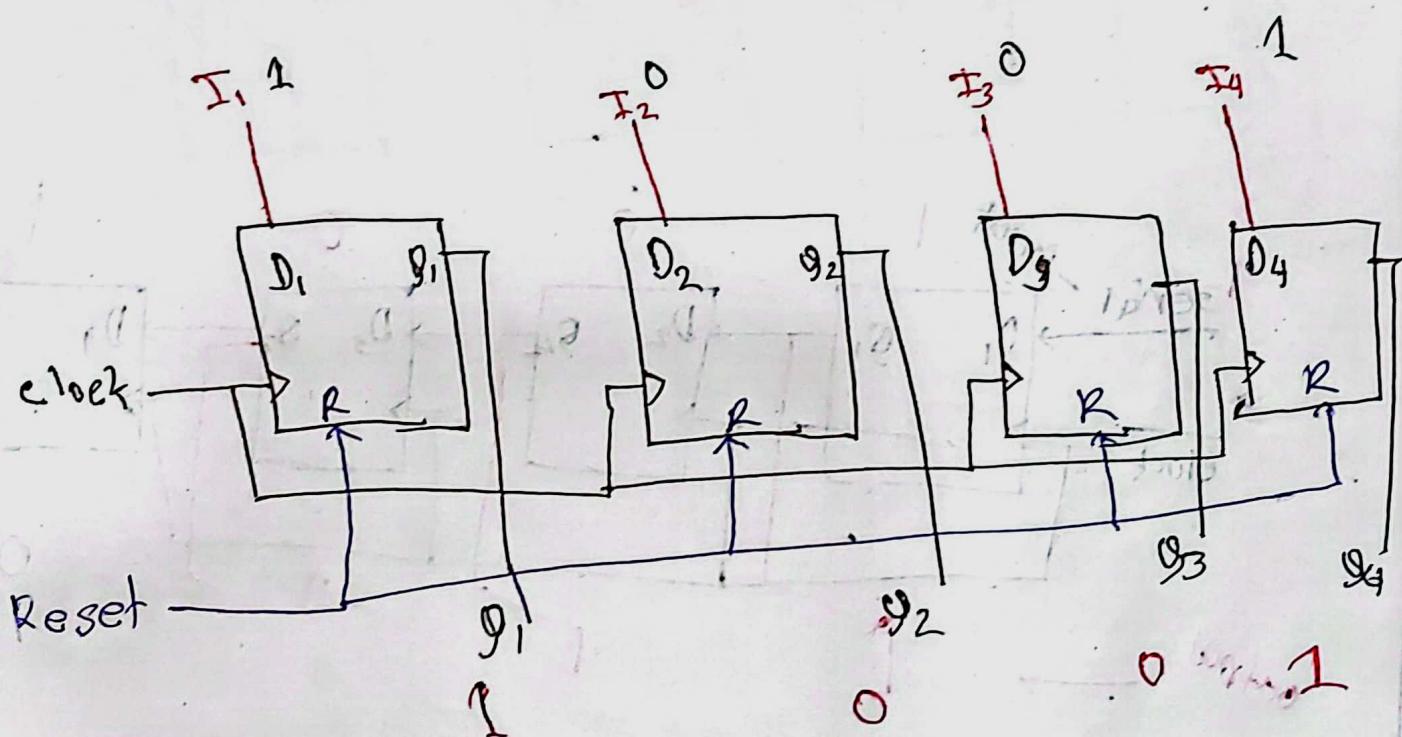
Register

মাত্র bit Register ওর bit memory store

কথা মাত্র

মাত্র bit store কোরে তত গুলা FF নাসকে।

① PIPD (Register with parallel load)



$R=1$ এর clock এর মাত্র ক্ষেত্রে পরিপন্থ নয় (o)

21st - খণ্ড 1

Shift Register (Right)

Right shift

Left shift

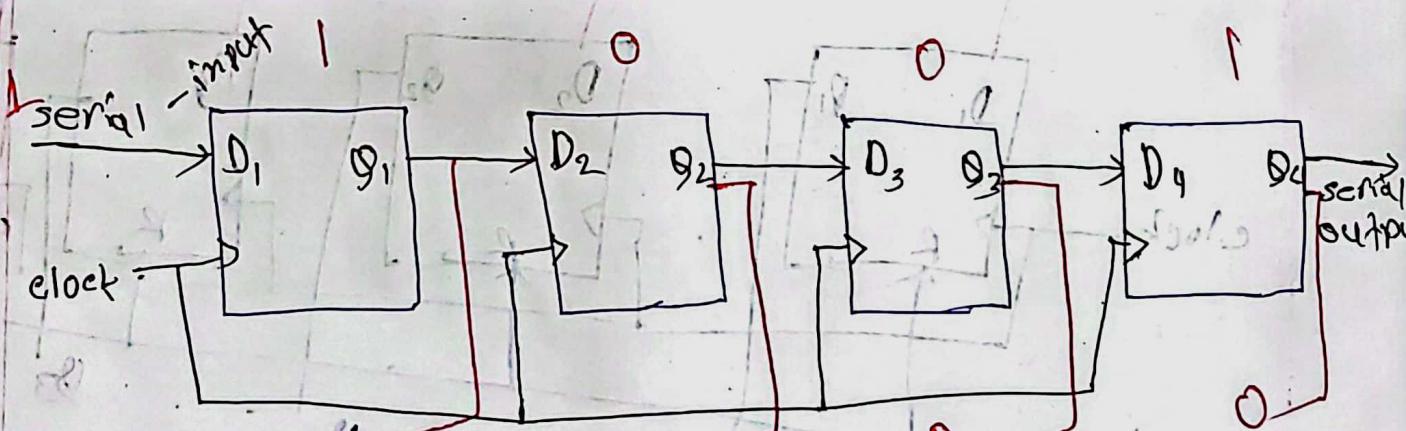
Left shift

Right shift

$\rightarrow 0101_0x$
entry

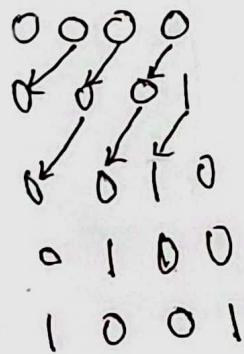
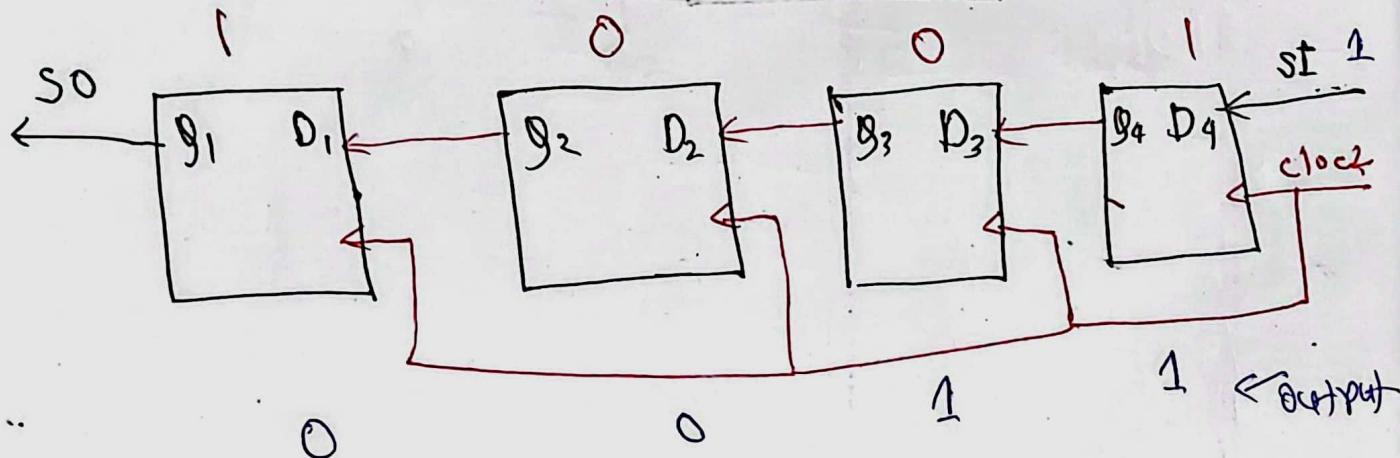
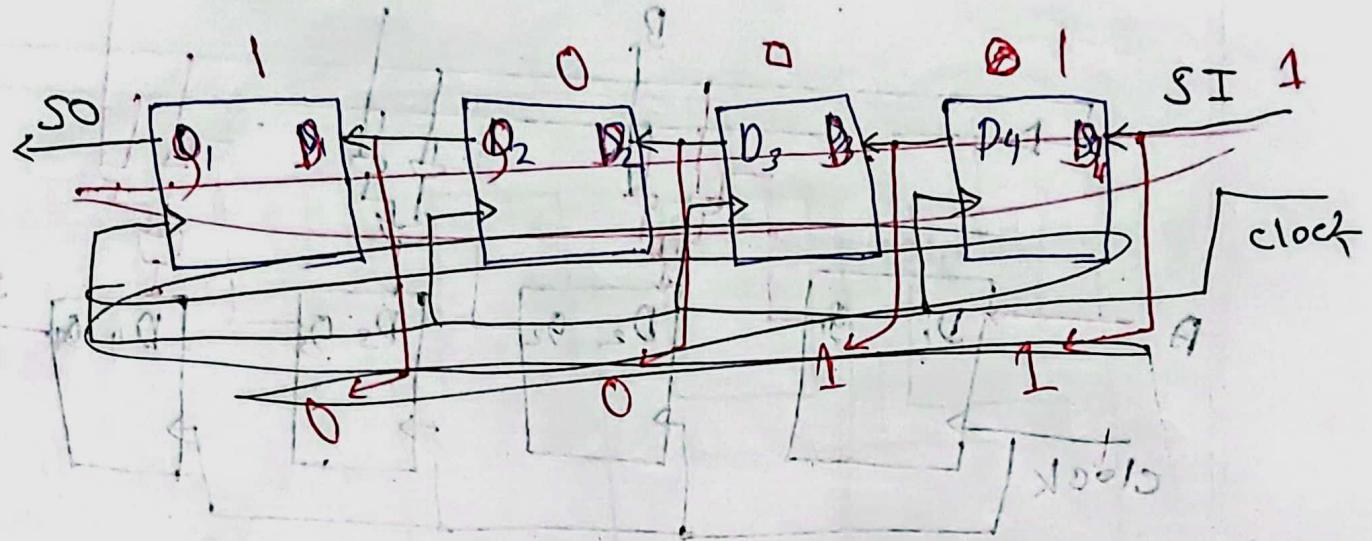
0101_0x

SISO (Right Shift Register)

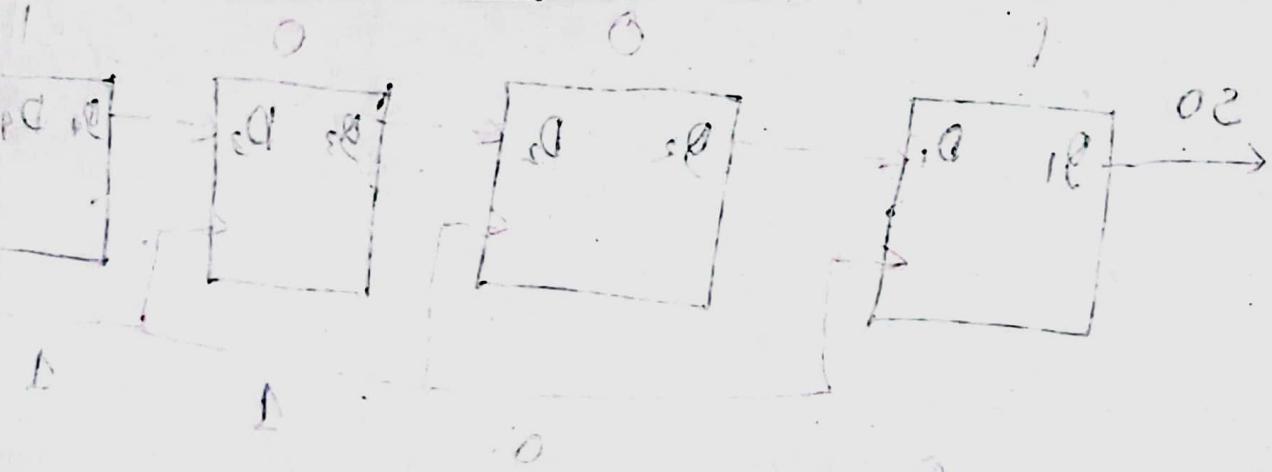
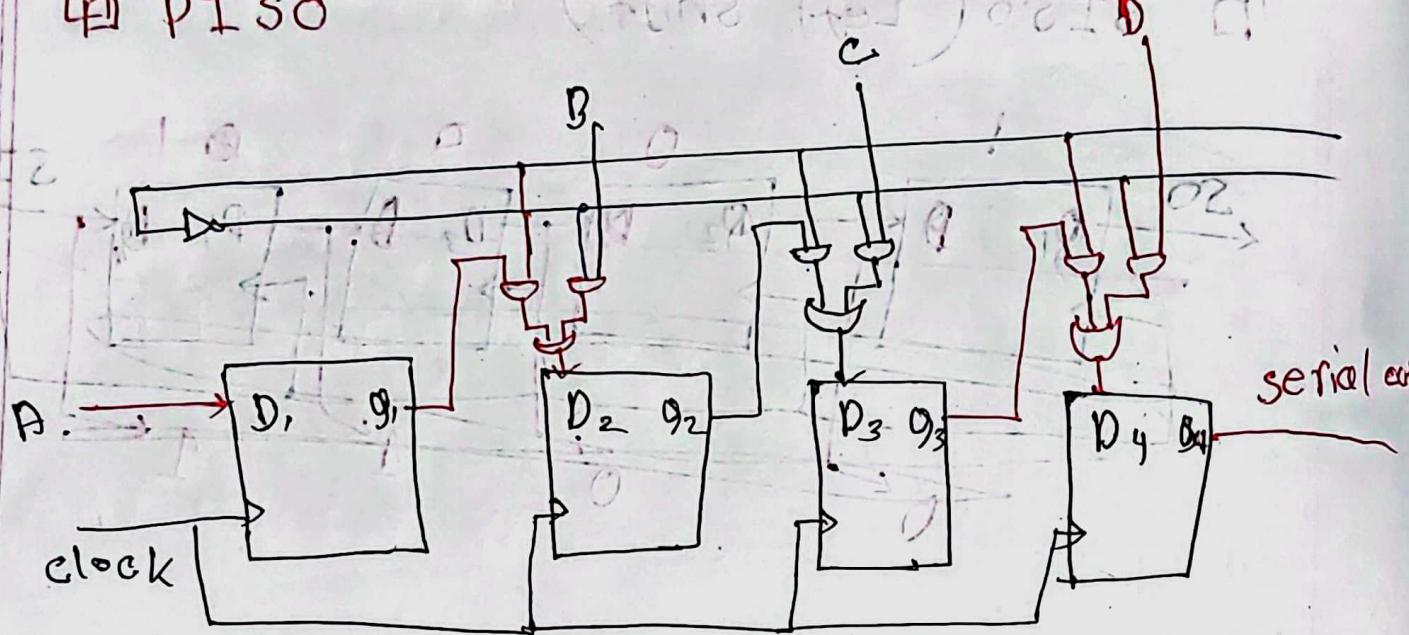


Q1 SISO (Left shift)

02/19/21

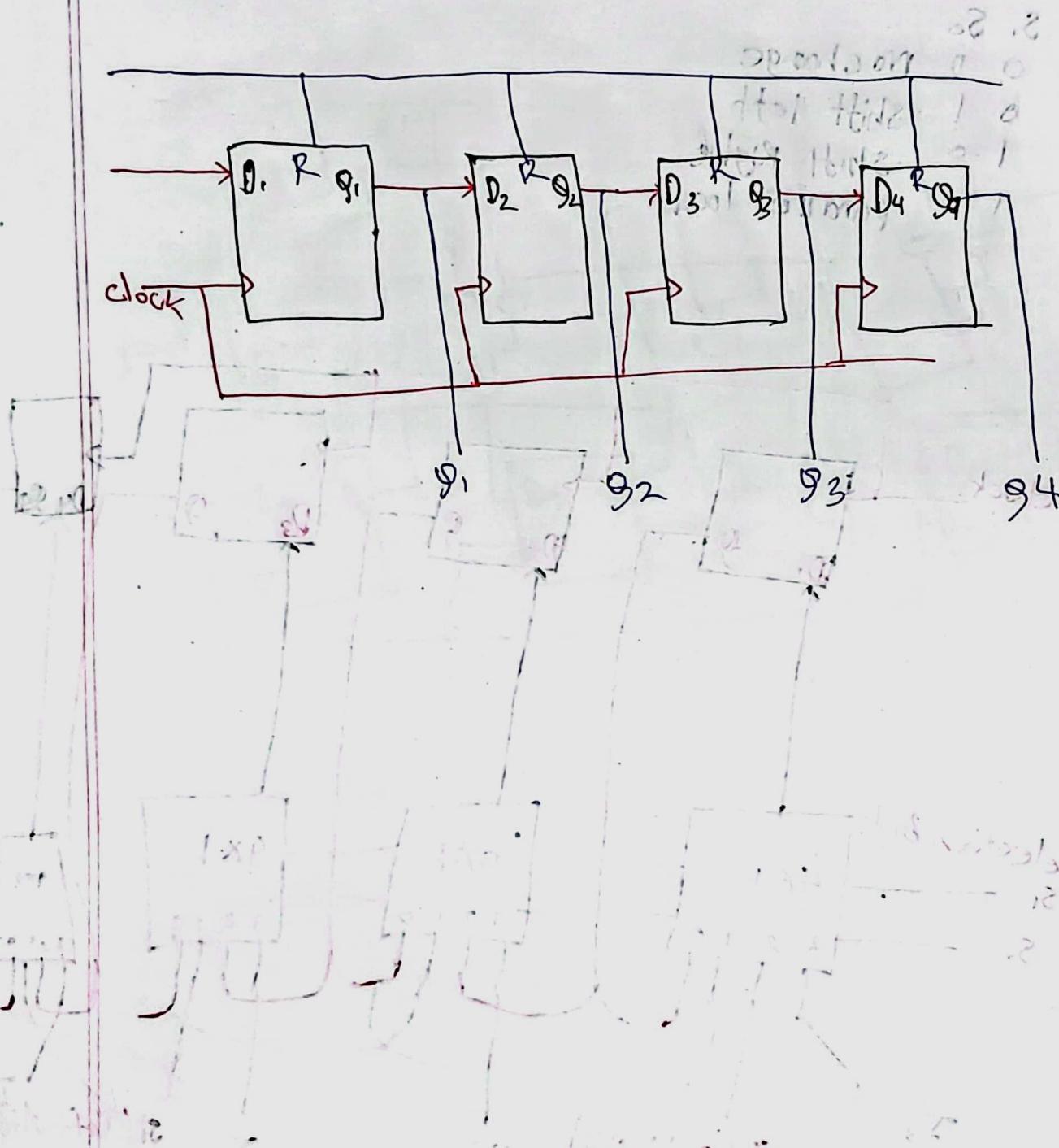


PISO



0000
0010
0011
1001

SISO



Q4 Universal shift register

Q5 Bidirectional shift with parallel Load

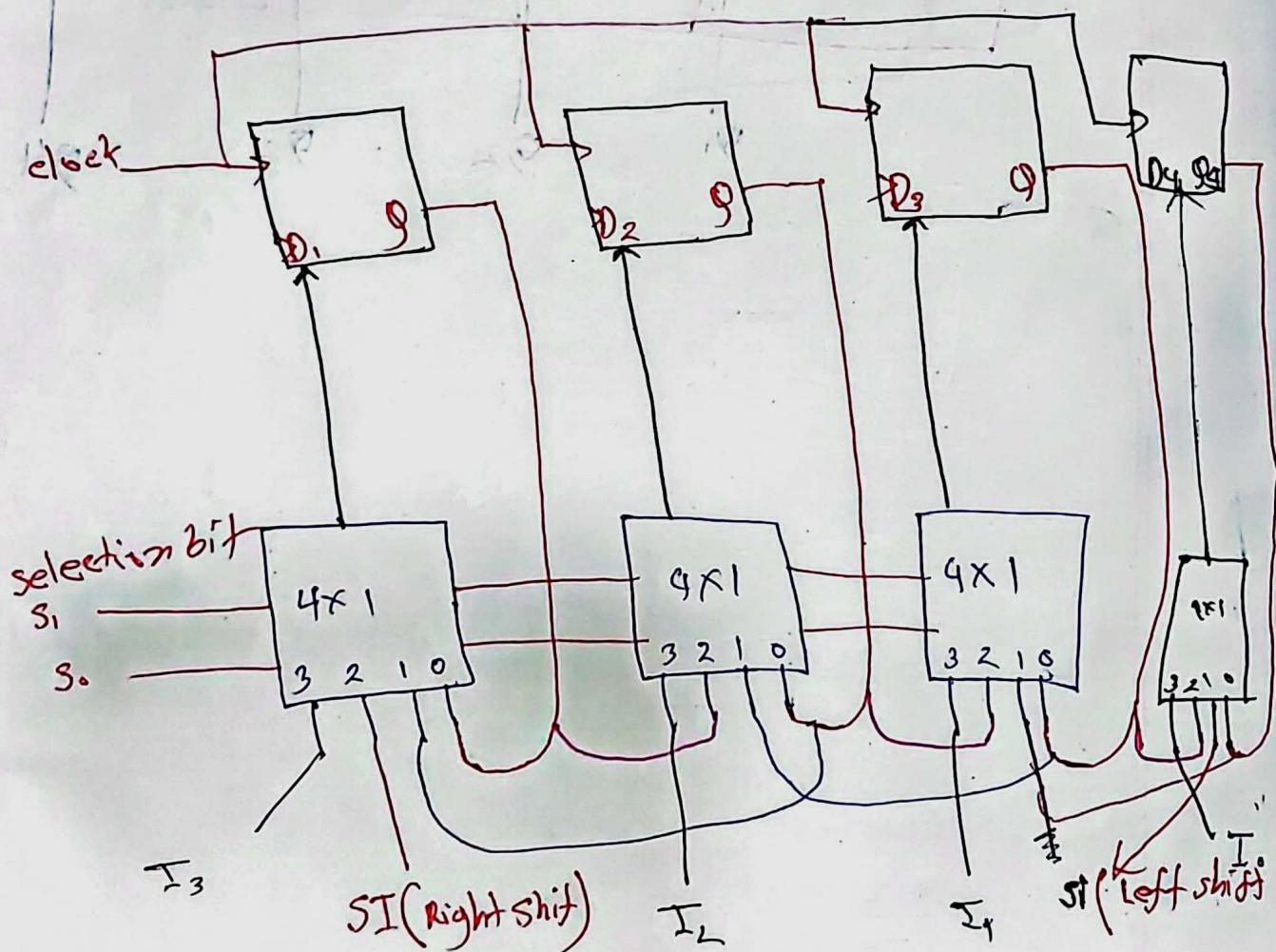
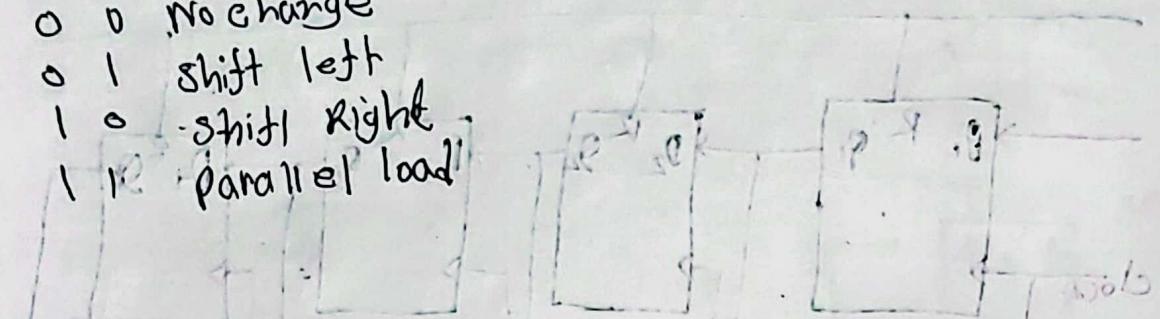
S₁ S₀

0 0 No change

0 1 Shift left

1 0 Shift Right

1 1 Parallel load



Bidirectional shift Register

mode control

