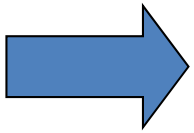
Chapter 7 Flip-Flops and Related Devices

触发器以及相关设备

- Logic circuits
  - Combinational Circuits（组合电路）
  - Sequential Circuits（时序电路）

Basic Block  Flip-Flops

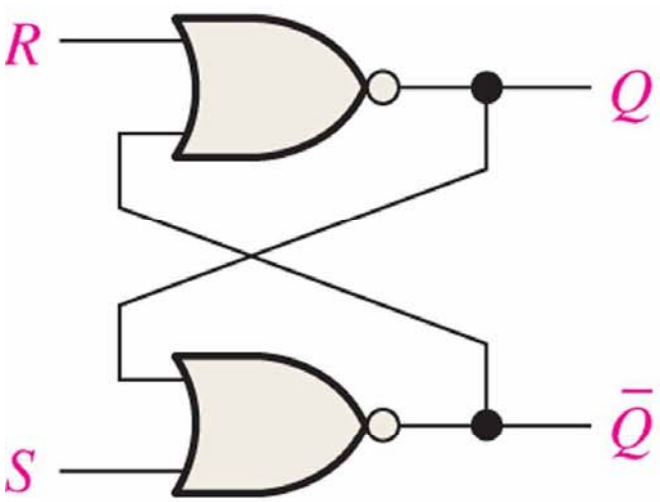
- ***Objectives***
  - Latches（锁存器）
  - Edge-triggered Flip-Flops（边沿触发器）
    - S-R FF
    - D FF
    - J-K FF
    - T FF

7.1 Latches（锁存器）

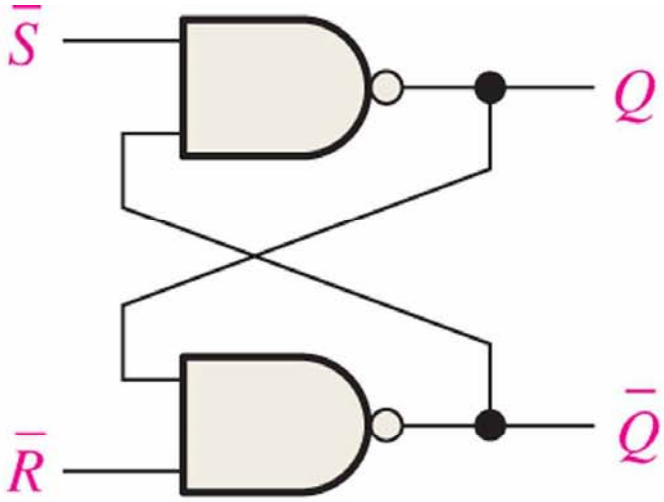
- The ***latch*** is a type of temporary device that has two stable states (***bistable***) and is normally placed in a category separate from that of ***flip-flops***.
- The difference between latches and flip-flops is the method used for changing their states.

- *Latches*
  - S-R (Set-Reset) Latch (SR锁存器)
  - Gated S-R Latch (门控锁存器)
  - Gated D (Data) Latch

7.1.1 S-R (Set-Reset) Latch

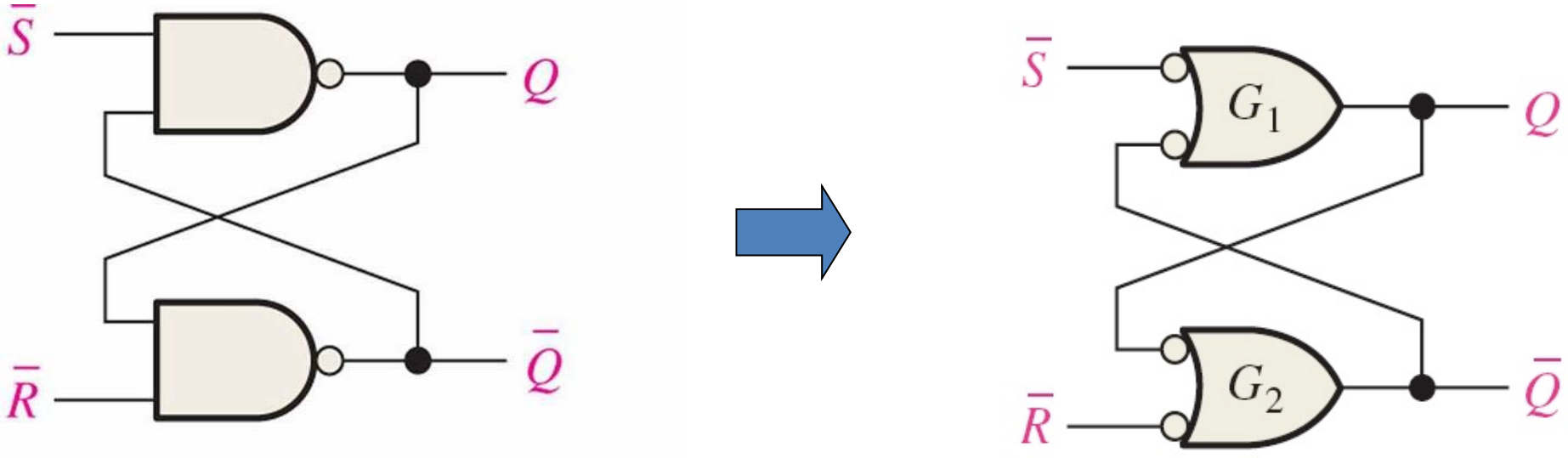


(a) Active-HIGH input S-R latch

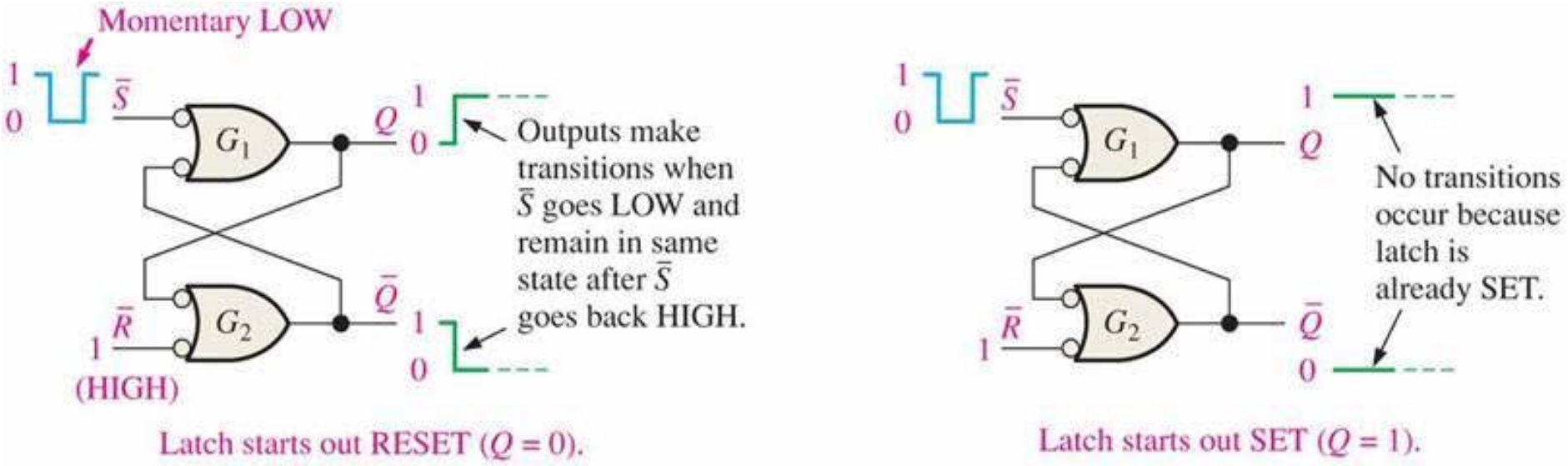


(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

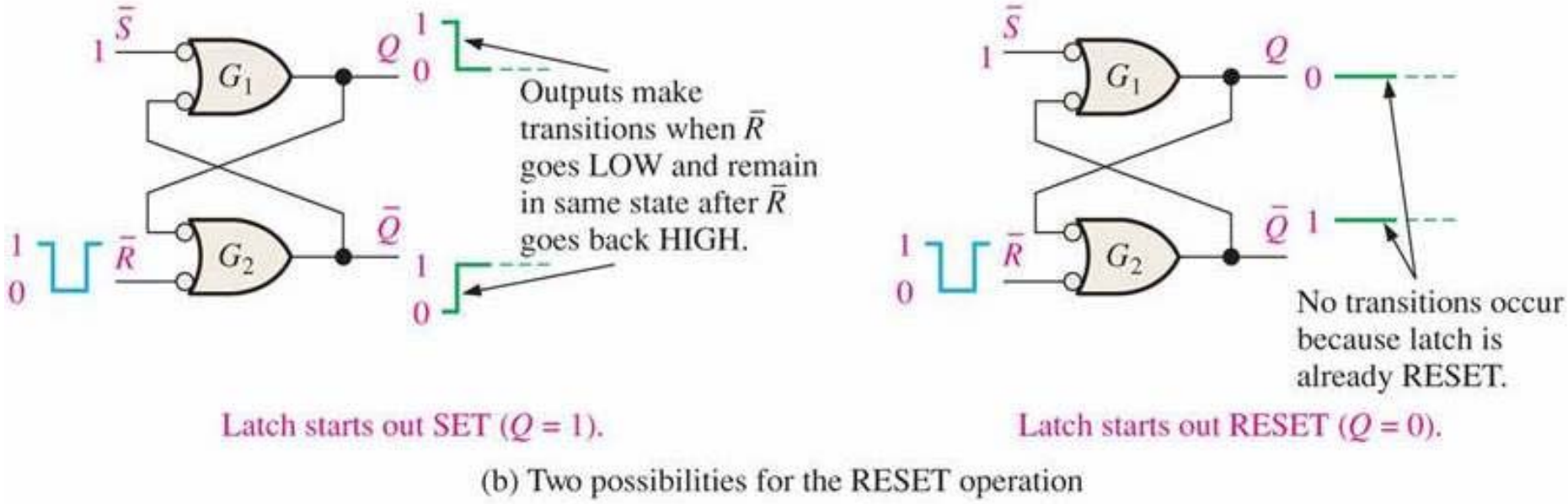
Active-LOW input S-R latch



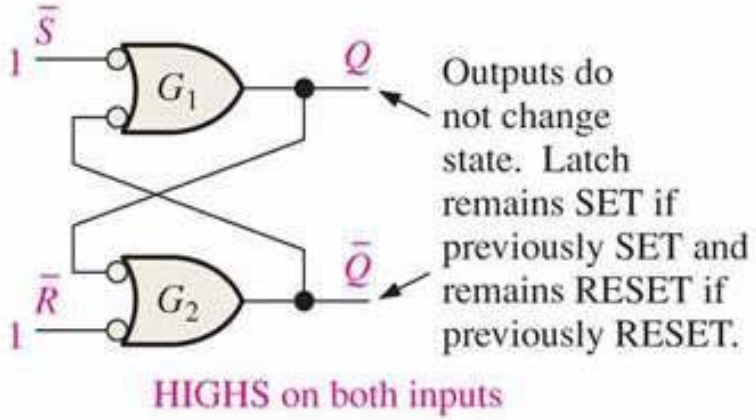
(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch



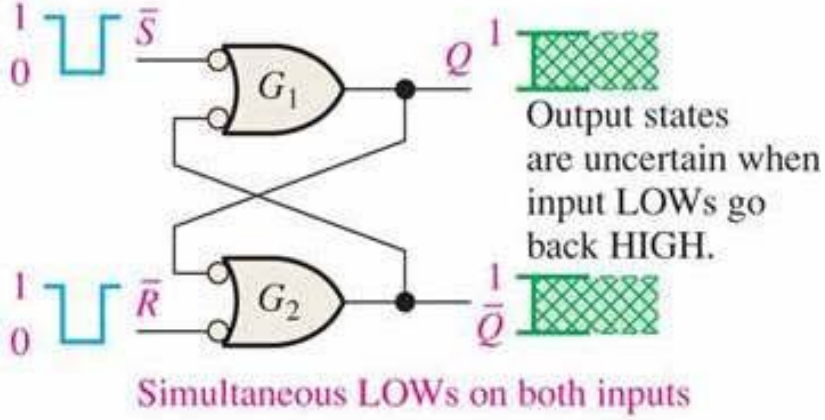
(a) Two possibilities for the SET operation



(b) Two possibilities for the RESET operation



(c) No-change condition

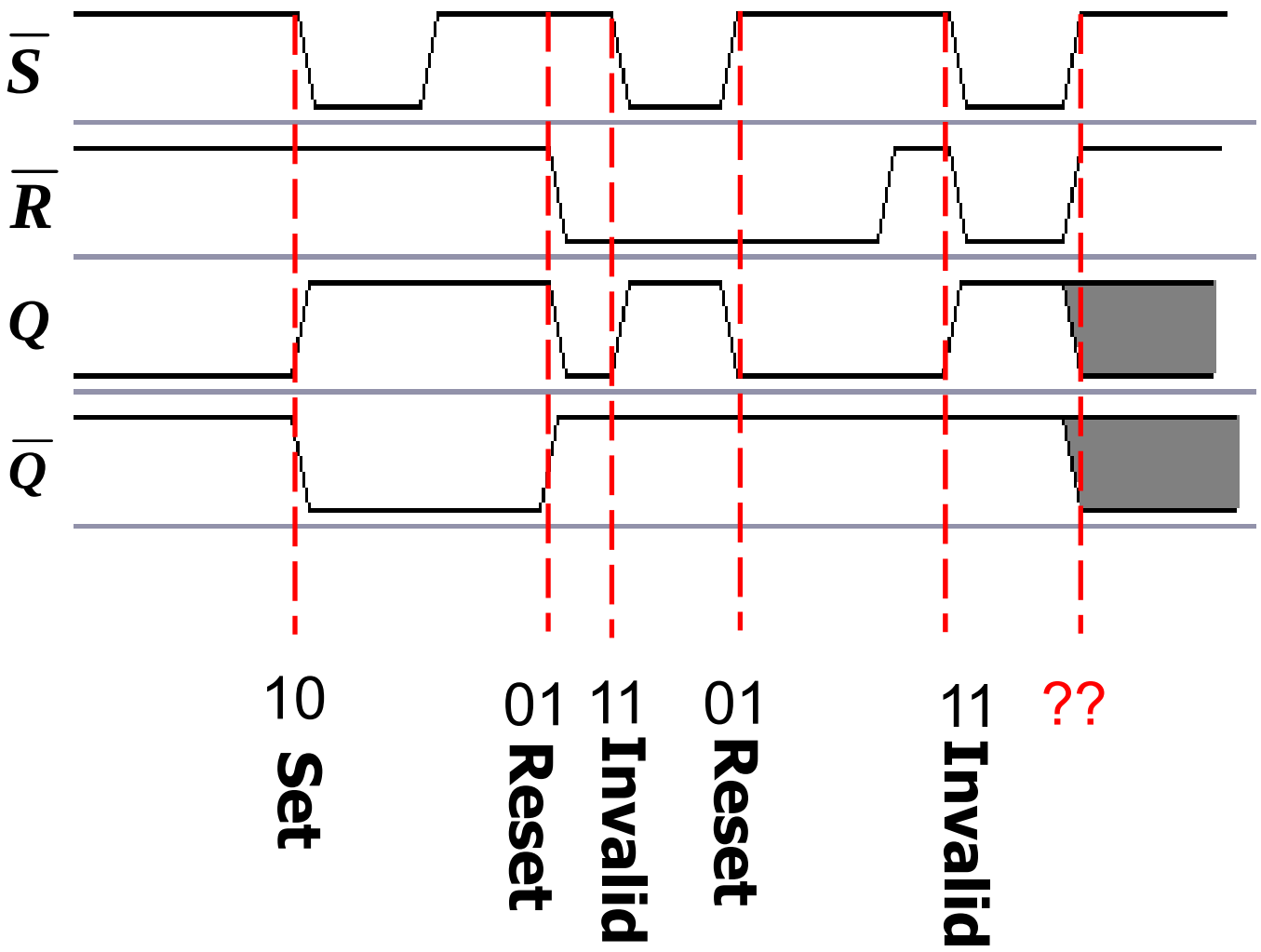


(d) Invalid condition

Truth Table（真值表）

Inputs		Outputs		Comments
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1*	1*	Invalid condition

Timing diagram



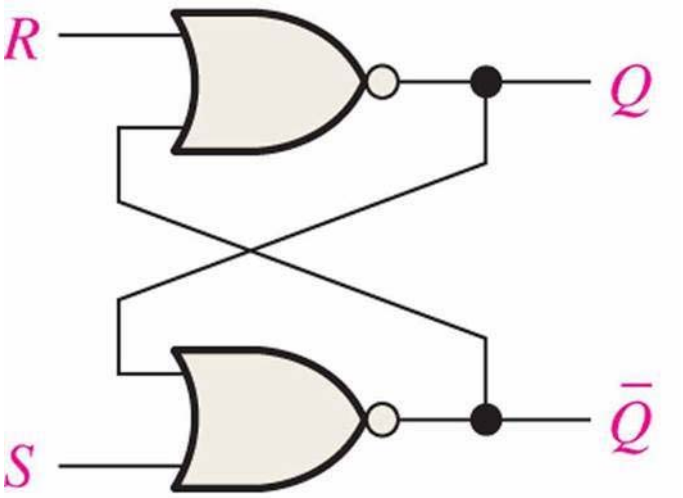
Memory Function

$S=1;\ R=0;\begin{cases} Q=0 \\ \overline{Q}=1 \end{cases}$ “0”, remember “0”

$S=0;\ R=1;\begin{cases} Q=1 \\ \overline{Q}=0 \end{cases}$ “1”, remember “1”

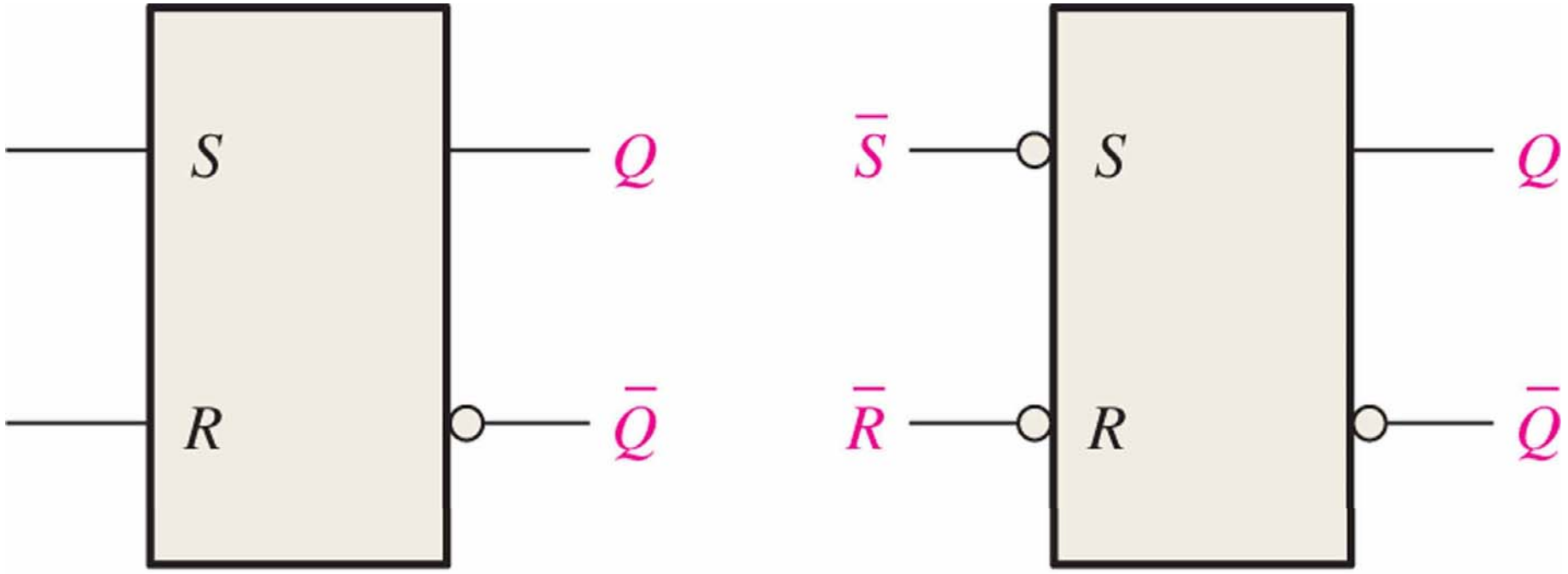
Bi-stable ⇒ **Used to store 1 bit binary number**

Active-HIGH input S-R latch



R	S	Q	$\bar{Q}$
0	0	Q_0	$\bar{Q}_0$
0	1	1	0
1	0	0	1
1	1	0^*	0^*

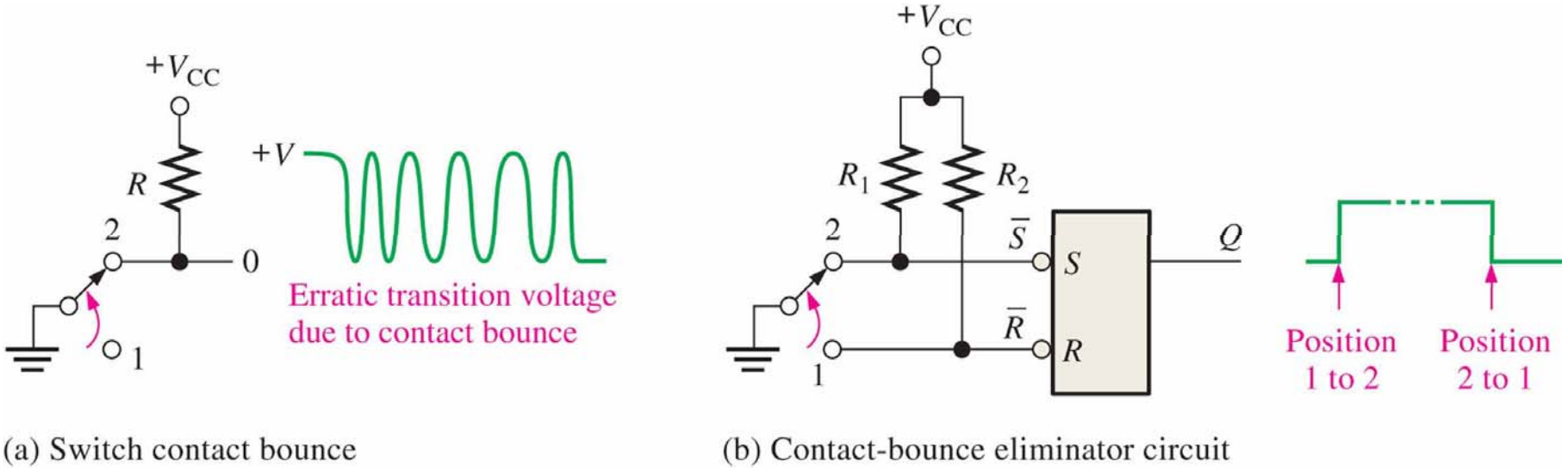
Logic Symbol



(a) Active-HIGH input S-R latch

(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

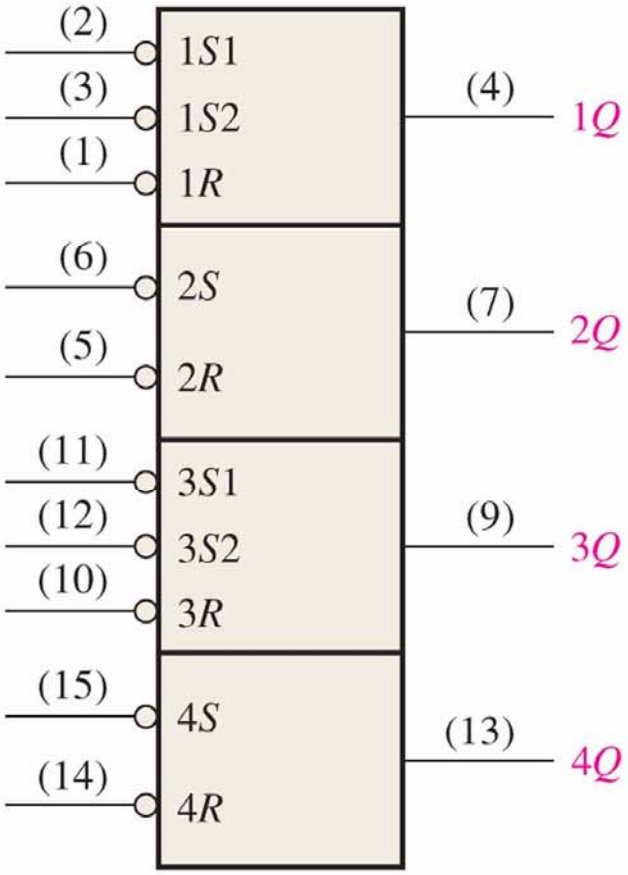
Application Example



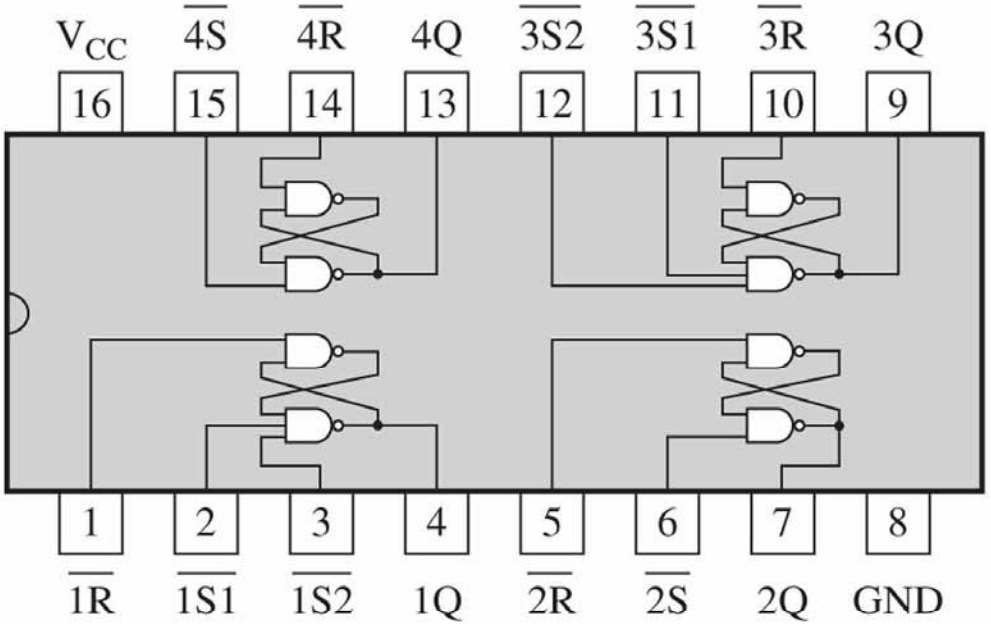
(a) Switch contact bounce

(b) Contact-bounce eliminator circuit

74LS279



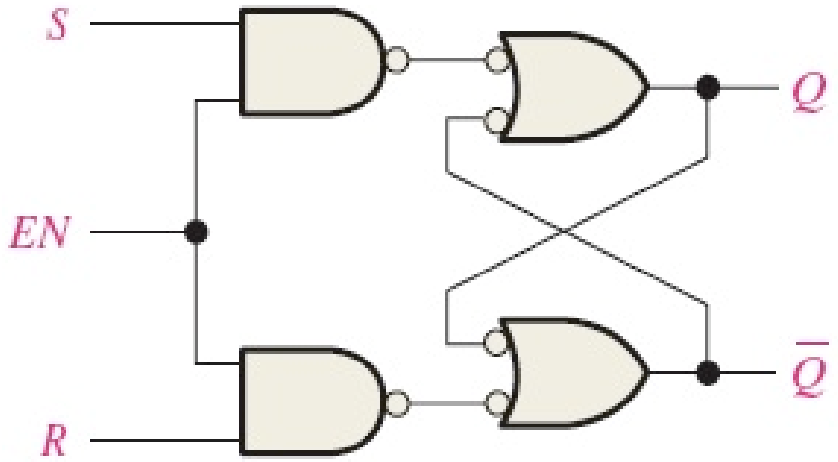
(a) Logic diagram



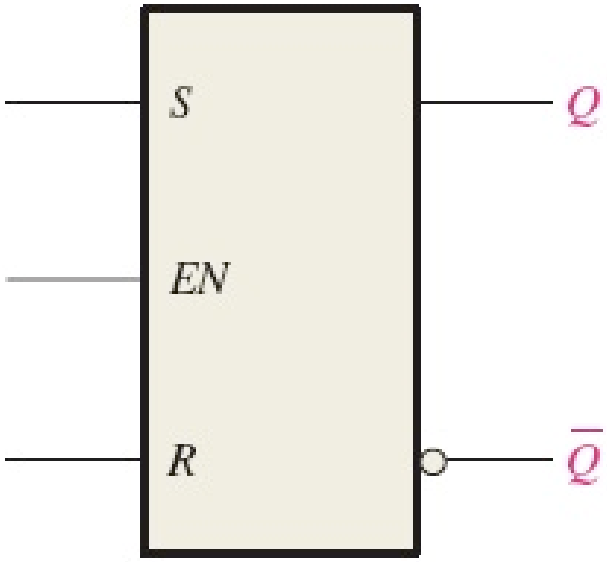
(b) Pin diagram

7.1.2 The Gated S-R Latch（门控S-R锁存器）

EN: control the time when the inputs S and R can control the output. (Level-triggered)

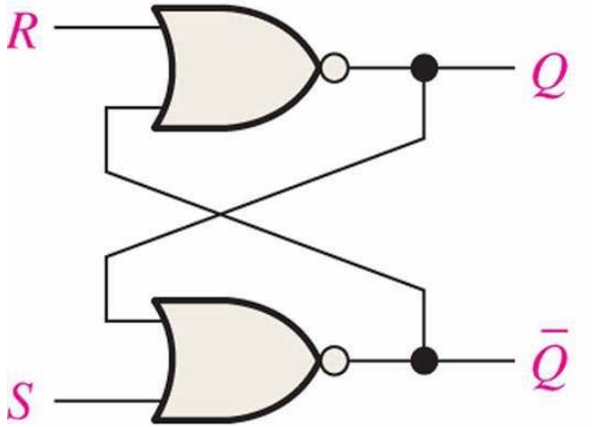


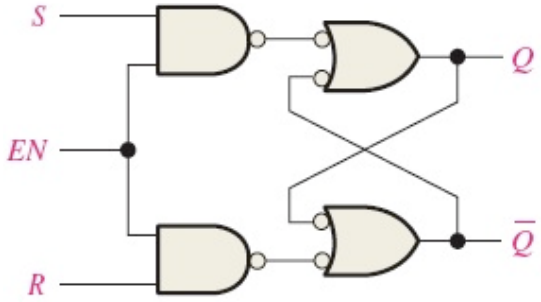
(a) Logic diagram



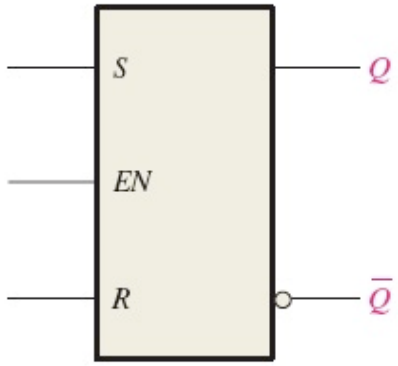
(b) Logic symbol

Comparison





(a) Logic diagram



(b) Logic symbol

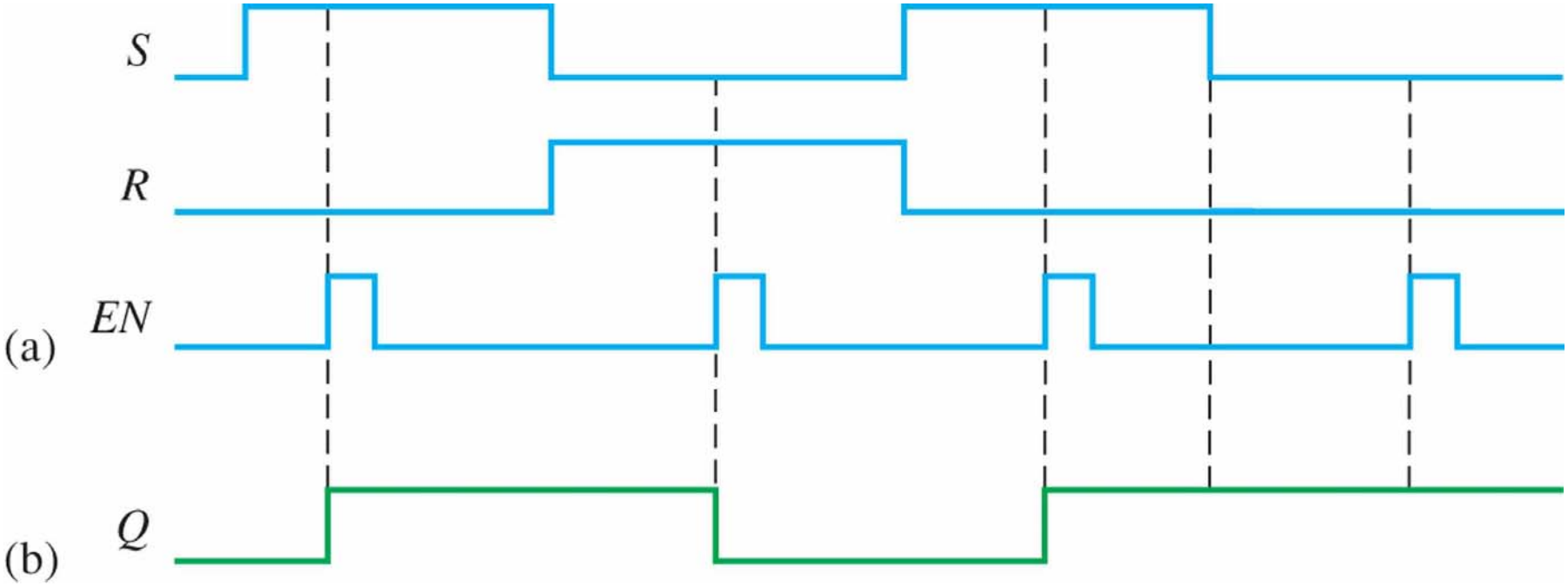
R	S	Q	$\overline{Q}$
0	0	Q_0	$\overline{Q_0}$
0	1	1	0
1	0	0	1
1	1	1^*	1^*

?

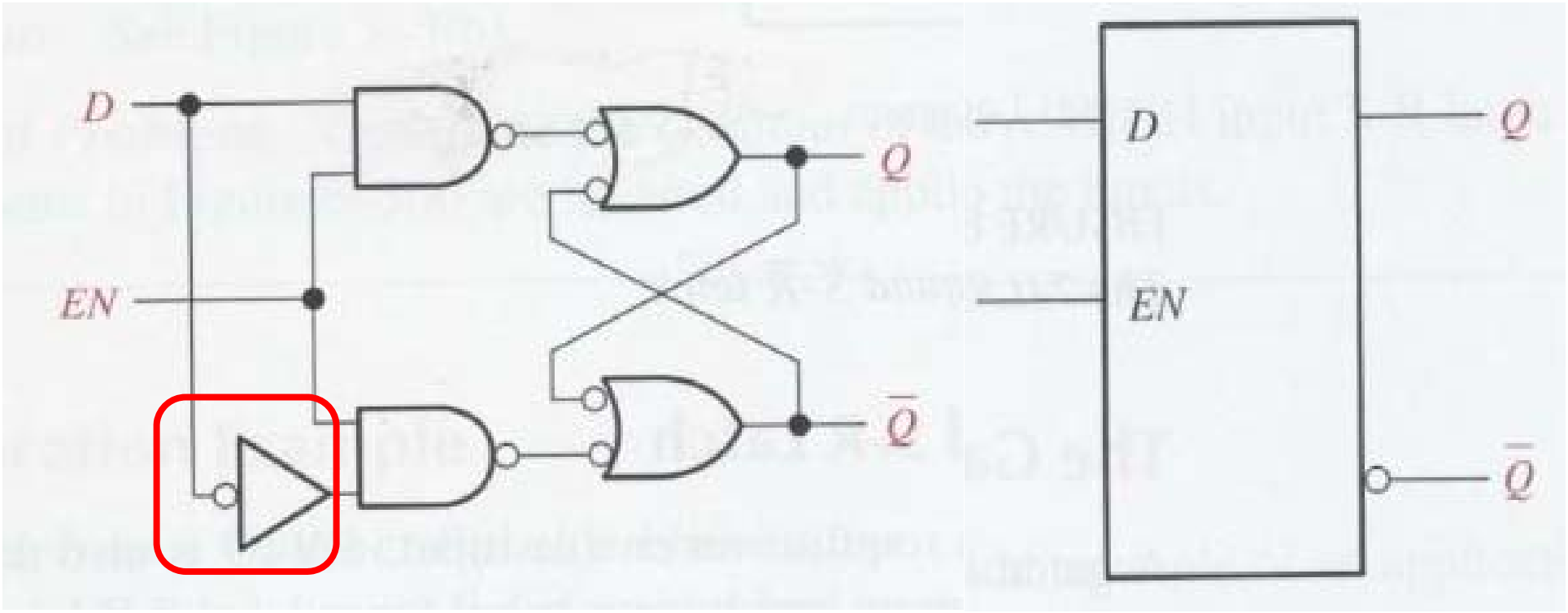
E	R	S	Q	$\overline{Q}$
0	X	X	Q_0	$\overline{Q_0}$
1	0	0	Q_0	$\overline{Q_0}$
1	0	1	1	0
1	1	0	0	1
1	1	1	1^*	1^*

?

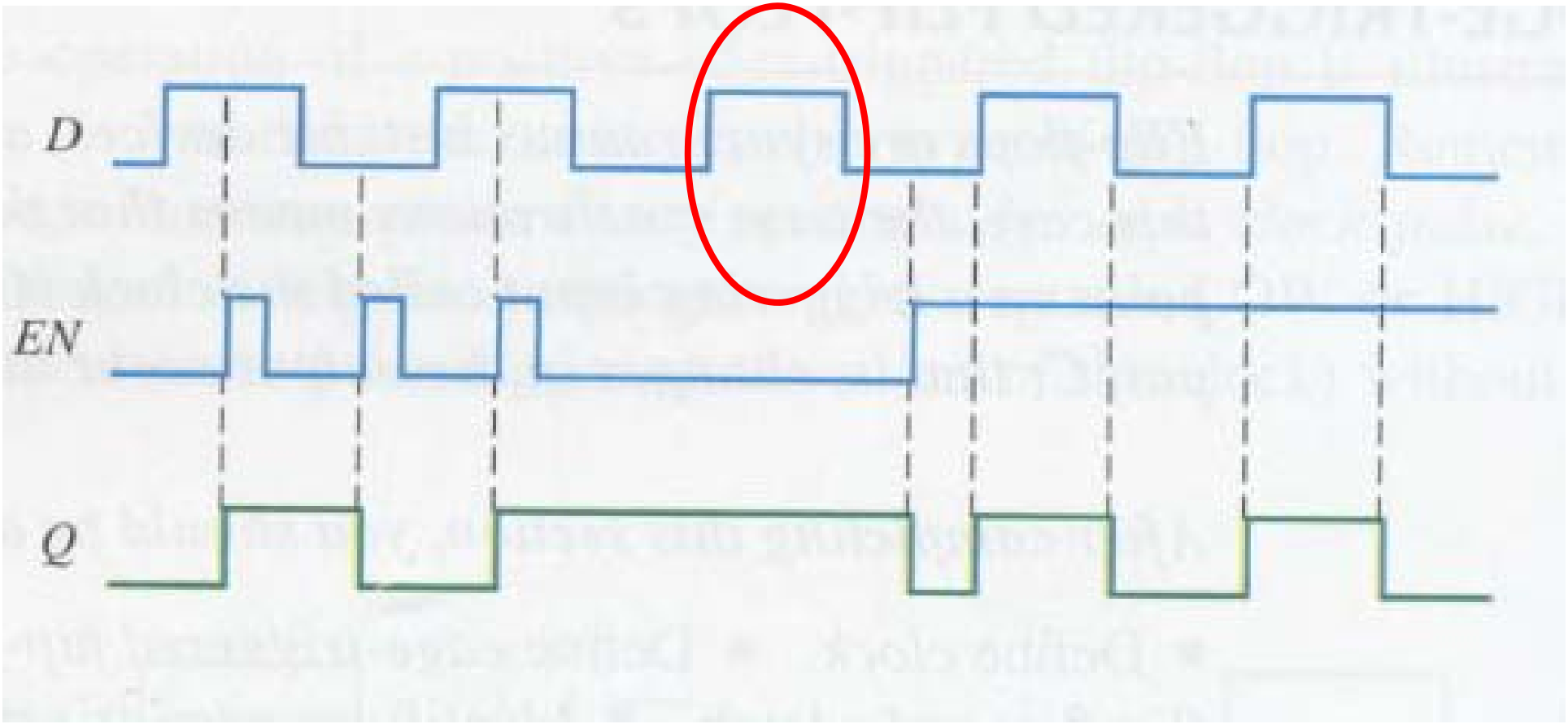
Gated S-R Latch Waveform



7.1.3 The Gated D Latch



Gated D Latch Waveform



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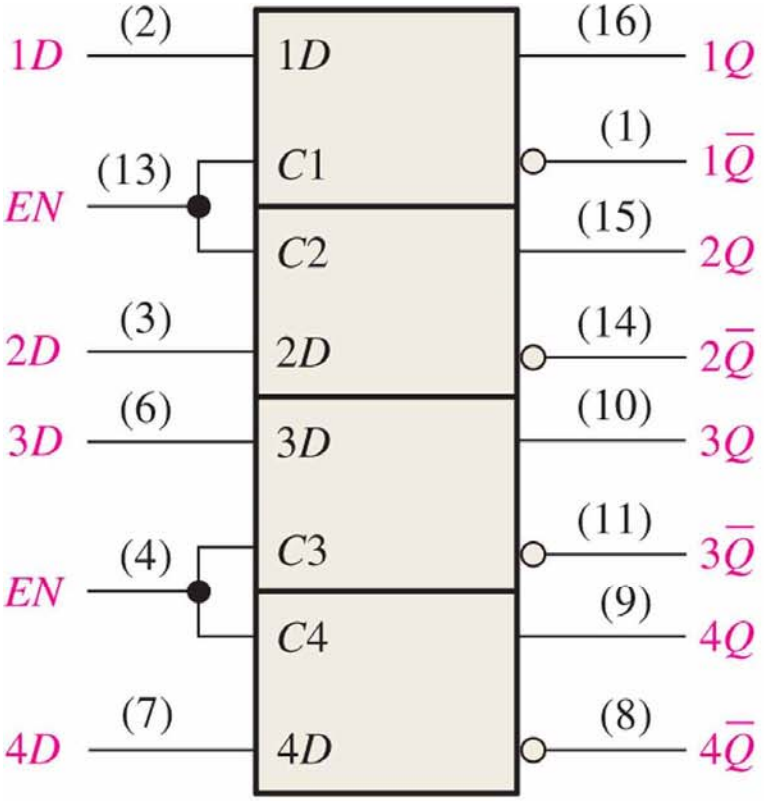


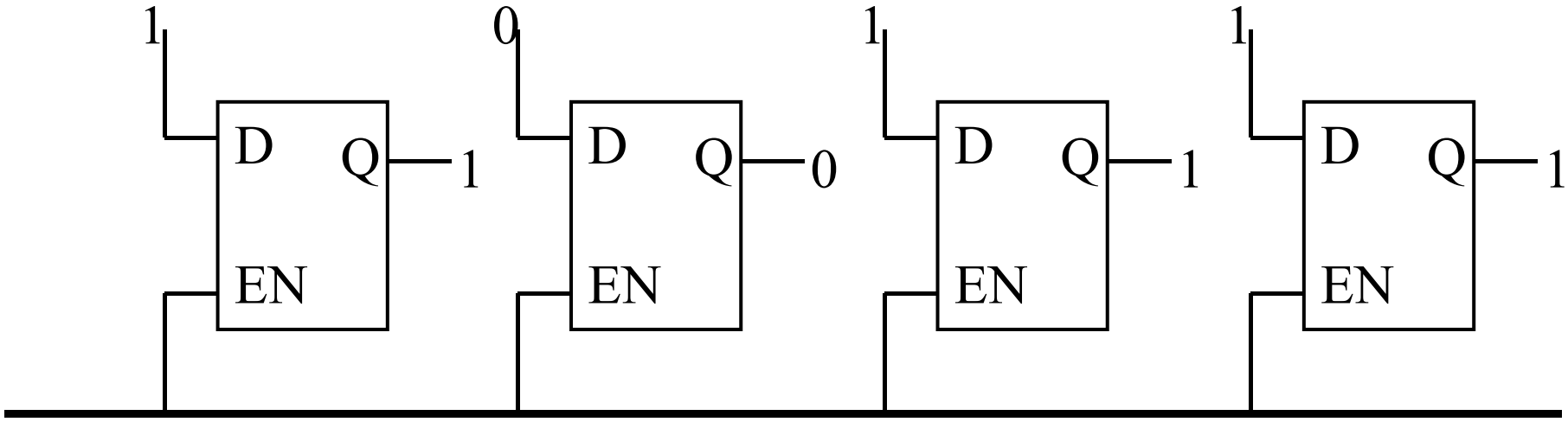
(a) Logic symbol

INPUTS		OUTPUTS		
D	*EN*	*Q*	$\overline{Q}$	COMMENTS
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\overline{Q}_0$	No change

Note: Q_0 is the prior output level before the indicated input conditions were established.

(b) Truth table (each latch)

Application example: Latches for temporary data storage



7.2 Edge-triggered Flip-Flops
边沿触发的触发器

- Flip-flops are ***synchronous bi-stable*** devices. The term ***synchronous*** means that the output changes state only at a specified point on a triggering input called the clock (CLK) is designated as a control input C. i.e., changes in the output occur in synchronous with the clock.

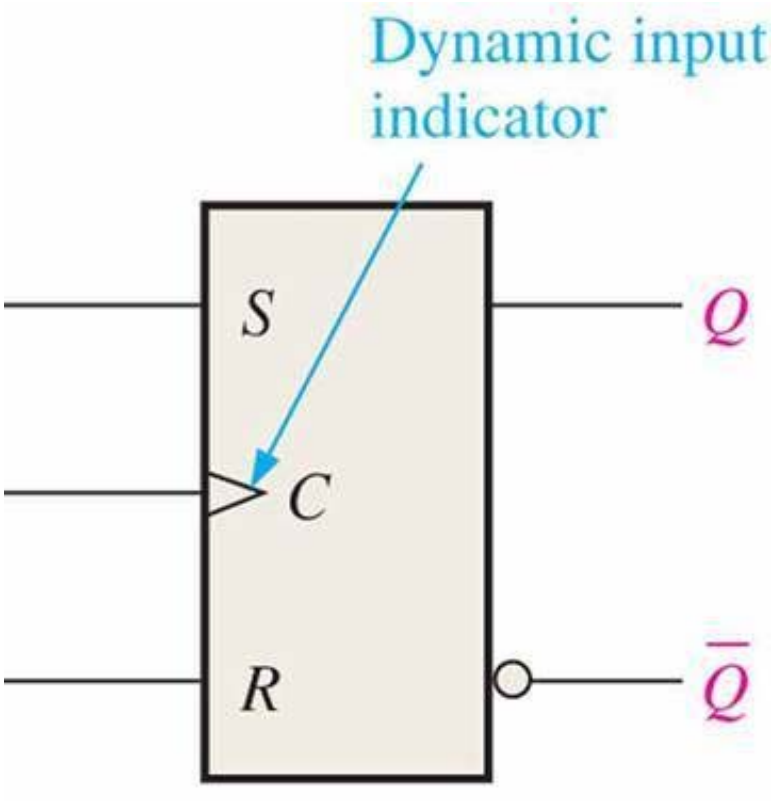
- An edge-triggered flip-flop changes state either at the ***positive edge*** (rising edge) or at the ***negative edge*** (falling edge) of the clock pulse and is sensitive to its input only at this transition of the clock.

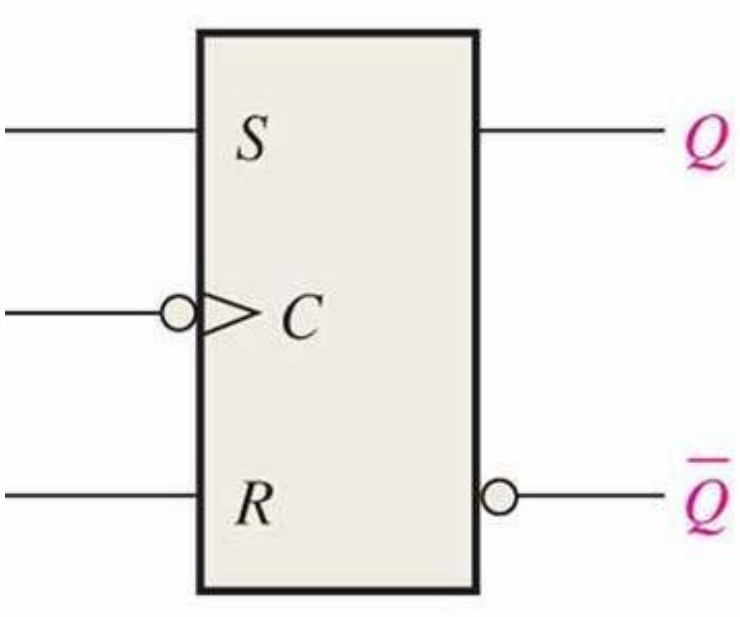
- ***Edge-triggered flip-flops*** (FF)
  - S-R flip-flop
  - J-K flip-flop
  - D flip-flop

7.2.1 The edge-triggered S-R FF

- The S and R inputs of the S-R flip-flop are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the ***triggering edge of the clock pulse***.
- When S is HIGH and R is LOW on the triggering edge of the clock pulse, Q is HIGH and the flip-flop is ***SET***. When S is LOW, R is HIGH, Q is LOW and flip-flop is ***RESET***. When S and R are both LOW, the output does not change from its prior state. When S and R are both HIGH, it is an invalid condition.

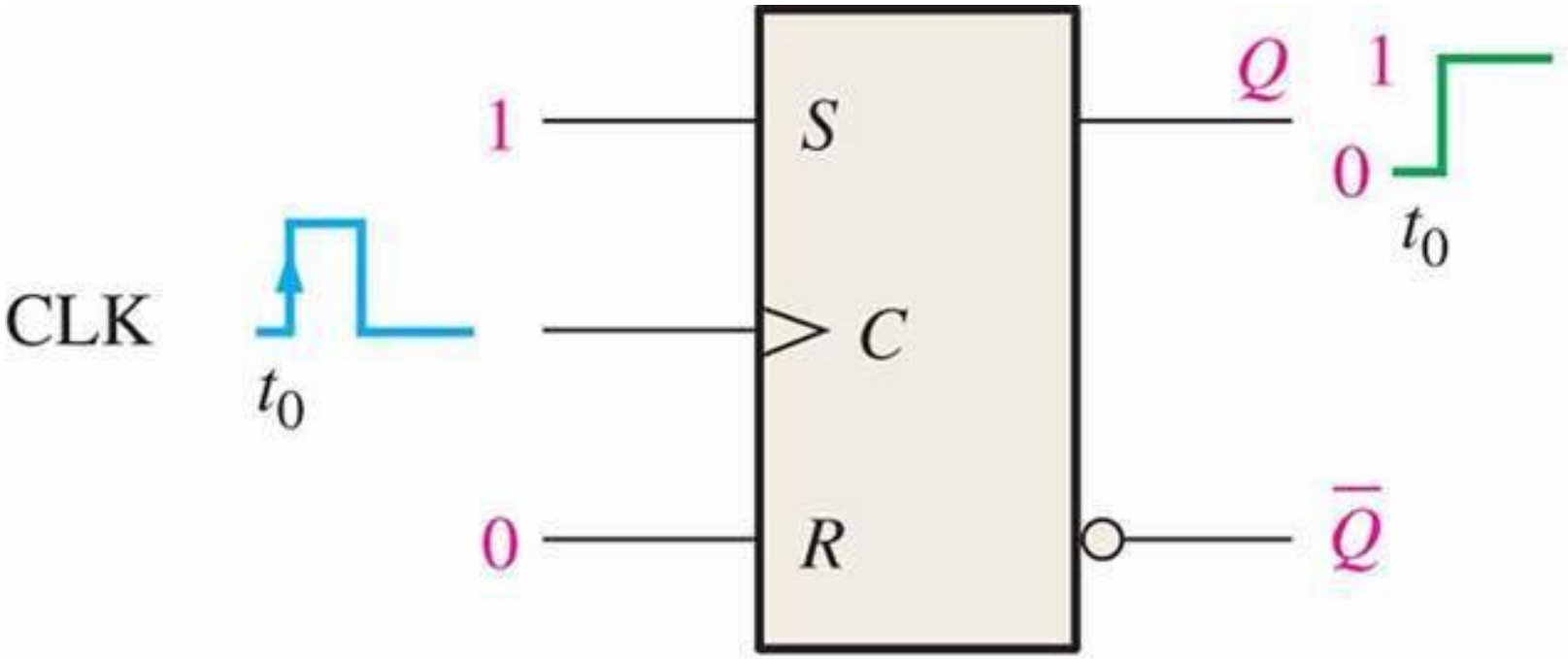
The edge-triggered S-R FF



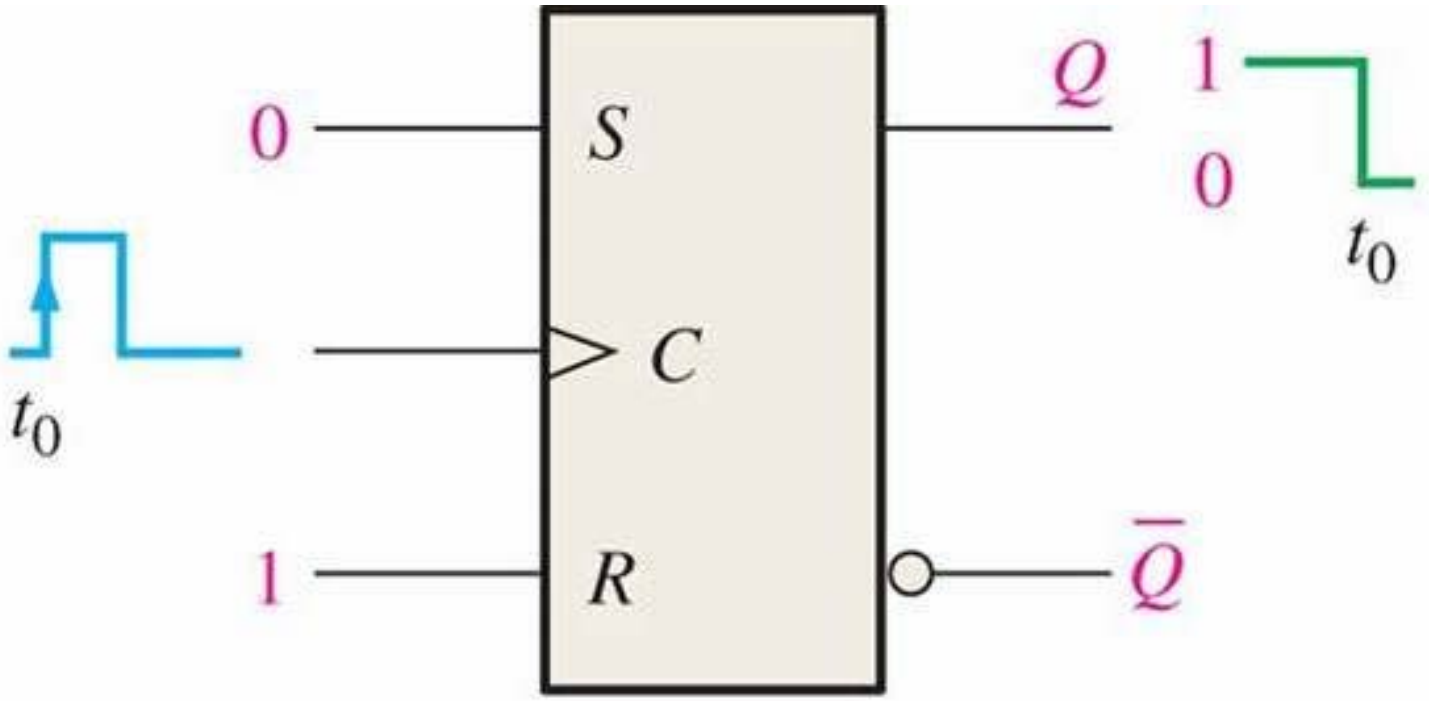


Truth Table of S-R FF

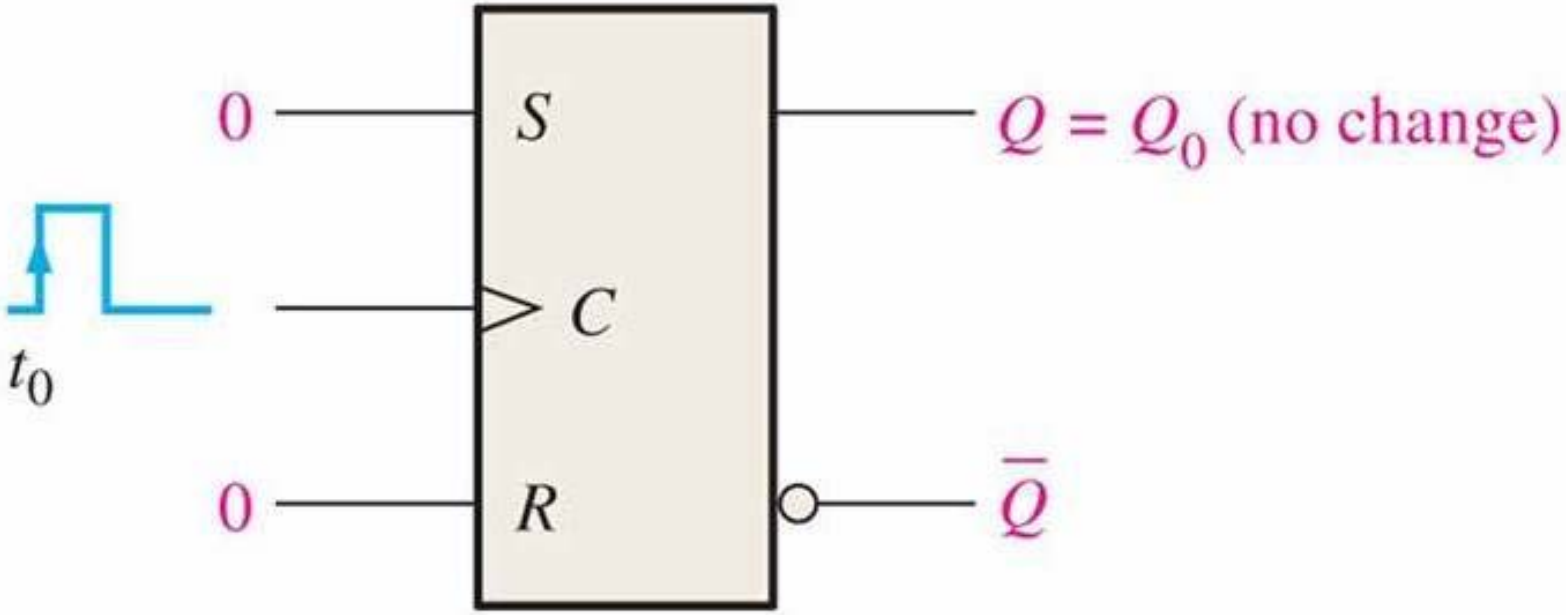
Inputs			Outputs		Comments
S	R	CLK	Q	$\overline{Q}$	
0	0	X	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid



(a) $S = 1, R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $S = 0$, $R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $S = 0$, $R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

Example

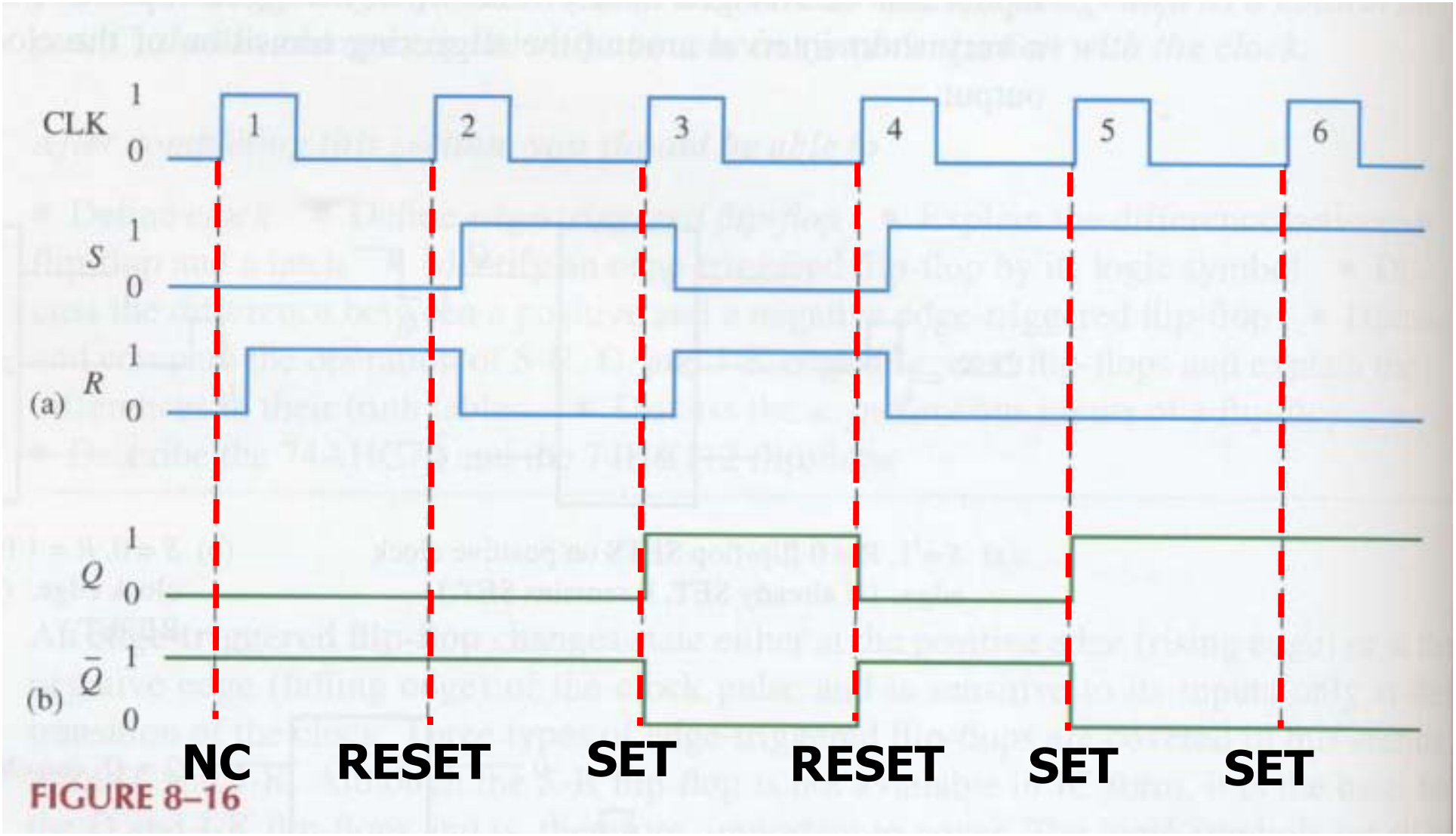
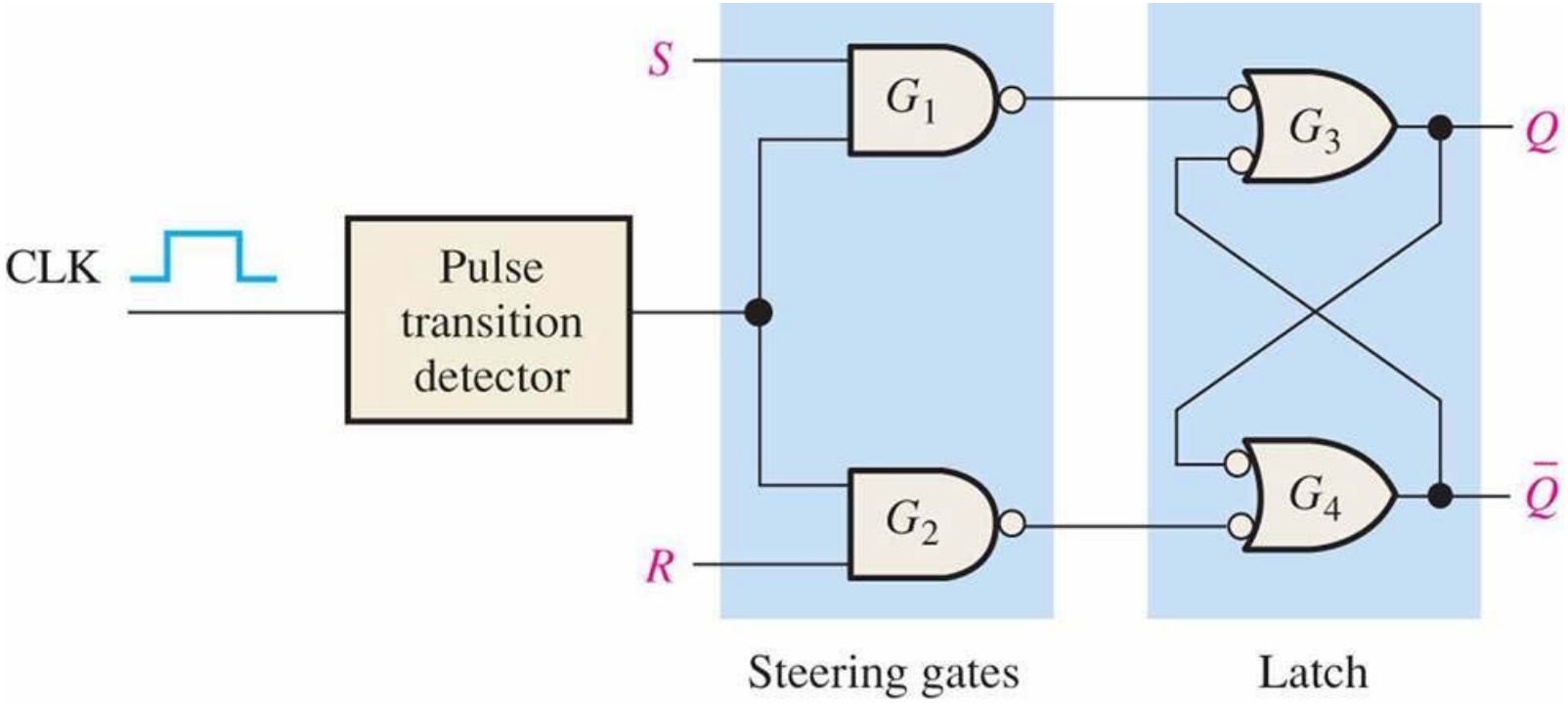


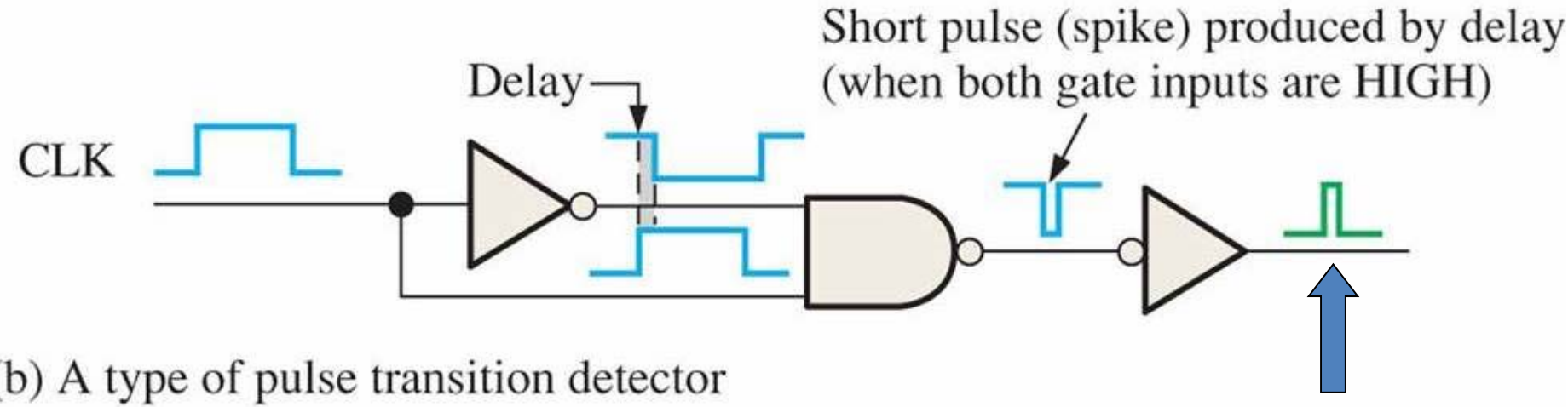
FIGURE 8–16

A method of Edge-triggering



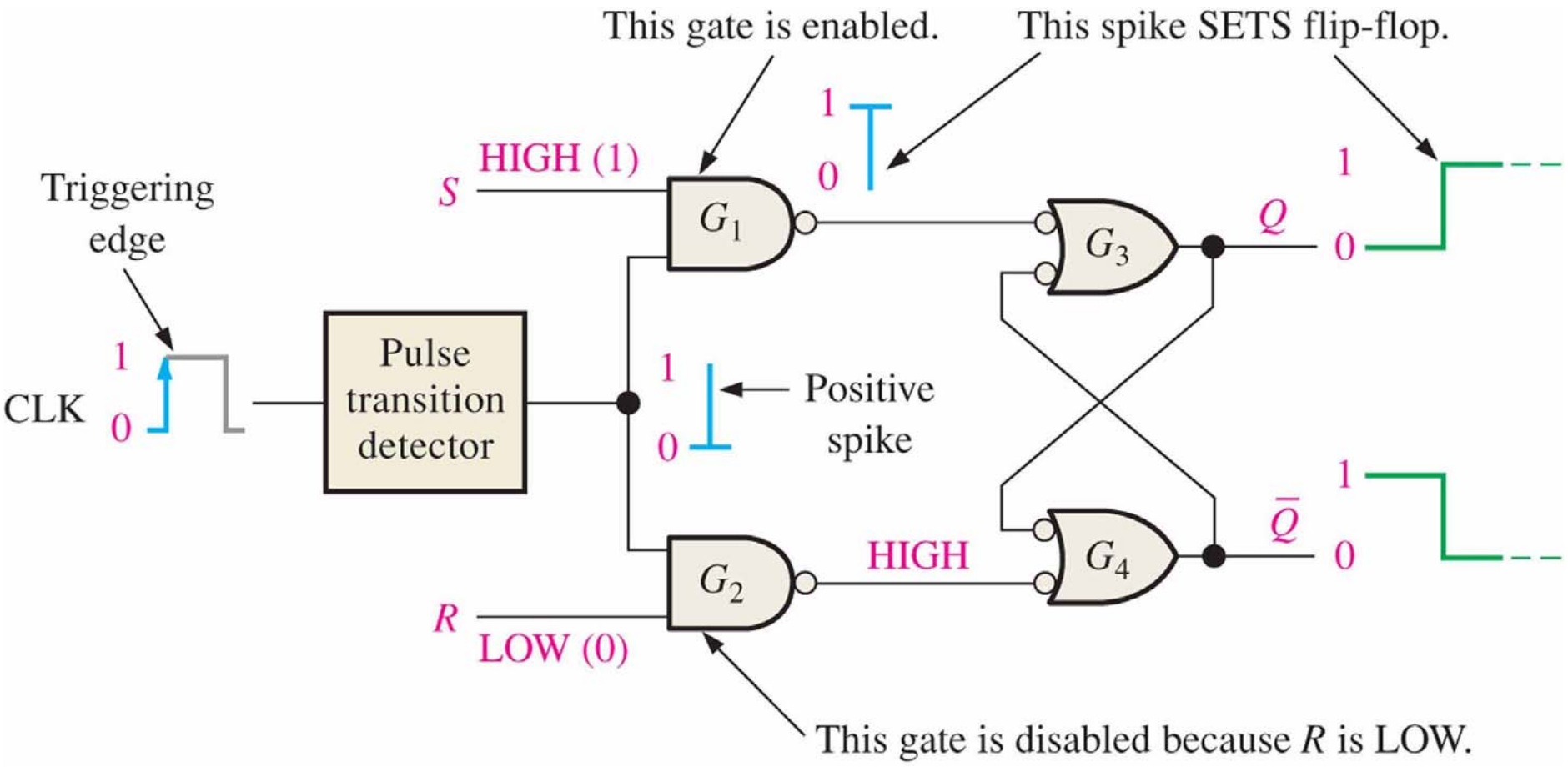
(a) A simplified logic diagram for a positive edge-triggered S-R flip-flop

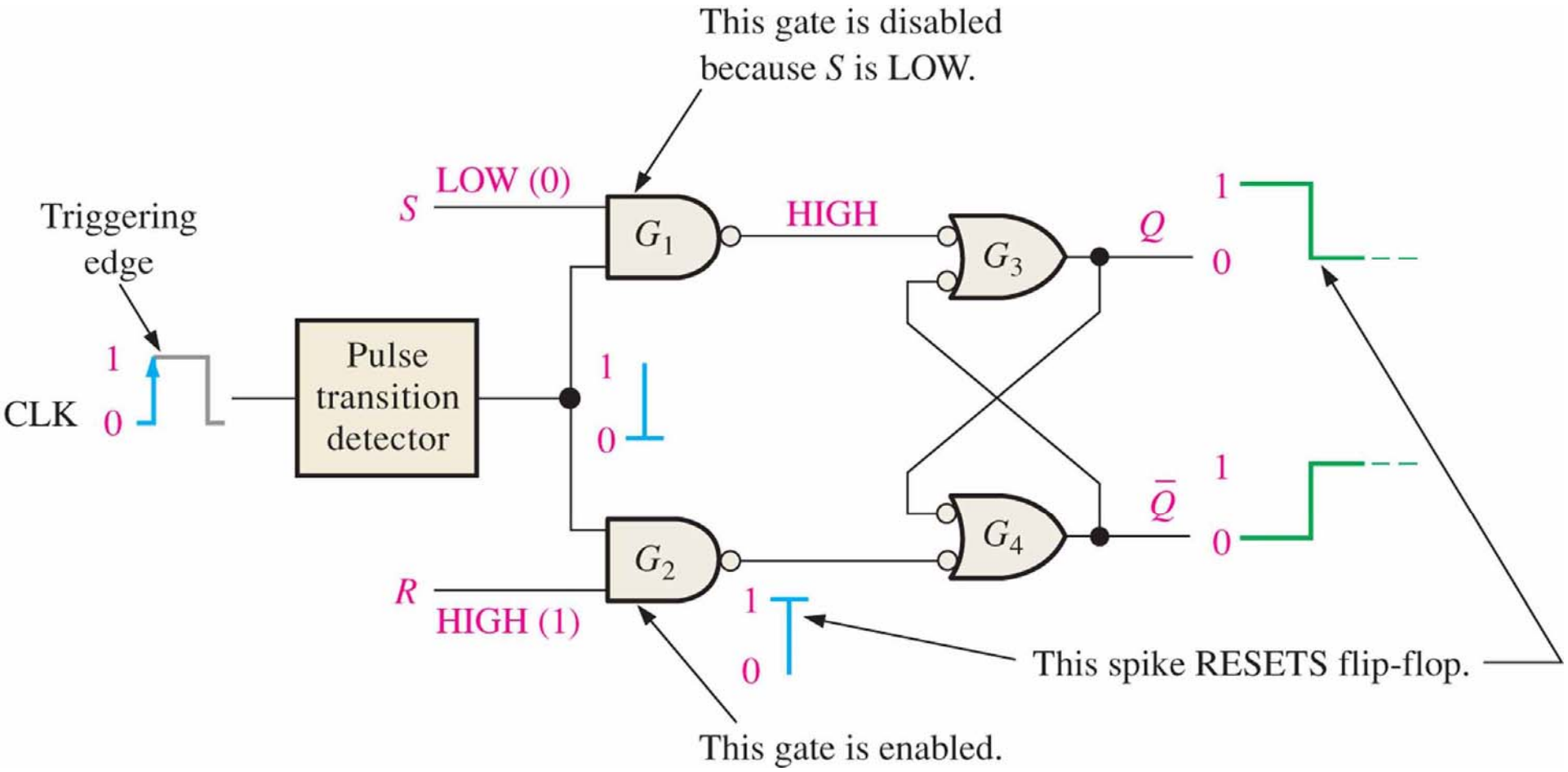
Pulse transition detector
脉冲变换检测器



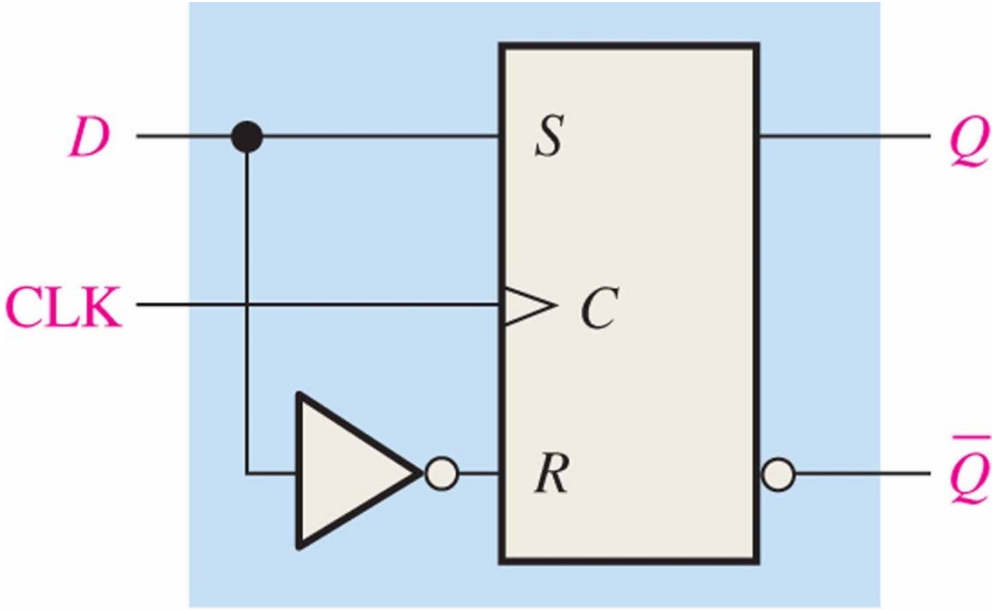
(b) A type of pulse transition detector

Narrow spike


This gate is enabled.
This spike SETS flip-flop.
Triggering edge
CLK
1
0
S
HIGH (1)
R
LOW (0)
Pulse transition detector
G_1
G_2
G_3
G_4
1
0
Positive spike
HIGH
Q
$\bar{Q}$
This gate is disabled because R is LOW.

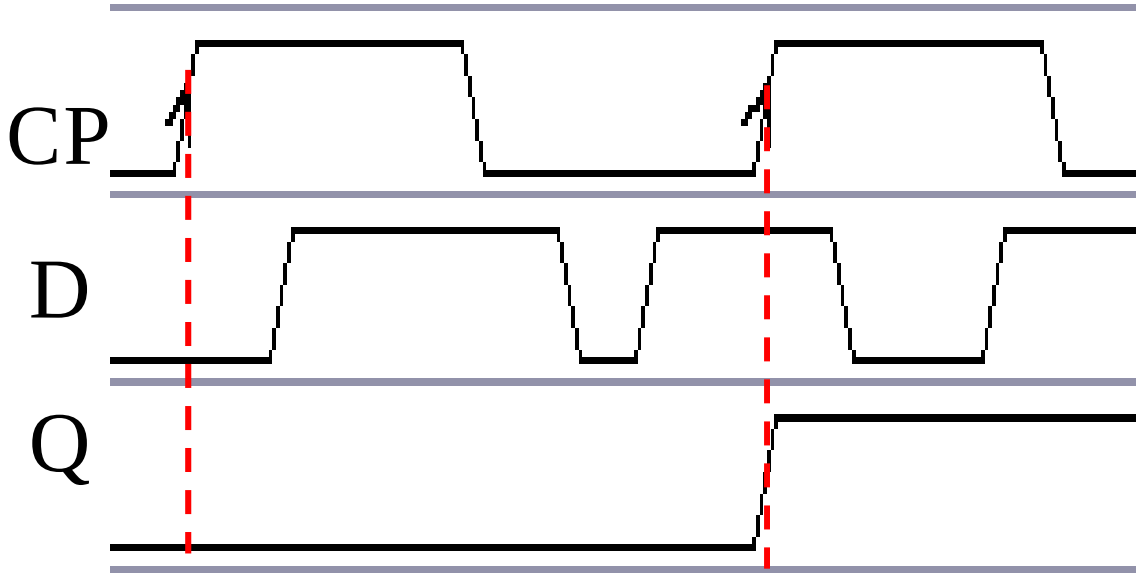

This gate is disabled
because S is LOW.
S
LOW (0)
Triggering
edge
1
CLK
0
Pulse
transition
detector
G1
HIGH
G3
Q
1
0
1
0
1
0
G2
G4
Q̄
1
0
R
HIGH (1)
1
0
This spike RESETS flip-flop.
This gate is enabled.

7.2.2 The Edge-Triggered D FF



Positive edge-triggered D flip-flop
The Q output of a D assumes the state of the D input on the triggering edge of the clock

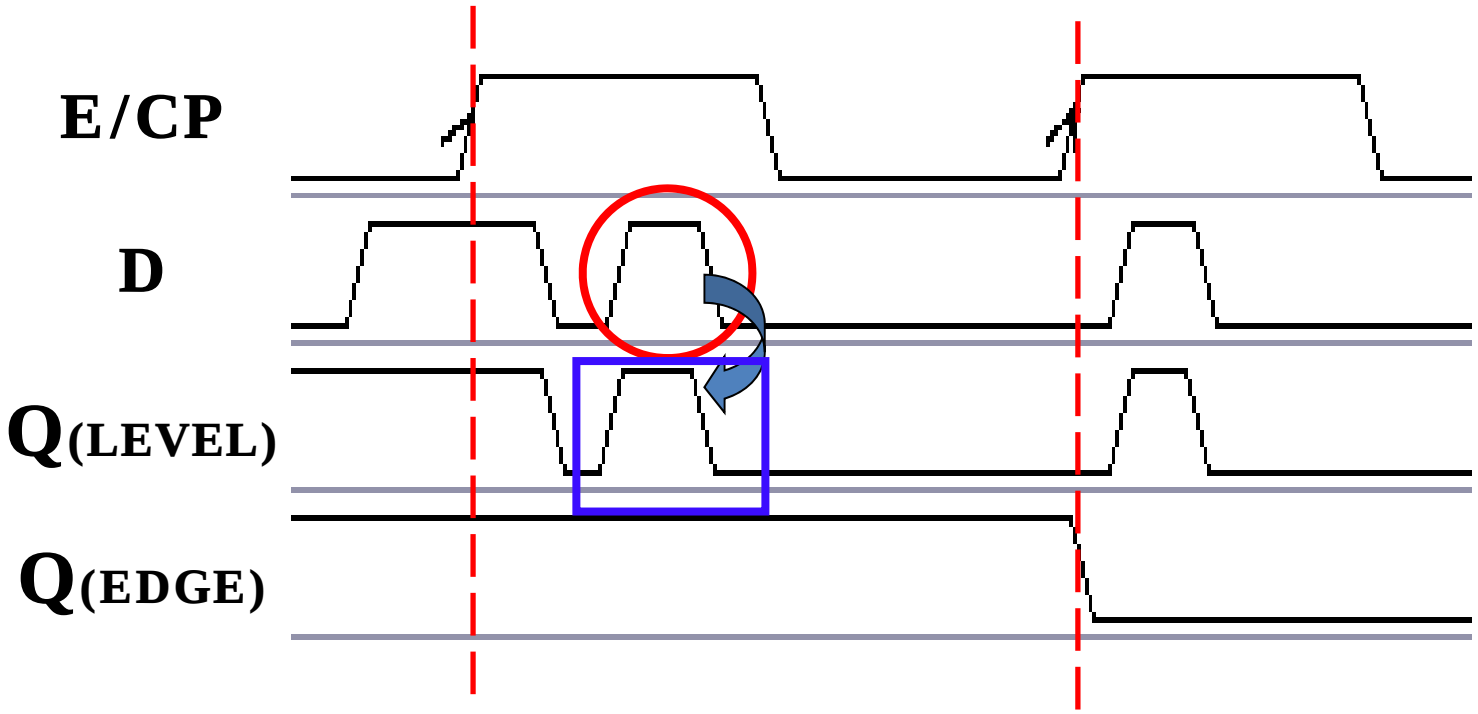
Timing diagram



Truth Table

CP	D	Q	$\overline{Q}$
↑	D	D	$\overline{D}$

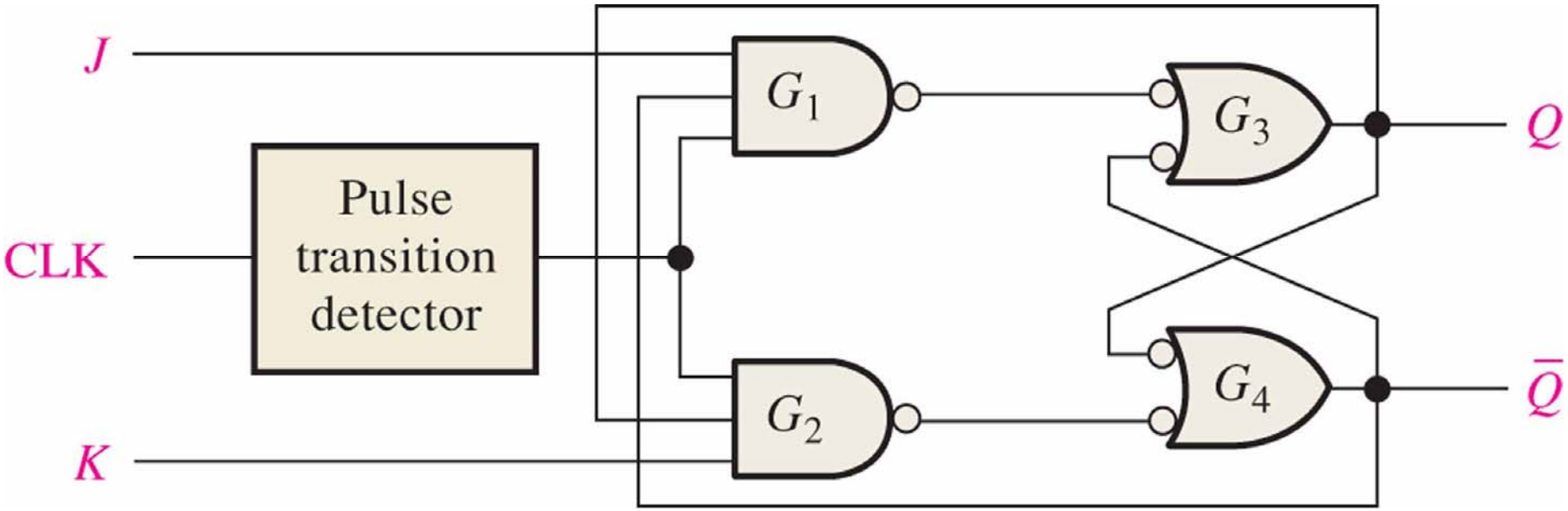
Comparison of edge-triggered and level-triggered



7.2.3 The Edge-Triggered J-K FF

****No invalid states.**

The two Set/Reset signals are labeled as J and K in honor of Jack Kilby.

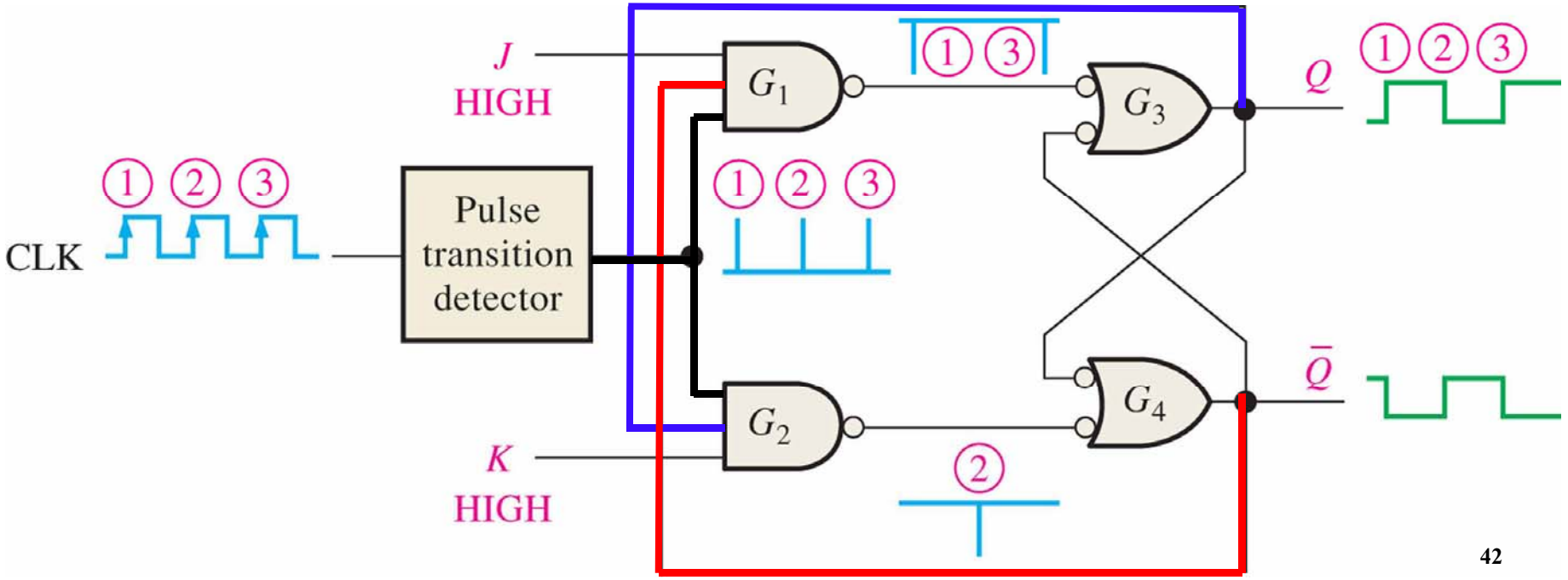


①IF J=1,K=0,Q_0=0;THEN G_1 enabled, Q=1 (SET)

②IF J=0,K=1,Q_0=1;THEN G_2 enabled, Q=0 (RESET)

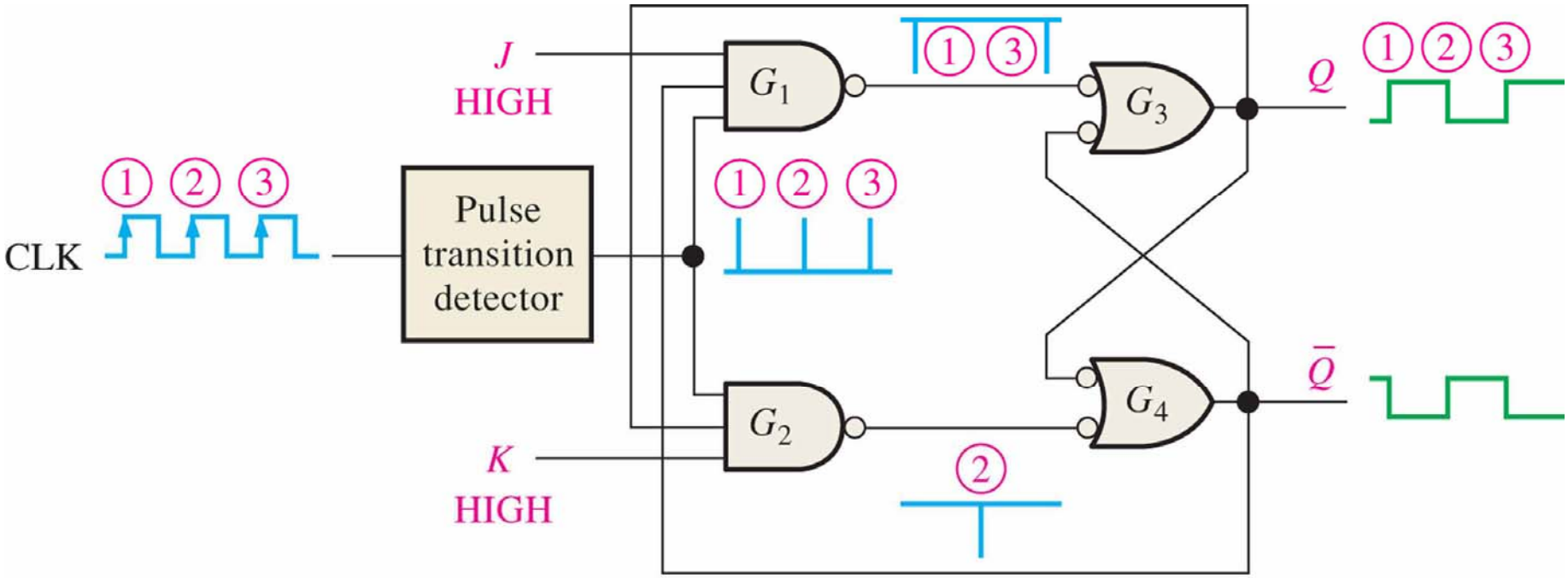
③IF J=0,K=0; THEN no change

④IF J=1,K=1; THEN change to opposite state(*Toggle*)

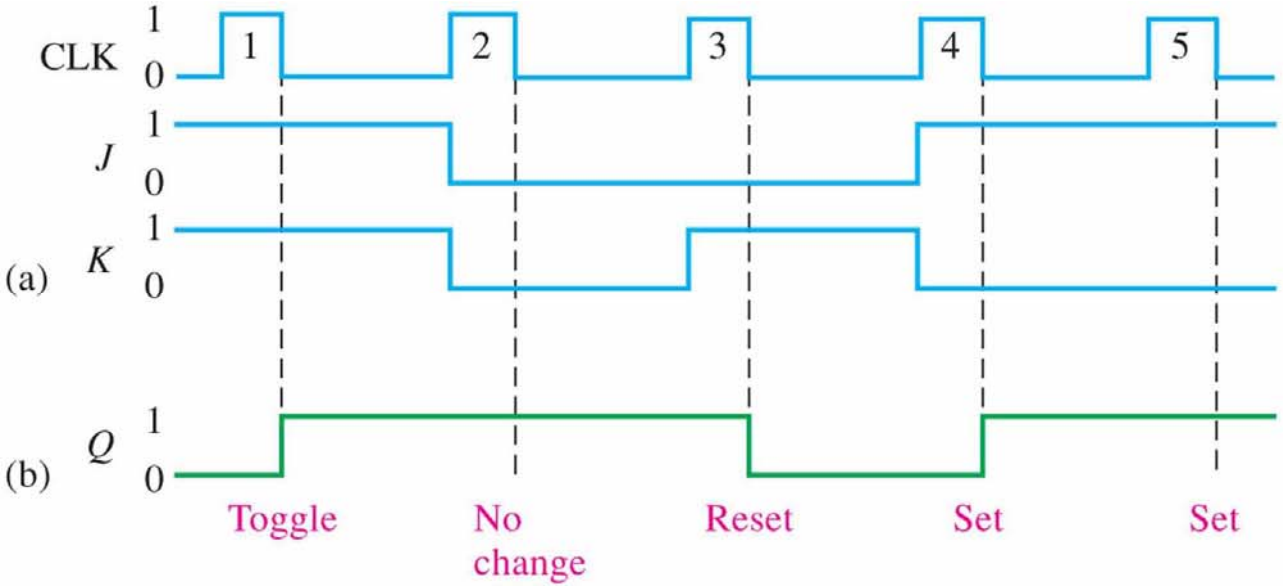


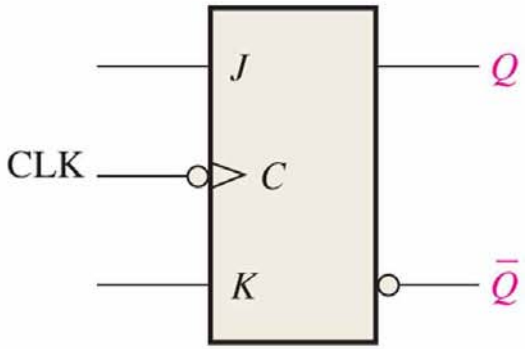
The Edge-Triggered Toggle FF

Toggle operation when J=K=1



Timing diagram





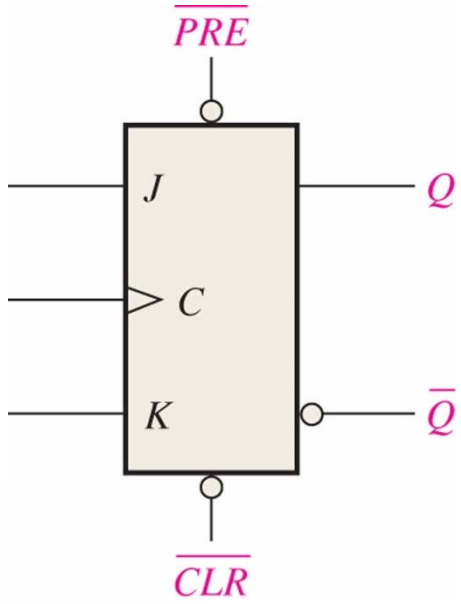
Truth Table

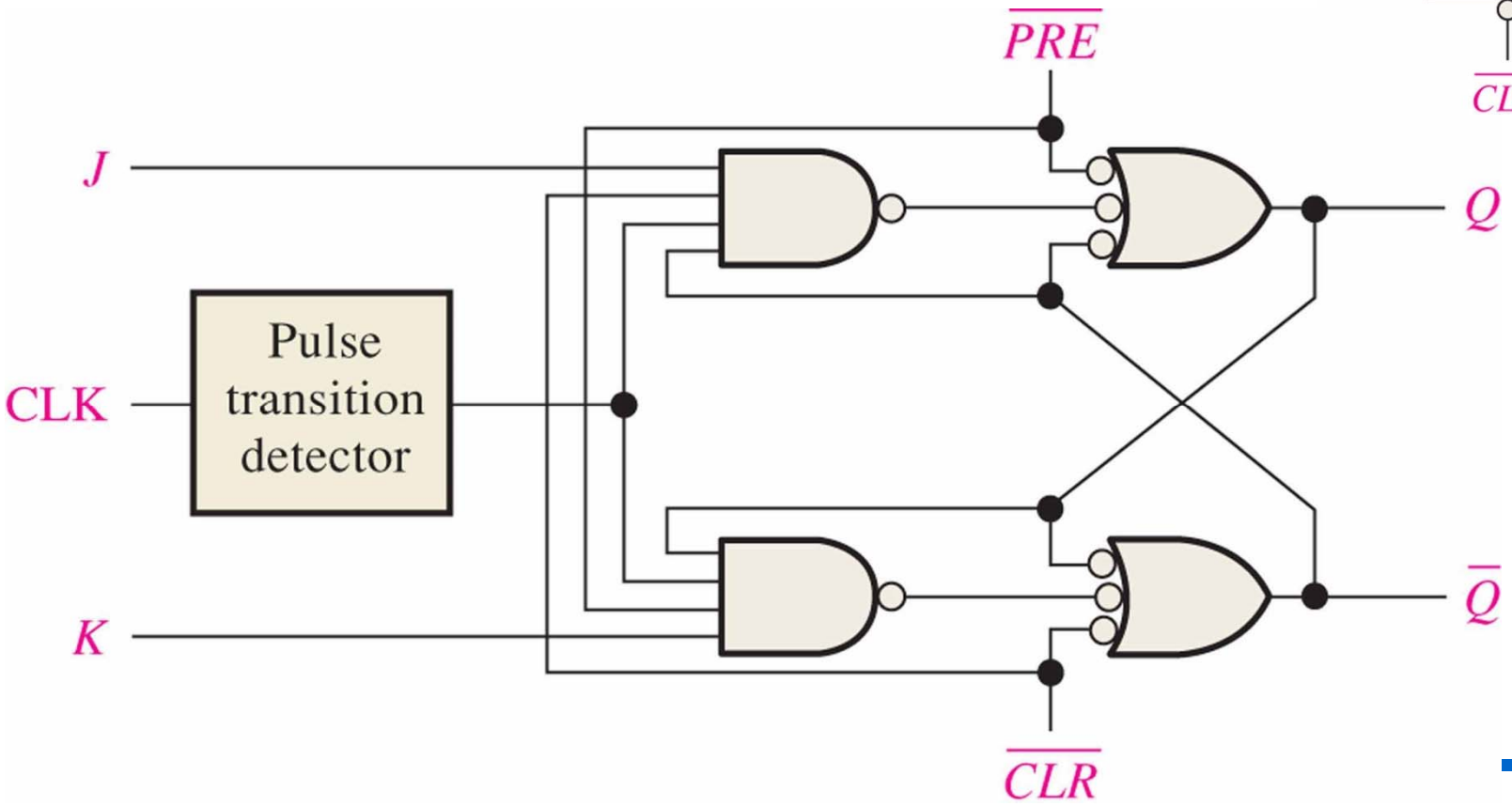
Inputs			Outputs		Comments
J	K	CLK	Q	$\overline{Q}$	
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

7.2.4.Asynchronous Preset and Clear Inputs（异步置位和复位）

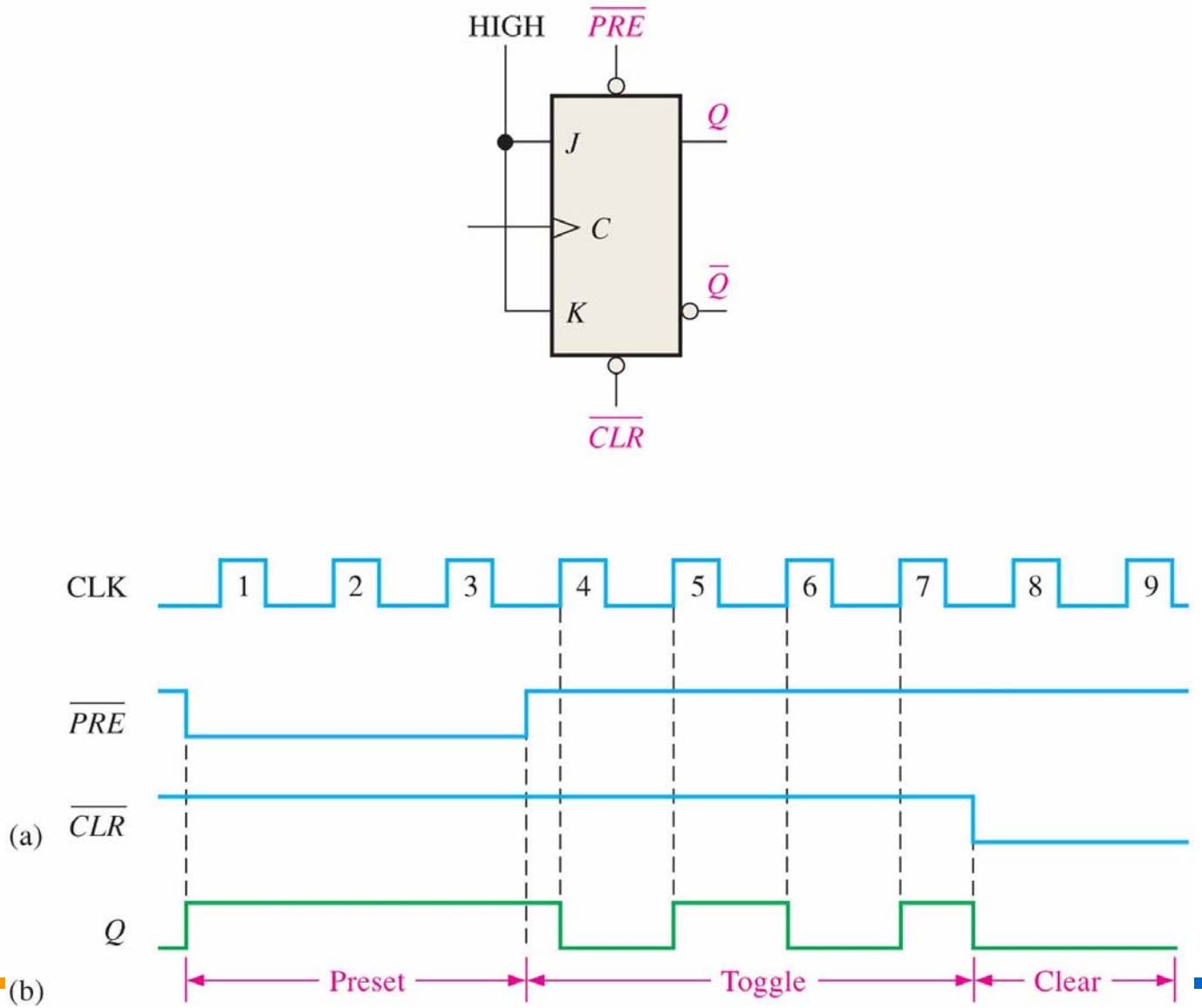
- Asynchronous inputs are independent of the clock. Usually labeled ***preset*** (***PRE***) and ***clear*** (***CLR***), or ***direct set (SD) and direct reset (RD).***
- An active level on the preset input will set the flip-flop, and an active level on the clear input will reset the flip-flop.

J-K FF with active-LOW preset and clear inputs

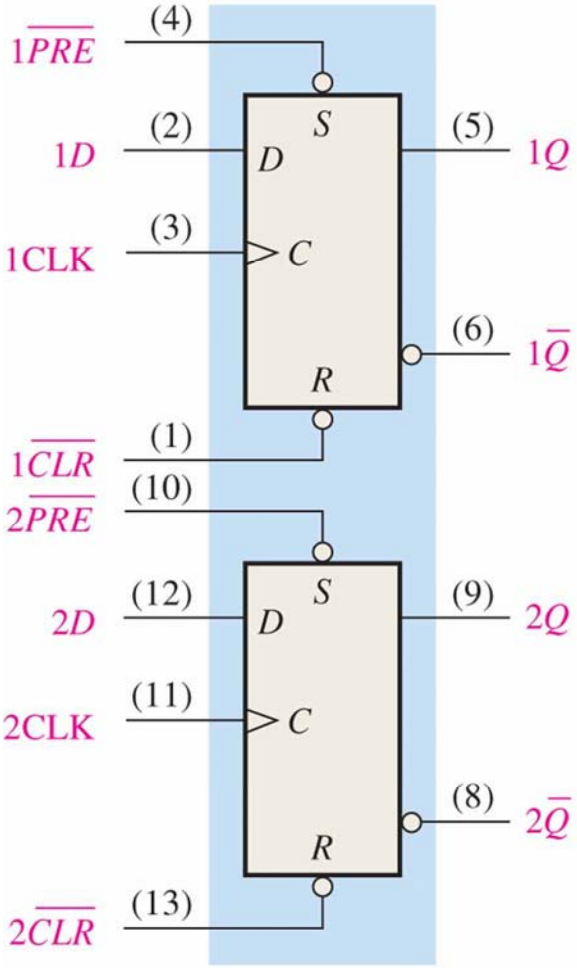




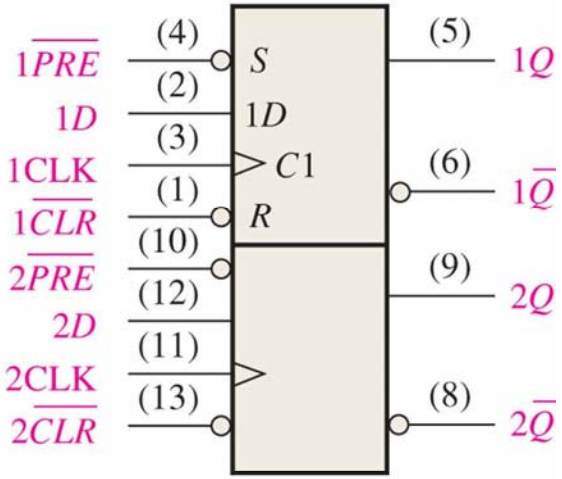
J-K FF with active-LOW preset and clear inputs



74AHC74 (dual D FF)



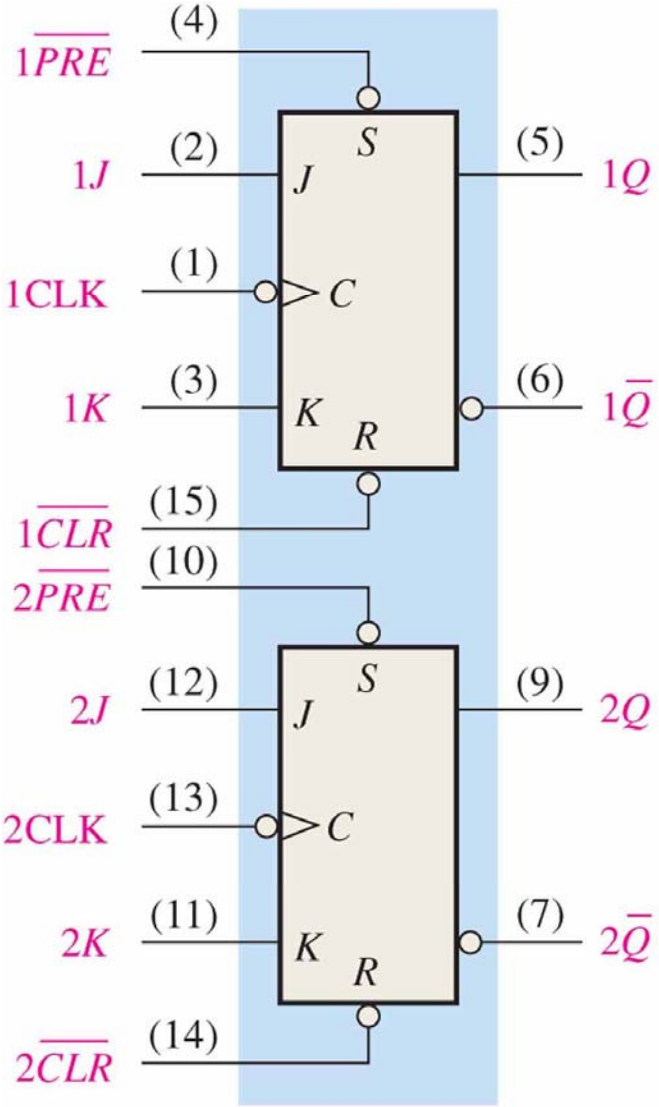
(a) Individual logic symbols



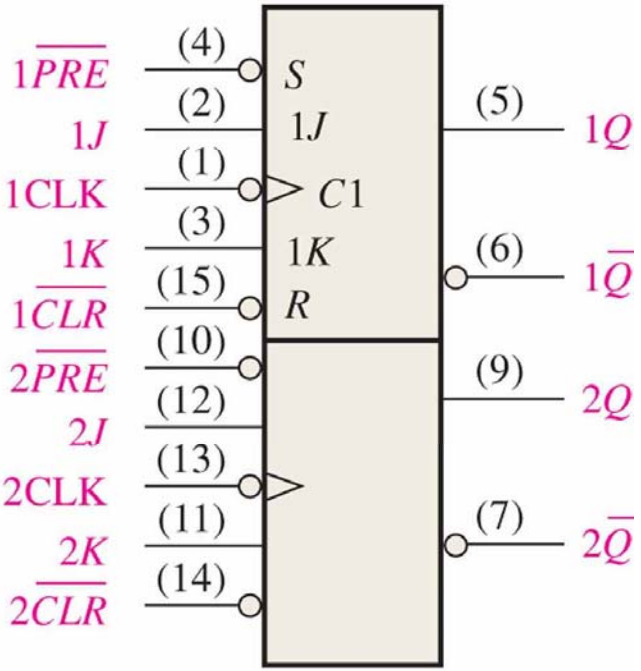
(b) Single block logic symbol

Note: The *S* and *R* inside the block indicate that $\overline{PRE}$ SETS and $\overline{CLR}$ RESETS.

74HC112 (dual JK FF)



(a) Individual logic symbols

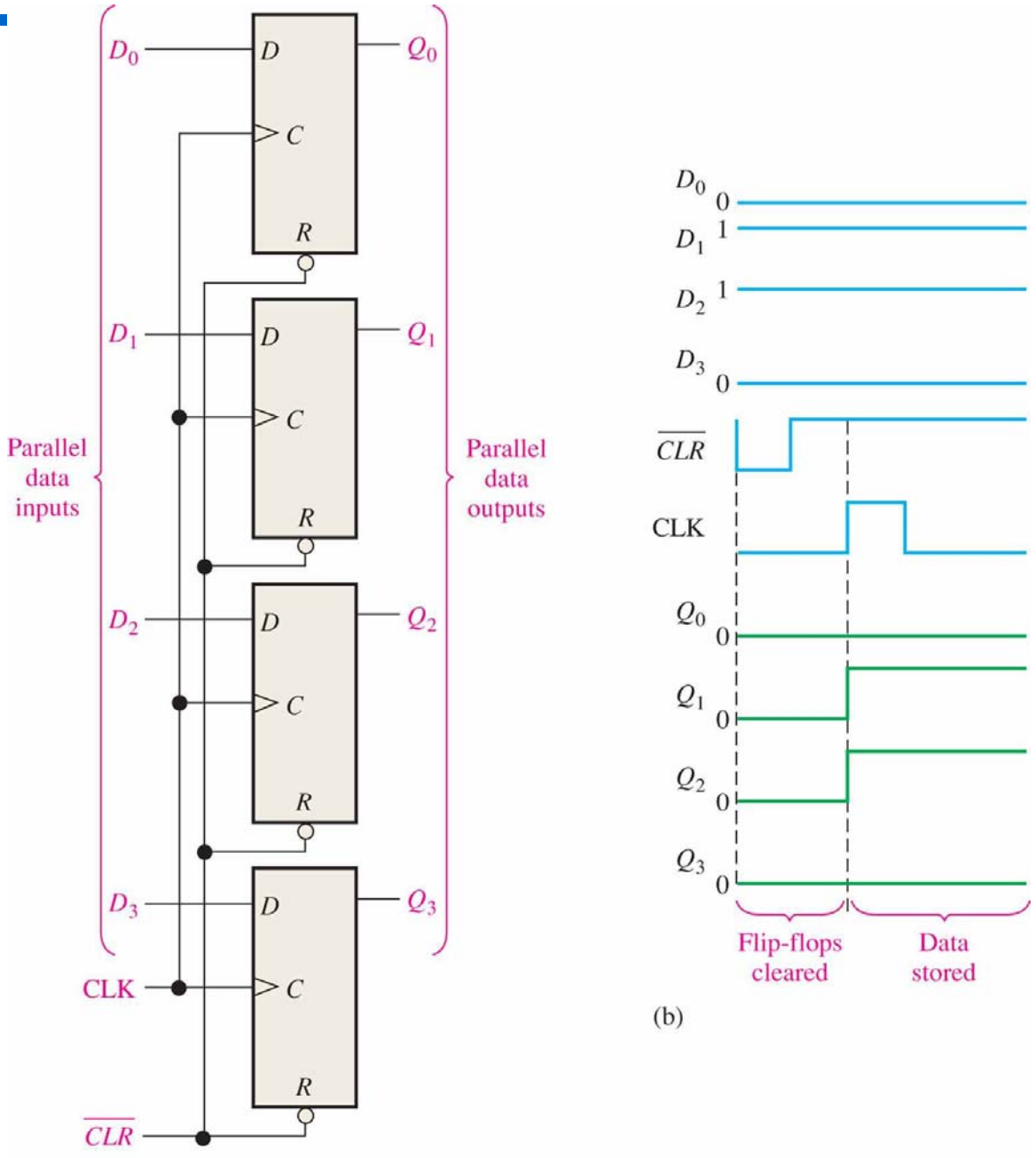


(b) Single block logic symbol

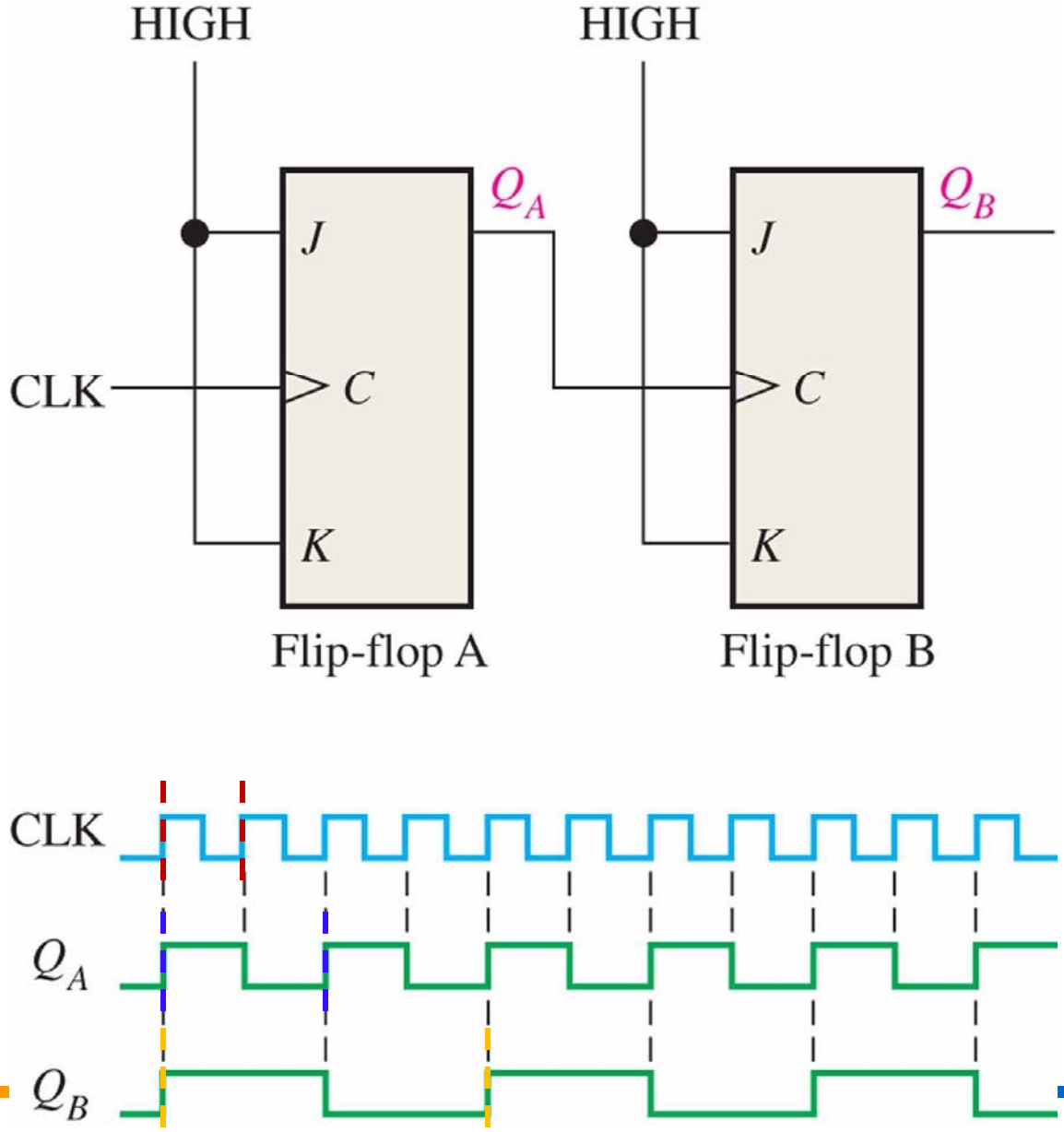
7.3 Flip-Flop Applications

- Parallel Data Storage (数据存储器)
- Frequency Division (分频器)
- Counter (计数器)

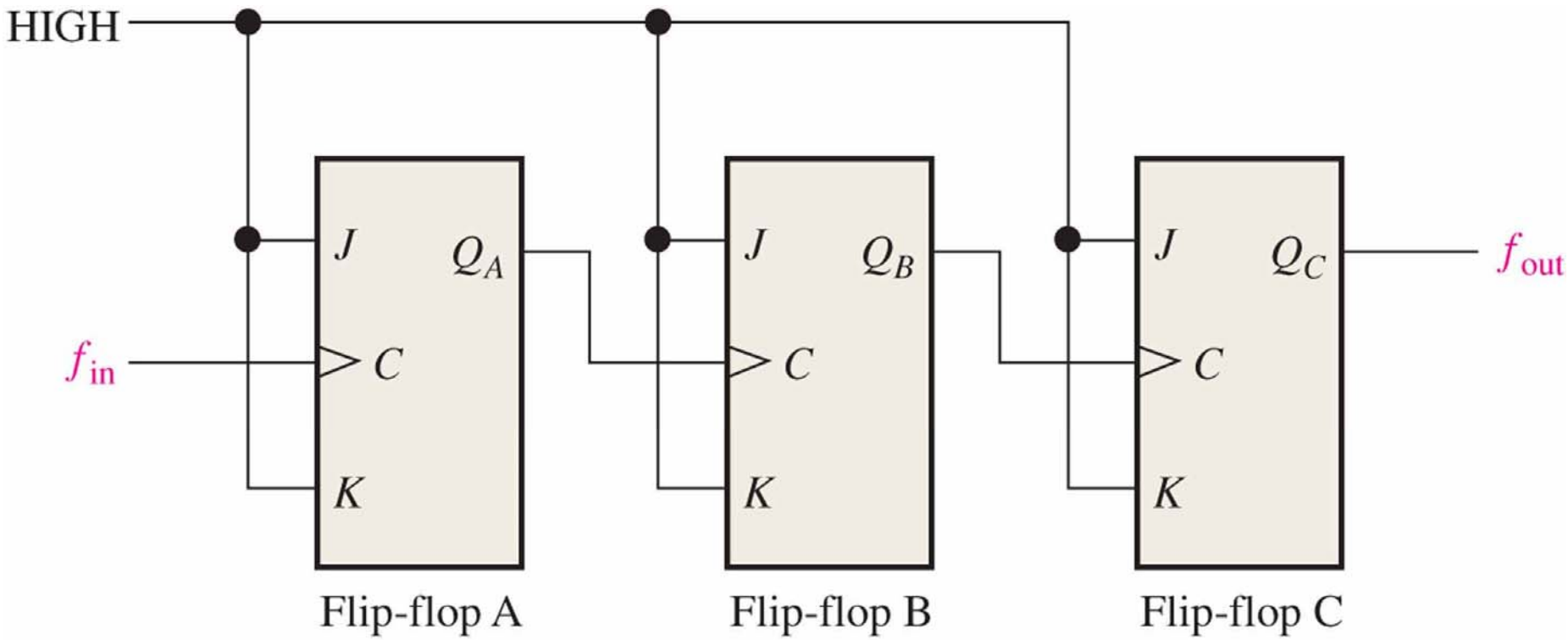
Application example: Basic register for parallel data storage

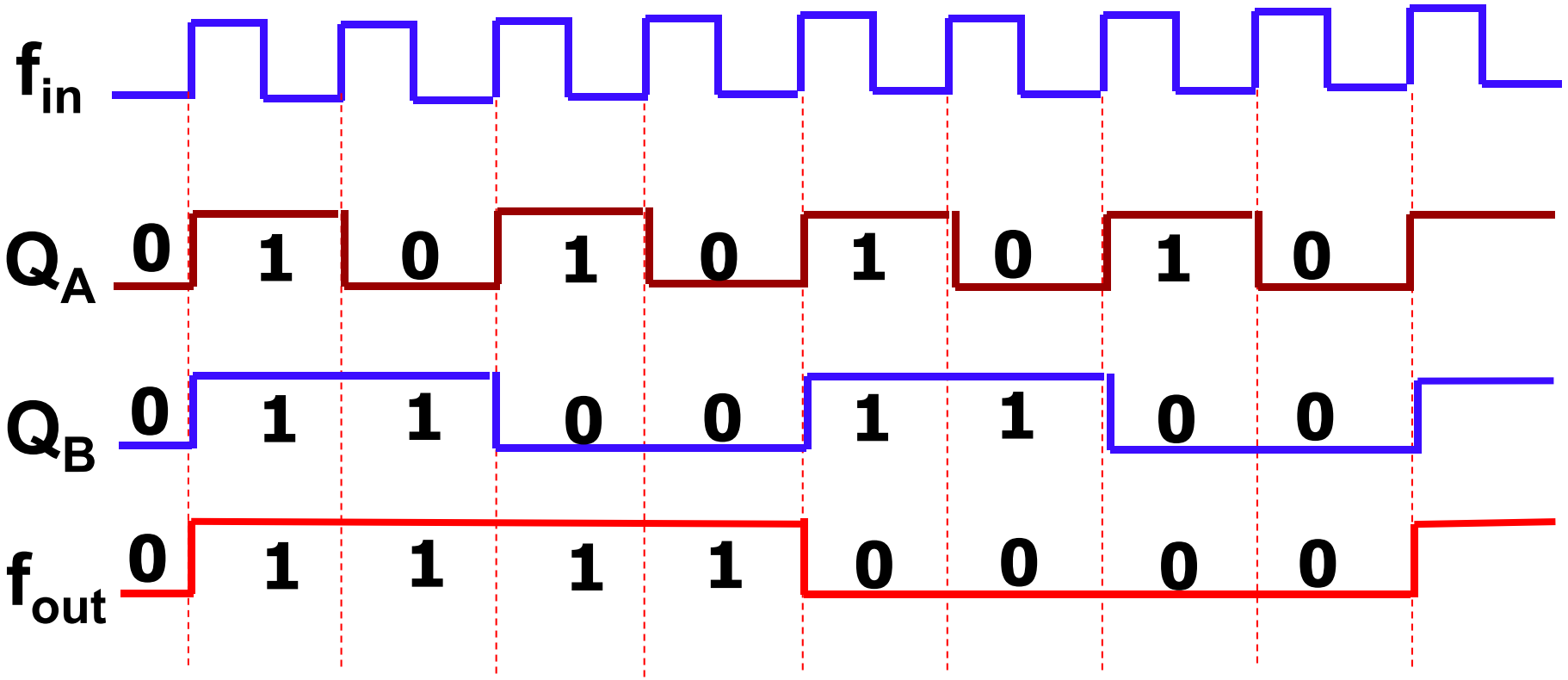


J-k FF as a devide-by-2 or 4 device

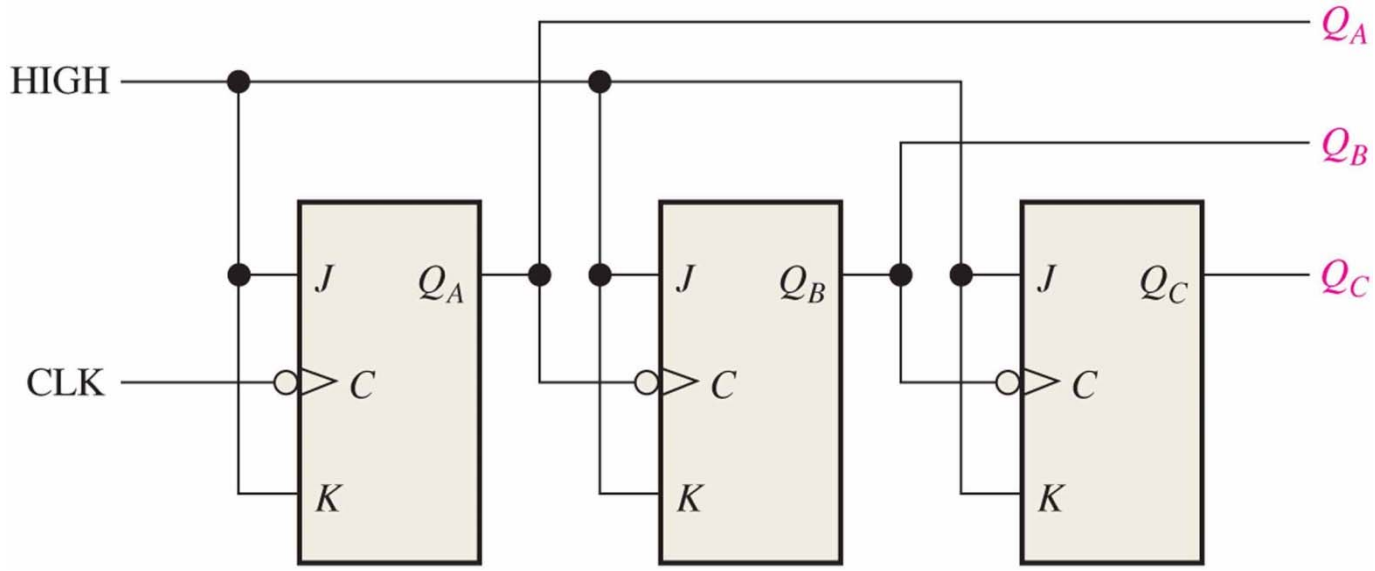


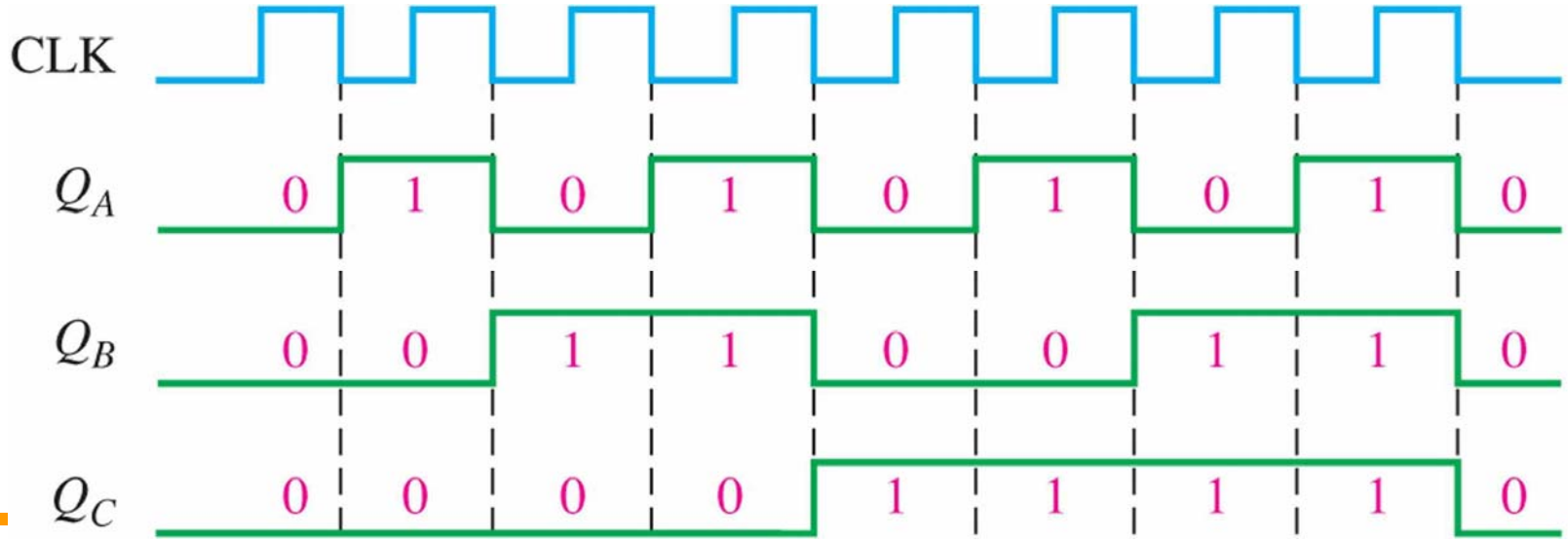
Exercise:


HIGH
f_{in}
J
Q_A
C
K
J
Q_B
C
K
J
Q_C
C
K
f_{out}
Flip-flop A
Flip-flop B
Flip-flop C


f_{in}
Q_A 0 1 0 1 0 1 0 1 0
Q_B 0 1 1 0 0 1 1 0 0
f_{out} 0 1 1 1 1 0 0 0 0

J-k FF as a counter





7.4 Flip-Flop Operating Characteristics

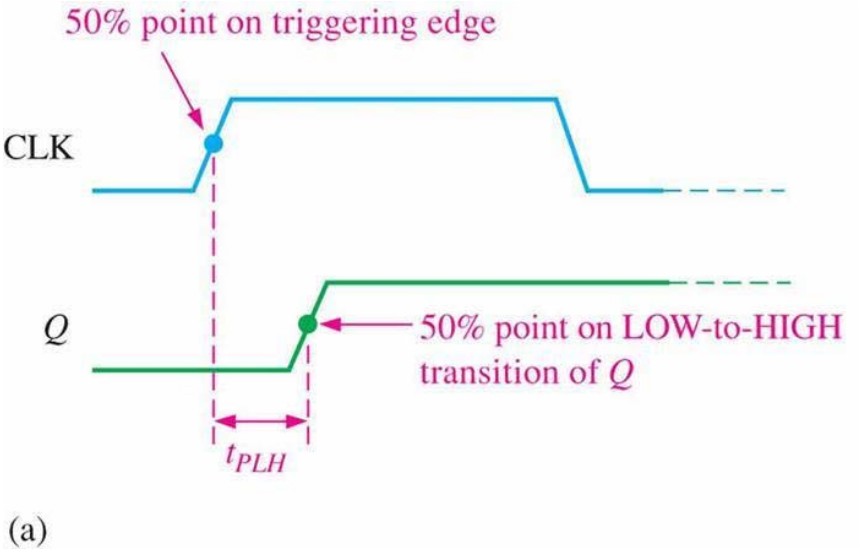
- Propagation delay time (传播时延)
- Set-up time (建立时间)
- Hold time (保持时间)
- Maximum of frequency (最大频率)
- Pulse width (脉冲宽度)
- Power dissipation (功耗)

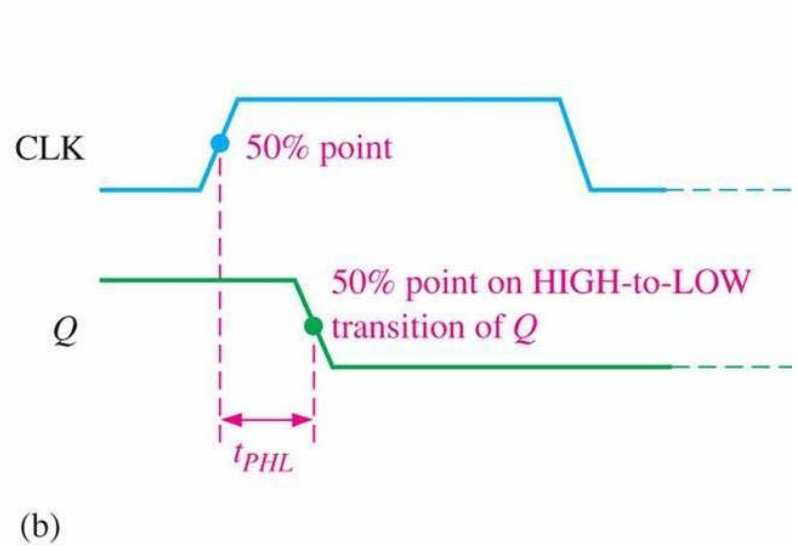
Propagation Delay Time

The propagation delay time is the interval of time required after an input signal has been applied for the resulting output change to occur.

Propagation Delay Time for a flip-flop(I)

1. t_{PLH} : Measured from the triggering edge of the clock pulse to the LOW-to-HIGH transition of the output
2. t_{PHL} : Measured from the triggering edge of the clock pulse to the HIGH-to-LOW transition of the output.

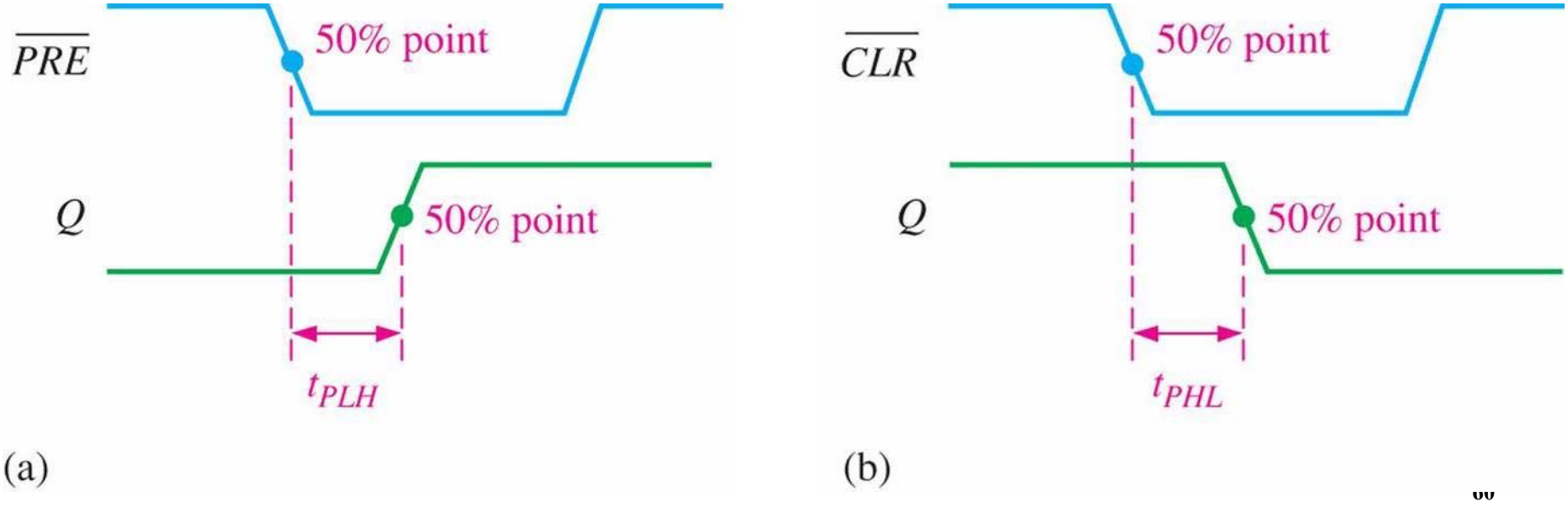




Propagation Delay Time for a flip-flop(II)

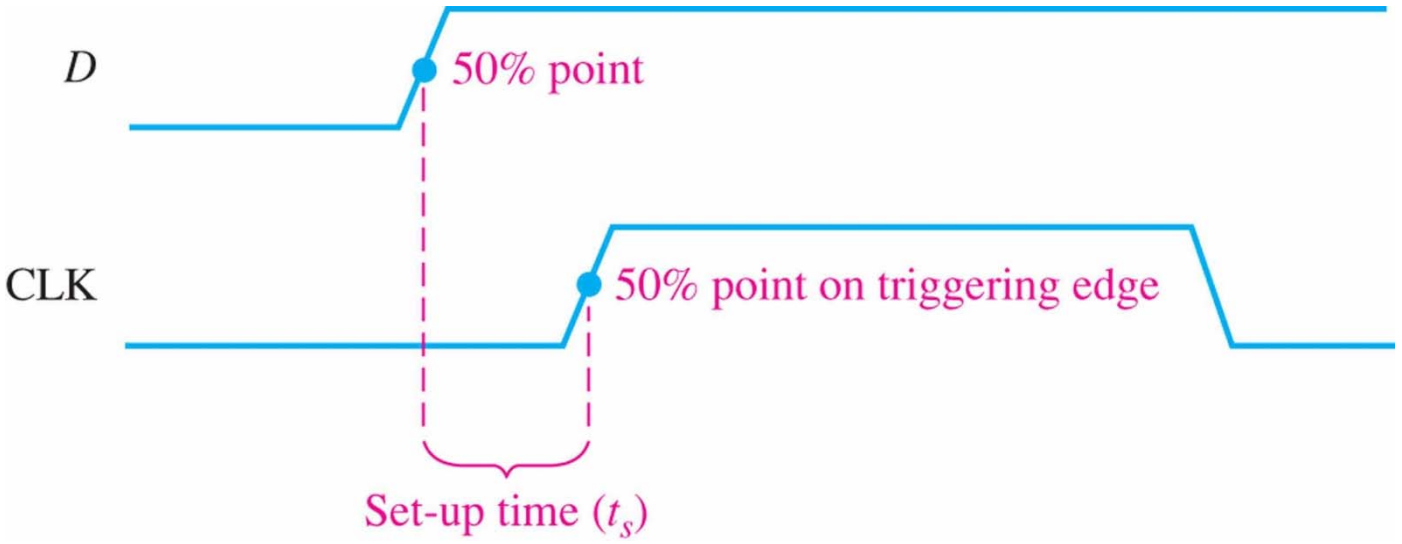
3. t_{PLH} : Measured from the leading edge of the preset input to the LOW-to-HIGH transition of the output

4. t_{PHL} : Measured from the leading edge of the clear input to the HIGH-to-LOW transition of the output.



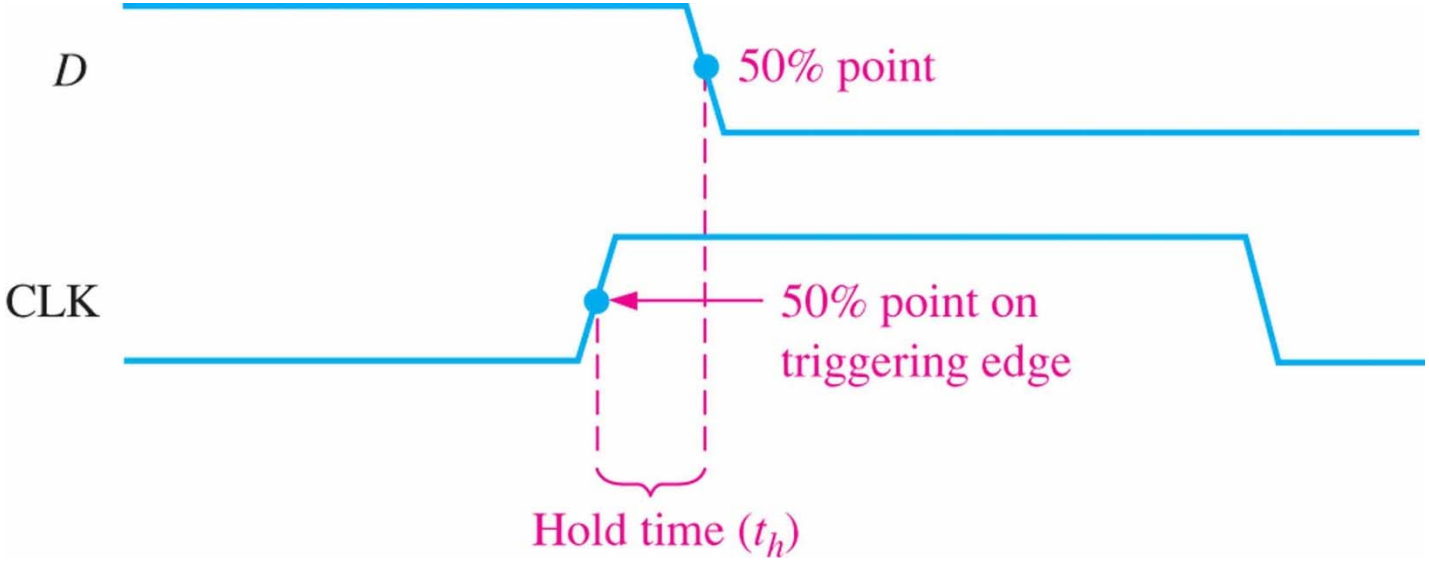
Set-up Time

The set-up time (t_s) is the minimum interval of time required for the logic levels to be maintained constantly on the inputs(J and K, or S and R, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop.



Hold Time

The Hold time (t_h) is the minimum interval of time required for the logic levels to remain constantly on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop.



Maximum Clock Frequency

The maximum clock frequency (f_{max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough and its operation would be impaired.

Pulse Widths

The minimum pulse widths (t_w) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically the clock is specified by its minimum HIGH time and its minimum LOW time.

Power Dissipation

The power dissipation is the total power consumption of the device.

$$P = V_{cc} \times I_{cc} = 5V \times 5mA = 25mW$$

脉冲波形的产生和整形

- 整形电路：
  - 施密特触发器
  - 单稳态
- 脉冲波形的产生
  - 多谐振荡器
- 555定时器

7.5 Schimitt Trigger（施密特触发器）

*A **Schmitt trigger*** is a special type of bi-stable device that has two threshold voltages (i.e. stable states).

Characteristics:

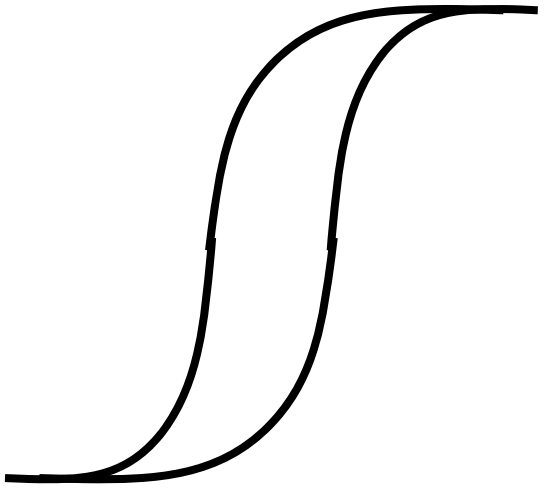
- using two voltage thresholds: a high threshold to switch the circuit during low-to-high transitions and a lower threshold to switch the circuit during high-to-low transitions.
- Generating pulse with sharp edges

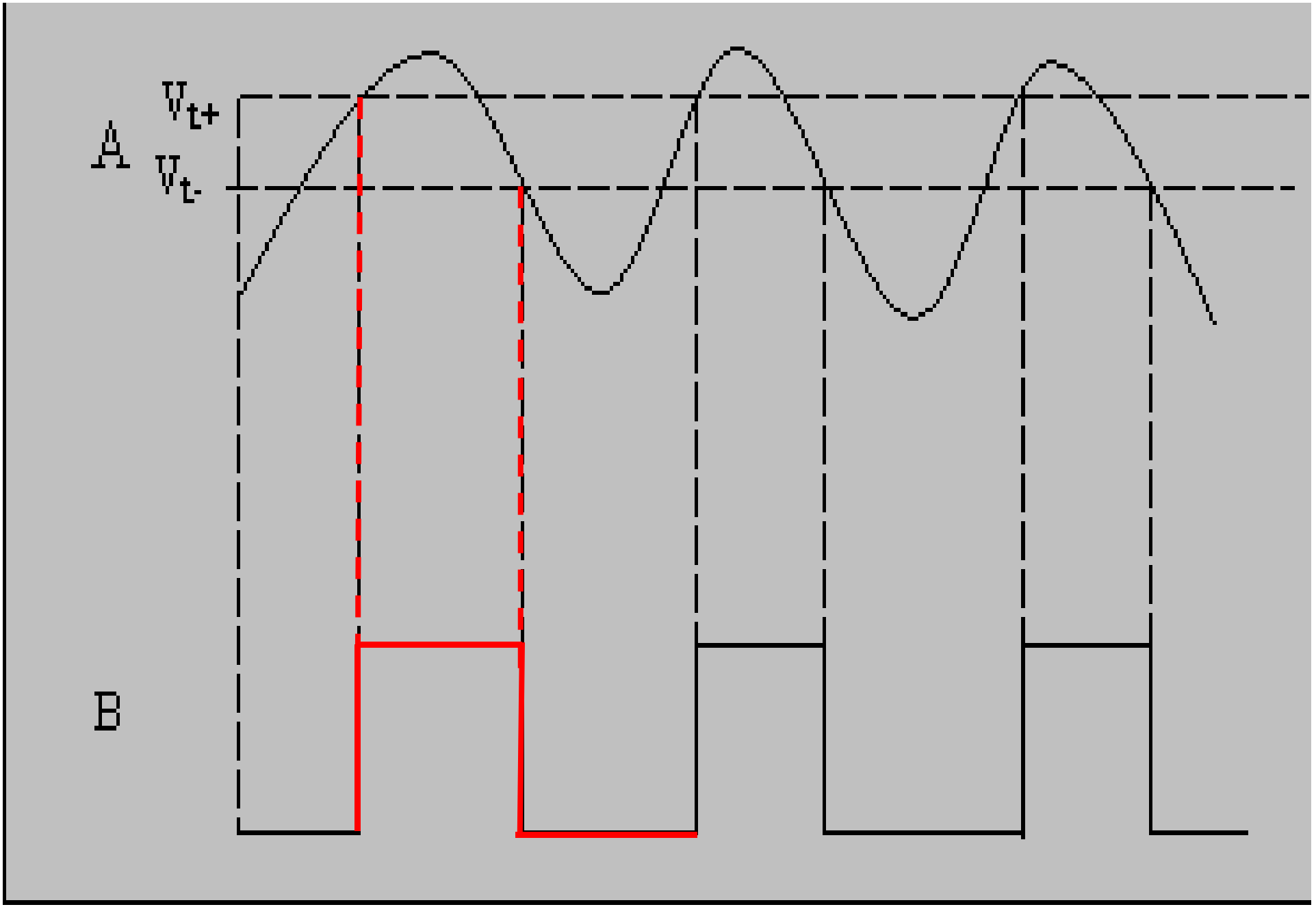
Advantages:

- conditioning slow or noisy signals
- increasing the noise immunity

Symbol

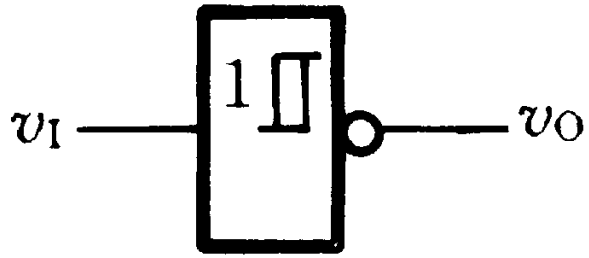
The ***hysteresis symbol*** indicates a Schmitt trigger input

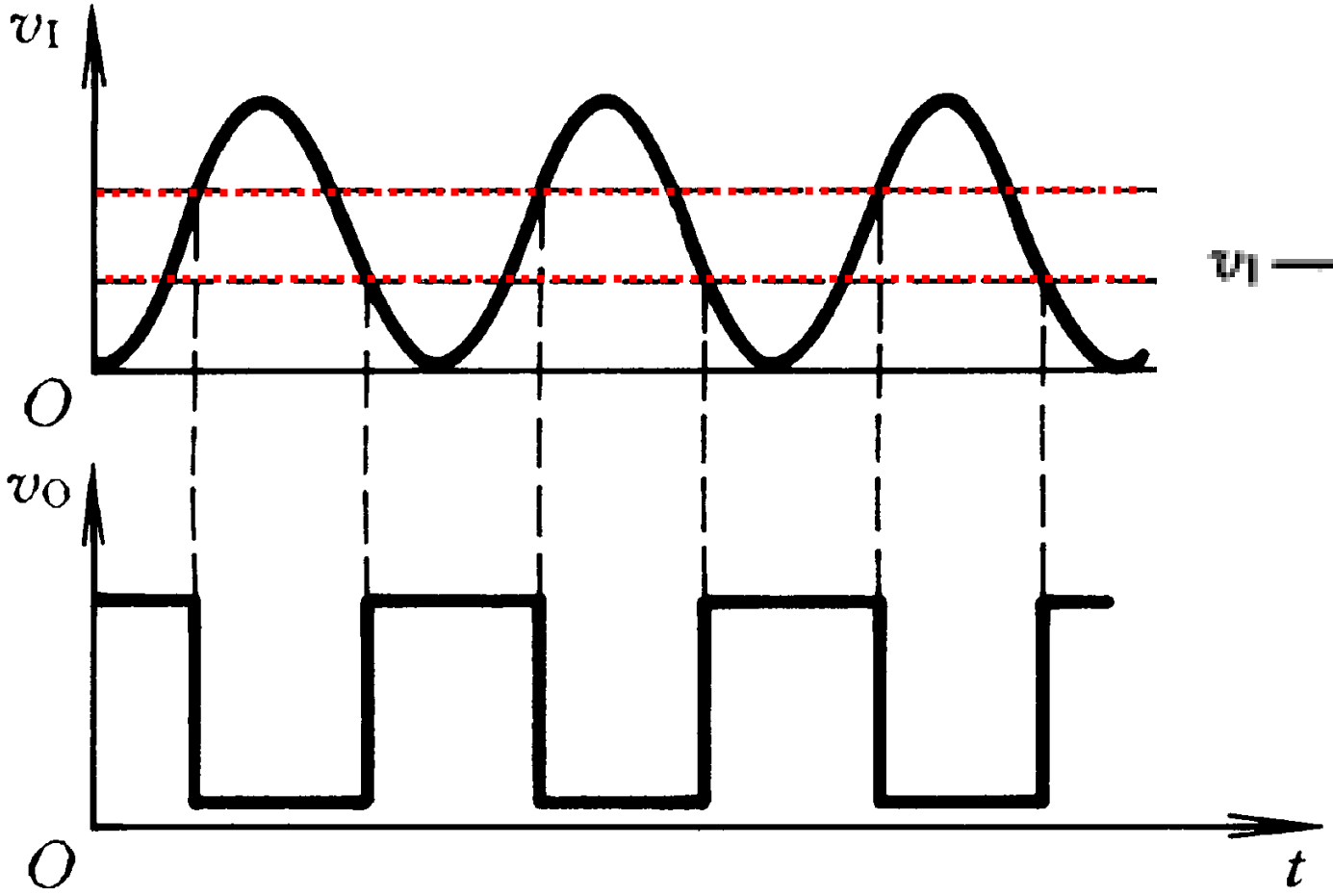


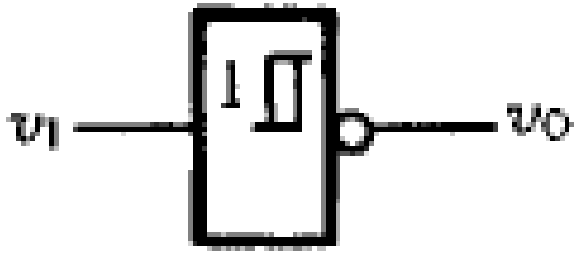

A
V_{t+}
V_{t-}
B

Applications of Schimitt Trigger

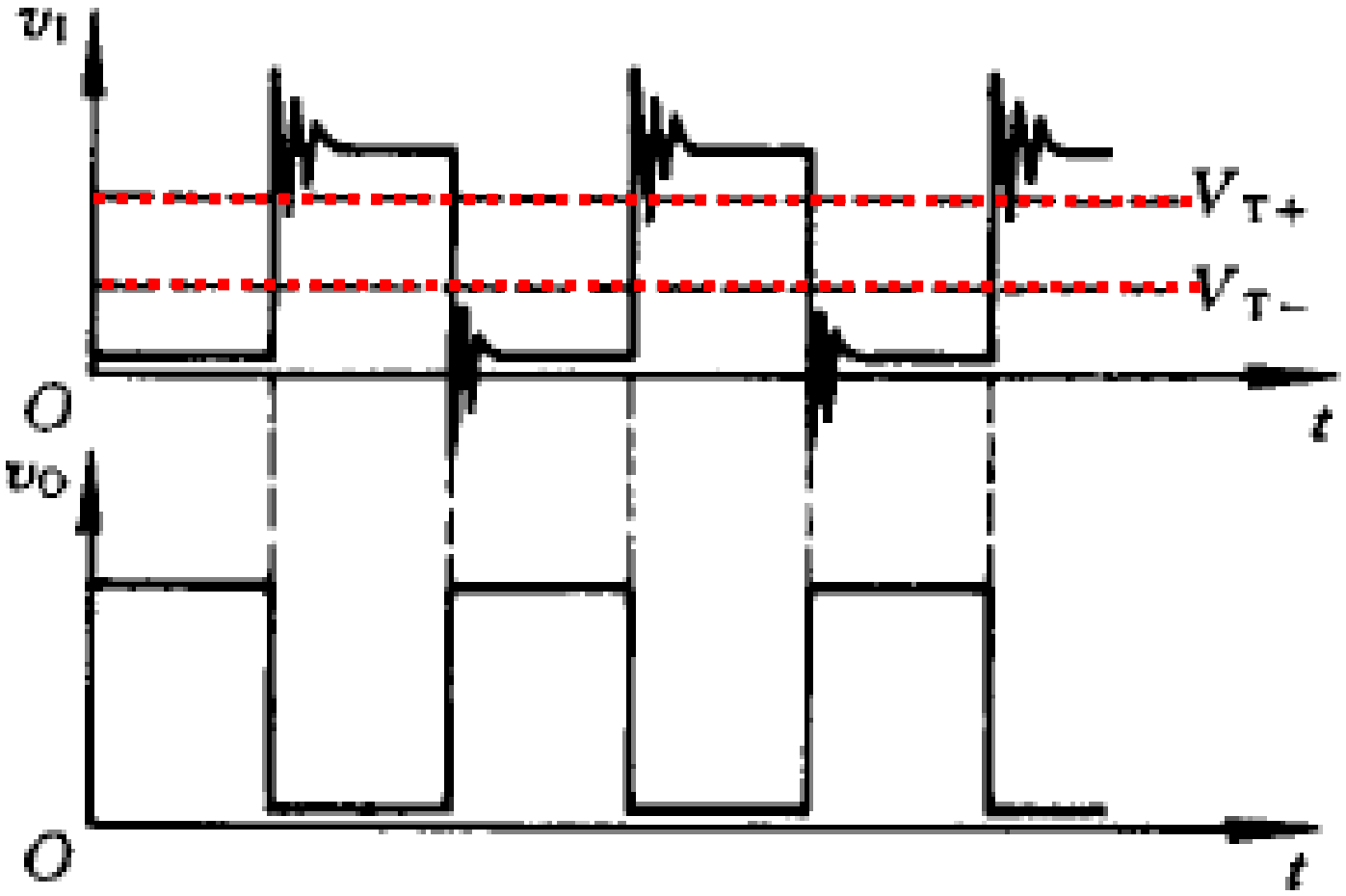
- Pulse conditioning
- Noise immunity
- Amplitude Checking


1
v_I
v_O


v_I
O
v_O
O
t


1
v_I
v_O

Noise immunity



Amplitude Checking