Chapter 3

Logic Gates
（逻辑门）

Objectives:

Basic gates: NOT（非）,AND（与）, OR（或）
Extend gates: NAND（与非）,NOR（或非）,
Exclusive-OR（异或）, Exclusive-NOR（同或）
Symbols

Introductory Paragraph

- Logic Gate is the smallest operational function unit in a digital system, which will perform the basic operations.

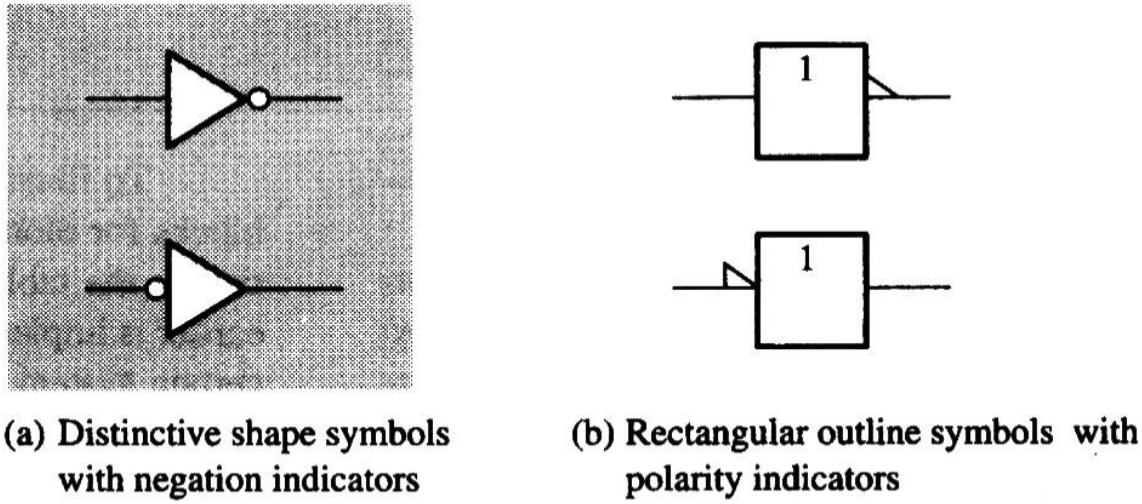
(在数字系统中，逻辑门是最小的功能单元)

- Logic Symbols are used to represent the logic gates in accordance with ANSI/IEEE standard.

(ANSI/IEEE国际组织规定了表示这些逻辑门的符号规范)

3-1 THE INVERTER（反相器）

- The inverter performs the operation called inversion（反相） or complementation（反码）.
- The polarity indicator is a "bubble" . When appearing on the input/output, it means that a LOW level is the active or asserted input/output state.



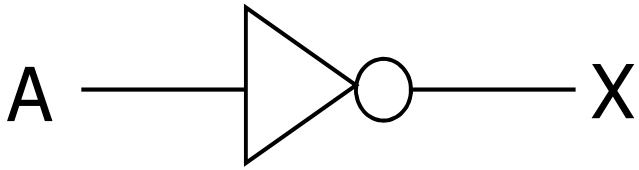
(a) Distinctive shape symbols with negation indicators

(b) Rectangular outline symbols with polarity indicators

FIGURE 3–1
Standard logic symbols for the inverter (ANSI/IEEE Std. 91–1984).

The Inverter

- ***Symbol***



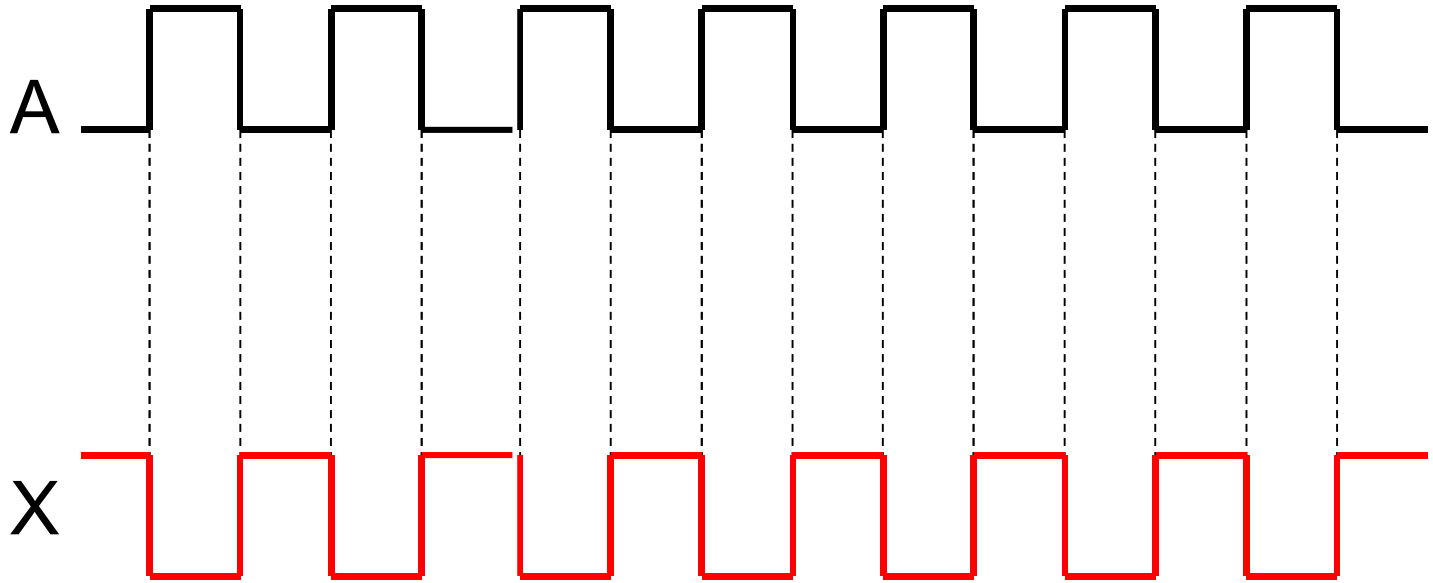
- ***Logic expression***

$$X = \bar{A}$$

- ***Truth table***
  （真值表）

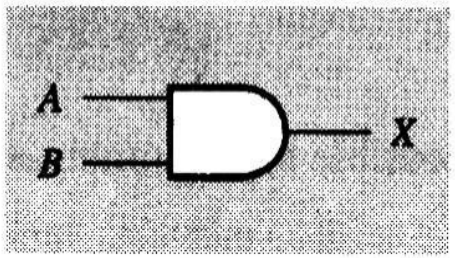
Input A	Output X
0	1
1	0

- ***Waveform***

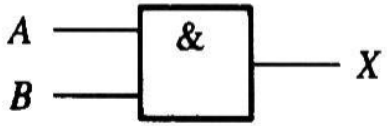


3-2 THE AND GATE（与门）

- The AND gate produces a HIGH only when all of the inputs are HIGH. When any of the inputs is LOW, the output is LOW.
- The basic purpose of an AND gate is to determine when certain conditions are simultaneously true.



(a) Distinctive shape



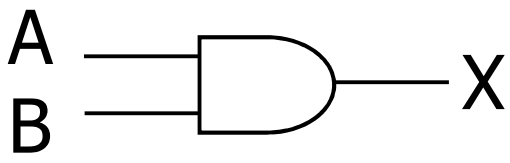
(b) Rectangular outline with the AND (&) qualifying symbol

FIGURE 3–8

Standard logic symbols for the AND gate showing two inputs (ANSI/IEEE Std. 91–1984).

The AND Gate

- ***Symbol***



- ***Logic expression***

$$X = AB$$

- ***Truth table***

Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	1
1	1	1

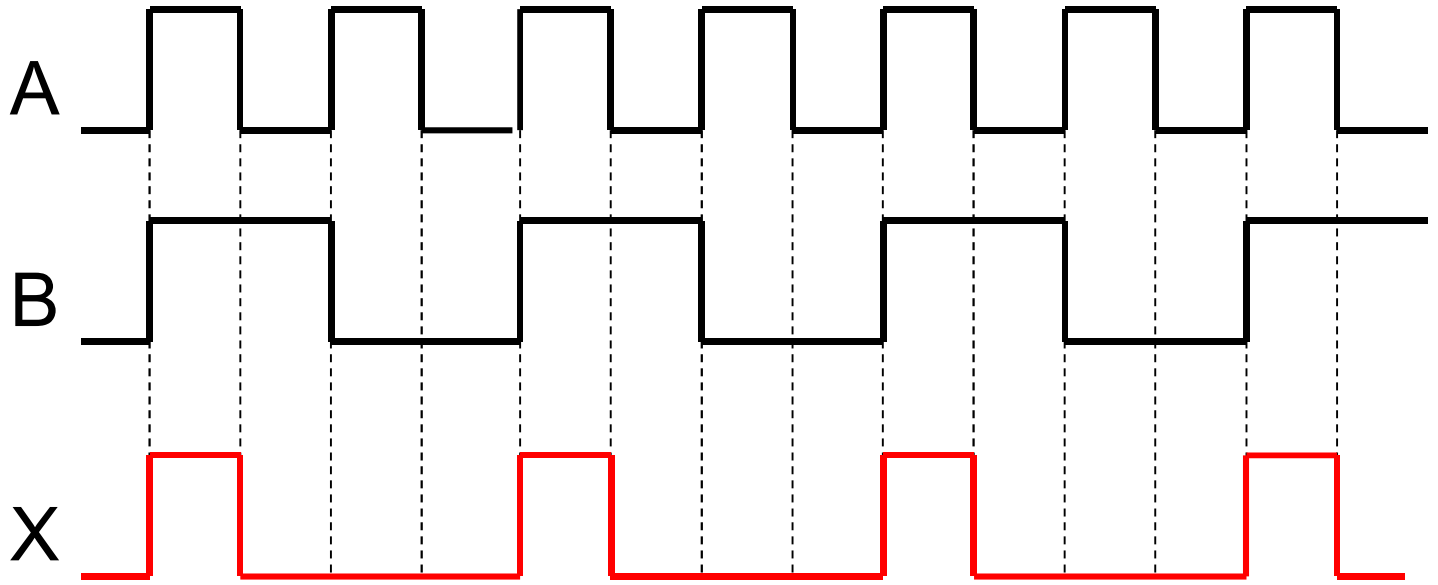
The AND Gate

- Boolean multiplication is the same as the AND function.

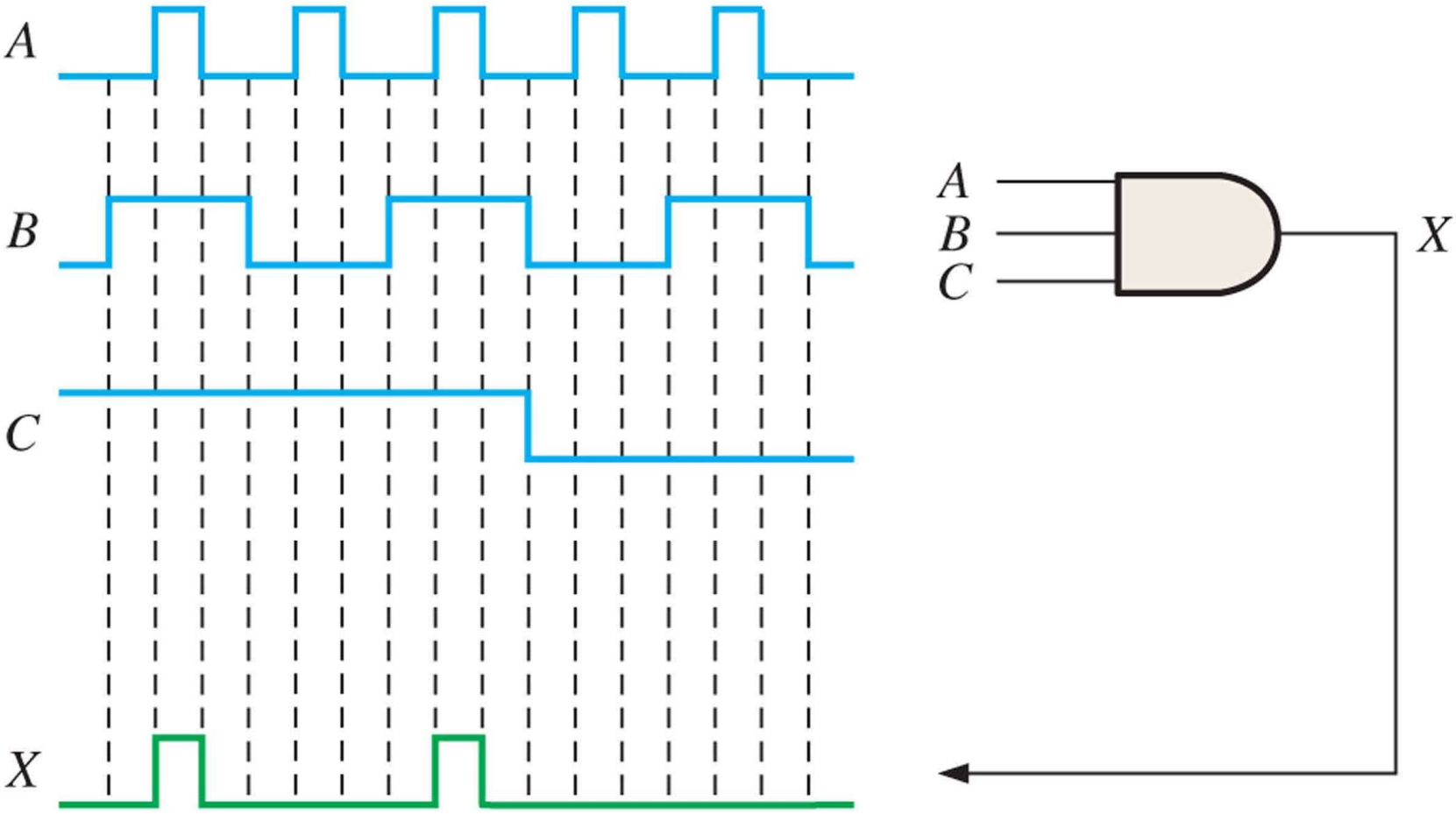
TABLE 3–4

A	B	$AB = X$
0	0	$0 \cdot 0 = 0$
0	1	$0 \cdot 1 = 0$
1	0	$1 \cdot 0 = 0$
1	1	$1 \cdot 1 = 1$

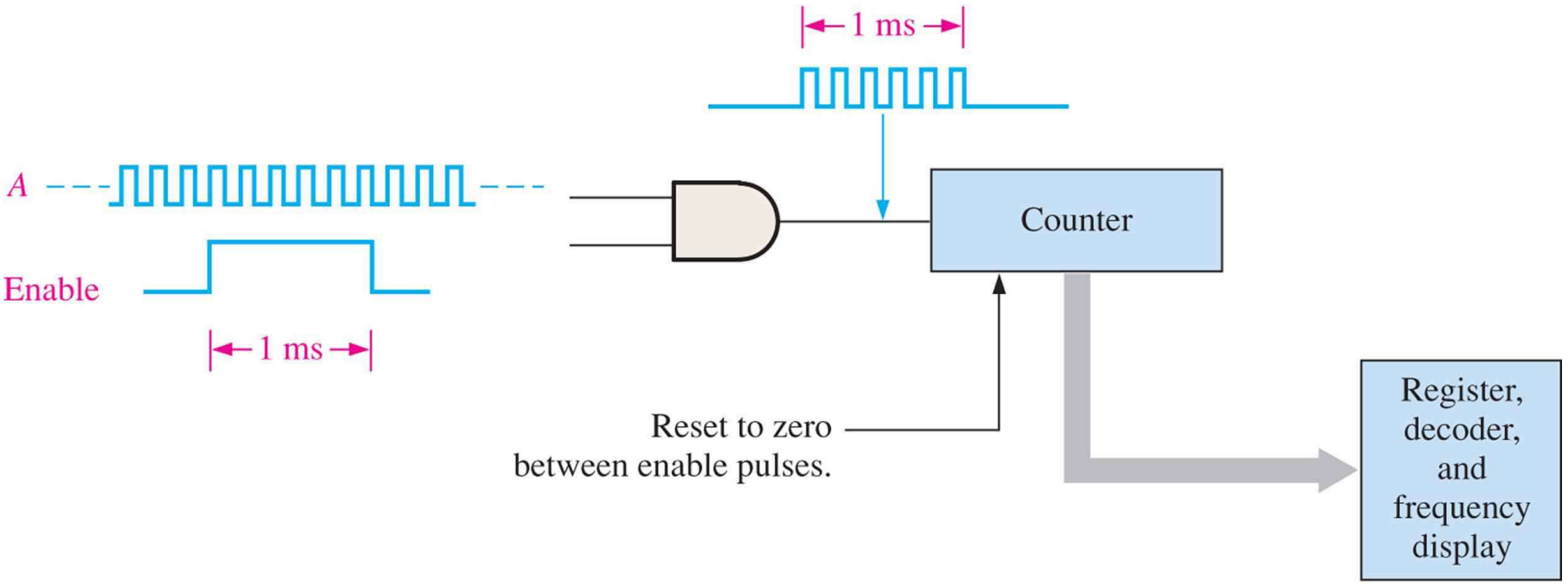
- ***Waveform***



The AND Gate can be extended to any number of inputs

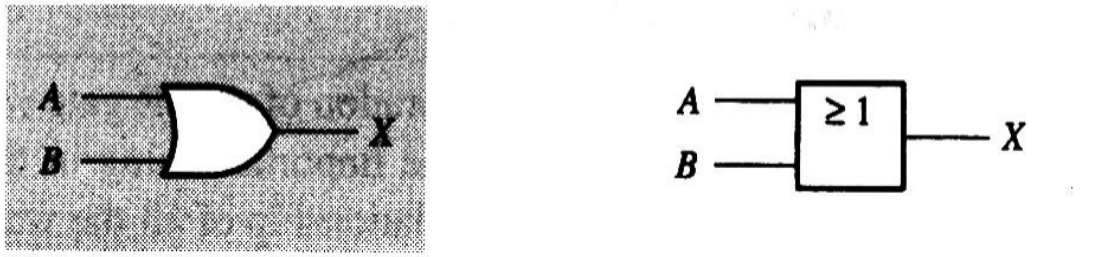


An AND gate performing an enable/inhibit function for a frequency counter.



3-3 THE OR GATE（或门）

- The OR gate produces a LOW only when all of the inputs are LOW. When any of the inputs is HIGH, the output is HIGH.
- The basic purpose of an OR gate is to determine when one or more conditions are true.



(a) Distinctive shape

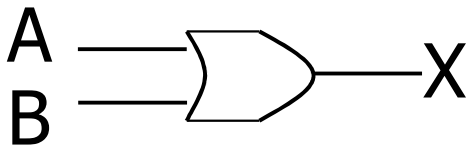
(b) Rectangular outline with the OR (≥ 1) qualifying symbol

FIGURE 3–17

Standard logic symbols for the OR gate showing two inputs (ANSI/IEEE Std. 91–1984).

The OR Gate

- ***Symbol***



- ***Logic expression***

$$X = A + B$$

- ***Truth table***

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

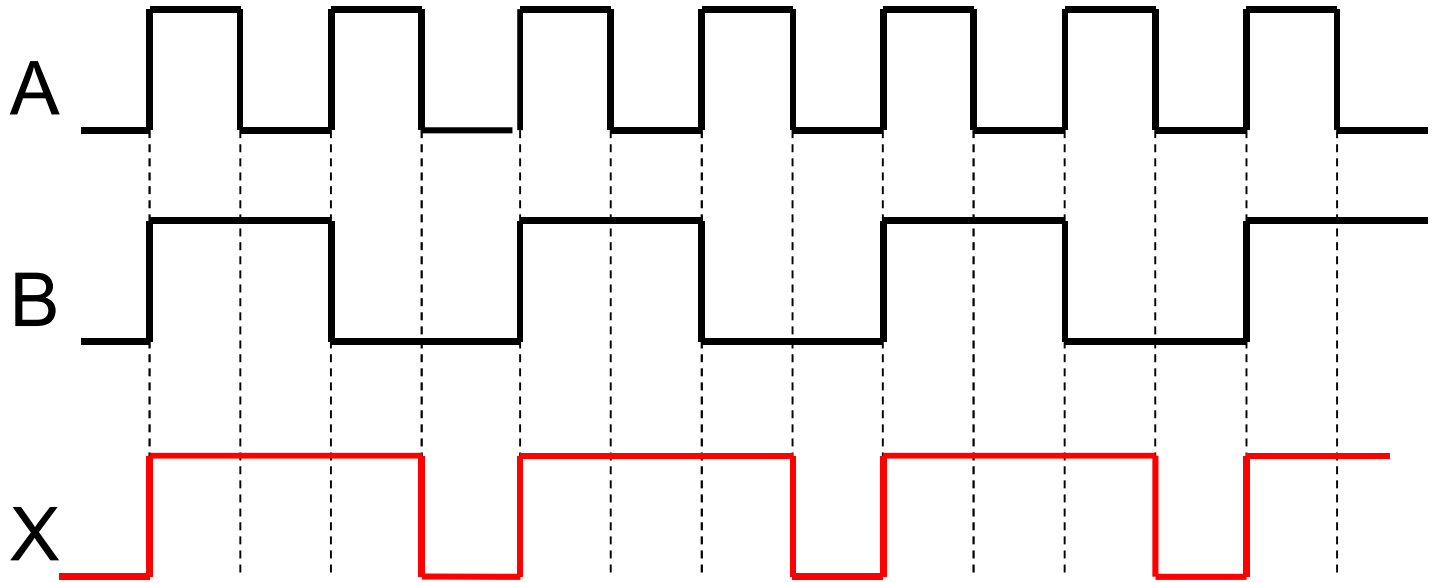
The OR Gate

- Boolean addition is the same as the OR function.

TABLE 3–6

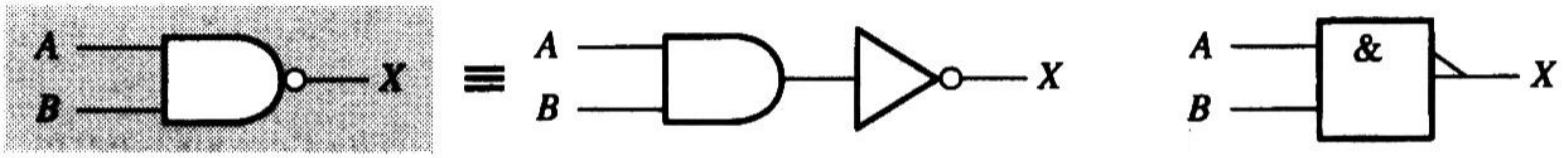
A	*B*	*A* + *B* = *X*
0	0	0 + 0 = 0
0	1	0 + 1 = 1
1	0	1 + 0 = 1
1	1	1 + 1 = 1

- ***Waveform***



3-4 THE NAND GATE（与非门）

- The NAND gate produces a LOW only when all of the inputs are HIGH. When any of the inputs is LOW, the output is HIGH.
- The term NAND is a contraction of NOT-AND and implies an AND function with a complemented (inverted) output.



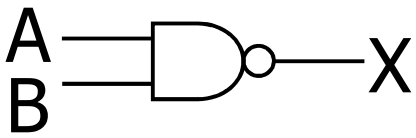
(a) Distinctive shape, 2-input NAND gate and its NOT/AND equivalent

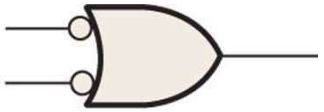
(b) Rectangular outline, 2-input NAND gate with polarity indicator

FIGURE 3–25
Standard NAND gate logic symbols (ANSI/IEEE Std. 91–1984).

The NAND Gate

- ***Symbol***





Negative-OR

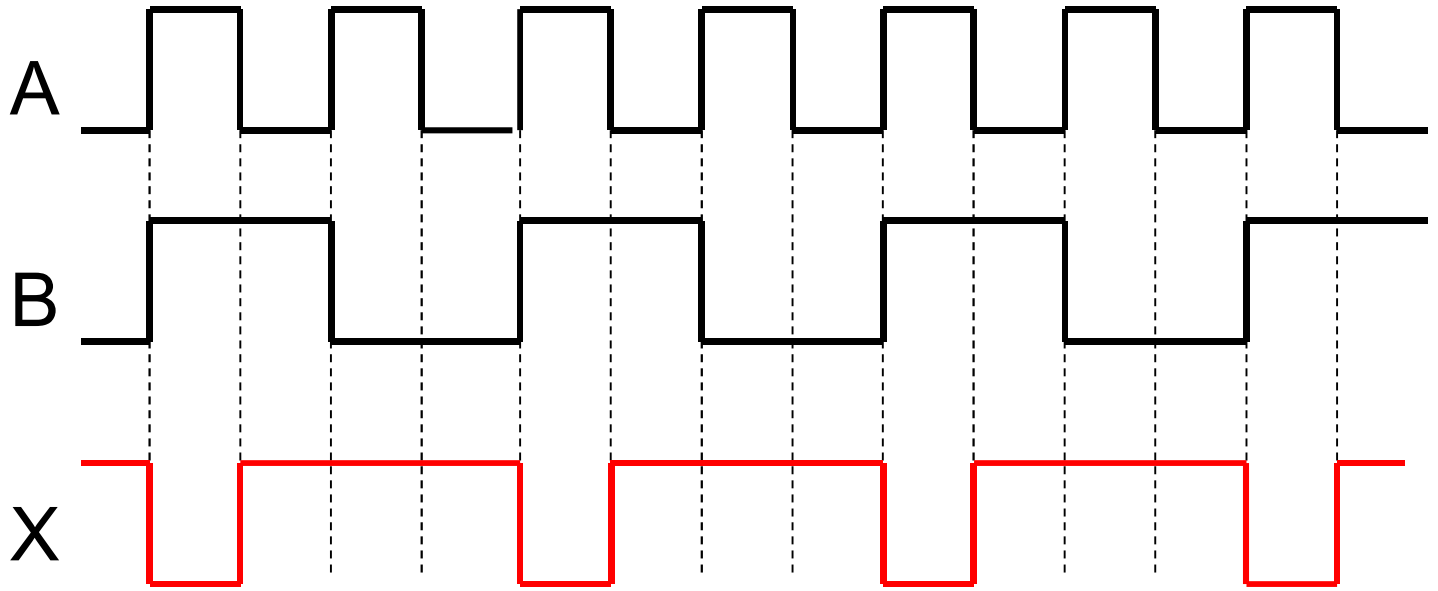
- ***Logic expression***

$$X = \overline{AB}$$

- ***Truth table***

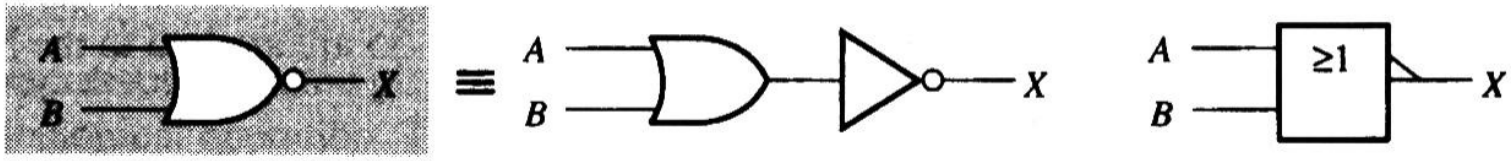
Inputs		Output
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

- ***Waveform***



3-5 THE NOR GATE（或非门）

- The NOR gate produces a HIGH only when all of the inputs are LOW. When any of the inputs is HIGH, the output is LOW.



(a) Distinctive shape, 2-input NOR gate and its NOT/OR equivalent

(b) Rectangular outline, 2-input NOR gate with polarity indicator

FIGURE 3–33
Standard NOR gate logic symbols (ANSI/IEEE Std. 91–1984).

The NOR Gate

- ***Symbol***

Negative-AND gate

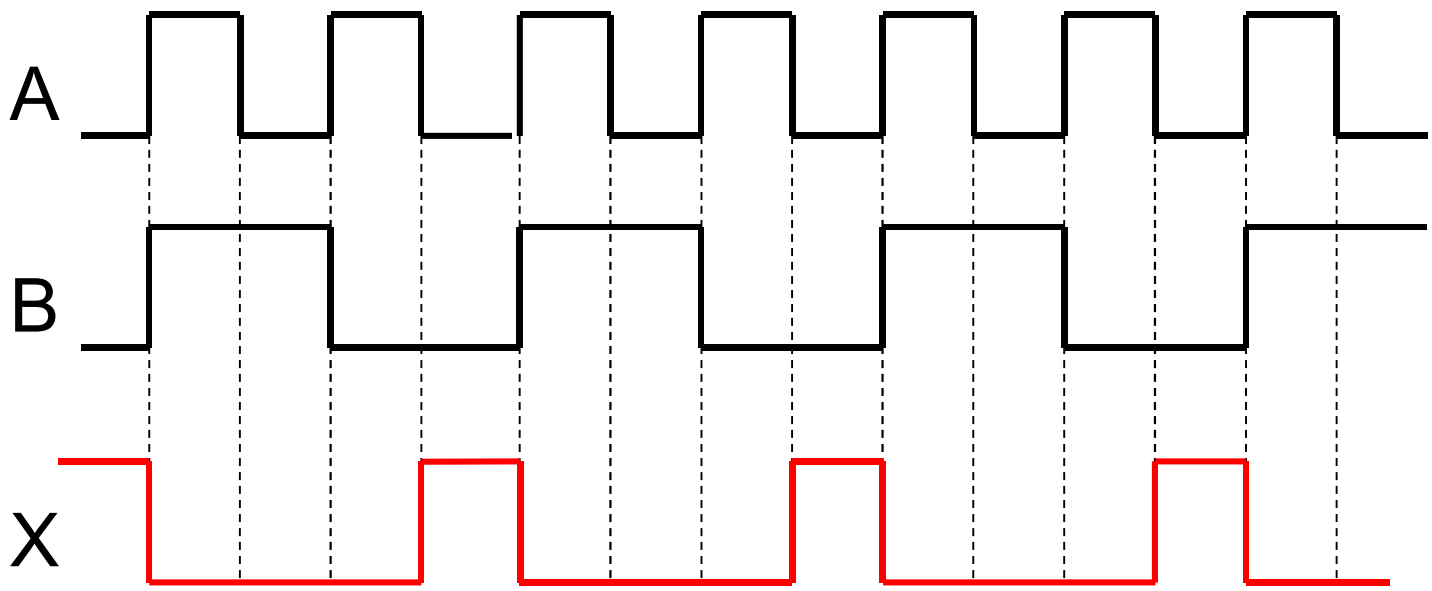
- ***Logic expression***

$$X = \overline{A + B}$$

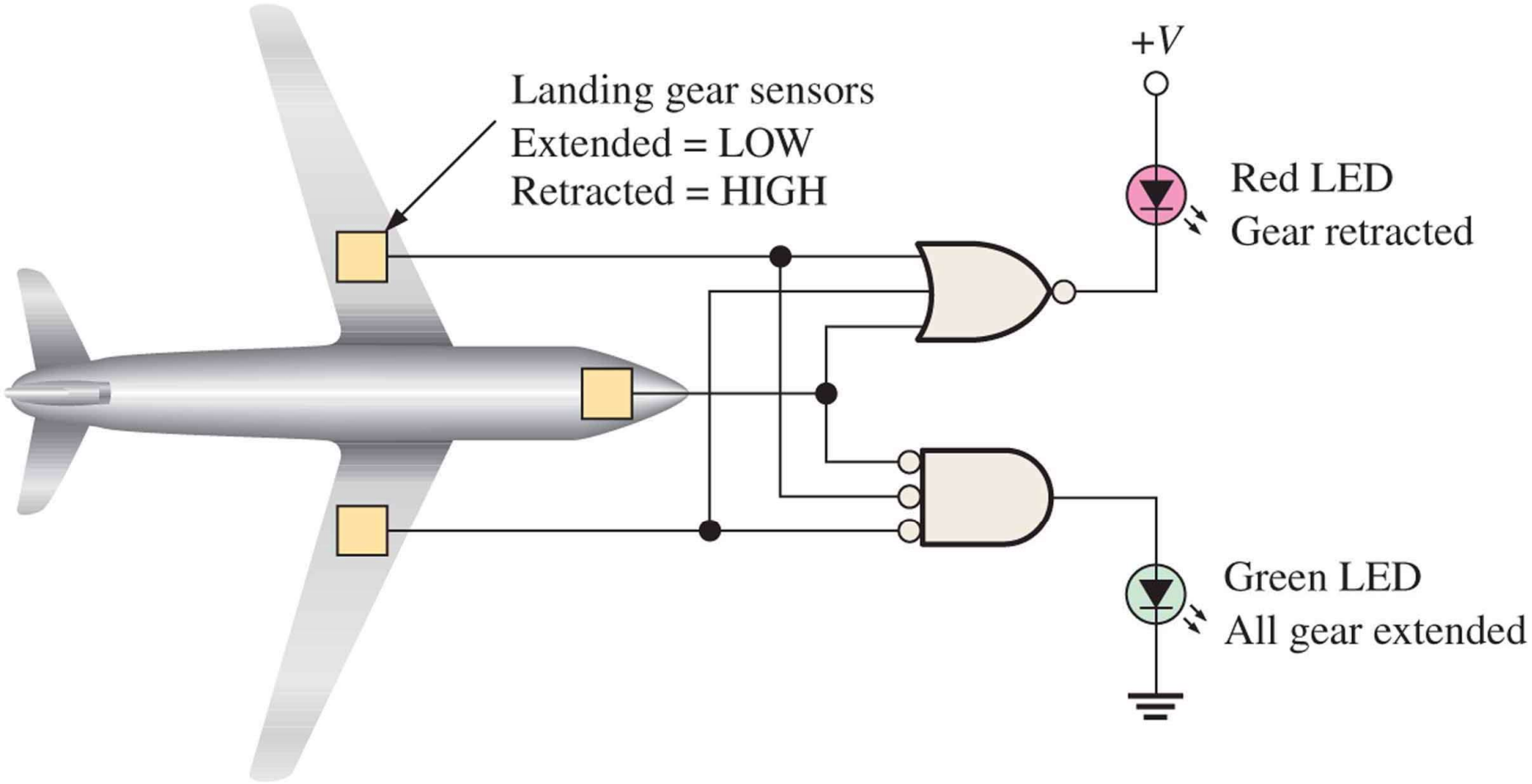
- ***Truth table***

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

- ***Waveform***

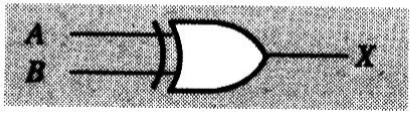


Example: Airplane gear monitoring system

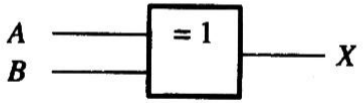


3-6 THE EXCLUSIVE-OR AND EXCLUSIVE-NOR GATES

- The exclusive-OR (XOR) gate has only two inputs.
- The output of an XOR gate is HIGH only when two inputs are at opposite logic levels.



(a) Distinctive shape

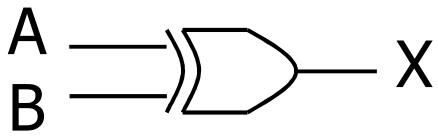


(b) Rectangular outline with the XOR qualifying symbol (= 1)

FIGURE 3–41
Standard logic symbols for the exclusive-OR gate.

The XOR Gates（异或门）

- ***Symbol***



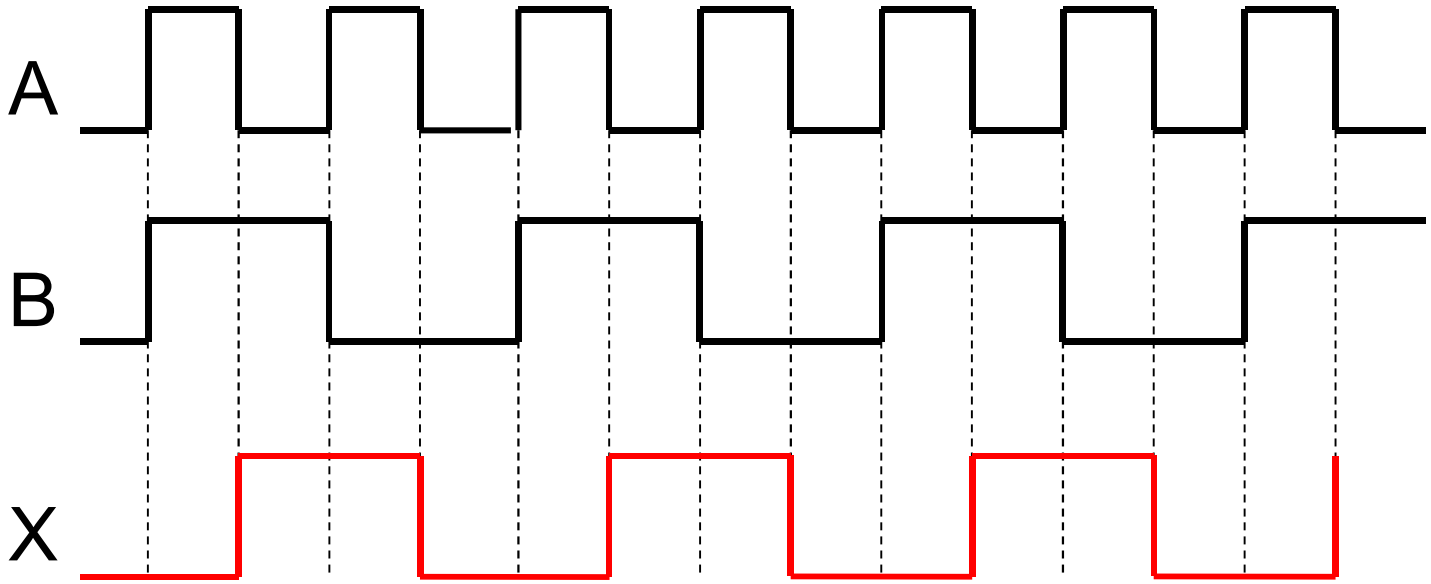
- ***Logic expression***

$$X = A \oplus B = A\overline{B} + \overline{A}B$$

- ***Truth table***

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

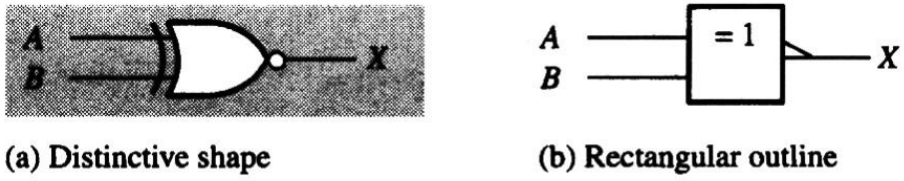
- ***Waveform***



The XNOR gates（同或门）

- The exclusive-NOR (XNOR) gate has only two inputs.
- The output of an XNOR gate is LOW only when two inputs are at opposite logic levels.

FIGURE 3–44
Standard logic symbols for the exclusive-NOR gate.

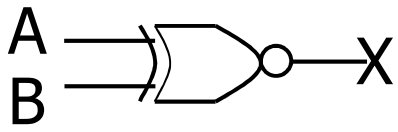


(a) Distinctive shape

(b) Rectangular outline

The XNOR Gates

- ***Symbol***



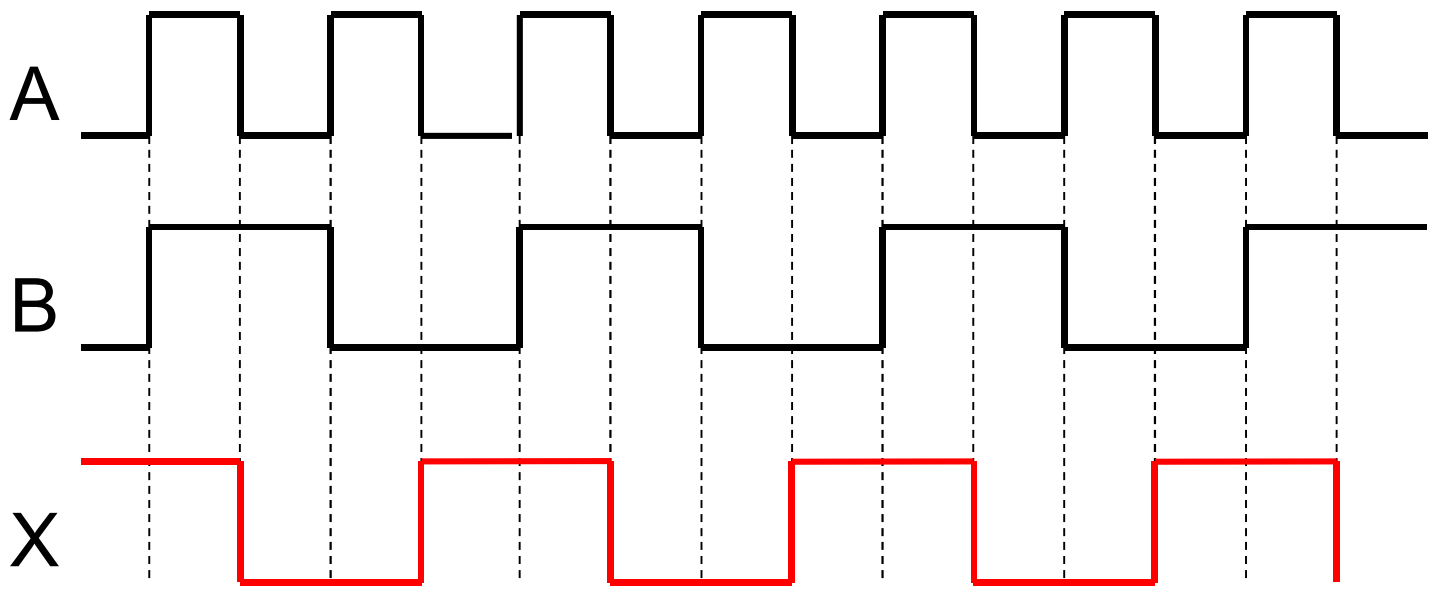
- ***Logic expression***

$$X = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$$

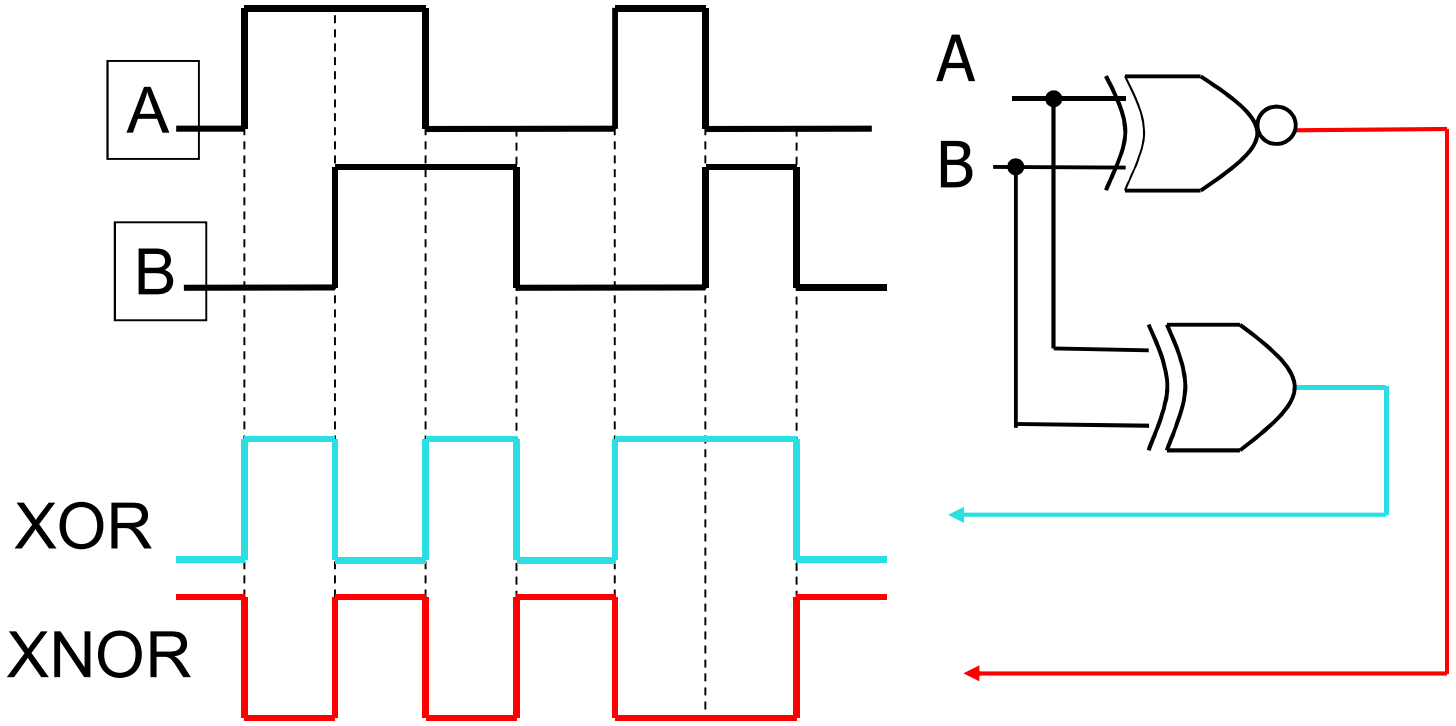
- ***Truth table***

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

- ***Waveform***

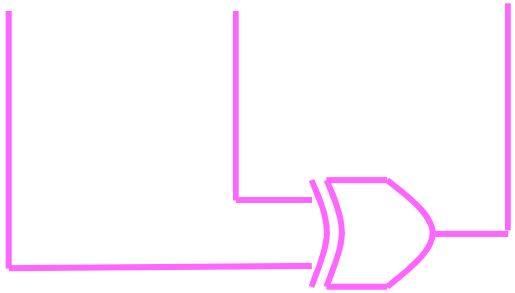


Example: Determine the output waveform for the XOR gate and for the XNOR, given the input waveforms of A and B as follows:



Example: The XOR gate used to add two bits.

Input bits		Output
A	B	Sum
0	0	0
0	1	1
1	0	1
1	1	0 (without 1 carry)



Quiz

1. The truth table for a 2-input AND gate is

a.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	0

b.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	0

c.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	0
1	0	0
1	1	1

d.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	1

Quiz

2. The truth table for a 2-input NOR gate is

a.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	0

b.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	0

c.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	0
1	0	0
1	1	1

d.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	1

Quiz

3. The truth table for a 2-input XOR gate is

a.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	0

b.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	0

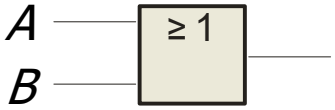
c.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	0
1	0	0
1	1	1

d.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	1

Quiz

4. The symbol 

is for a(n)

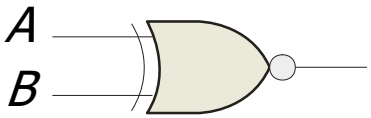
a. OR gate

b. AND gate

c. NOR gate

d. XOR gate

Quiz

5. The symbol 

is for a(n)

a. OR gate

b. XNOR gate

c. NOR gate

d. XOR gate

Quiz

6. A logic gate that produces a HIGH output only when all of its inputs are HIGH is a(n)

a. OR gate

b. AND gate

c. NOR gate

d. NAND gate

Quiz

7. The expression $X = A + B$ means

a. A OR B

b. A AND B

c. A XOR B

d. A XNOR B

Quiz

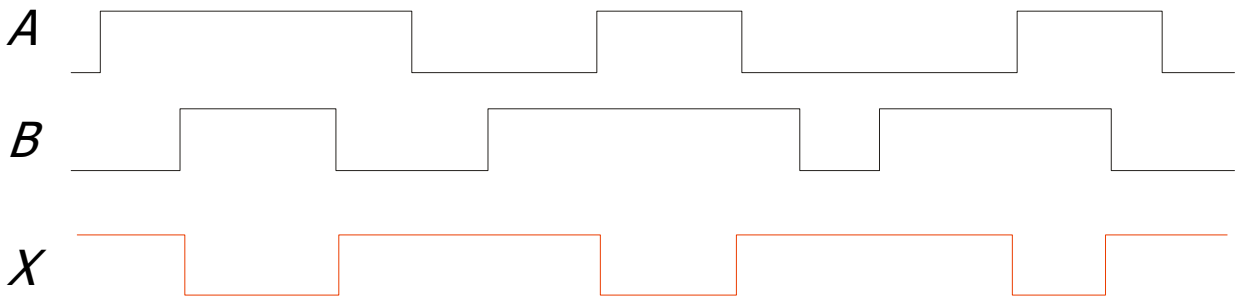
8. A 2-input gate produces the output shown. (*X* represents the output.) This is a(n)

a. OR gate

b. AND gate

c. NOR gate

d. NAND gate



Quiz

9. A 2-input gate produces a HIGH output only when the inputs agree. This type of gate is a(n)

a. OR gate

b. AND gate

c. NOR gate

d. XNOR gate

Quiz

10. The required logic for a PLD can be specified in an Hardware Description Language by

a. text entry

b. schematic entry

c. state diagrams

d. all of the above

Homework

- Problems: 2, 7, 10, 12, 15, 17, 19, 24

Answers

1. c
2. b
3. a
4. a
5. d
6. b
7. c
8. d
9. d
10. d