Chapter 7 Flip-Flops and Related Devices

触发器以及相关设备

- Logic circuits
  - Combinational Circuits（组合电路）
  - Sequential Circuits（时序电路）

Basic Block → **Flip-Flops**

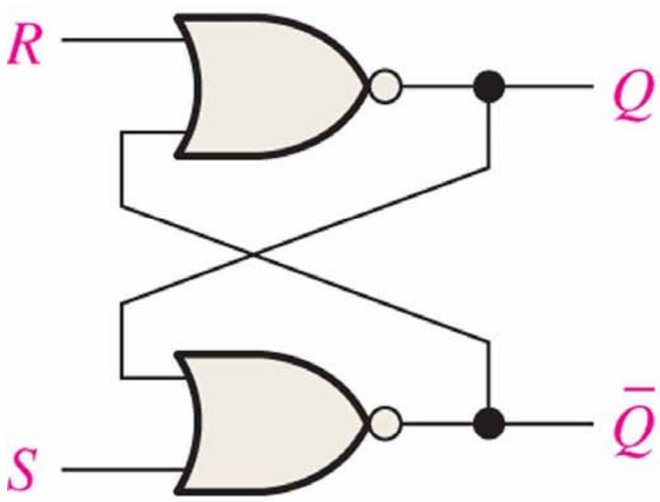
- ***Objectives***
  - Latches（锁存器）
  - Edge-triggered Flip-Flops（边沿触发器）
    - S-R FF
    - D FF
    - J-K FF
    - T FF

7.1 Latches（锁存器）

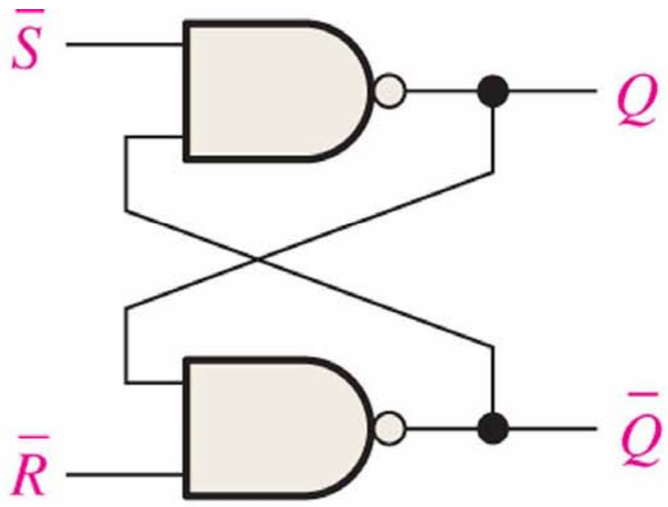
- The ***latch*** is a type of temporary device that has two stable states (***bistable***) and is normally placed in a category separate from that of ***flip-flops***.
- The difference between latches and flip-flops is the method used for changing their states.

- ***Latches***
  - **S-R (Set-Reset) Latch (SR锁存器)**
  - **Gated S-R Latch (门控锁存器)**
  - **Gated D (Data) Latch**

7.1.1 S-R (Set-Reset) Latch

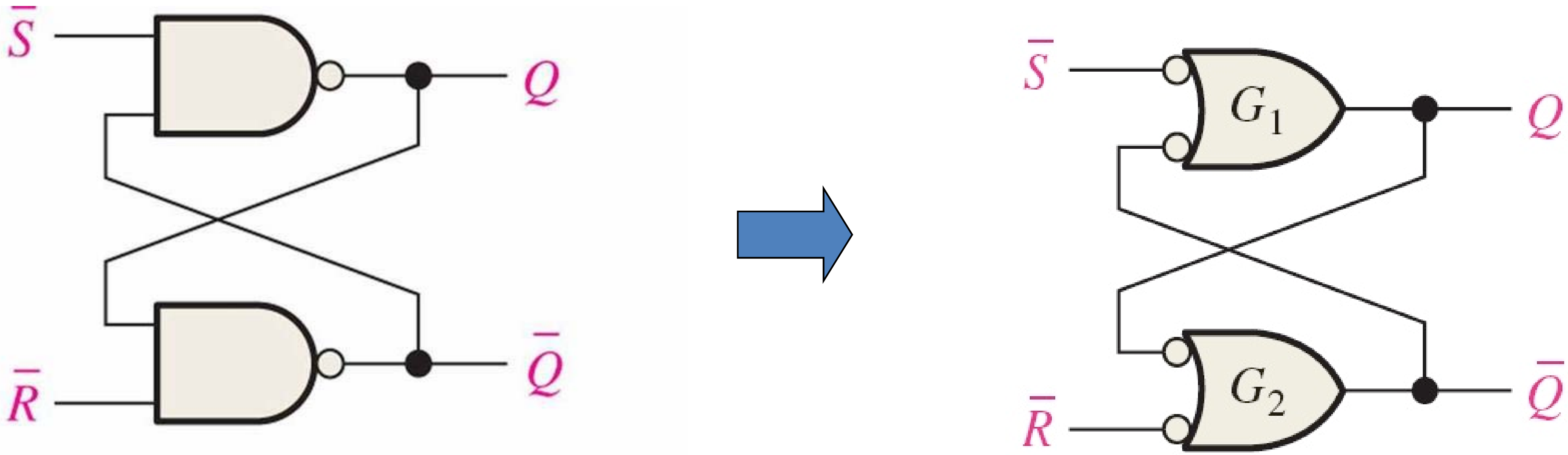


(a) Active-HIGH input S-R latch

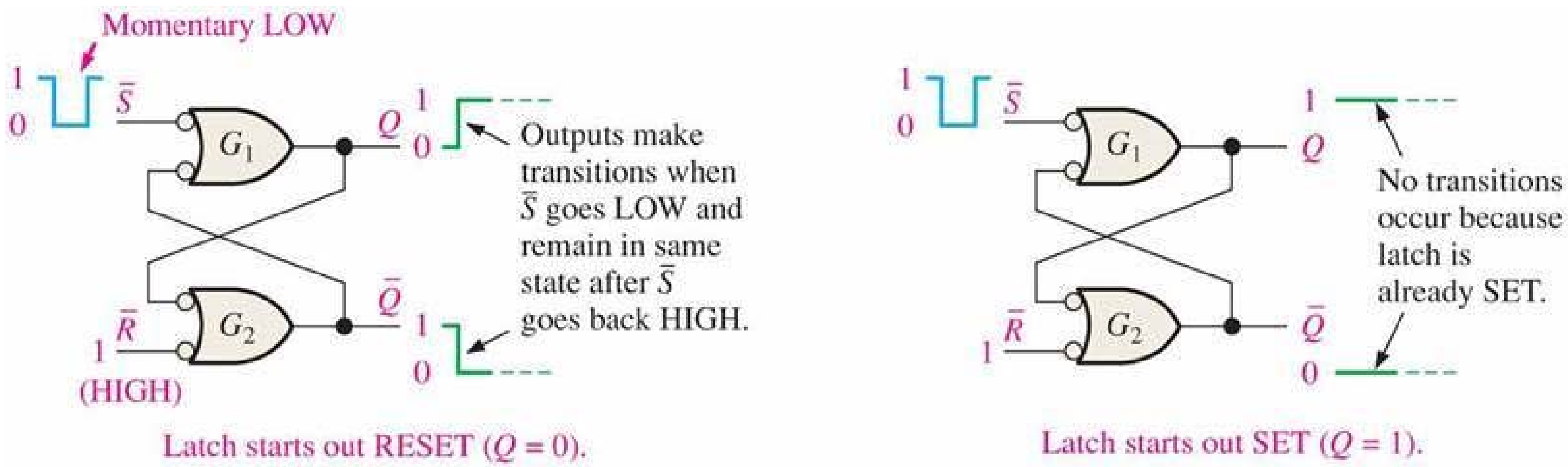


(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

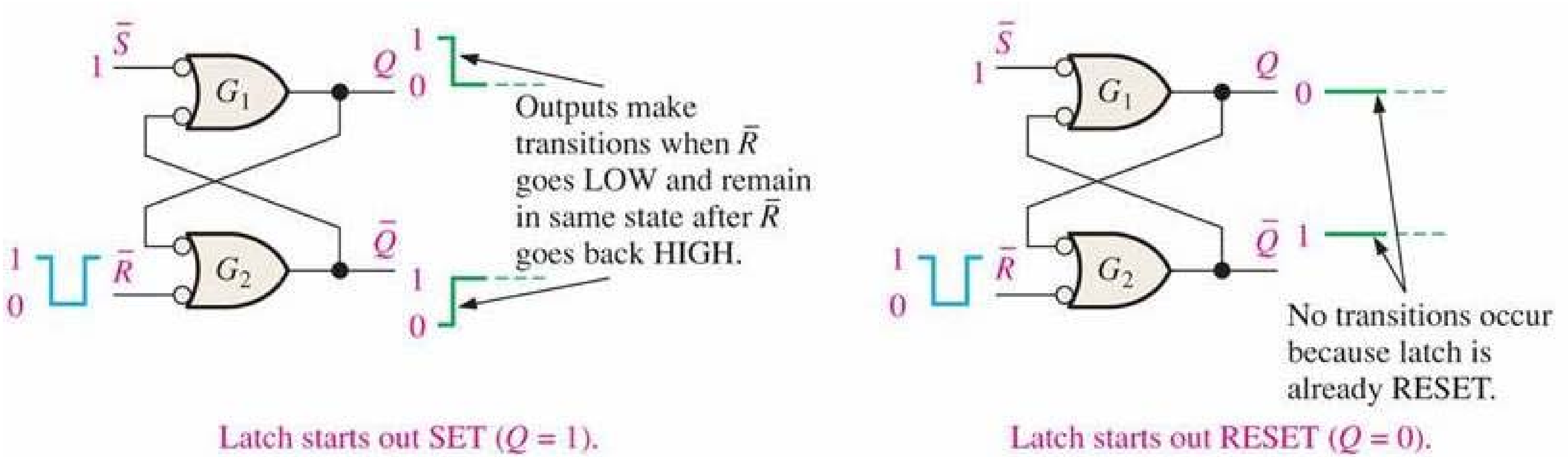
Active-LOW input S-R latch



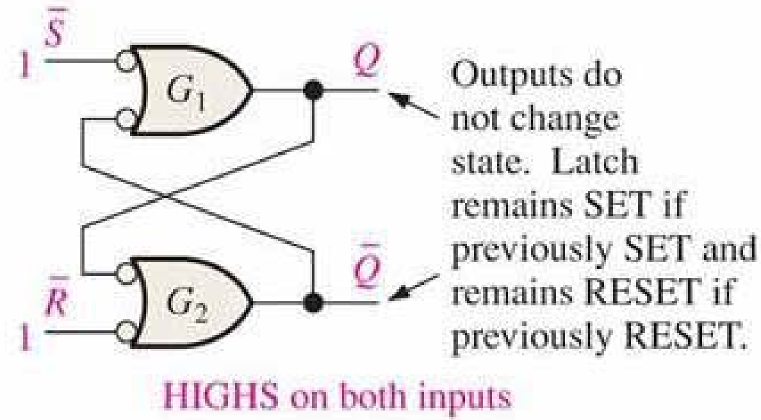
(b) Active-LOW input $\overline{\text{S}}$-$\overline{\text{R}}$ latch



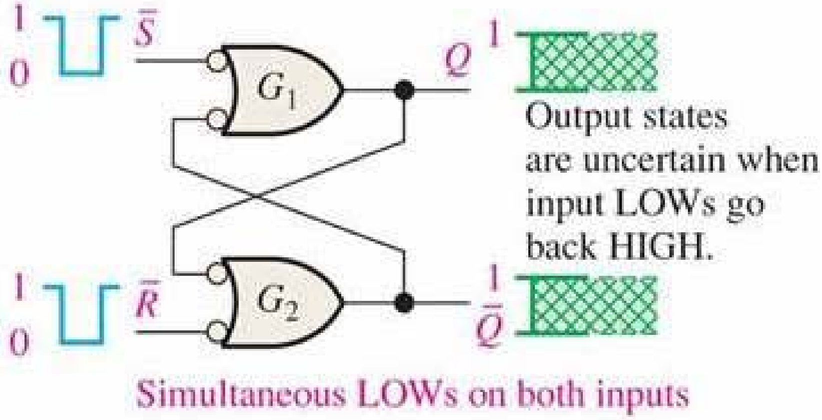
(a) Two possibilities for the SET operation



(b) Two possibilities for the RESET operation



(c) No-change condition

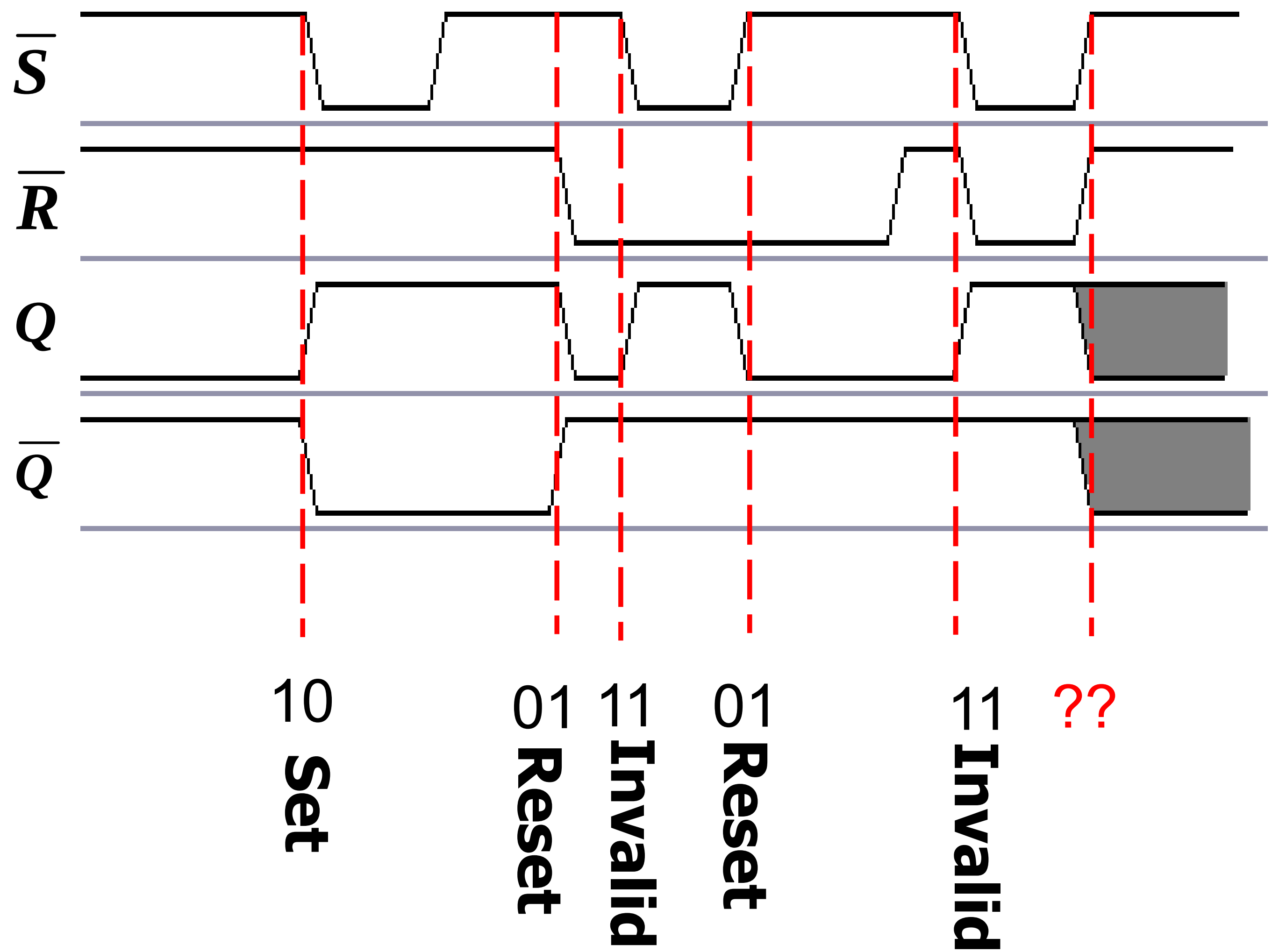


(d) Invalid condition

Truth Table（真值表）

Inputs $\overline{S}$	$\overline{R}$	Outputs Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1*	1*	Invalid condition

Timing diagram



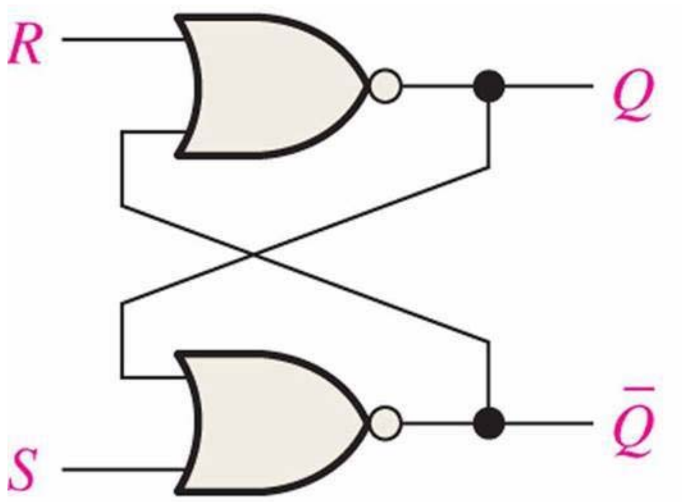
Memory Function

$$S=1;\ R=0;\ \begin{cases} Q=0 \\ \overline{Q}=1 \end{cases} \quad \text{“0”}, \quad \text{remember “0”}$$

$$S=0;\ R=1;\ \begin{cases} Q=1 \\ \overline{Q}=0 \end{cases} \quad \text{“1”}, \quad \text{remember “1”}$$

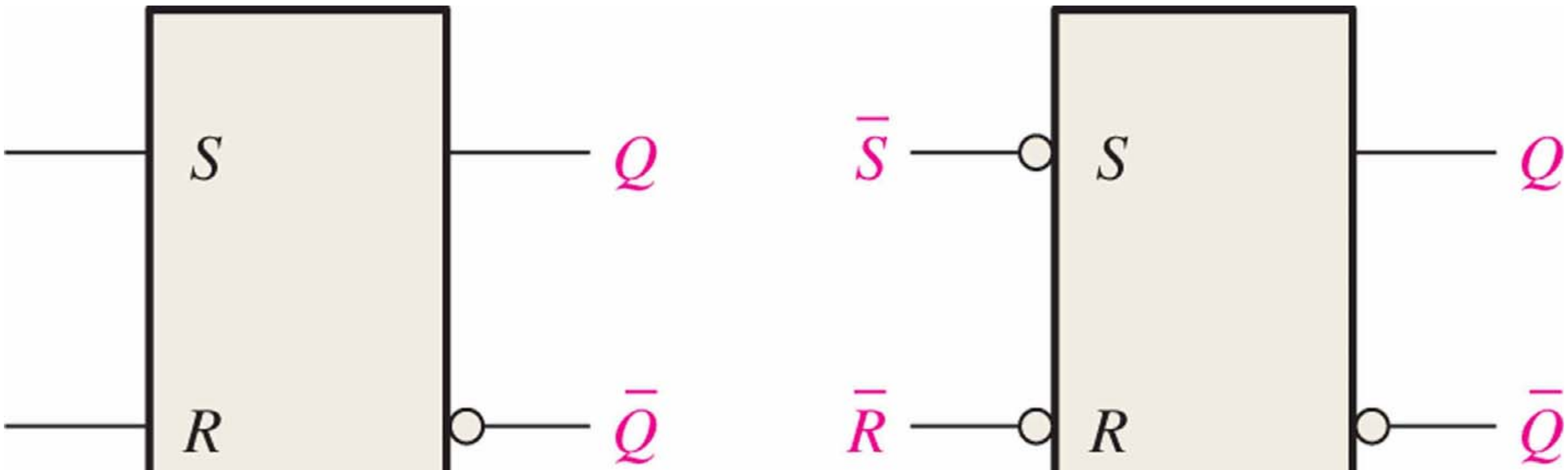
Bi-stable ⇨ **Used to store 1 bit binary number**

Active-HIGH input S-R latch



R	S	Q	$\overline{Q}$
0	0	Q_0	$\overline{Q_0}$
0	1	1	0
1	0	0	1
1	1	0^*	0^*

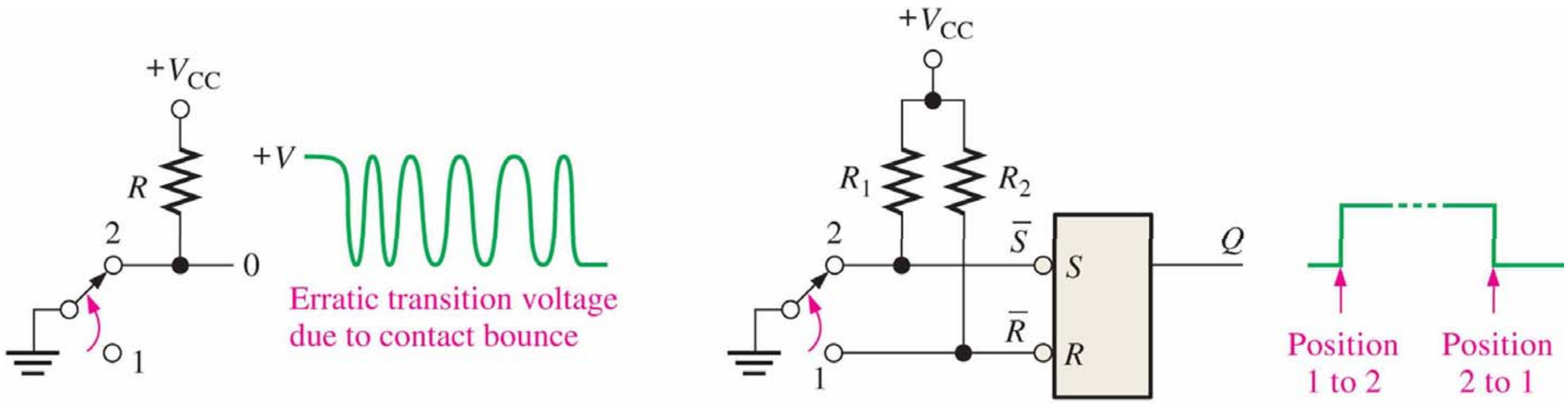
Logic Symbol



(a) Active-HIGH input S-R latch

(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

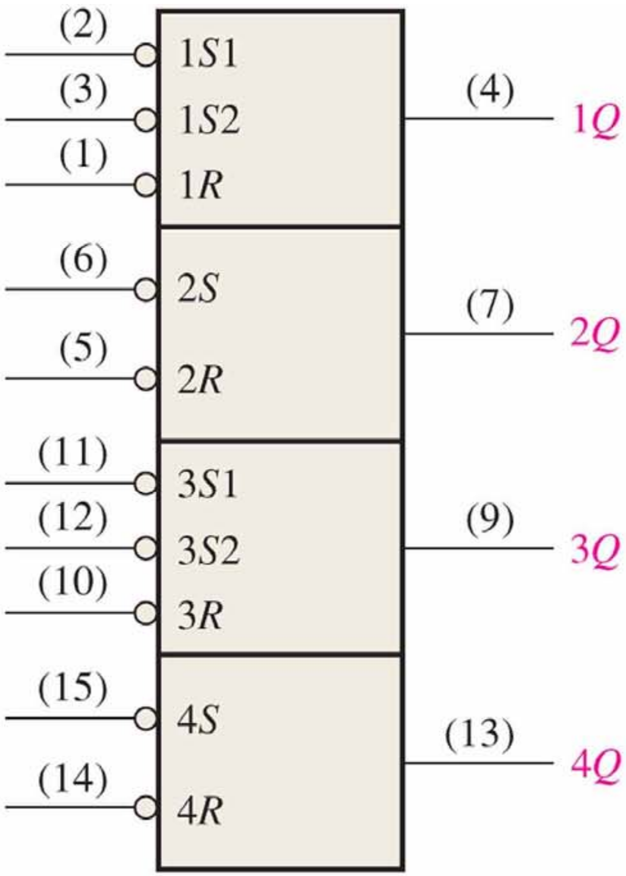
Application Example



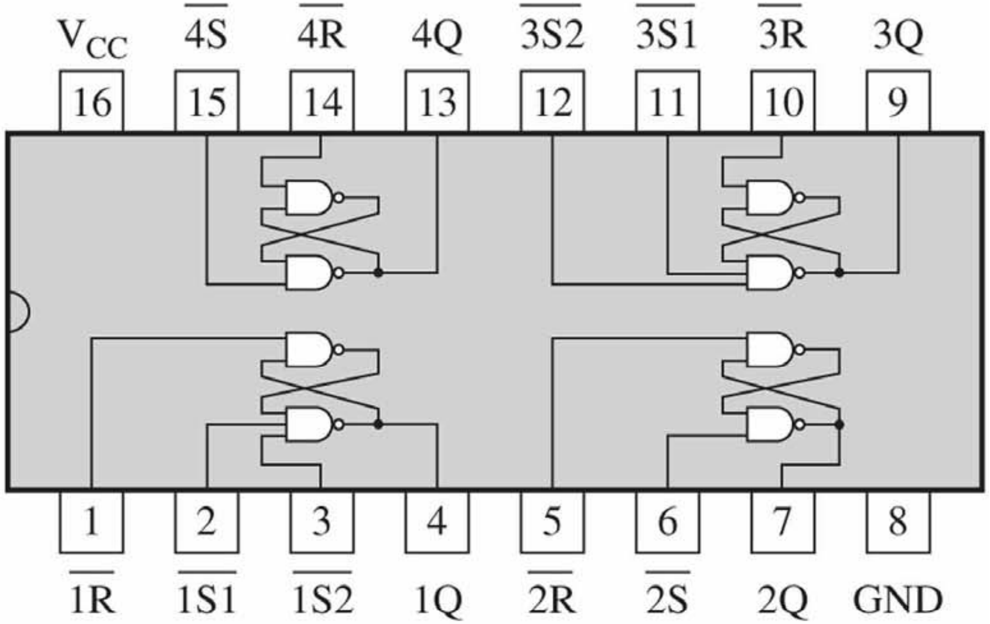
(a) Switch contact bounce

(b) Contact-bounce eliminator circuit

74LS279



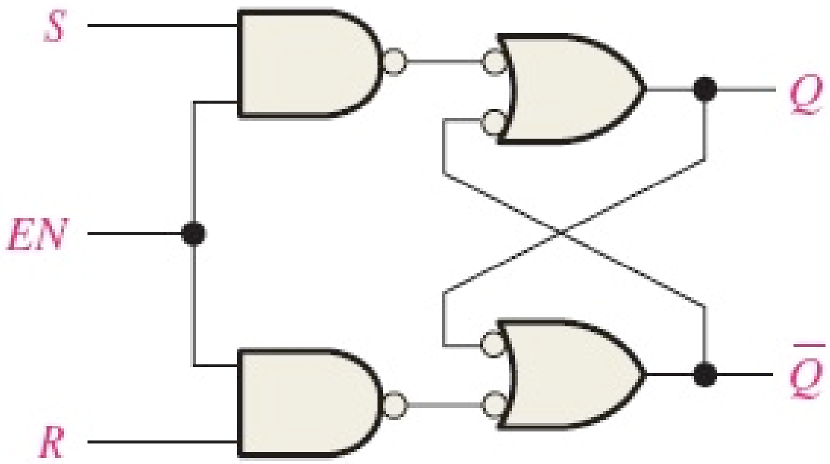
(a) Logic diagram



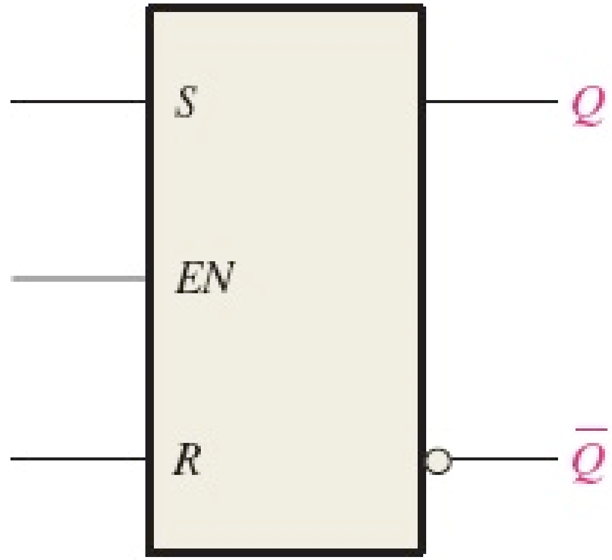
(b) Pin diagram

7.1.2 The Gated S-R Latch（门控S-R锁存器）

EN: control the time when the inputs S and R can control the output. (Level-triggered)

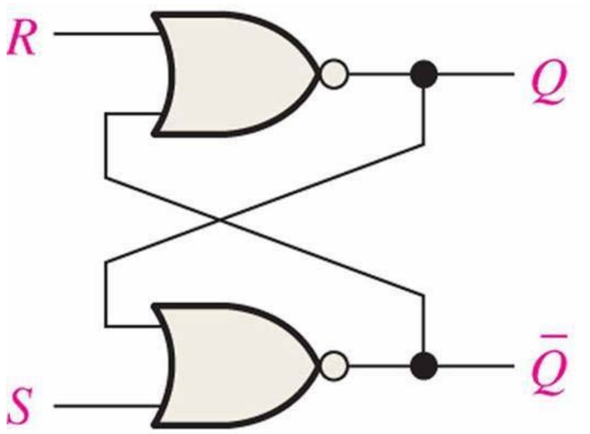


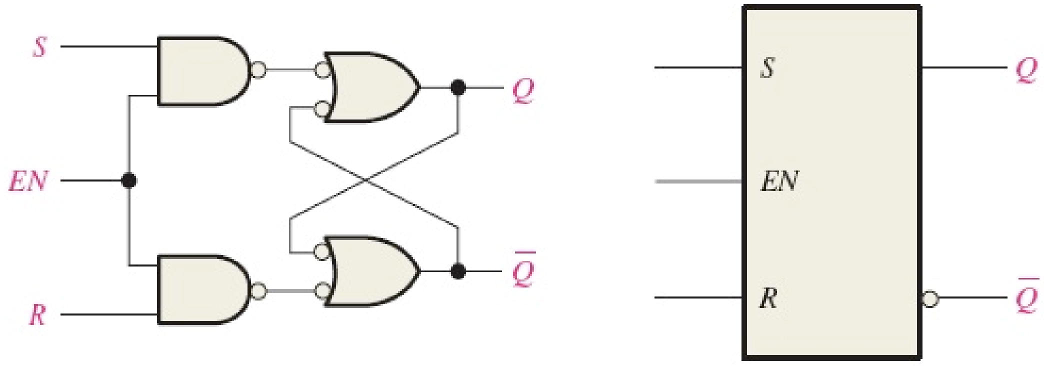
(a) Logic diagram



(b) Logic symbol

Comparison





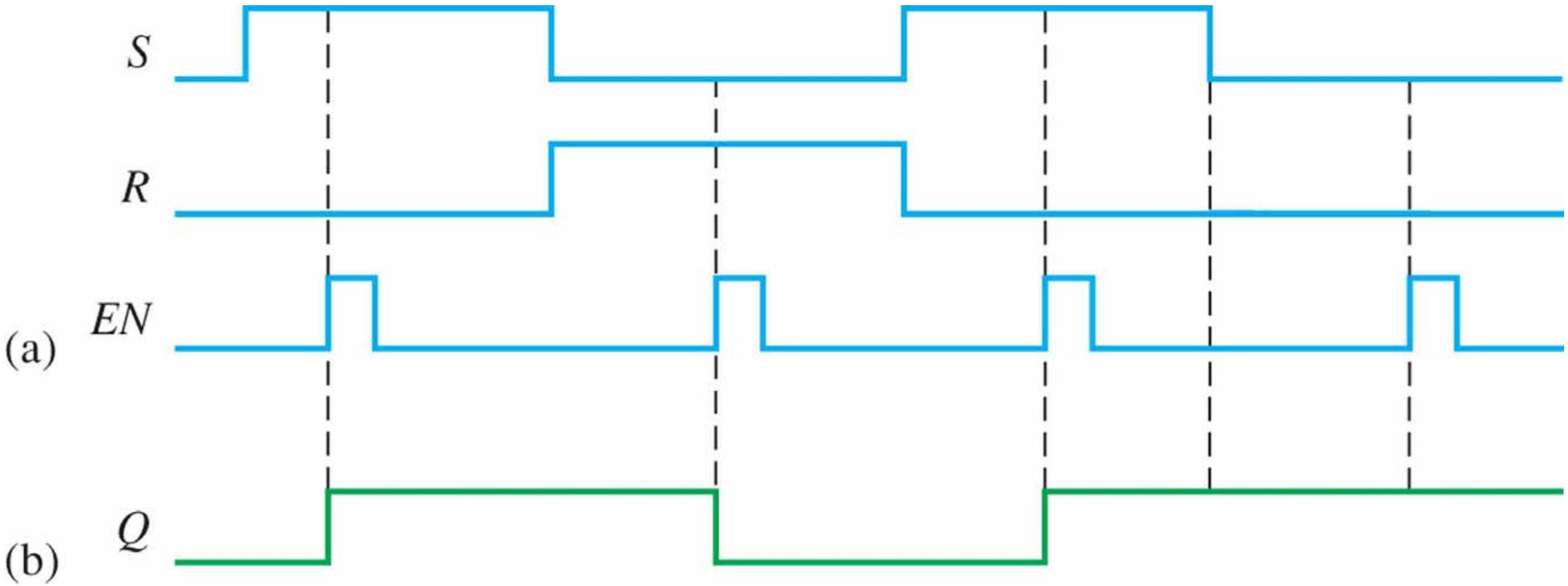
(a) Logic diagram

(b) Logic symbol

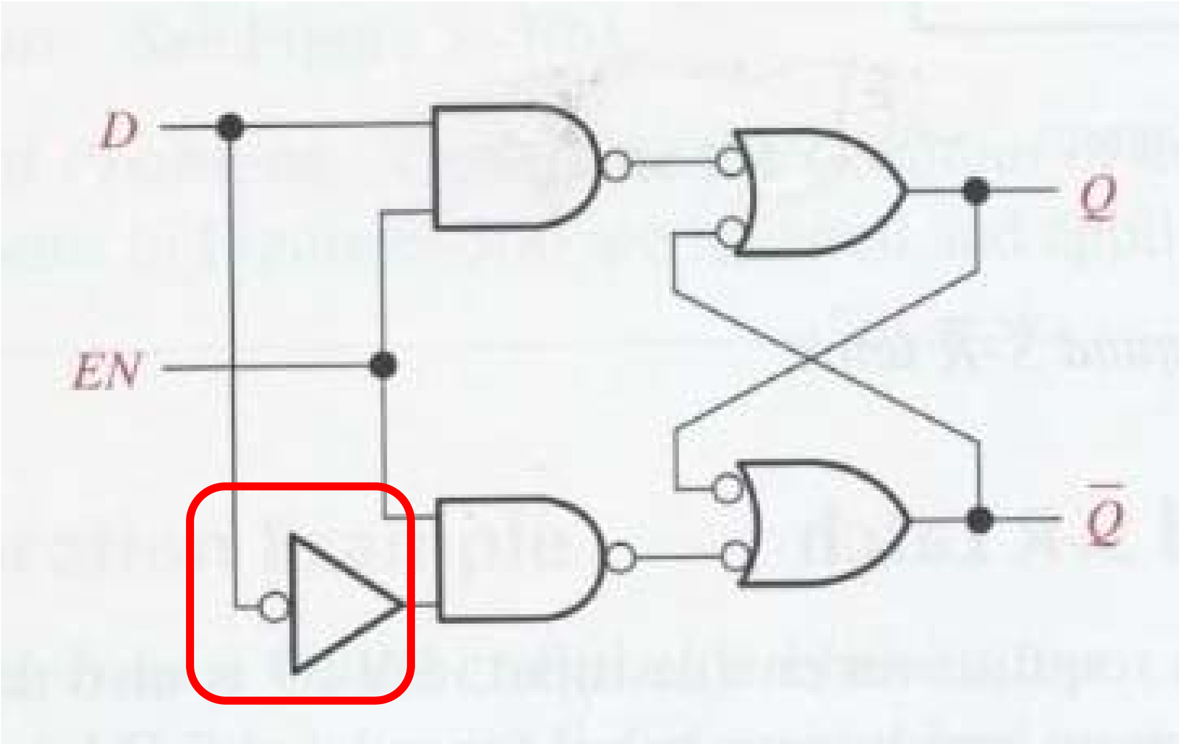
R	S	Q	$\overline{Q}$
0	0	Q_0	$\overline{Q_0}$
0	1	1	0
1	0	0	1
1	1	1^* ?	1^*

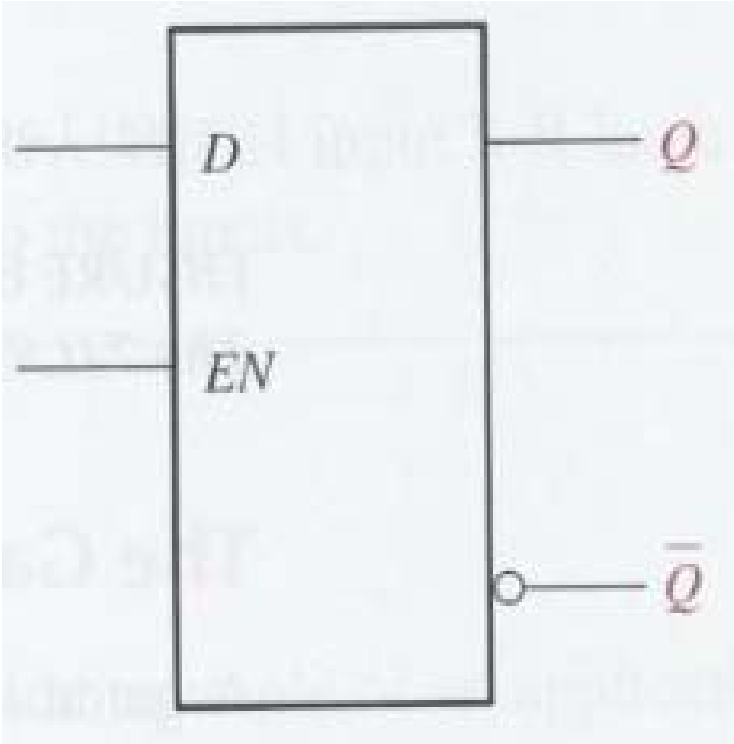
E	R	S	Q	$\overline{Q}$
0	X	X	Q_0	$\overline{Q_0}$
1	0	0	Q_0	$\overline{Q_0}$
1	0	1	1	0
1	1	0	0	1
1	1	1	1^* ?	1^*

Gated S-R Latch Waveform

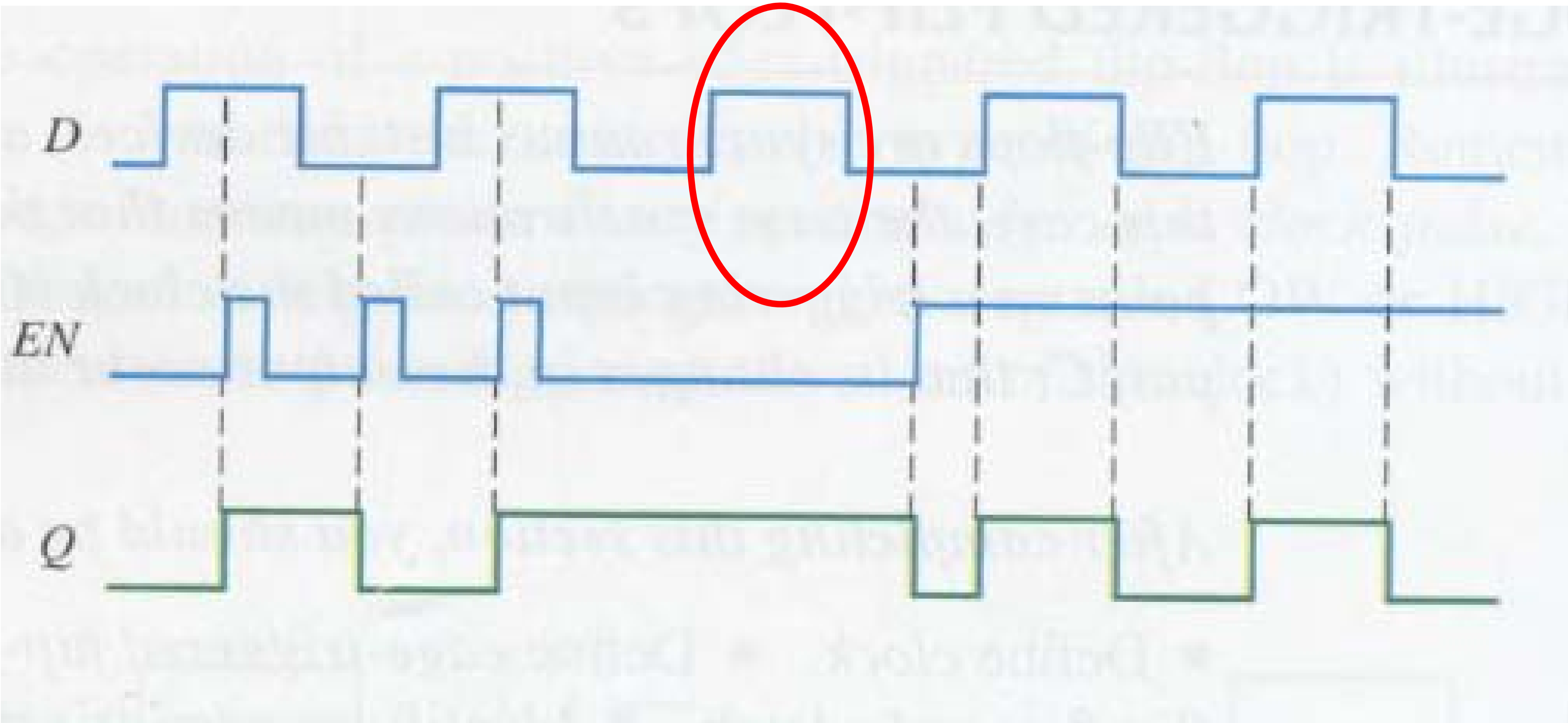


7.1.3 The Gated D Latch





Gated D Latch Waveform



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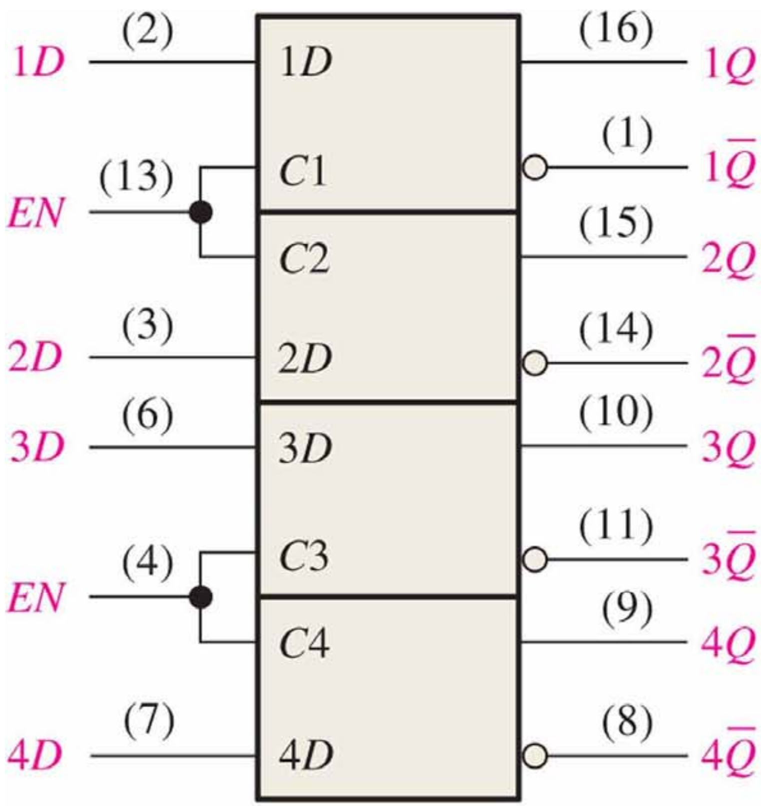


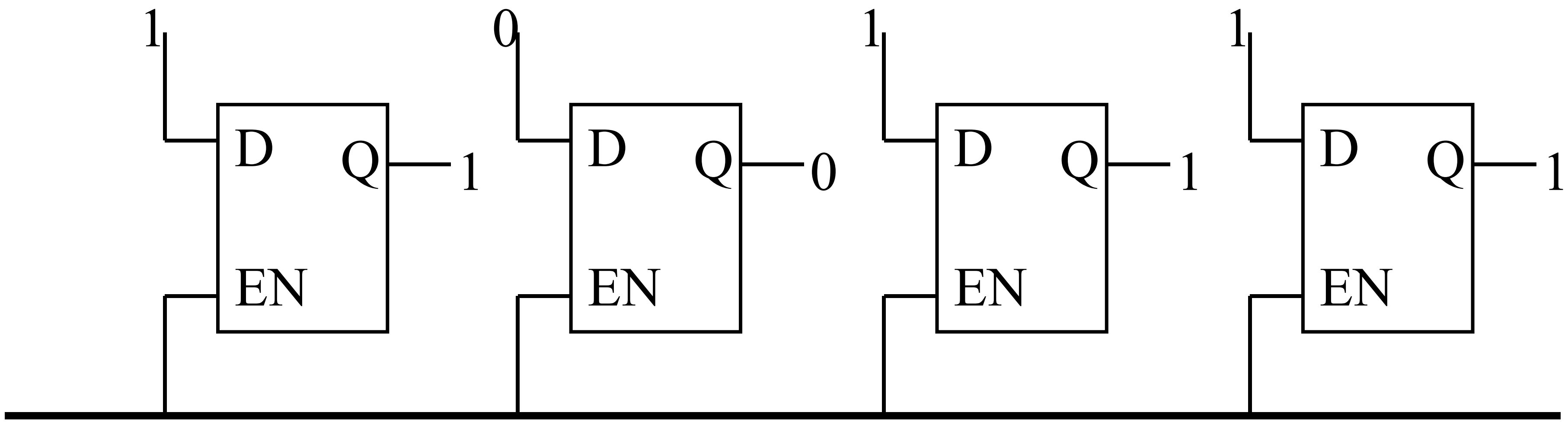
(a) Logic symbol

INPUTS		OUTPUTS		
D	EN	Q	$\overline{Q}$	COMMENTS
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\overline{Q}_0$	No change

Note: Q_0 is the prior output level before the indicated input conditions were established.

(b) Truth table (each latch)

Application example: Latches for temporary data storage



7.2 Edge-triggered Flip-Flops 边沿触发的触发器

- Flip-flops are ***synchronous bi-stable*** devices. The term ***synchronous*** means that the output changes state only at a specified point on a triggering input called the clock (CLK) is designated as a control input C. i.e., changes in the output occur in synchronous with the clock.

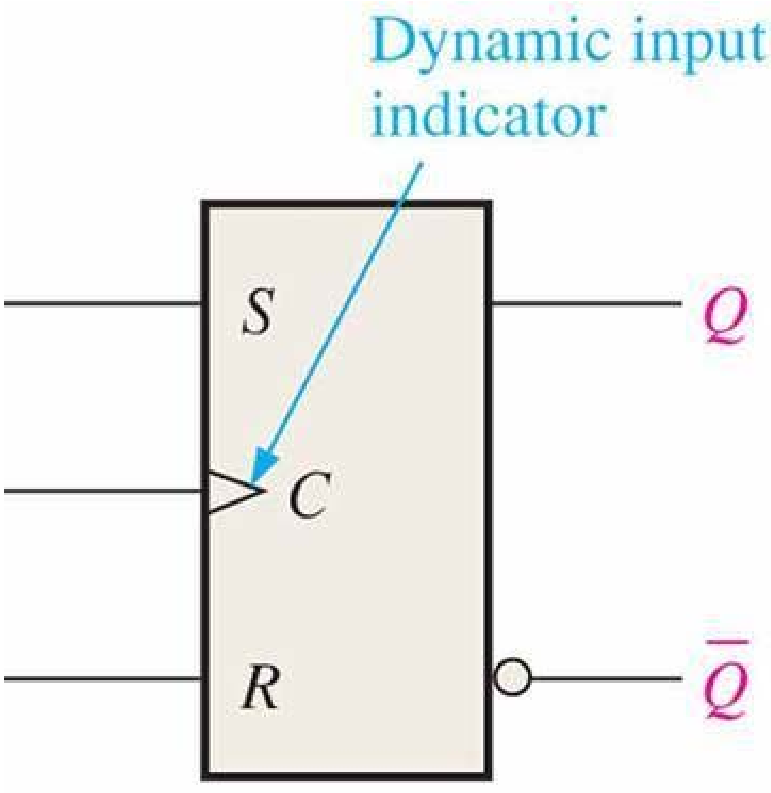
- An edge-triggered flip-flop changes state either at the ***positive edge*** (rising edge) or at the ***negative edge*** (falling edge) of the clock pulse and is sensitive to its input only at this transition of the clock.

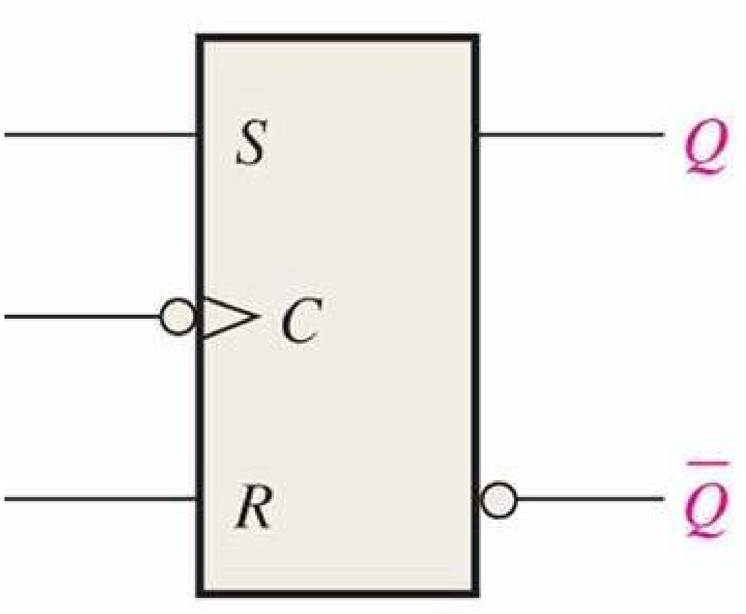
- ***Edge-triggered flip-flops*** (FF)
  - S-R flip-flop
  - J-K flip-flop
  - D flip-flop

7.2.1 The edge-triggered S-R FF

- The S and R inputs of the S-R flip-flop are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the ***triggering edge of the clock pulse***.
- When S is HIGH and R is LOW on the triggering edge of the clock pulse, Q is HIGH and the flip-flop is ***SET***. When S is LOW, R is HIGH, Q is LOW and flip-flop is ***RESET***. When S and R are both LOW, the output does not change from its prior state. When S and R are both HIGH, it is an invalid condition.

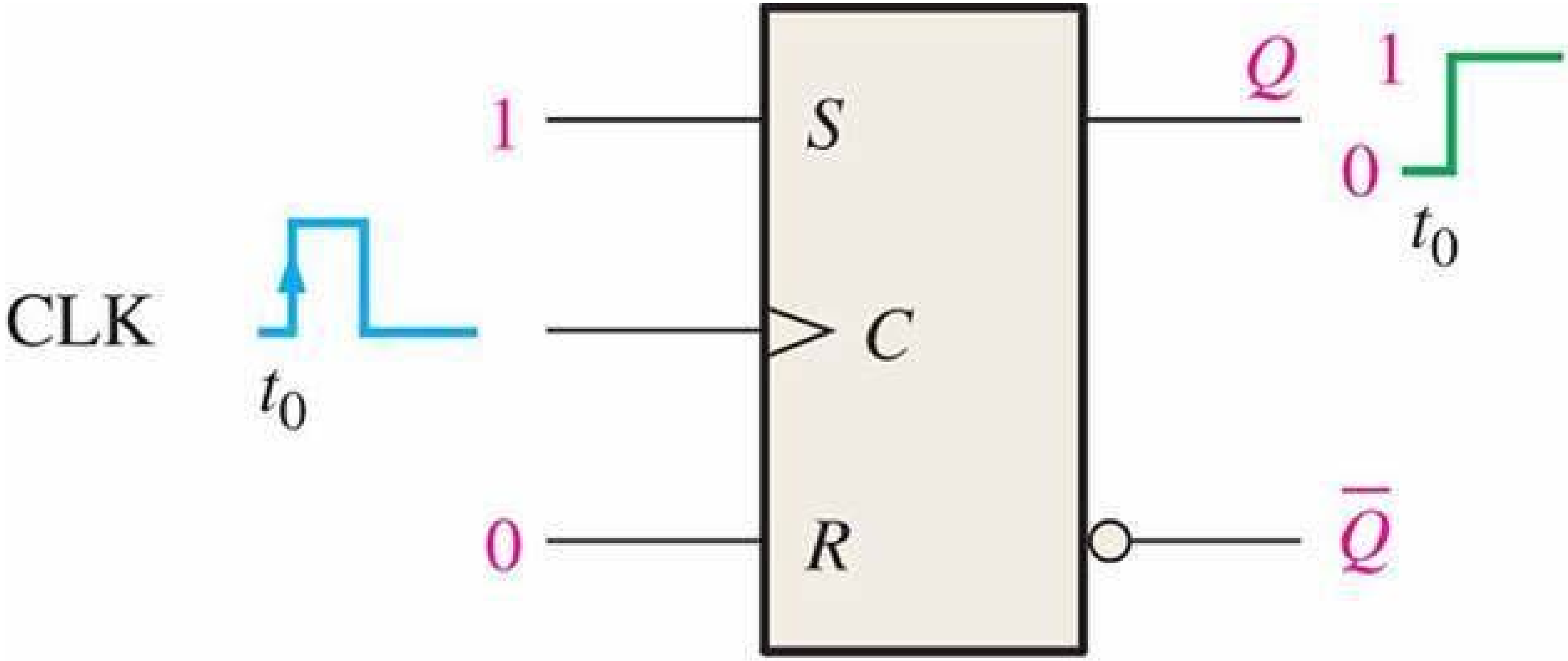
The edge-triggered S-R FF



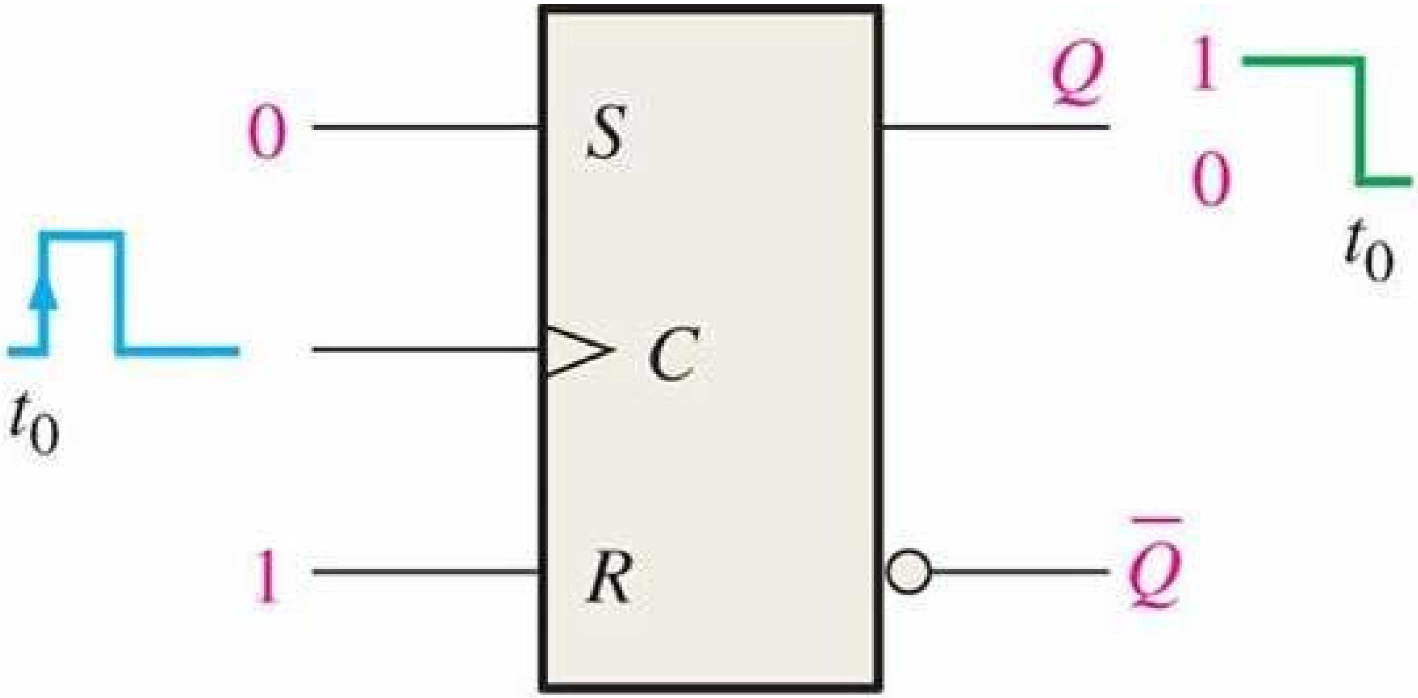


Truth Table of S-R FF

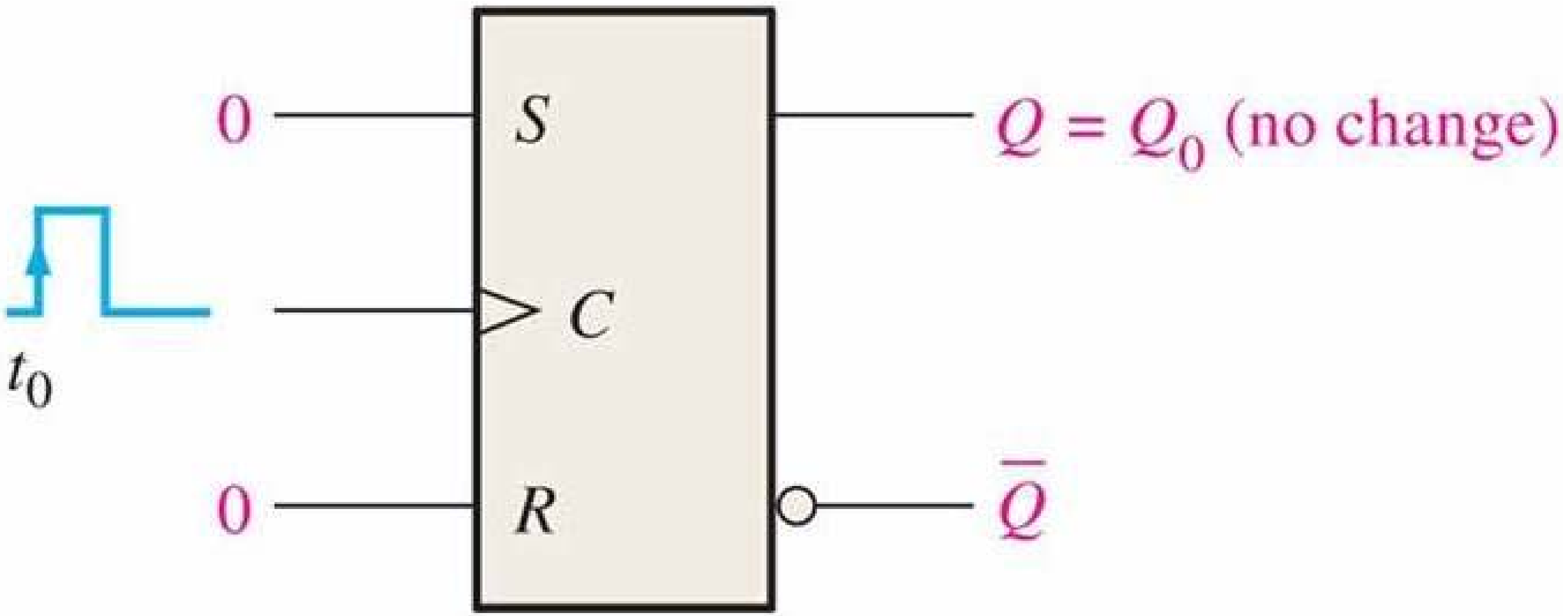
Inputs			Outputs		
S	R	CLK	Q	$\overline{Q}$	Comments
0	0	X	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid



(a) $S = 1$, $R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $S = 0$, $R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $S = 0$, $R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

Example

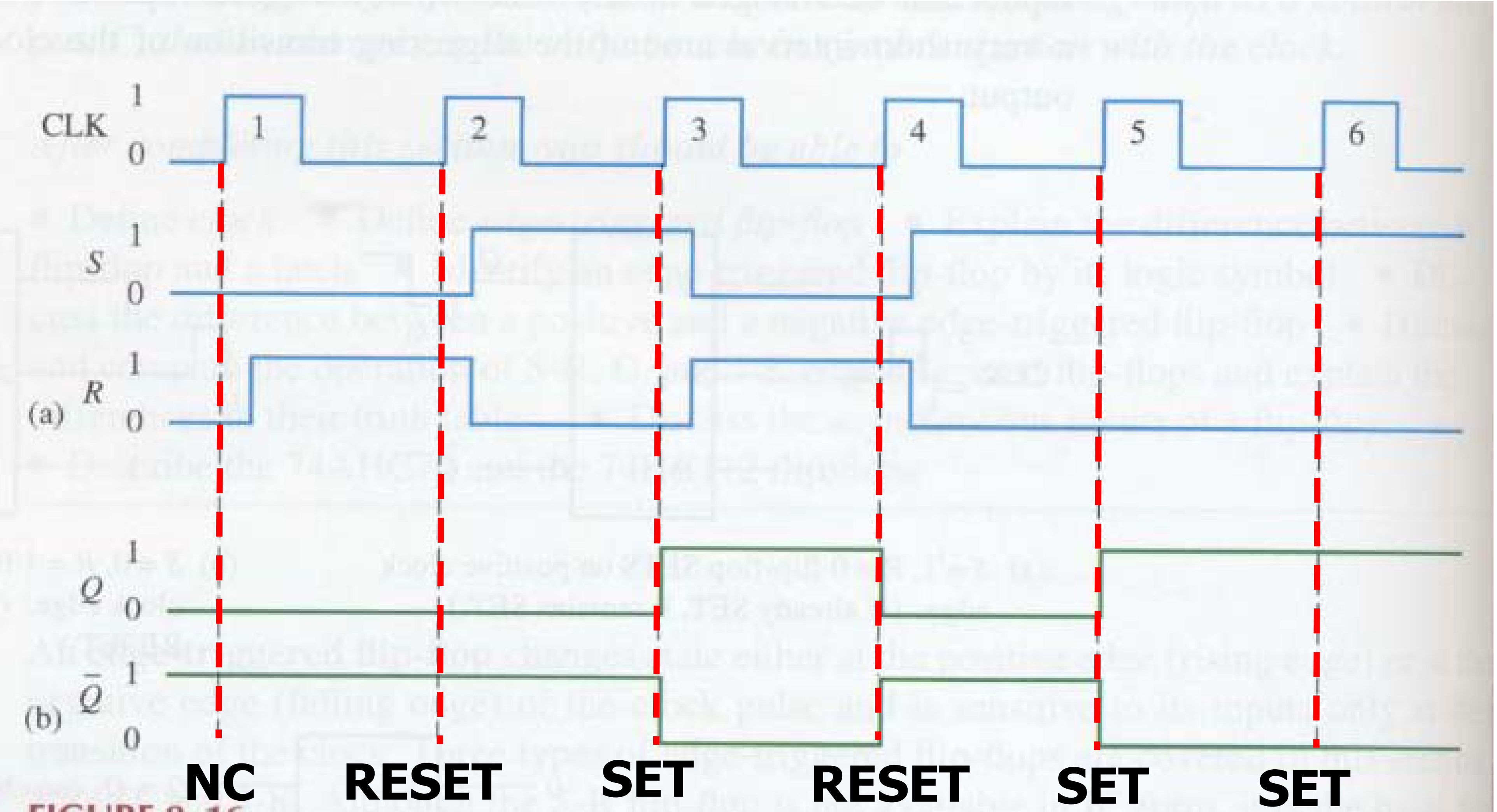
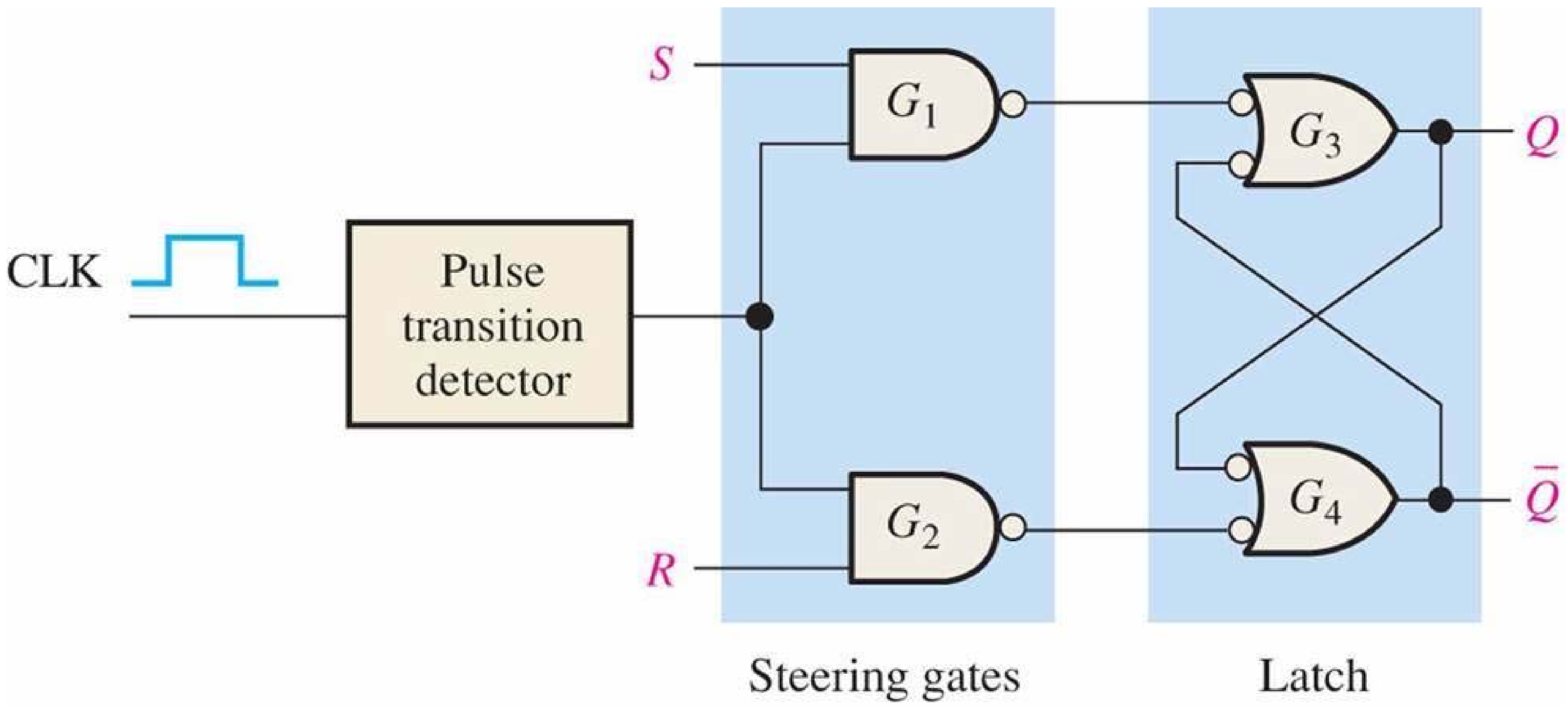


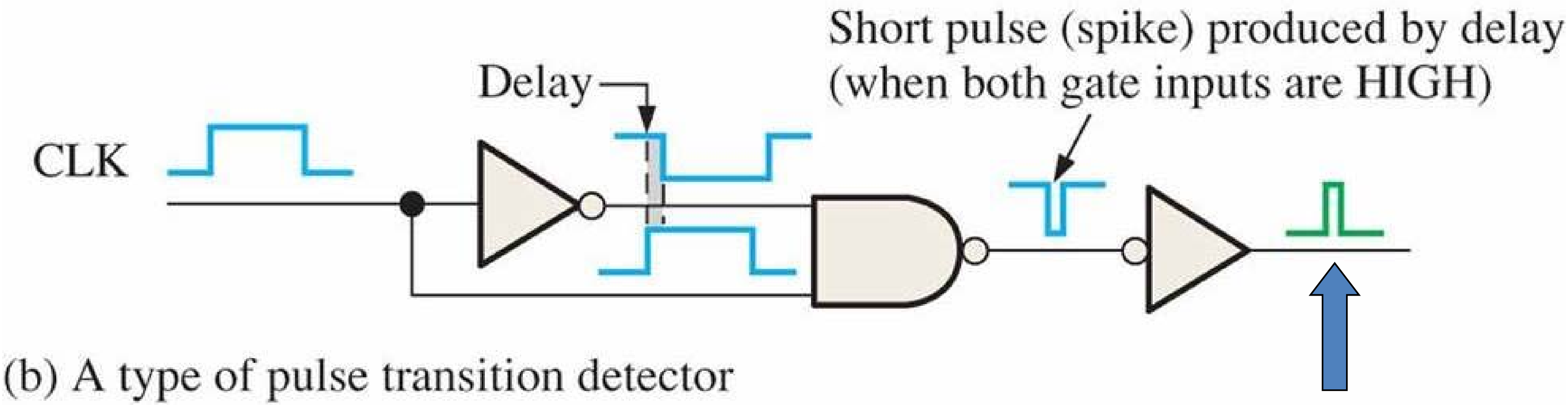
FIGURE 8–16

A method of Edge-triggering



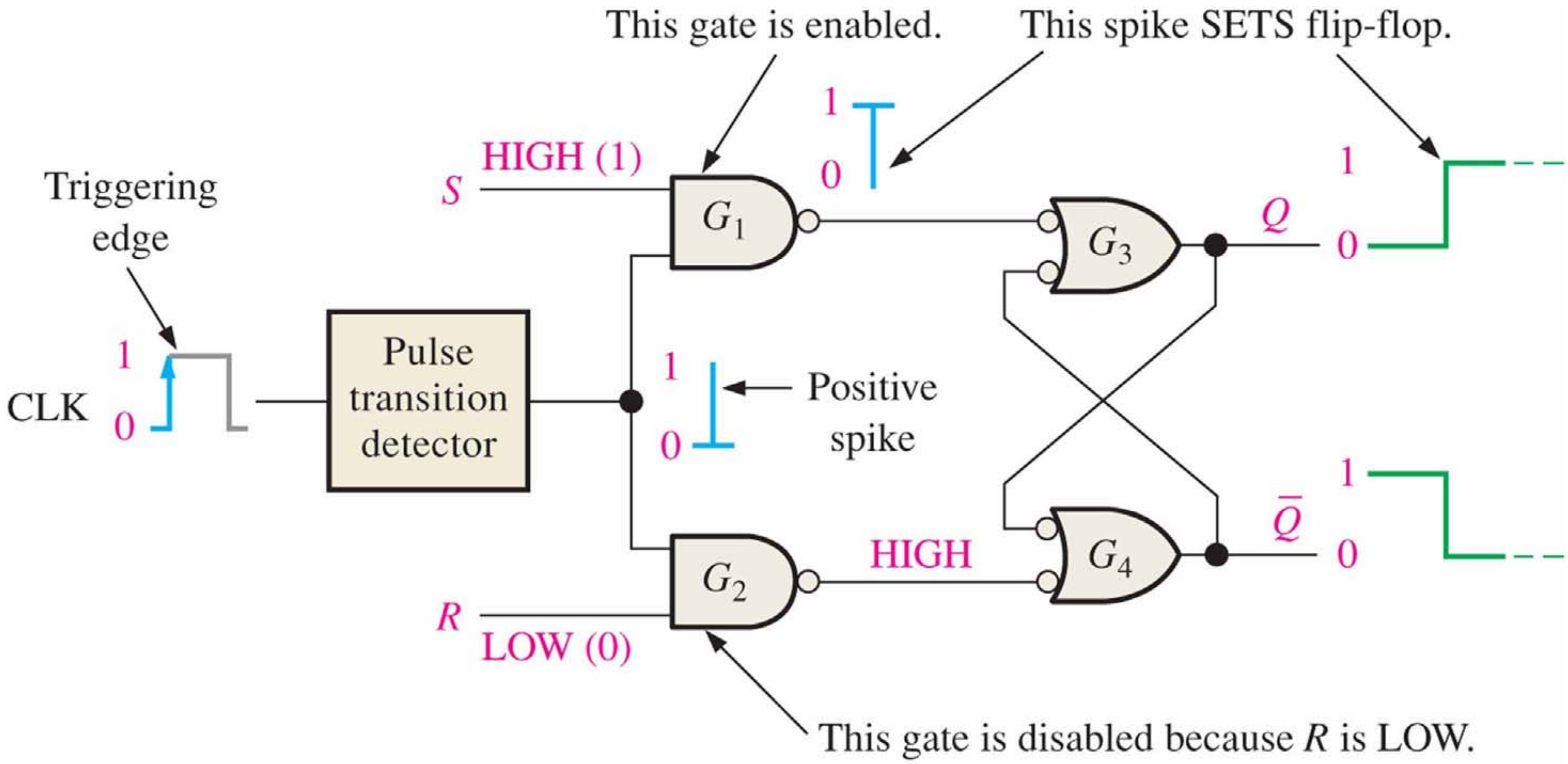
(a) A simplified logic diagram for a positive edge-triggered S-R flip-flop

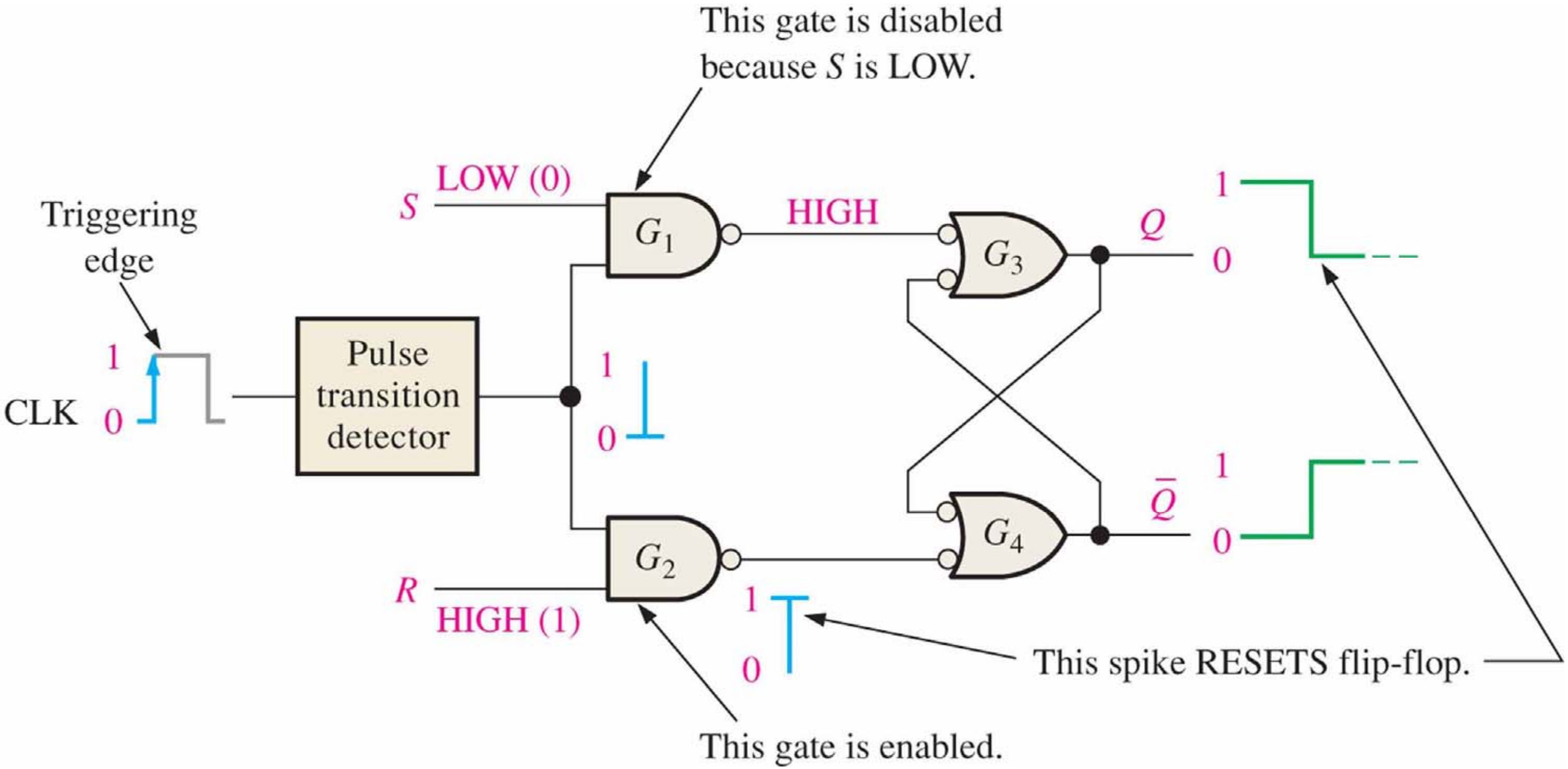
Pulse transition detector
脉冲变换检测器



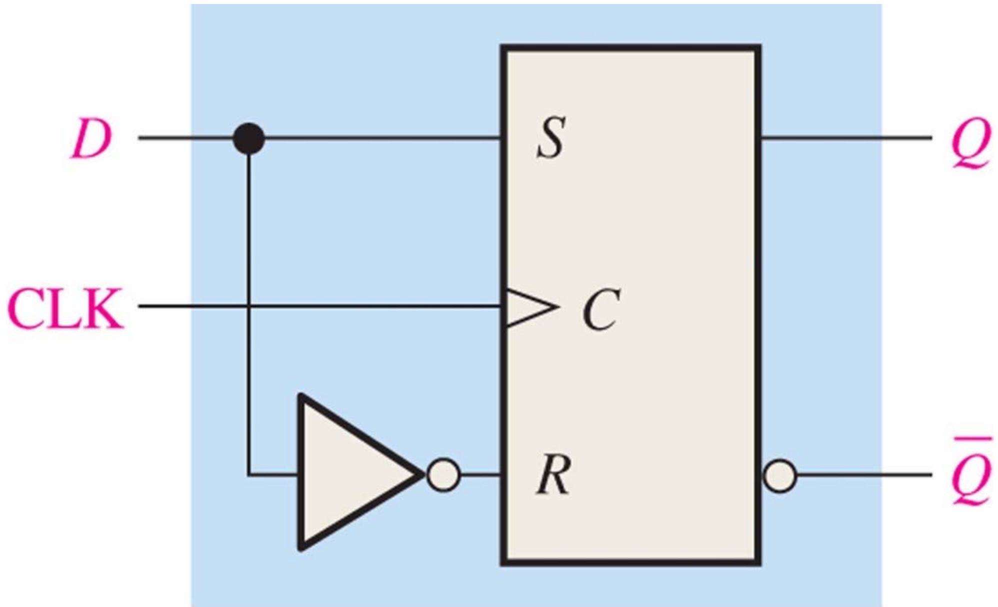
(b) A type of pulse transition detector

Narrow spike


This gate is enabled.
This spike SETS flip-flop.
Triggering edge
HIGH (1)
S
1
0
CLK
Pulse transition detector
Positive spike
G_1
G_2
G_3
G_4
HIGH
Q
$\overline{Q}$
R
LOW (0)
This gate is disabled because R is LOW.


This gate is disabled
because S is LOW.
S
LOW (0)
Triggering
edge
1
CLK
0
Pulse
transition
detector
1
0
HIGH
Q
1
0
1
0
Q̄
1
0
R
HIGH (1)
1
0
This spike RESETS flip-flop.
This gate is enabled.

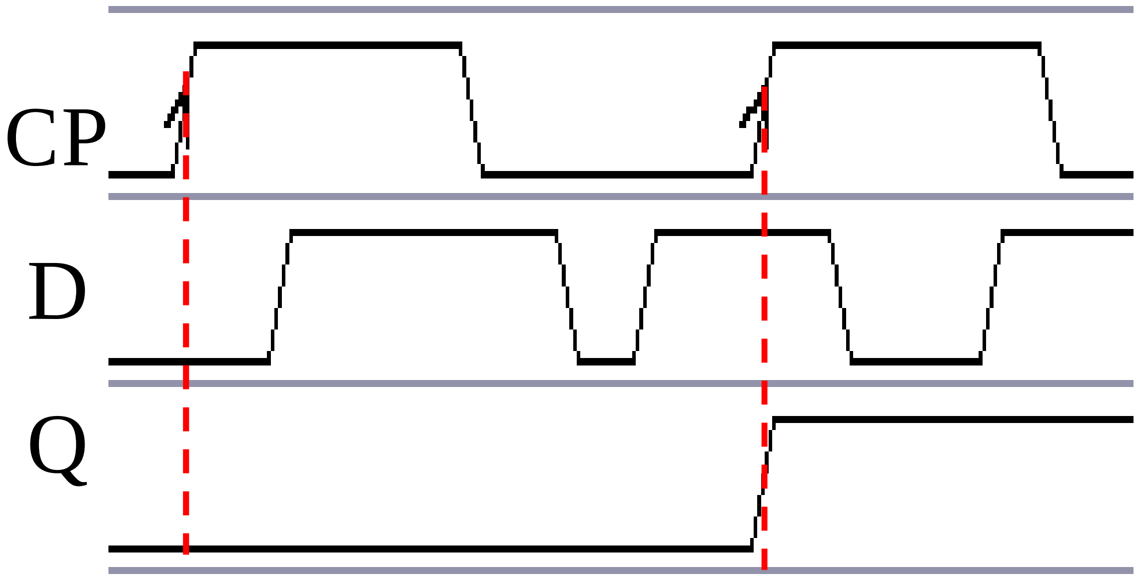
7.2.2 The Edge-Triggered D FF



Positive edge-triggered D flip-flop

The Q output of a D assumes the state of the D input on the triggering edge of the clock

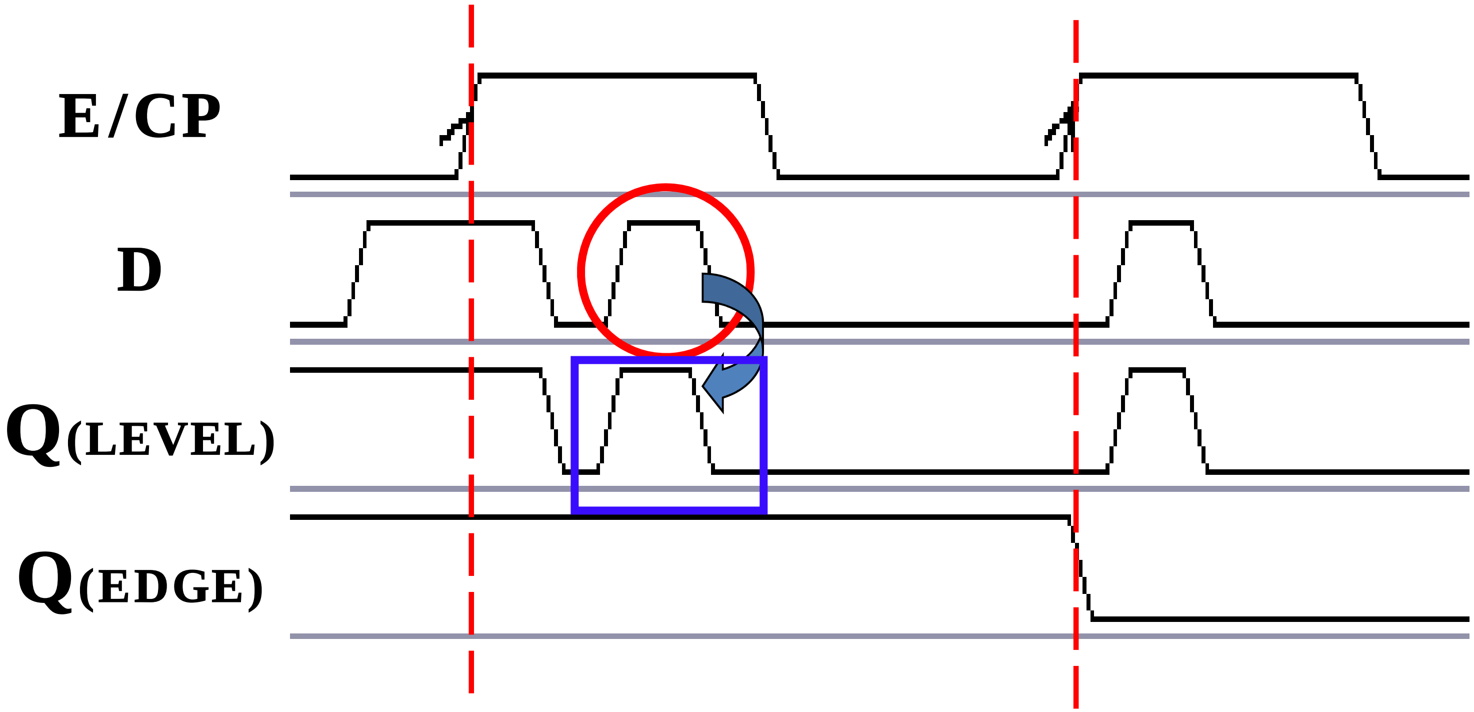
Timing diagram



Truth Table

CP	D	Q	$\overline{Q}$
↑	D	D	$\overline{D}$

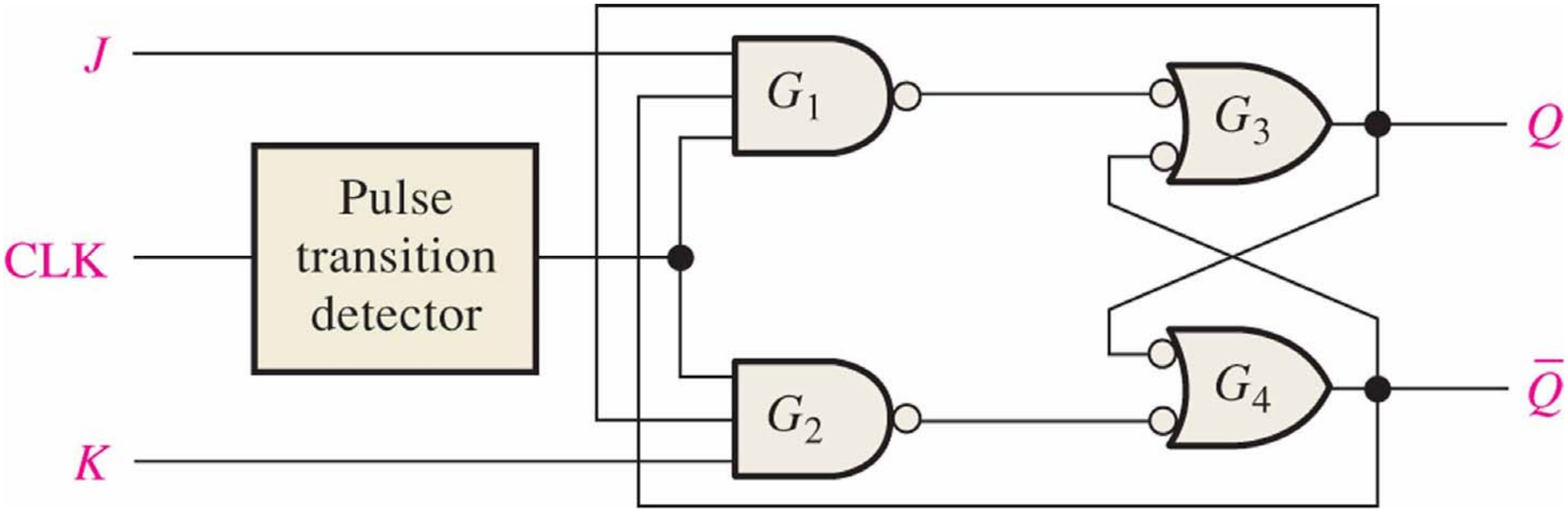
Comparison of edge-triggered and level-triggered



7.2.3 The Edge-Triggered J-K FF

****No invalid states.**

The two Set/Reset signals are labeled as J and K in honor of Jack Kilby.

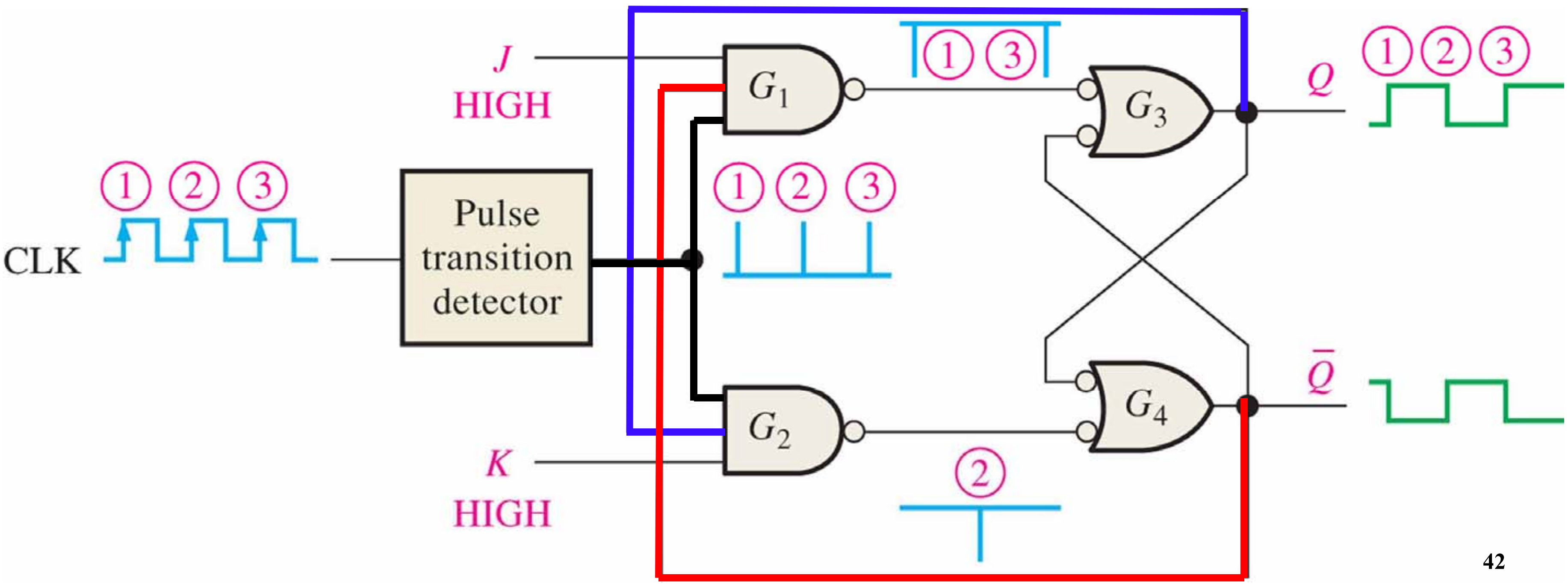


①IF $J=1, K=0, Q_0=0$; THEN G_1 enabled, $Q=1$ (SET)

②IF $J=0, K=1, Q_0=1$; THEN G_2 enabled, $Q=0$ (RESET)

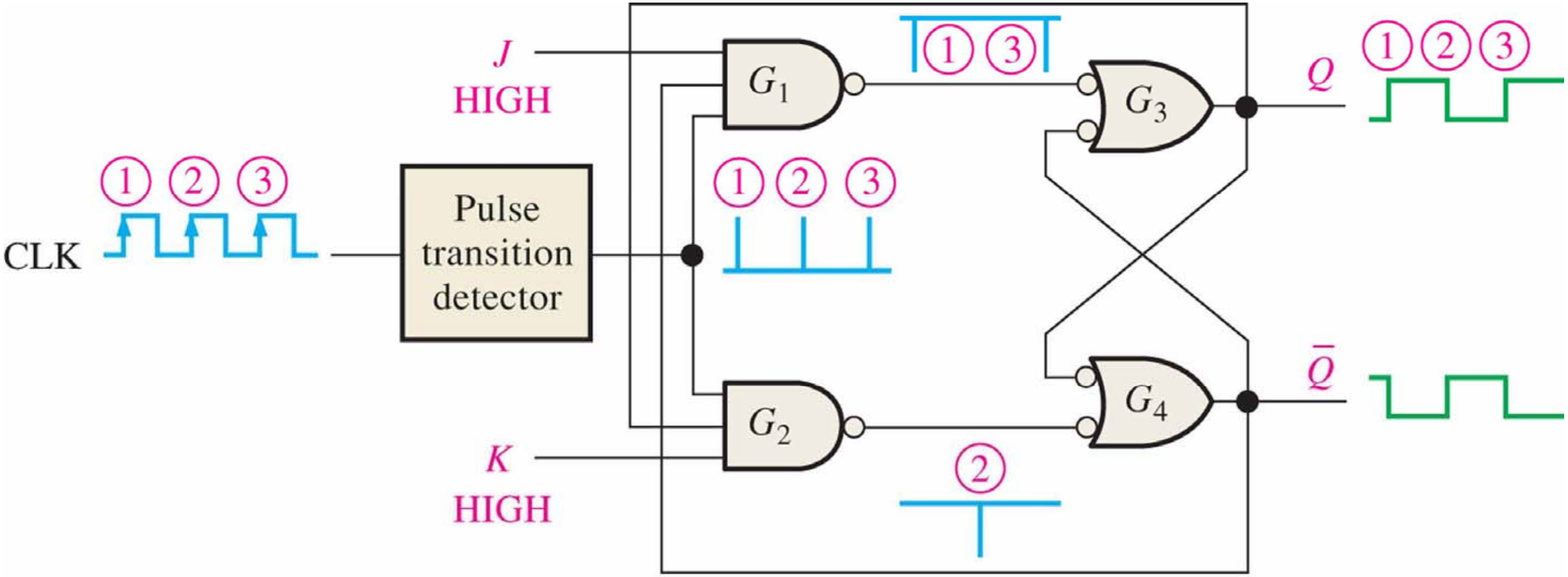
③IF $J=0, K=0$; THEN no change

④IF $J=1, K=1$; THEN change to opposite state(*Toggle*)

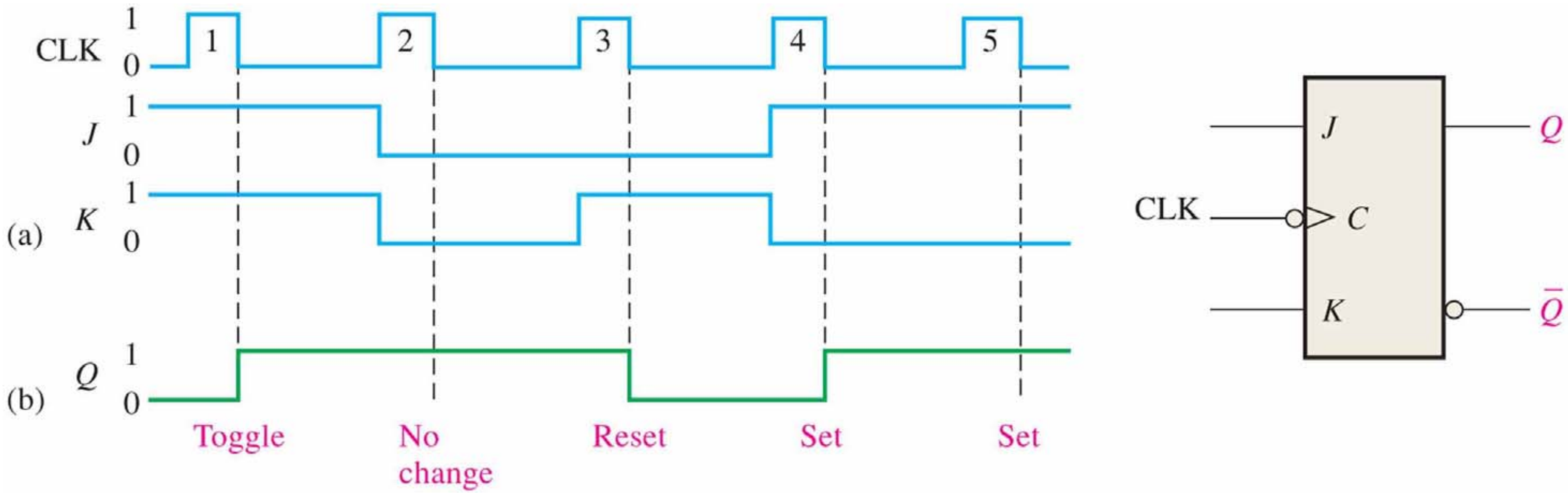


The Edge-Triggered Toggle FF

Toggle operation when J=K=1



Timing diagram



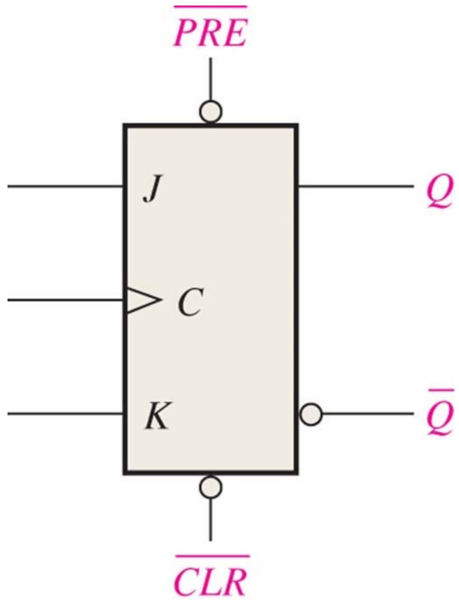
Truth Table

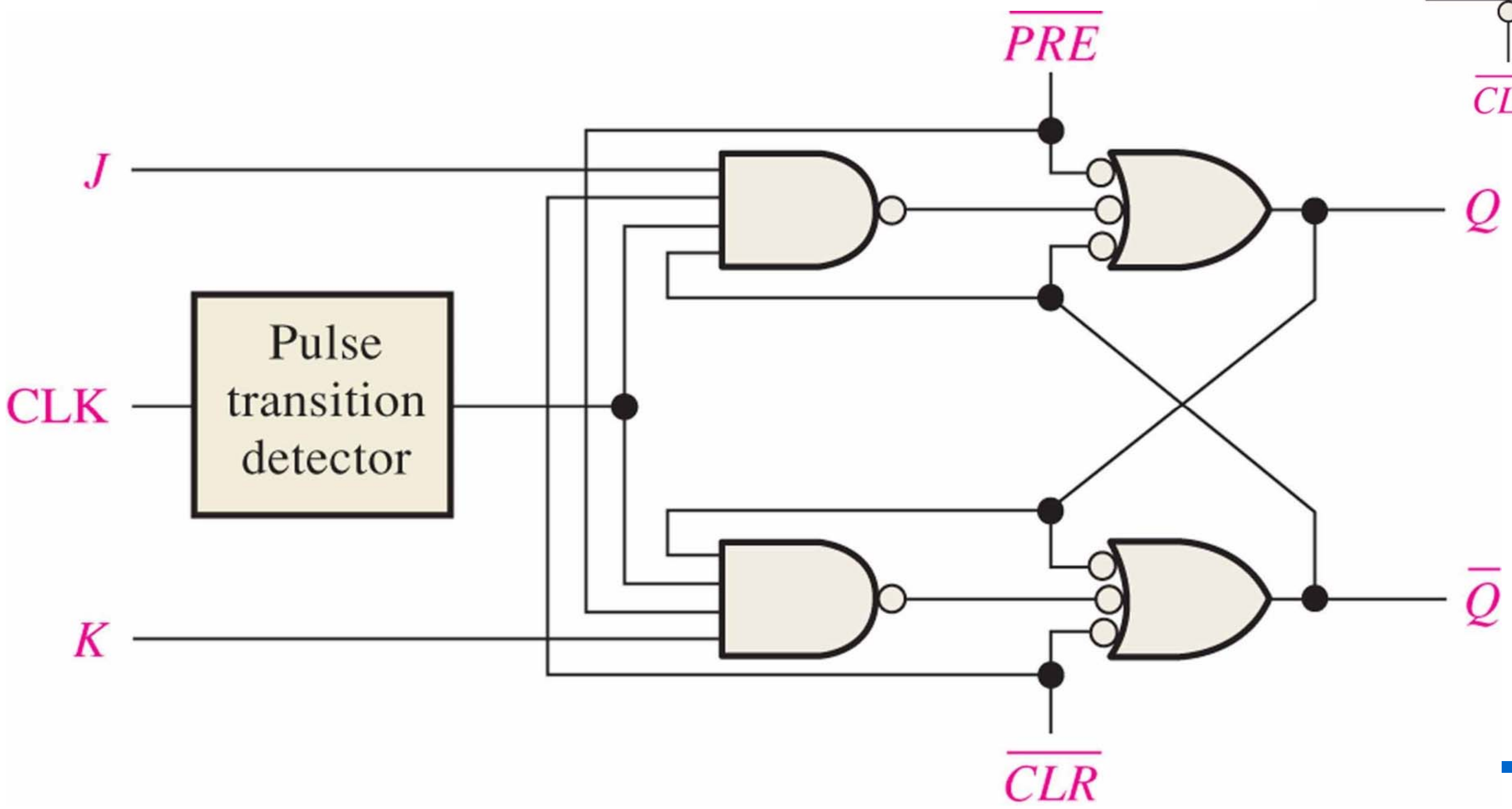
Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

7.2.4.Asynchronous Preset and Clear Inputs（异步置位和复位）

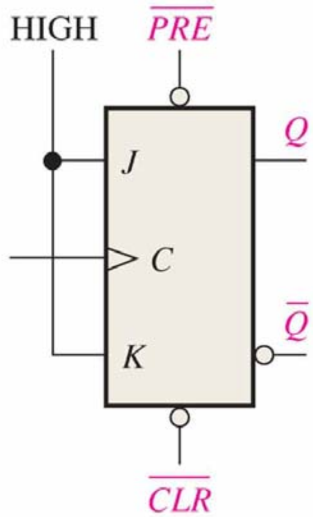
- Asynchronous inputs are independent of the clock. Usually labeled ***preset*** (***PRE***) and ***clear*** (***CLR***), or ***direct set (SD) and direct reset (RD).***
- An active level on the preset input will set the flip-flop, and an active level on the clear input will reset the flip-flop.

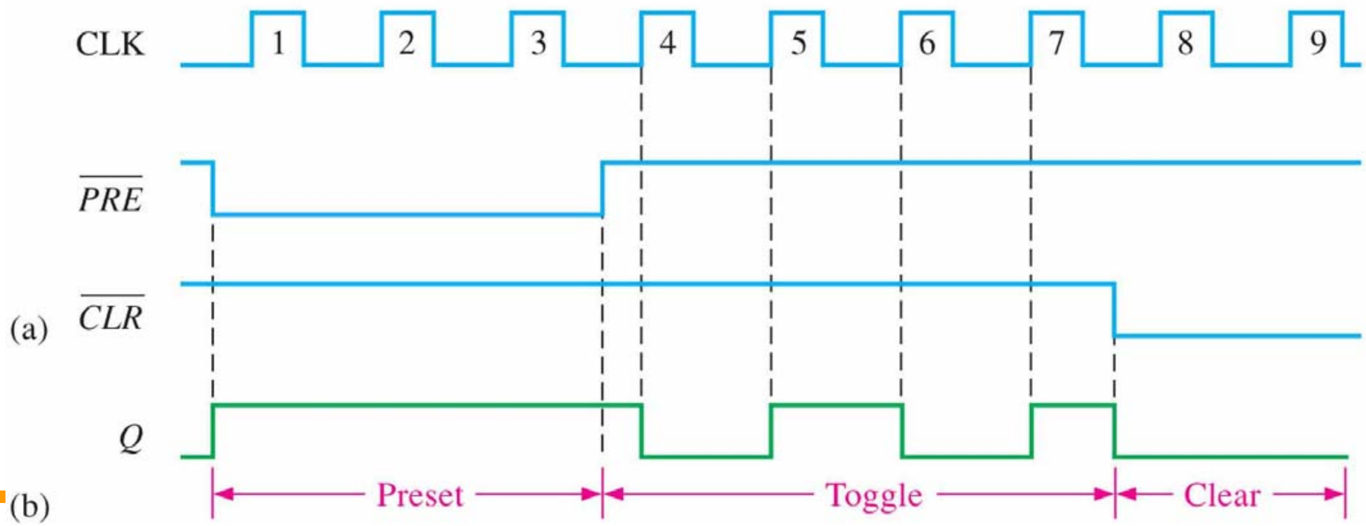
J-K FF with active-LOW preset and clear inputs



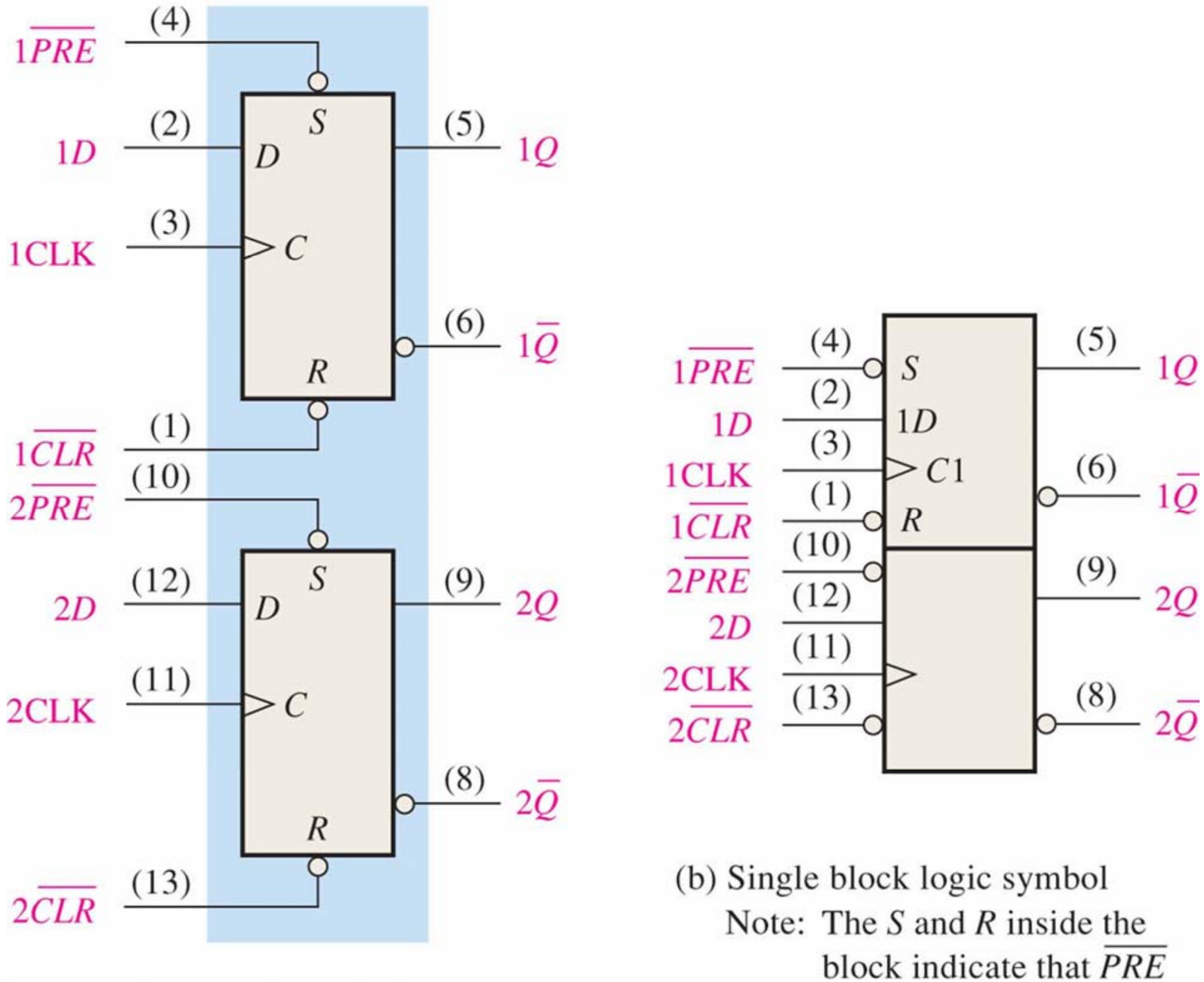


J-K FF with active-LOW preset and clear inputs





74AHC74 (dual D FF)

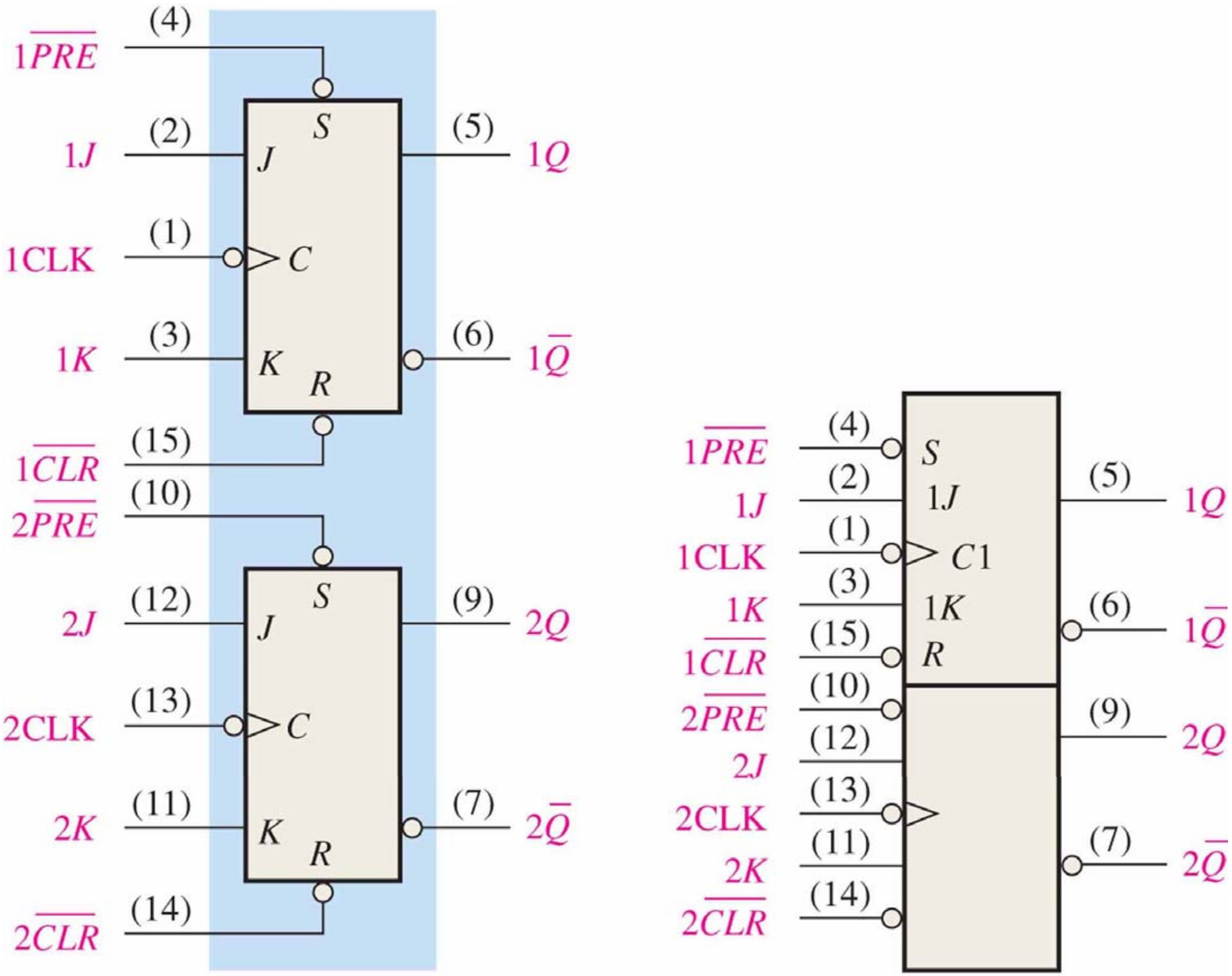


(a) Individual logic symbols

(b) Single block logic symbol

Note: The S and R inside the block indicate that $\overline{PRE}$ SETS and $\overline{CLR}$ RESETS.

74HC112 (dual JK FF)

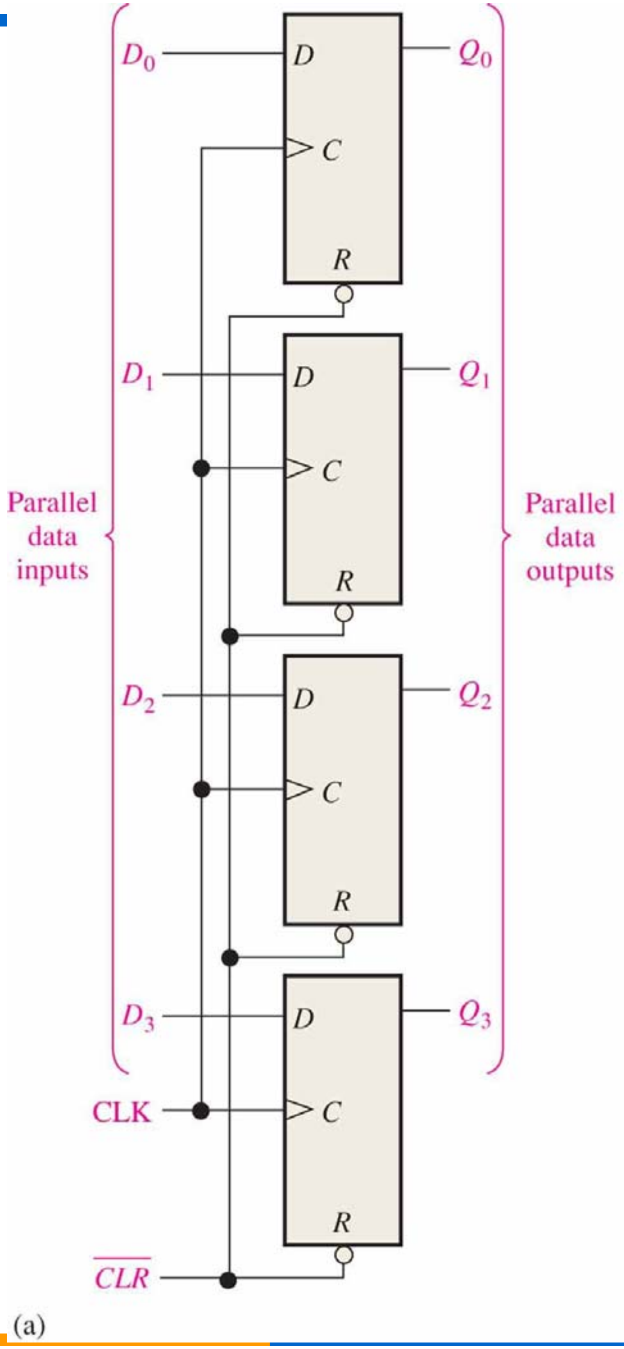


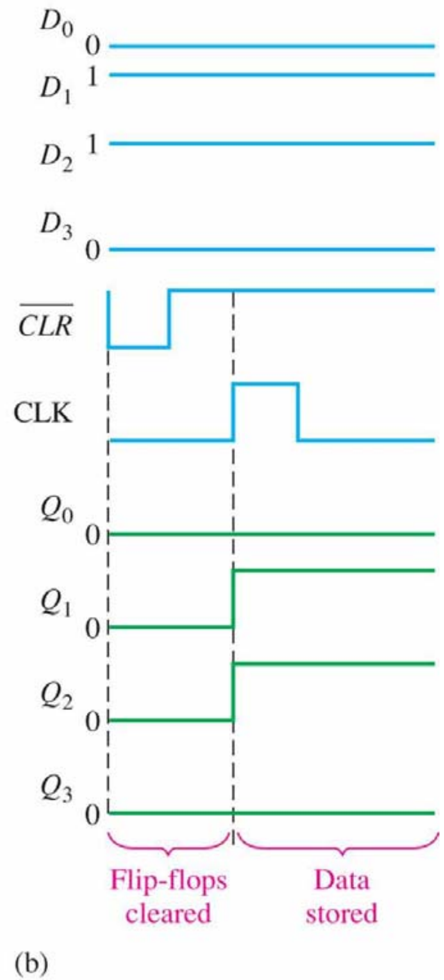
(a) Individual logic symbols (b) Single block logic symbol

7.3 Flip-Flop Applications

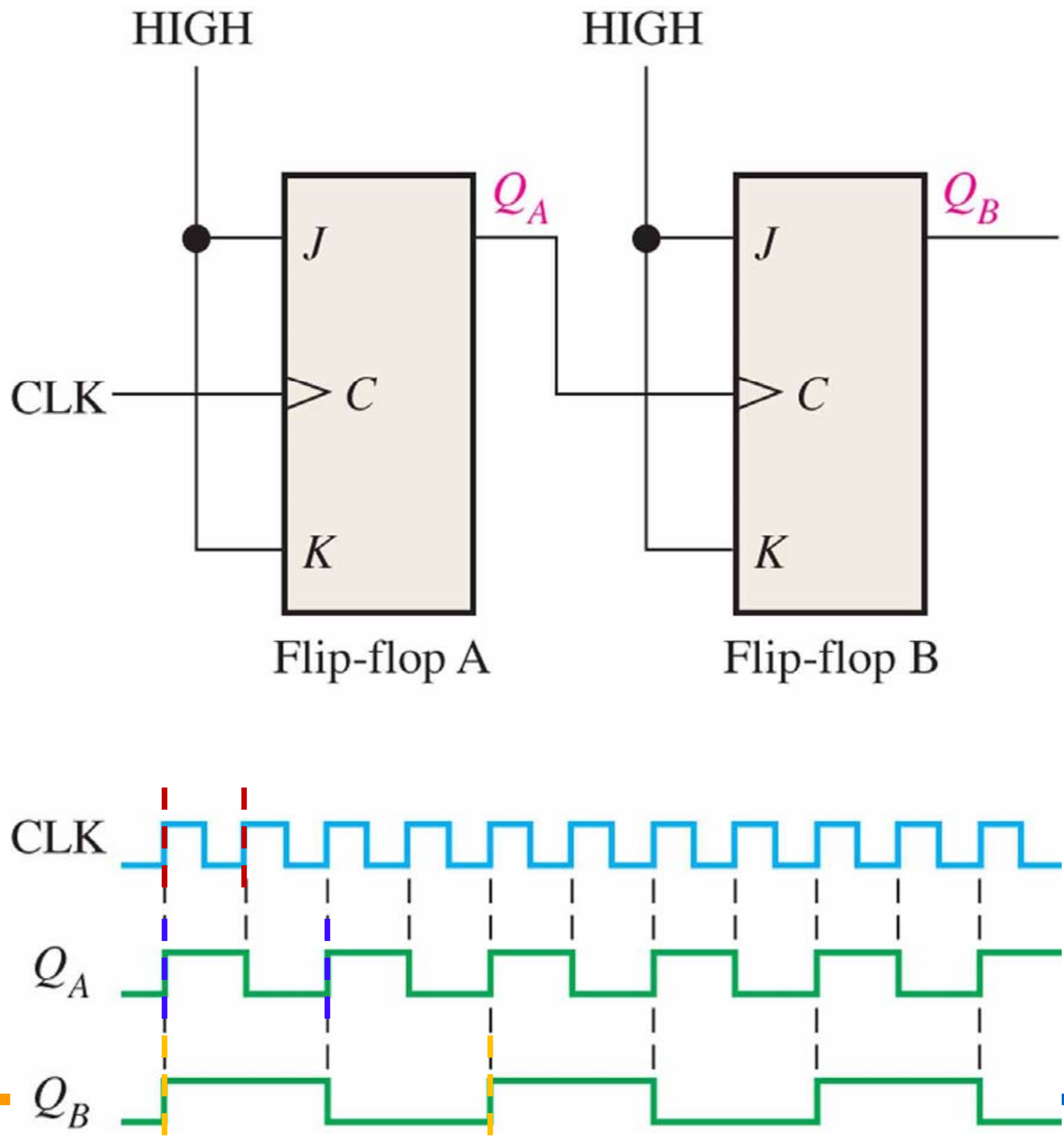
- Parallel Data Storage (数据存储器)
- Frequency Division (分频器)
- Counter (计数器)

Application example: Basic register for parallel data storage

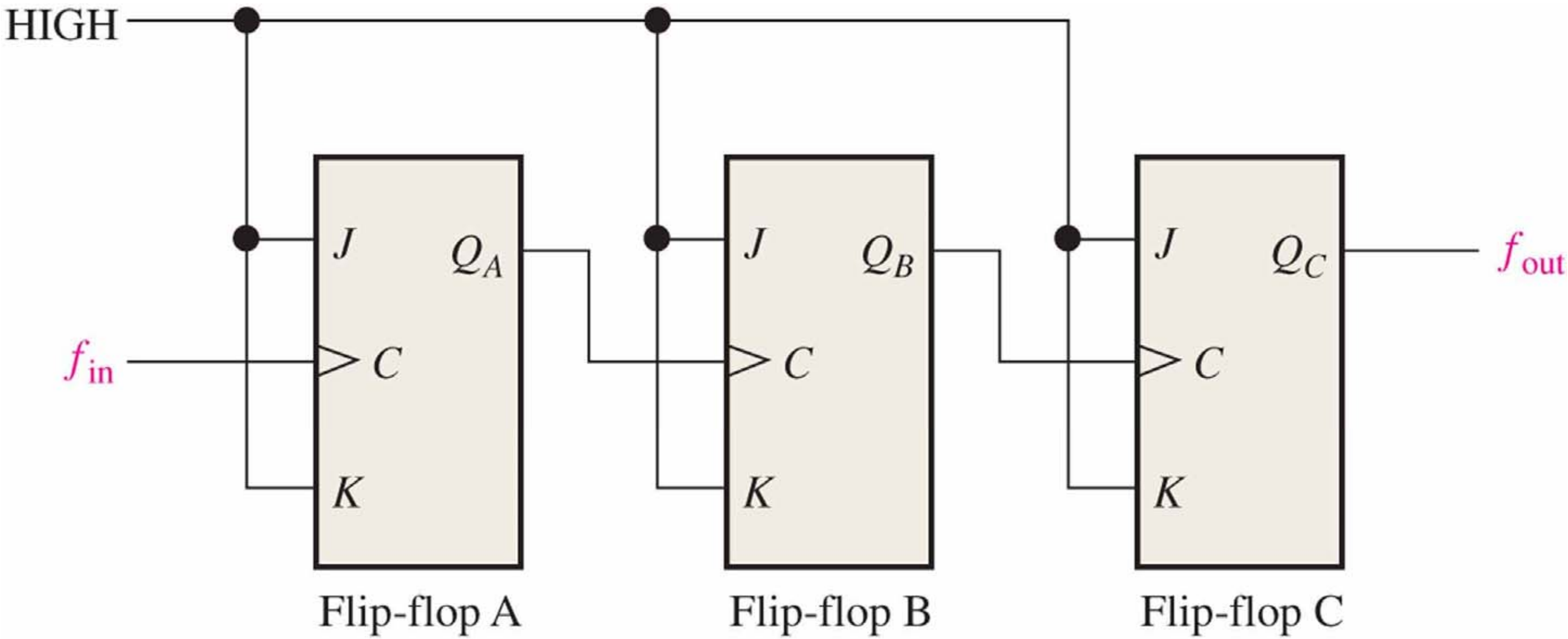


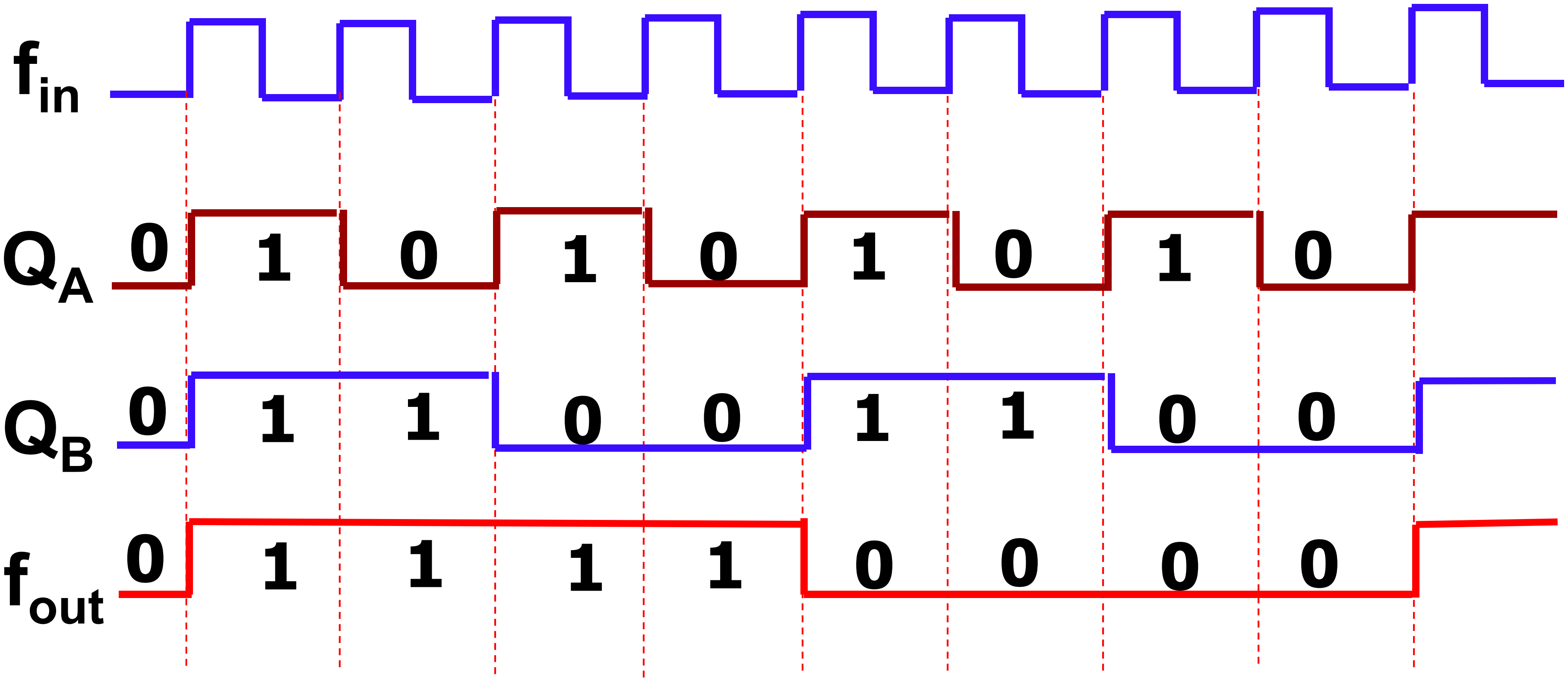


J-k FF as a devide-by-2 or 4 device



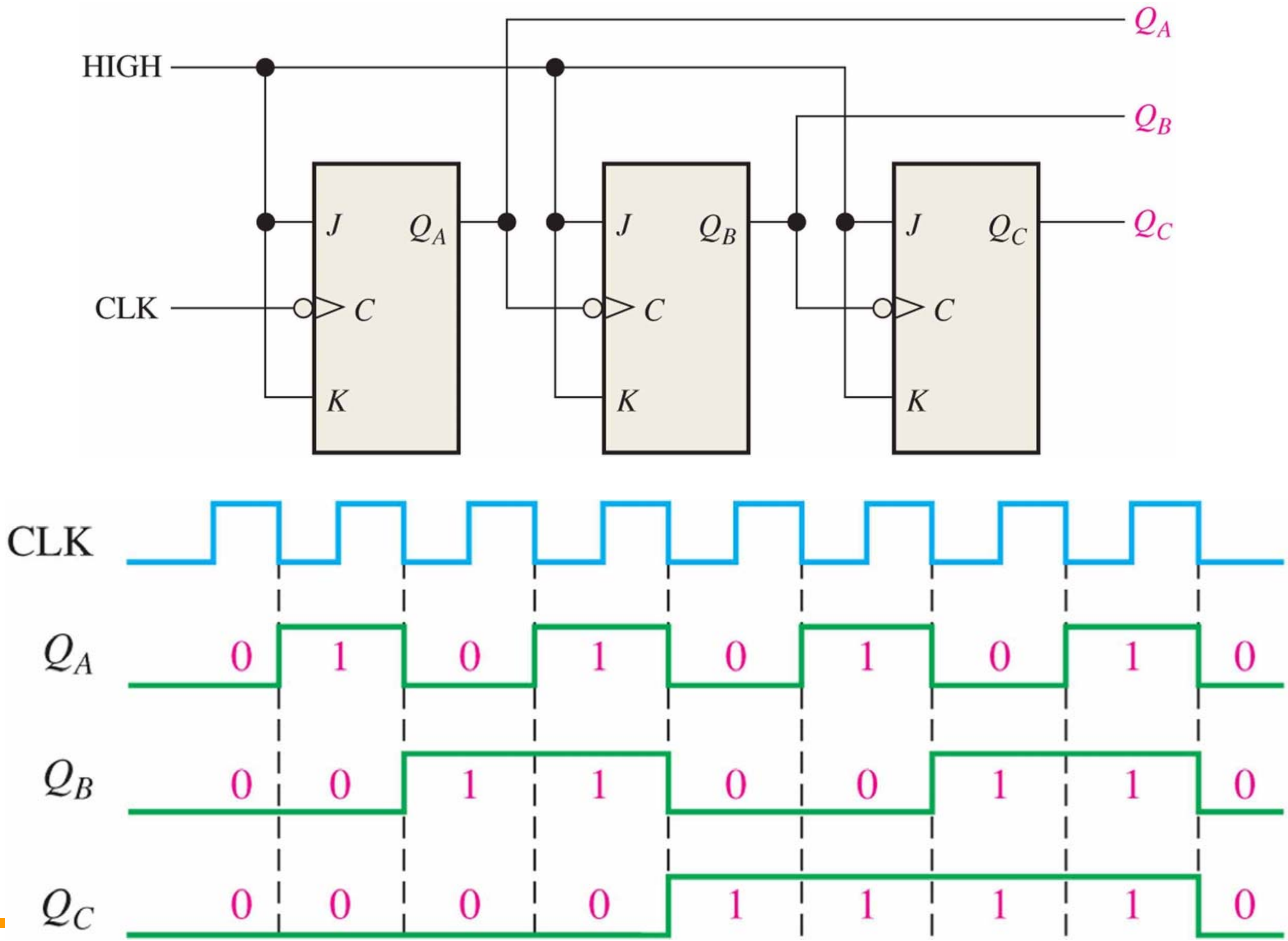
Exercise:


HIGH
f_{in}
J
Q_A
C
K
J
Q_B
C
K
J
Q_C
C
K
f_{out}
Flip-flop A
Flip-flop B
Flip-flop C



f_in
Q_A
0 1 0 1 0 1 0 1 0
Q_B
0 1 1 0 0 1 1 0 0
f_out
0 1 1 1 1 0 0 0 0

J-k FF as a counter



7.4 Flip-Flop Operating Characteristics

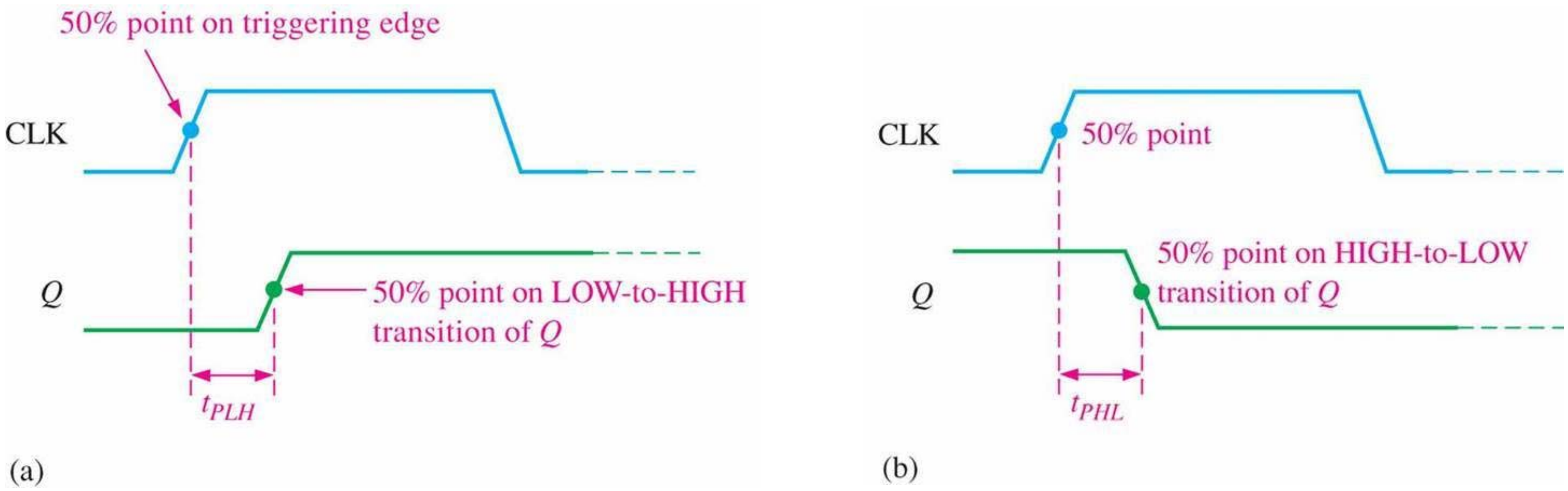
- Propagation delay time (传播时延)
- Set-up time (建立时间)
- Hold time (保持时间)
- Maximum of frequency (最大频率)
- Pulse width (脉冲宽度)
- Power dissipation (功耗)

Propagation Delay Time

The propagation delay time is the interval of time required after an input signal has been applied for the resulting output change to occur.

Propagation Delay Time for a flip-flop(I)

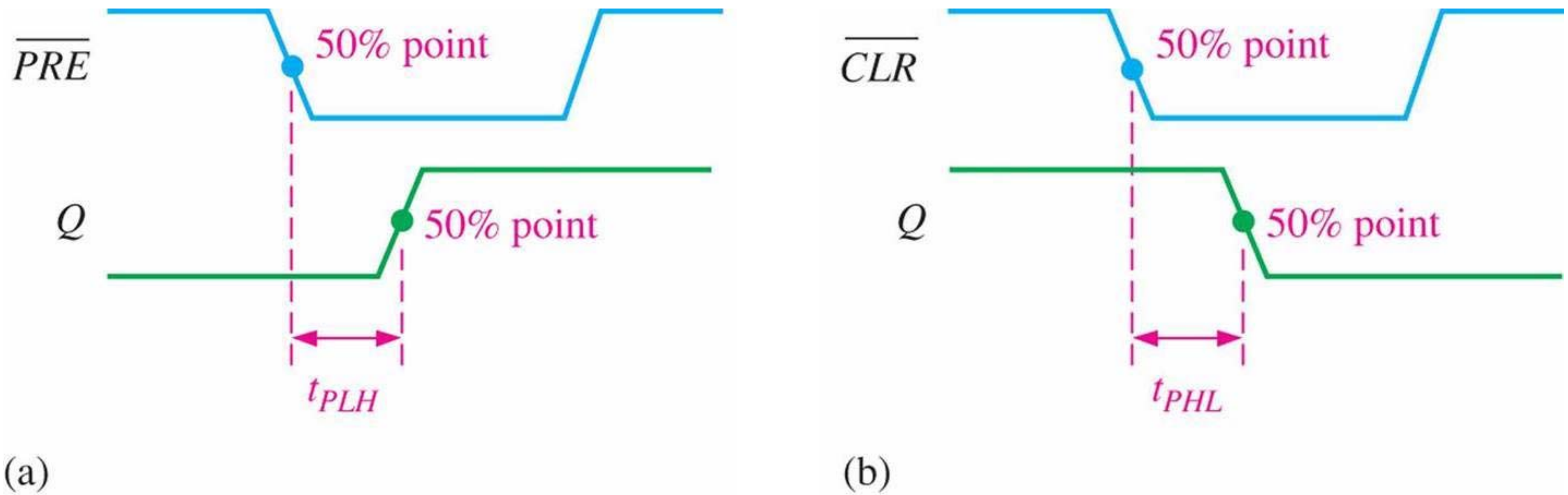
1. t_{PLH} : Measured from the triggering edge of the clock pulse to the LOW-to-HIGH transition of the output
2. t_{PHL} : Measured from the triggering edge of the clock pulse to the HIGH-to-LOW transition of the output.



Propagation Delay Time for a flip-flop(II)

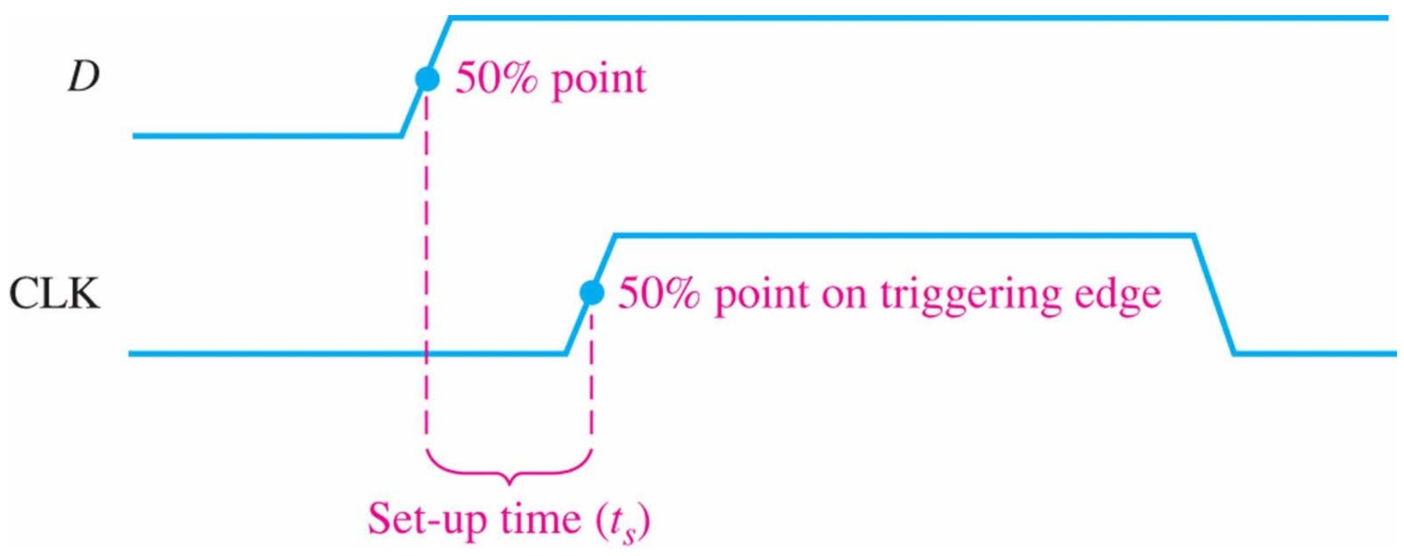
3. t_{PLH} : Measured from the leading edge of the preset input to the LOW-to-HIGH transition of the output

4. t_{PHL} : Measured from the leading edge of the clear input to the HIGH-to-LOW transition of the output.



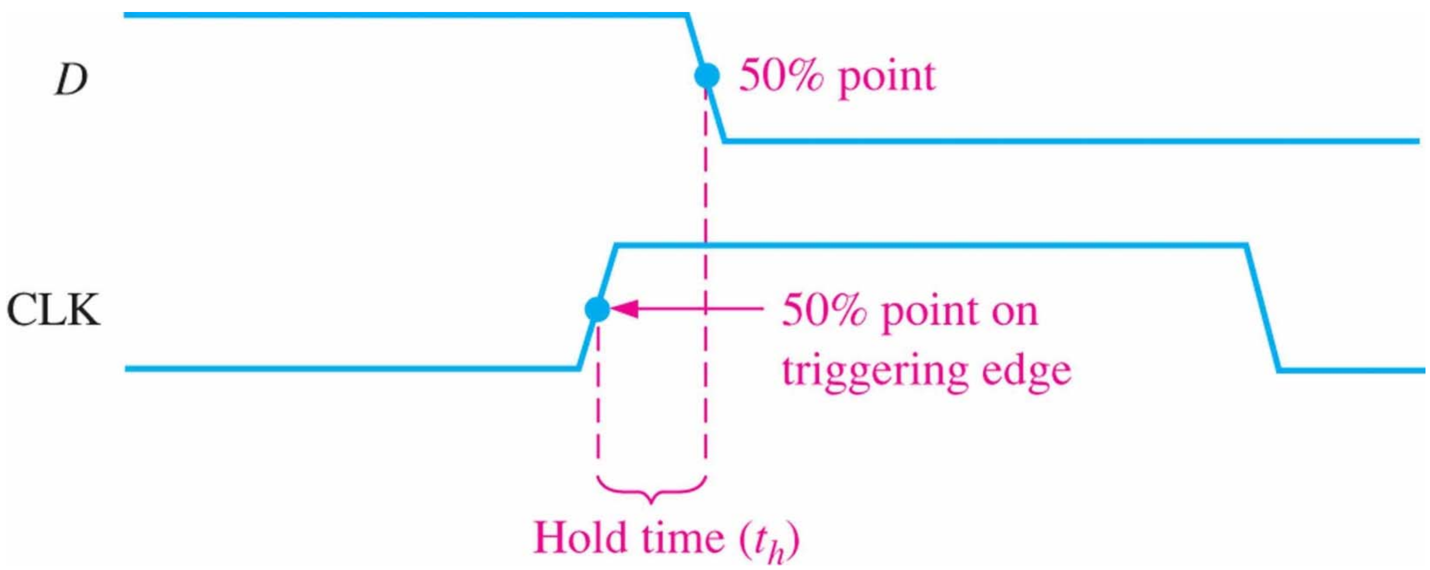
Set-up Time

The set-up time (t_s) is the minimum interval of time required for the logic levels to be maintained constantly on the inputs(J and K, or S and R, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop.



Hold Time

The Hold time (t_h) is the minimum interval of time required for the logic levels to remain constantly on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop.



Maximum Clock Frequency

The maximum clock frequency ($f_{\max}$) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough and its operation would be impaired.

Pulse Widths

The minimum pulse widths (t_w) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically the clock is specified by its minimum HIGH time and its minimum LOW time.

Power Dissipation

The power dissipation is the total power consumption of the device.

$$P = V_{cc} \times I_{cc} = 5V \times 5mA = 25mW$$

脉冲波形的产生和整形

- 整形电路：
  - 施密特触发器
  - 单稳态
- 脉冲波形的产生
  - 多谐振荡器
- 555定时器

7.5 Schimitt Trigger（施密特触发器）

A ***Schmitt trigger*** is a special type of bi-stable device that has two threshold voltages (i.e. stable states).

Characteristics:

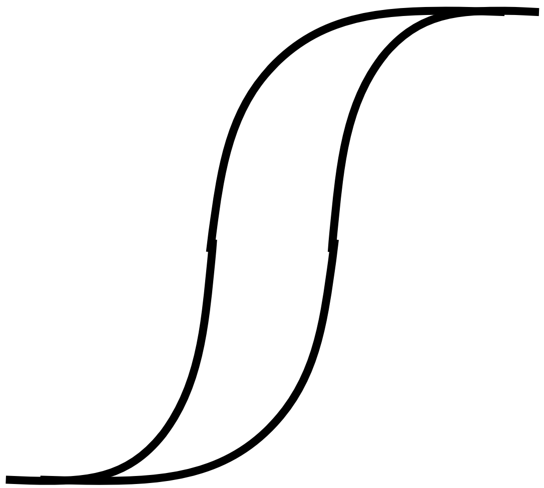
- using two voltage thresholds: a high threshold to switch the circuit during low-to-high transitions and a lower threshold to switch the circuit during high-to-low transitions.
- Generating pulse with sharp edges

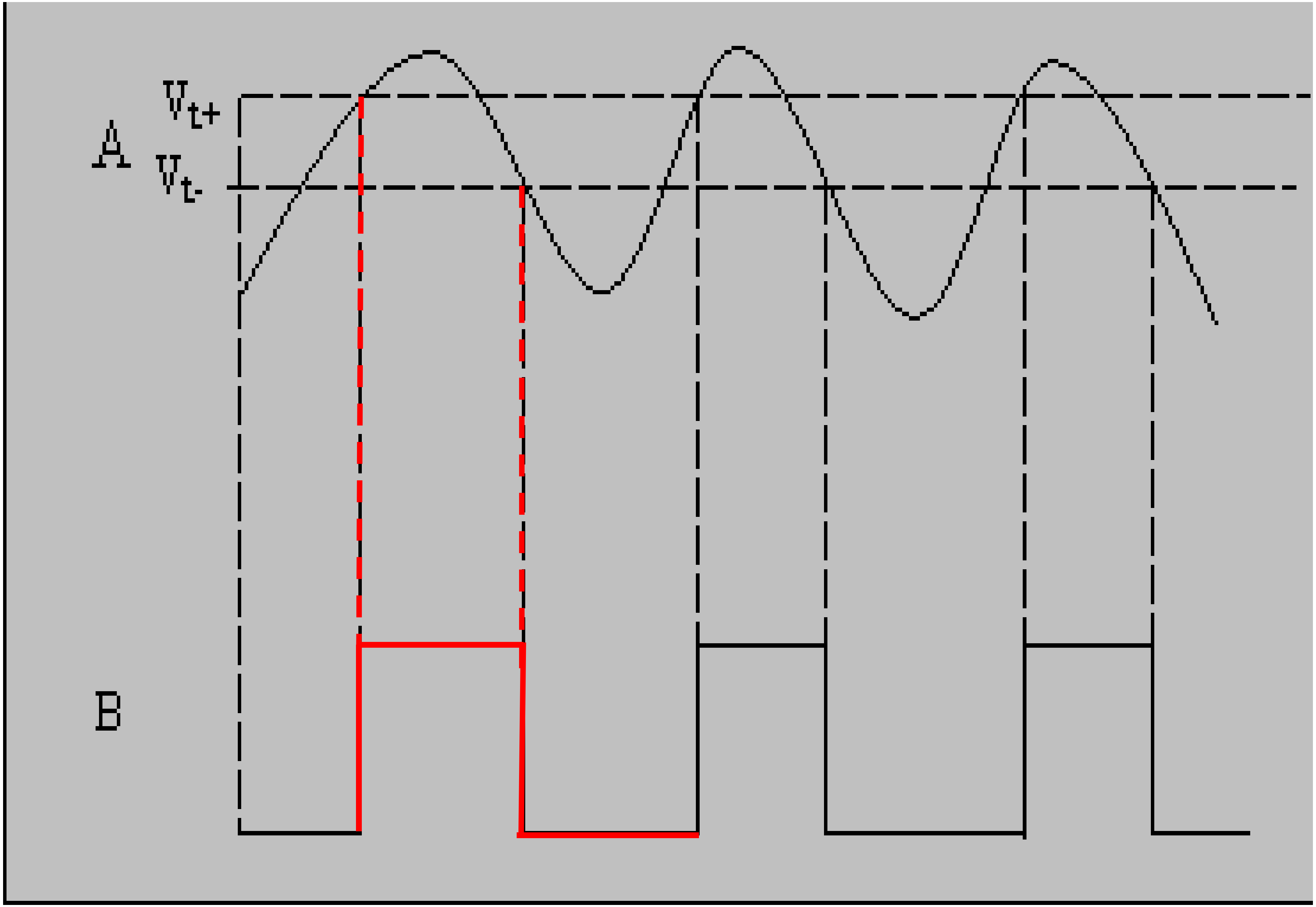
Advantages:

- conditioning slow or noisy signals
- increasing the noise immunity

Symbol

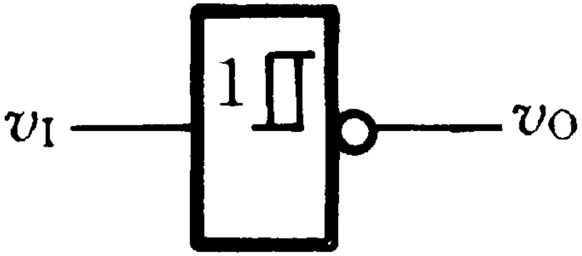
The ***hysteresis symbol*** indicates a Schmitt trigger input

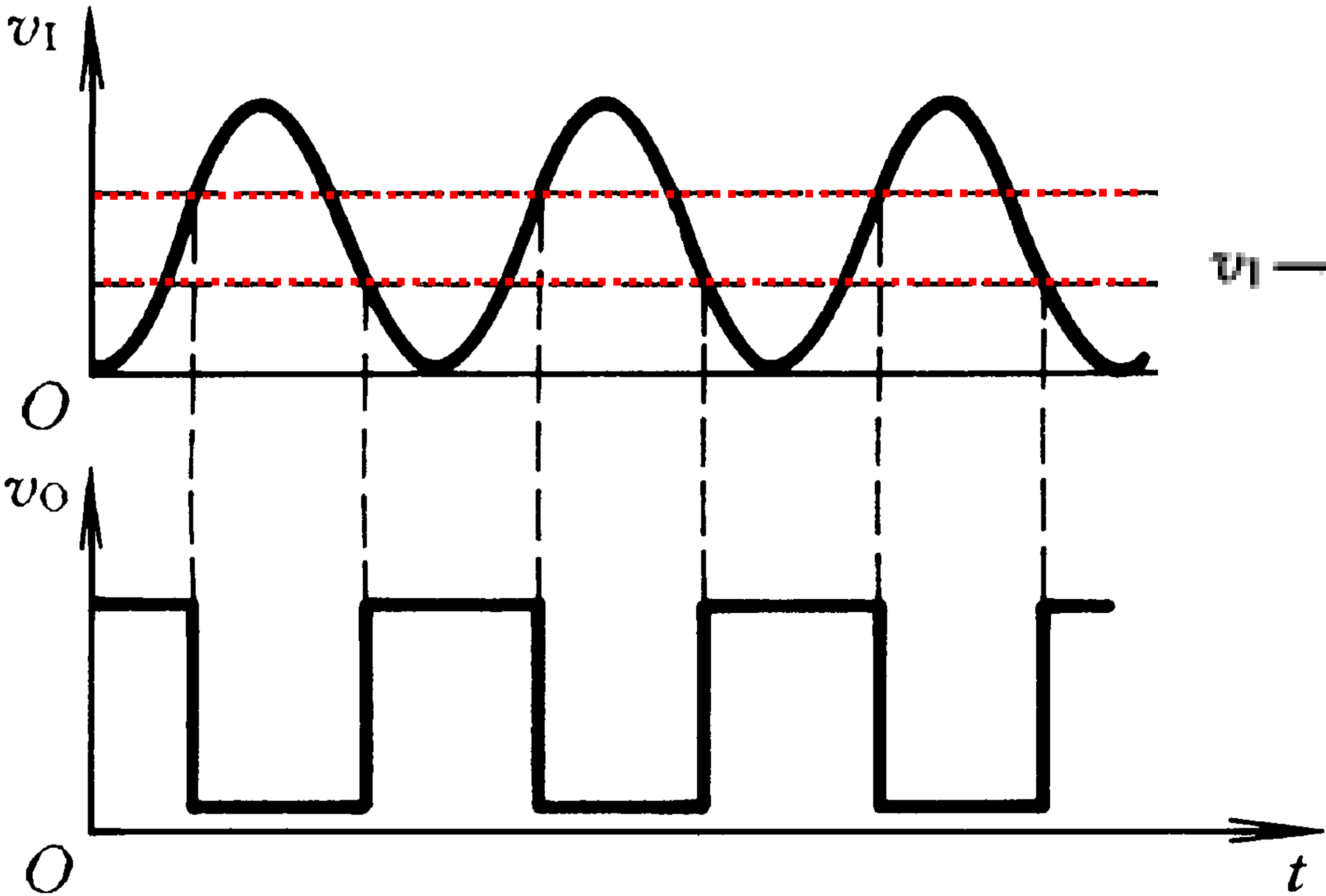


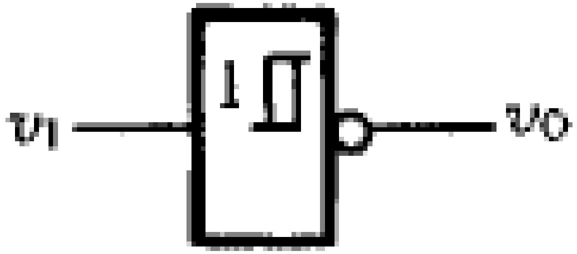

A
V_{t+}
V_{t-}
B

Applications of Schimitt Trigger

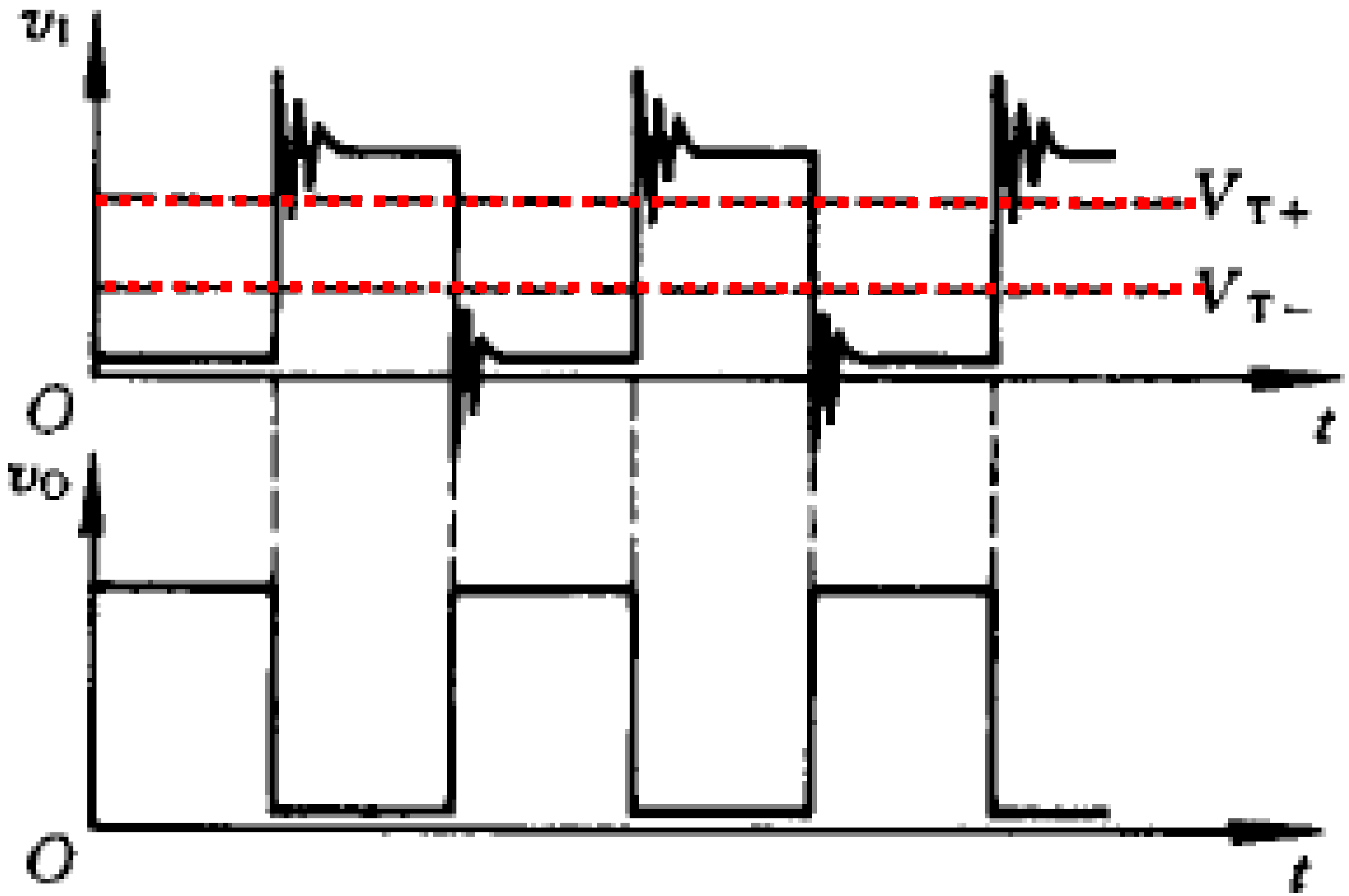
- Pulse conditioning
- Noise immunity
- Amplitude Checking


v_I
1
v_O

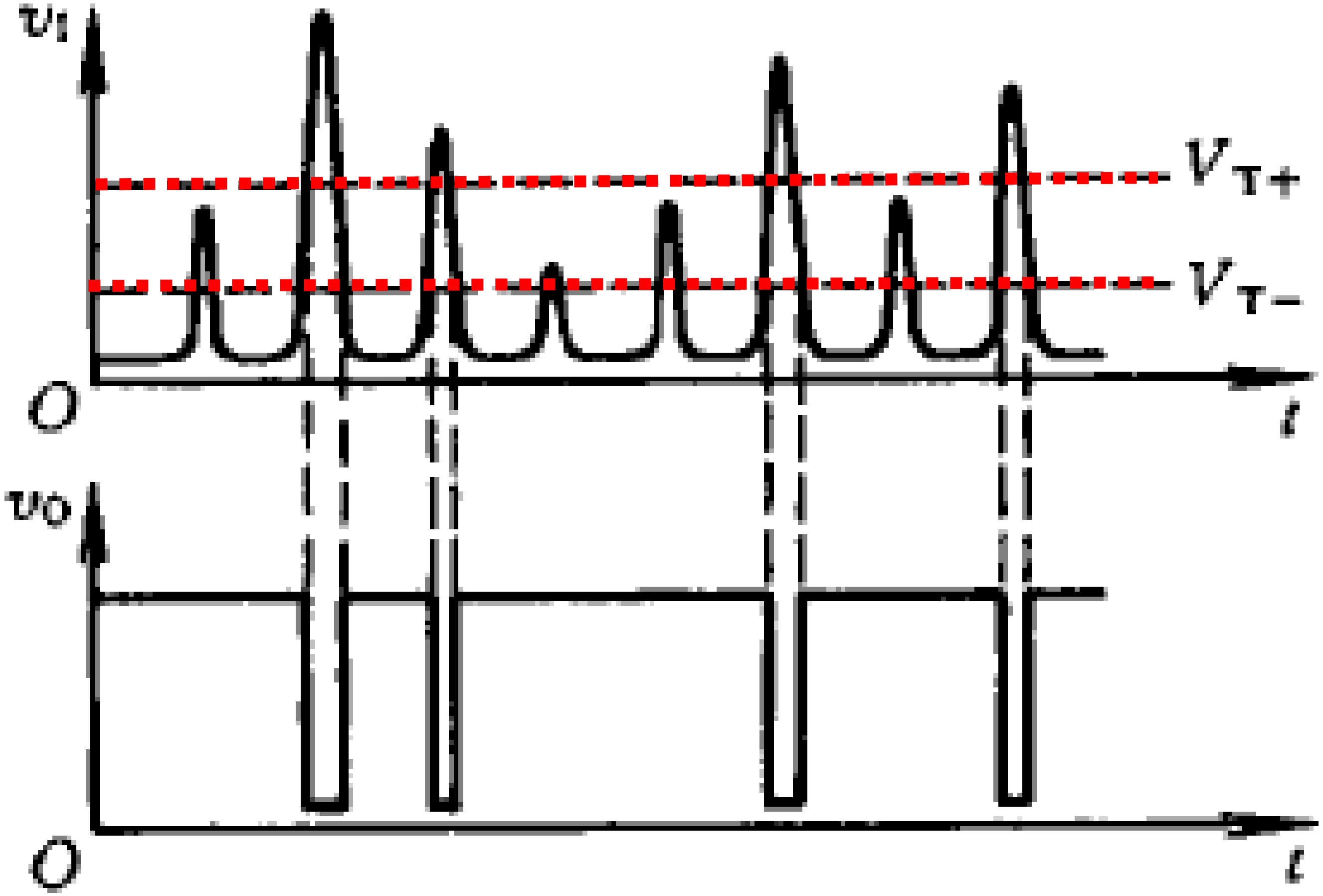

v_I
O
v_O
O
t


v_I
1
v_O

Noise immunity

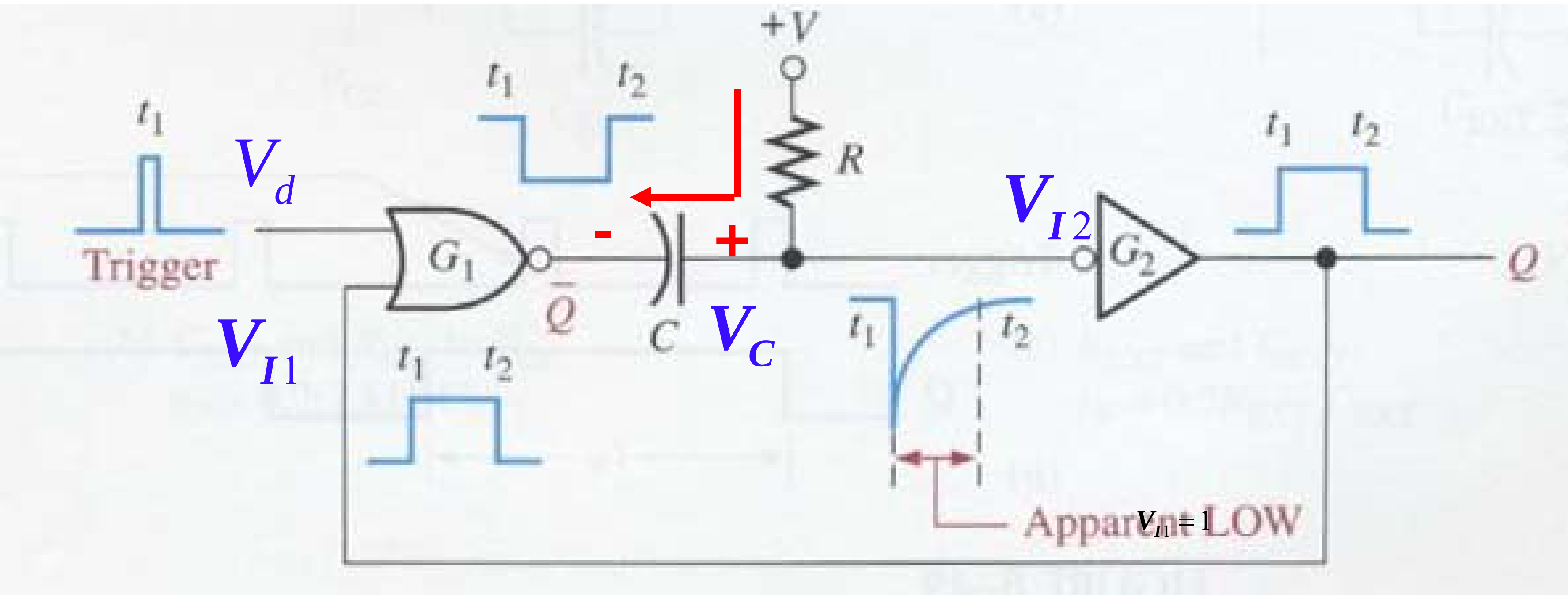


Amplitude Checking



7.6 One-Shots (单稳态触发器)

- ***One shot*** (monostable multivibrator) only has one stable state and one unstable state.
- When triggered, the device changes from its stable state to its unstable state and remains there for a fixed period of time, known as the ***pulse width***, before returning to its stable state.
- The duration time of the unstable state determined by the circuit parameters, no related with the triggered pulse.
- The duration time of the unstable state determines the pulse width of the output pulse.



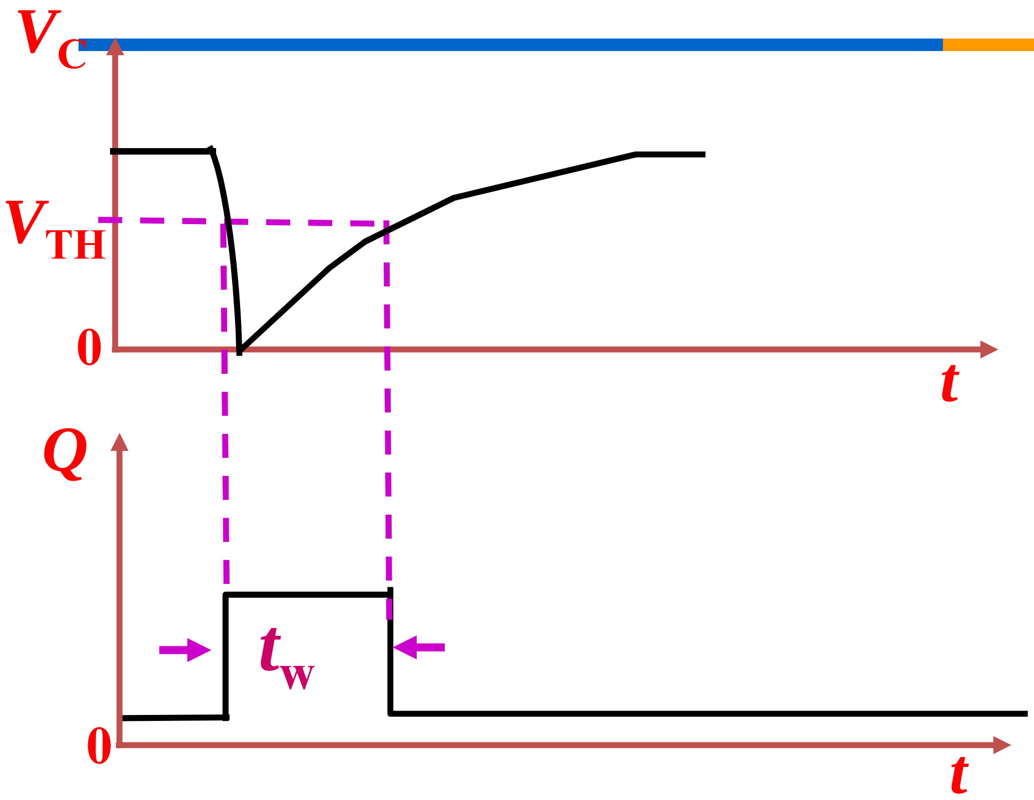
When triggered:

$$\bar{Q} = 0 \rightarrow V_C \approx \bar{Q} \rightarrow V_{I2} \approx 0 \rightarrow Q = 1 \rightarrow$$

$$\bar{Q} = 0 \rightarrow V_C \uparrow \rightarrow V_{I2} \uparrow \rightarrow Q \downarrow \rightarrow Q = 0 \rightarrow V_{I1} \downarrow \rightarrow V_{I1} = 0$$

$$\bar{Q} = 1$$

A single narrow trigger pulse produces a single output pulse whose time duration is controlled by the RC time Constant



$$v_c(t) = v_c(\infty) + [v_c(0_+) - v_c(\infty)]e^{-\frac{t}{\tau}}$$

$$v_c(\infty) = V_{DD} \qquad v_c(0_+) = 0 \qquad \tau = RC$$

$$v_c(t_w) = V_{TH} \quad \Rightarrow \quad t_W = RC \ln \frac{V_{DD}}{V_{DD} - V_{TH}}$$

- Stable state: Q=0
- Unstable state: Q=1
- The time duration determined by the charge time of C and R , i.e. the RC time constant.

$$t_W = RC \ln \frac{V_{DD}}{V_{DD} - V_{TH}} = RC \ln 2 \approx 0.69 RC$$

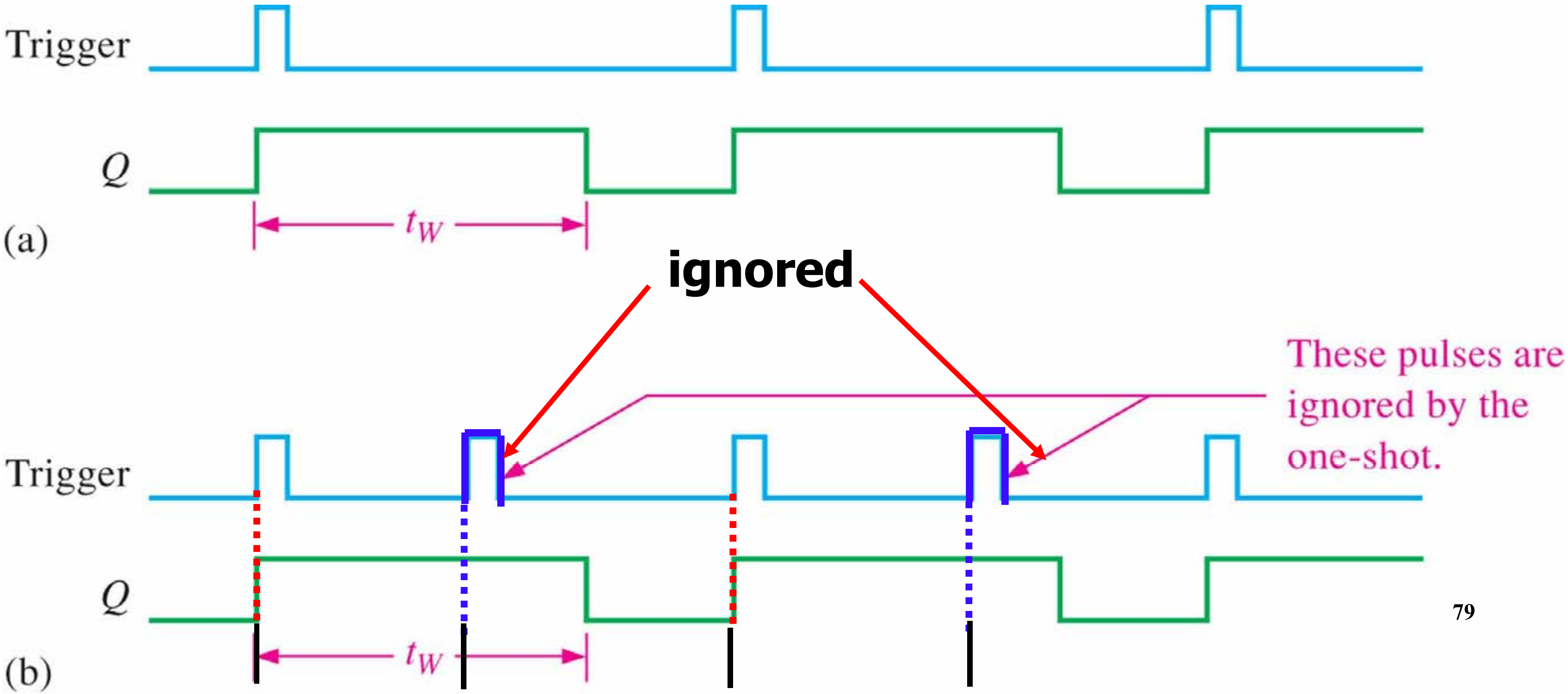
$$\approx 0.7 RC$$

Two basic types of IC one-shot

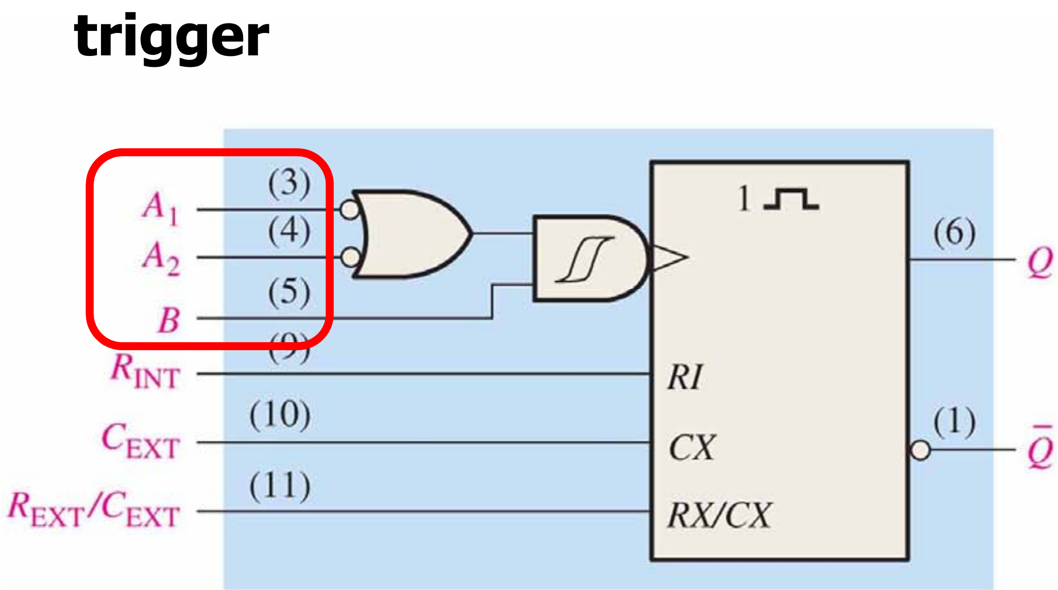
- ***Nonretriggerable*** one-shot
- ***Retriggerable*** one-shot

Non-retriggerable one-shot

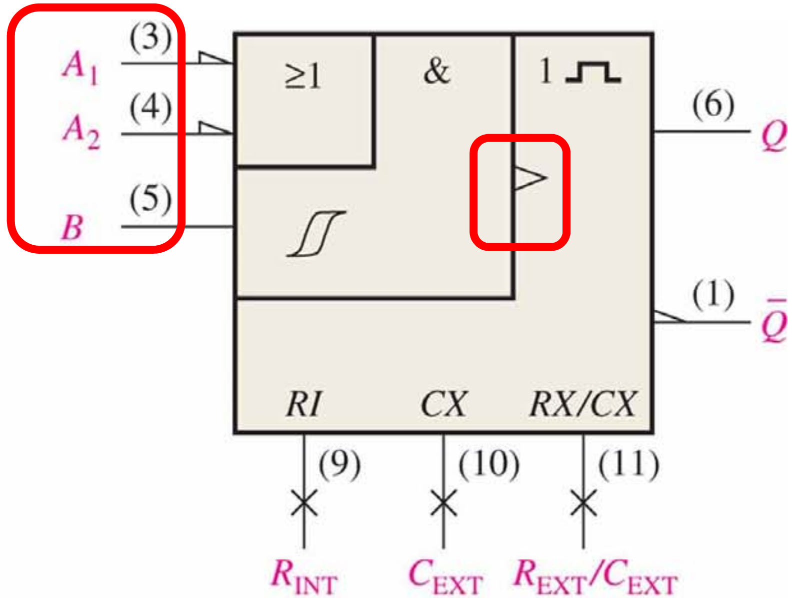
Not respond to any additional trigger pulse from the time it is triggered until it returns to stable state.



74LS121: non-retriggered one-shot

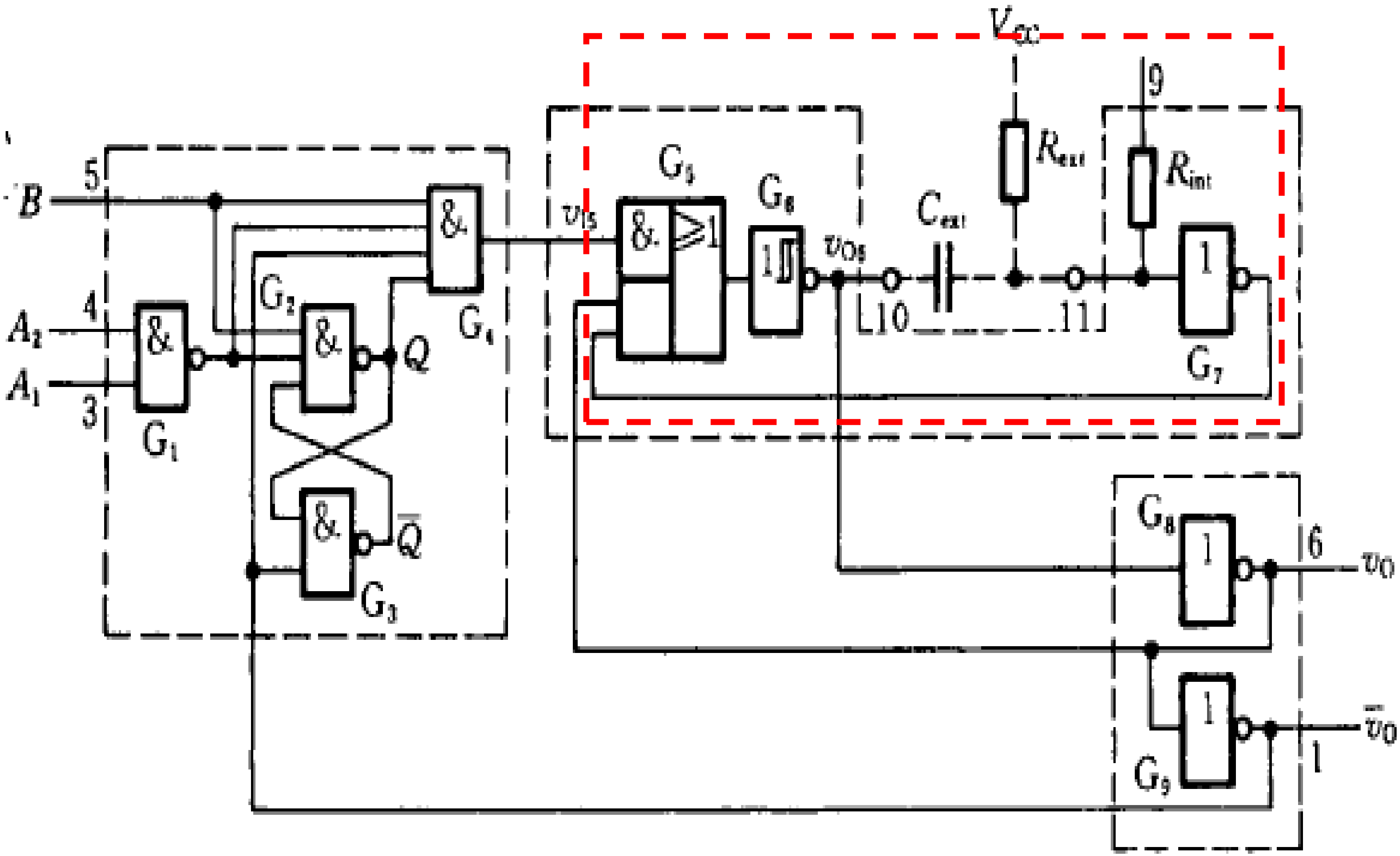


(a) Traditional logic symbol

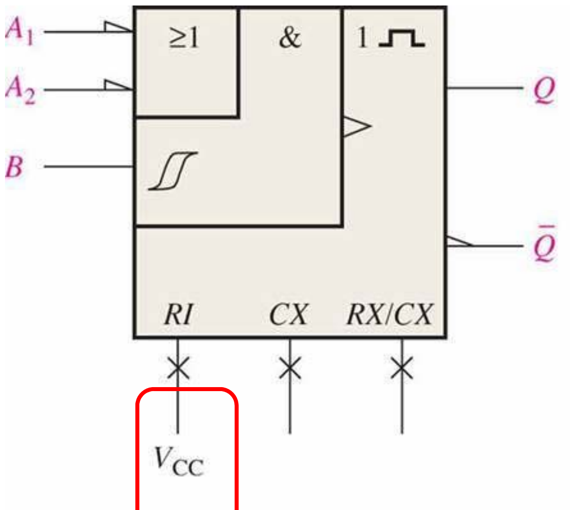


(b) ANSI/IEEE std. 91–1984 logic symbol (✕ = nonlogic connection). "1⎍" is the qualifying symbol for a nonretriggerable one-shot.

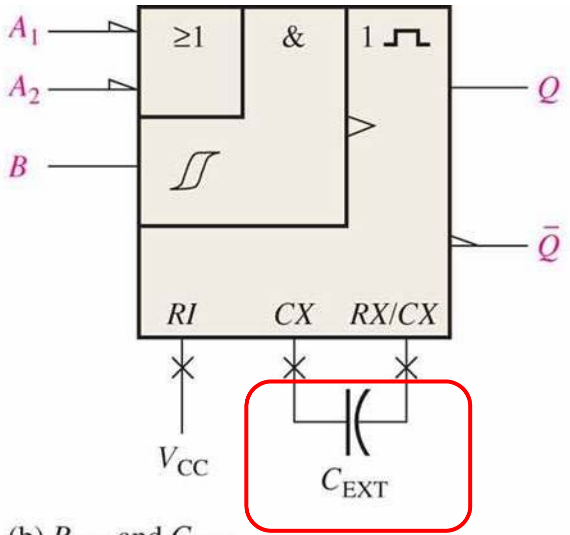
R_{INT}=2KΩ



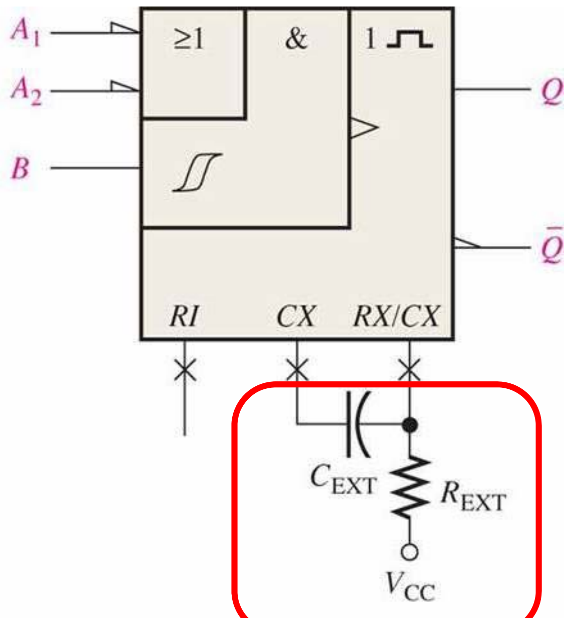
B
5
A2
4
A1
3
G1
G2
G3
G4
Q
v_I5
G5
G6
v_O6
C_ext
V_CC
R_ext
R_int
9
10
11
G7
G8
G9
6
v_O
1



(a) No external components
R_{INT} to V_{CC}
$t_W \cong 30$ ns



(b) R_{INT} and C_{EXT}
$t_W = 0.7(2\ \text{k}\Omega)C_{EXT}$



(c) R_{EXT} and C_{EXT}
$t_W = 0.7R_{EXT}\,C_{EXT}$

$$t_W \approx 0.7(2K\Omega)\ C_{EXT}$$

$$t_W \approx 30ns$$

$$t_W \approx 0.7R_{EXT}\ C_{EXT}$$

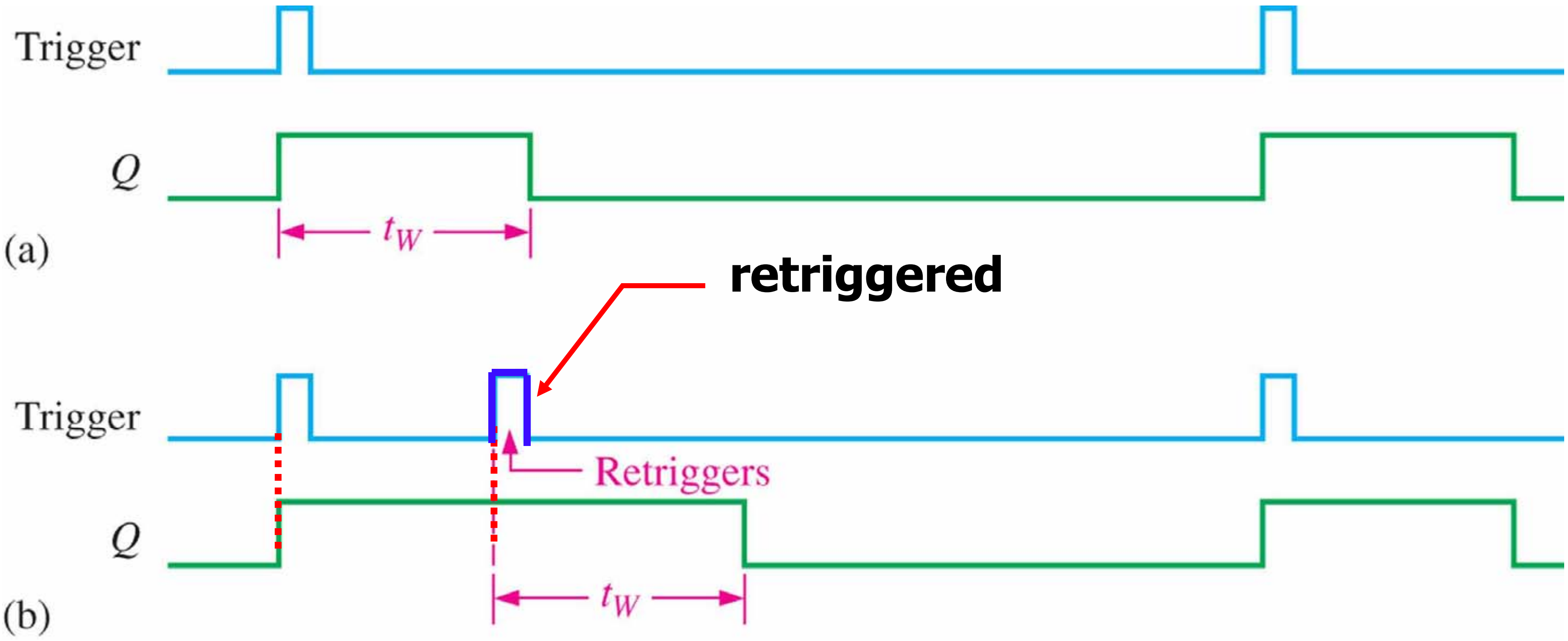
Homework: Exercise

To achieve a one-shot with a pulse width of approximately 10ms, using a 74121.

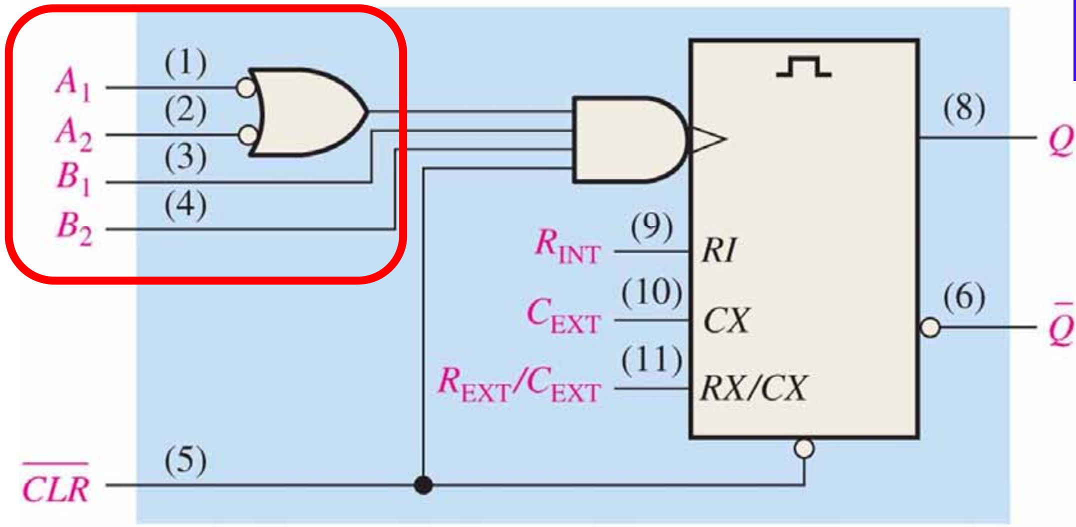
If select R_{EXT}=20KΩ, calculate the capacitance:

C_{EXT}=?

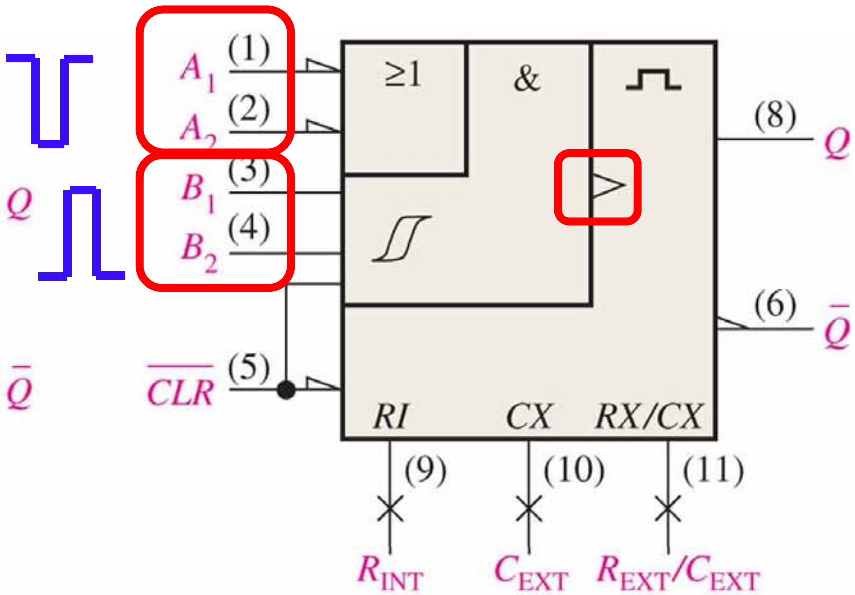
Retriggerable One-shots



74LS122



(a) Traditional logic symbol



(b) ANSI/IEEE std. 91–1984 logic symbol (✕ = nonlogic connection). ⎍ is the qualifying symbol for a retriggerable one-shot.

R_{INT}=10KΩ

Calculation

With no external resistor and capacitor:

$t_W \approx 45ns$

With external resistor and capacitor:

$$t_W = 0.32 RC_{EXT}(1 + \frac{0.7}{R})$$

Exercise:

$$t_W = 0.32 R C_{EXT} (1 + \frac{0.7}{R})$$

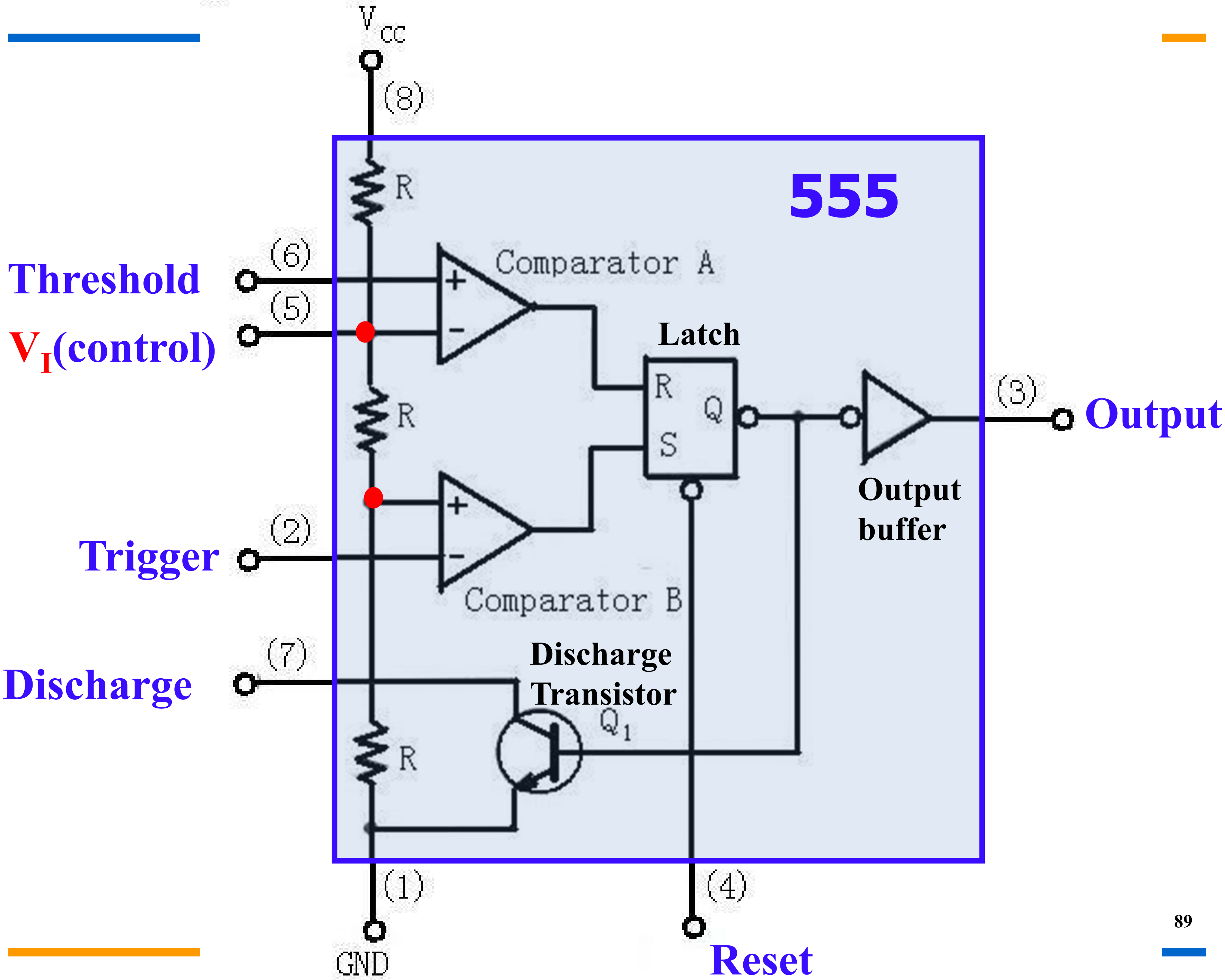
$$= 0.32 \times 47 K\Omega \times 68 \mu F \times (1 + \frac{0.7}{47 K\Omega})$$

$$= 1.0227(s)$$

$$\approx 1(s)$$

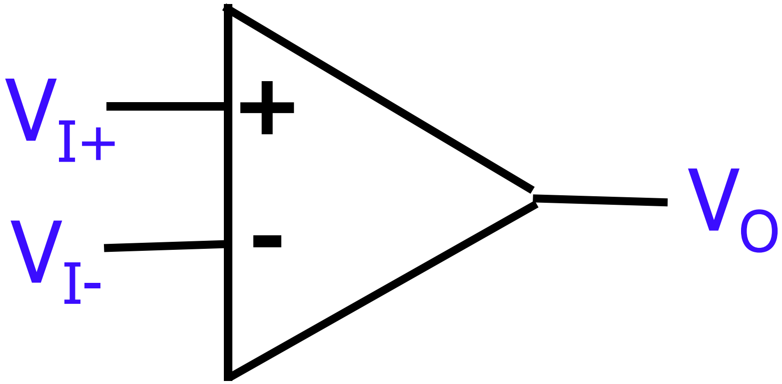
7.7 555 Timer

- Basic Operation
- One-shot Operation
- Schimitt Trigger Operation
- Astable Operation



VCC
(8)
555
R
Comparator A
Threshold
(6)
(5)
VI(control)
Latch
R
Q
S
R
(3)
Output
Output buffer
Trigger
(2)
Comparator B
Discharge
(7)
Discharge Transistor
Q1
R
(1)
GND
(4)
Reset

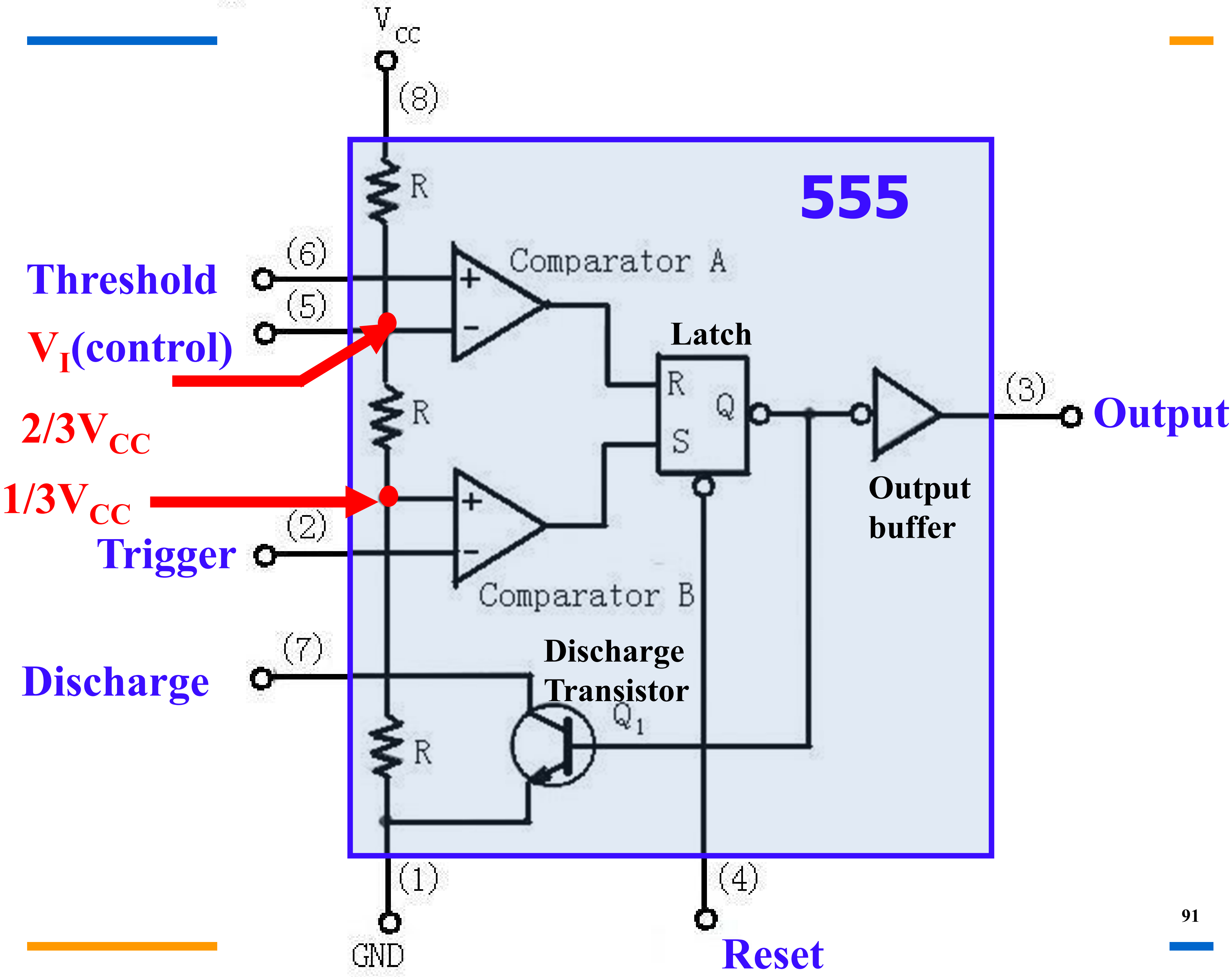
Comparator



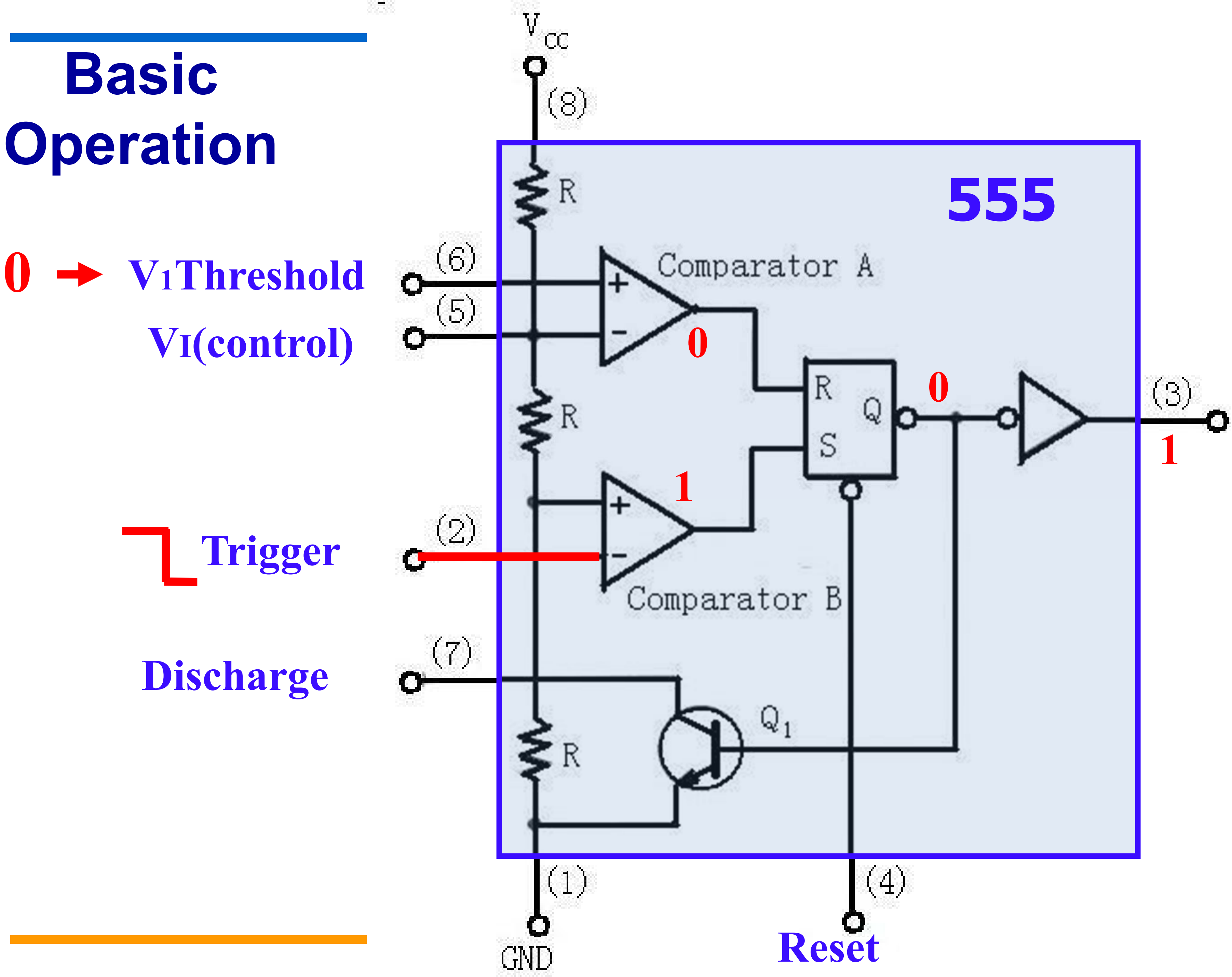
V_{I+}, V_{I-}, V_O

If $V_{I+}>V_{I-}$, then V_O=HIGH

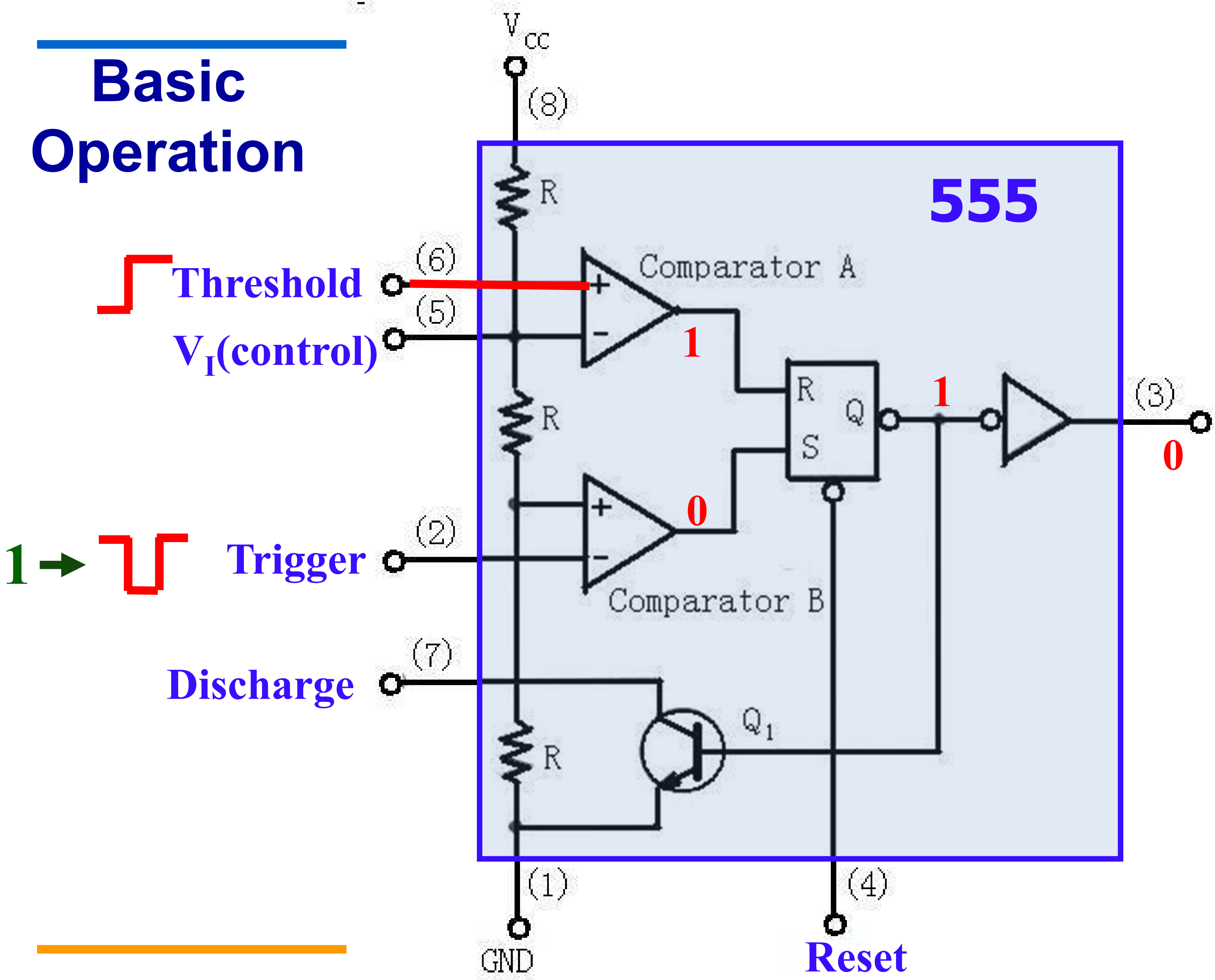
If $V_{I+}<V_{I-}$, then V_O=LOW

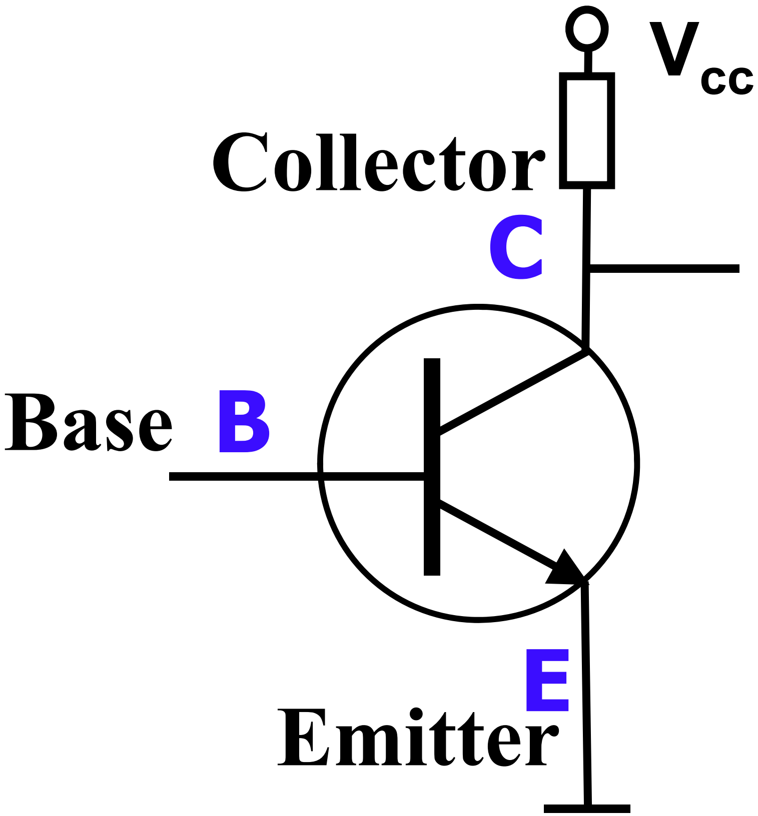

V CC
(8)
555
R
Comparator A
Threshold
(6)
(5)
V I (control)
Latch
R
Q
S
(3)
Output
R
2/3V CC
1/3V CC
+
−
Output
buffer
(2)
Trigger
Comparator B
(7)
Discharge
Discharge
Transistor
Q 1
R
(1)
GND
(4)
Reset

Basic Operation



Basic Operation

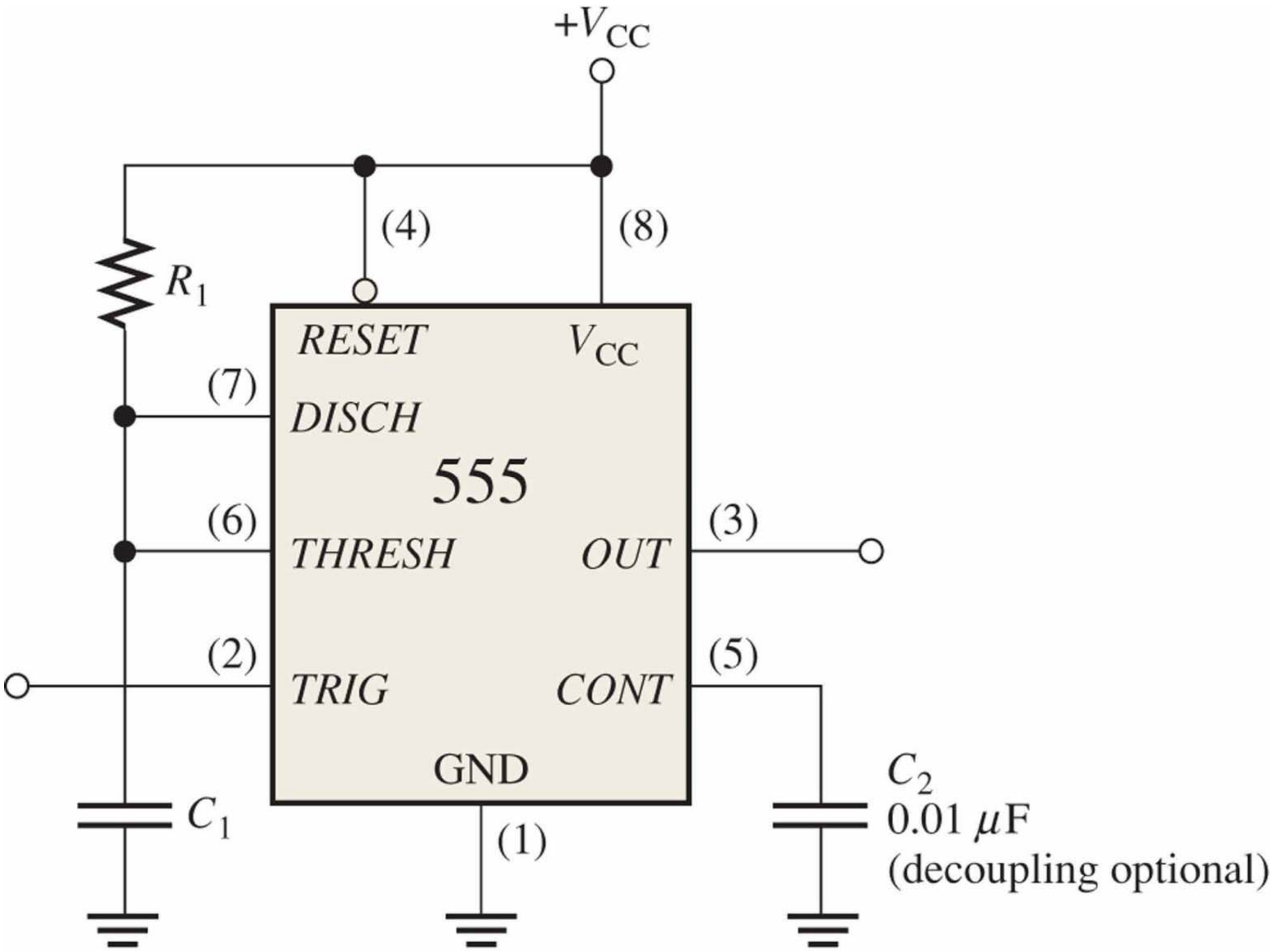


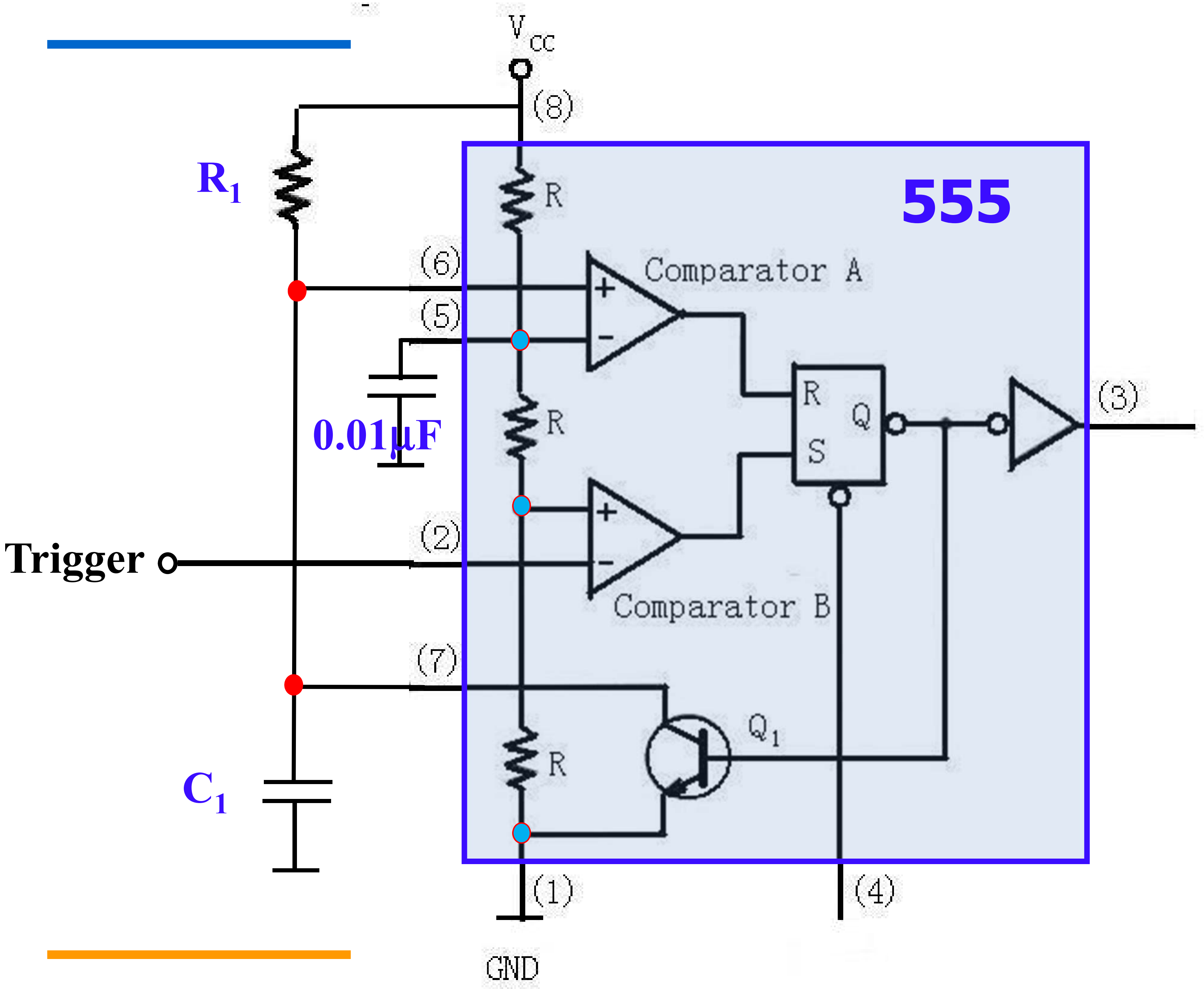


If $V_{BE} > V_{bias}$, V_c=LOW

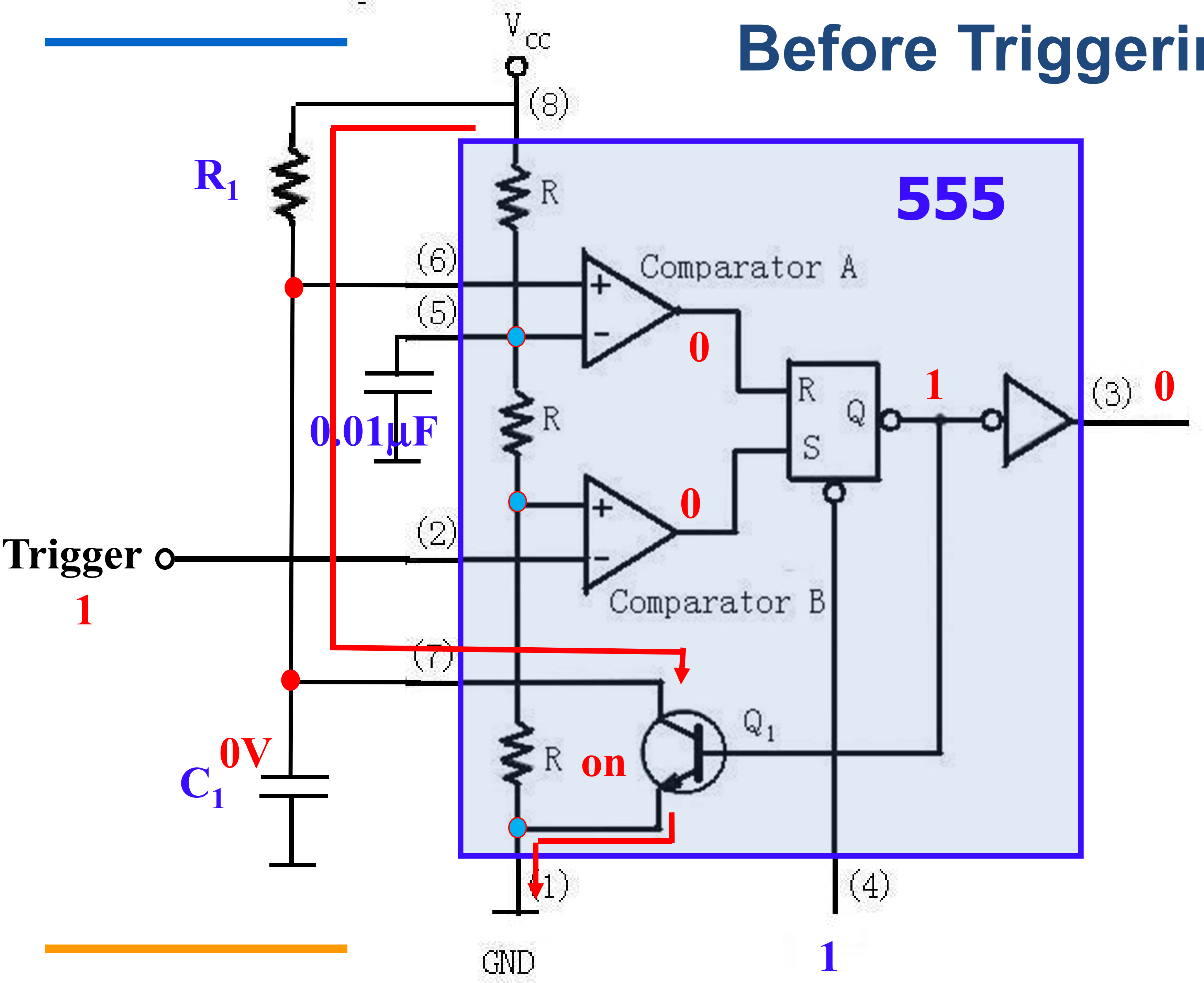
If $V_{BE} < V_{bias}$, V_c=HIGH

One-shot Operation

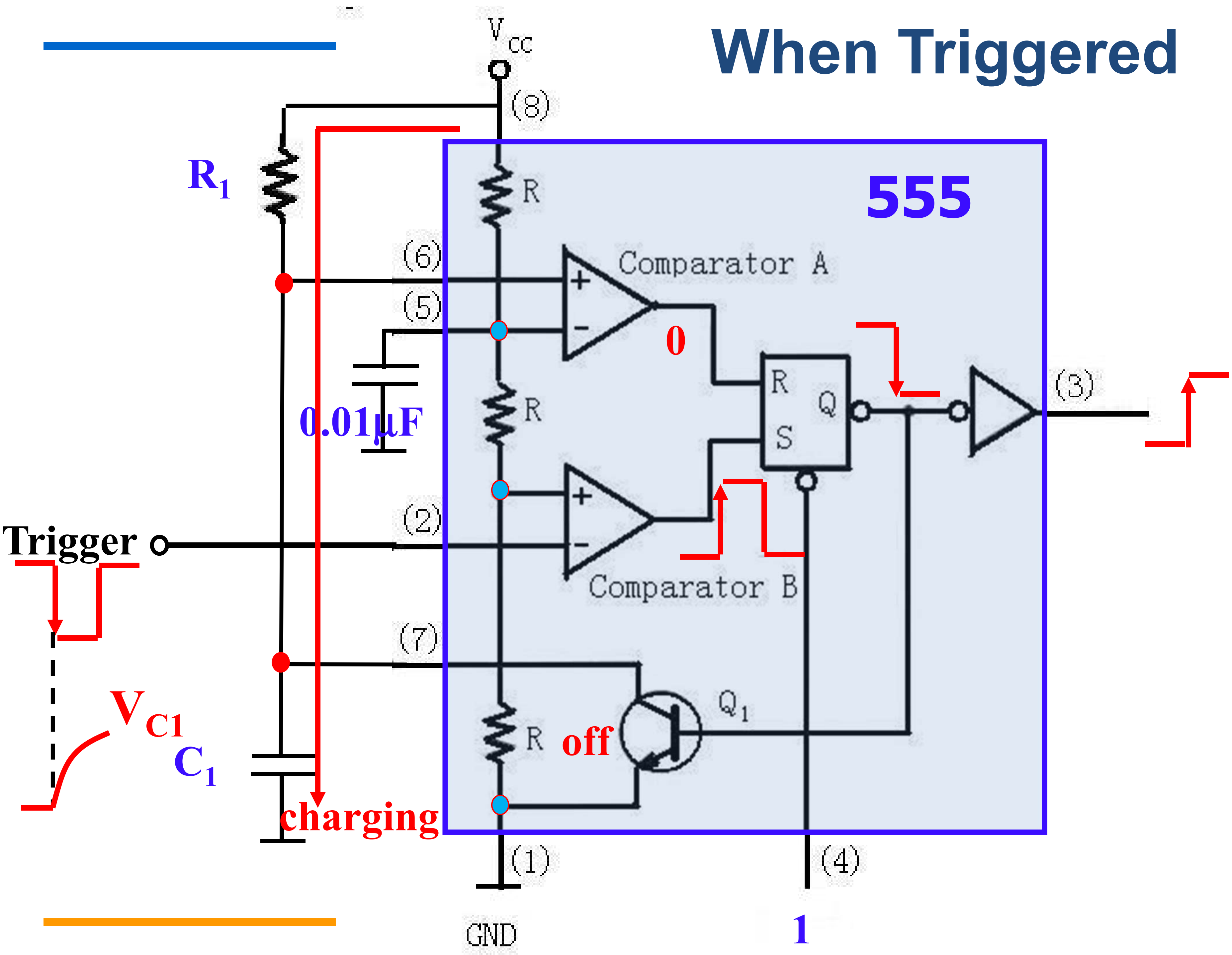



Vcc
(8)
R1
R
555
(6)
Comparator A
(5)
R
Q
S
(3)
0.01μF
R
(2)
Trigger
Comparator B
(7)
Q1
C1
R
(1)
(4)
GND

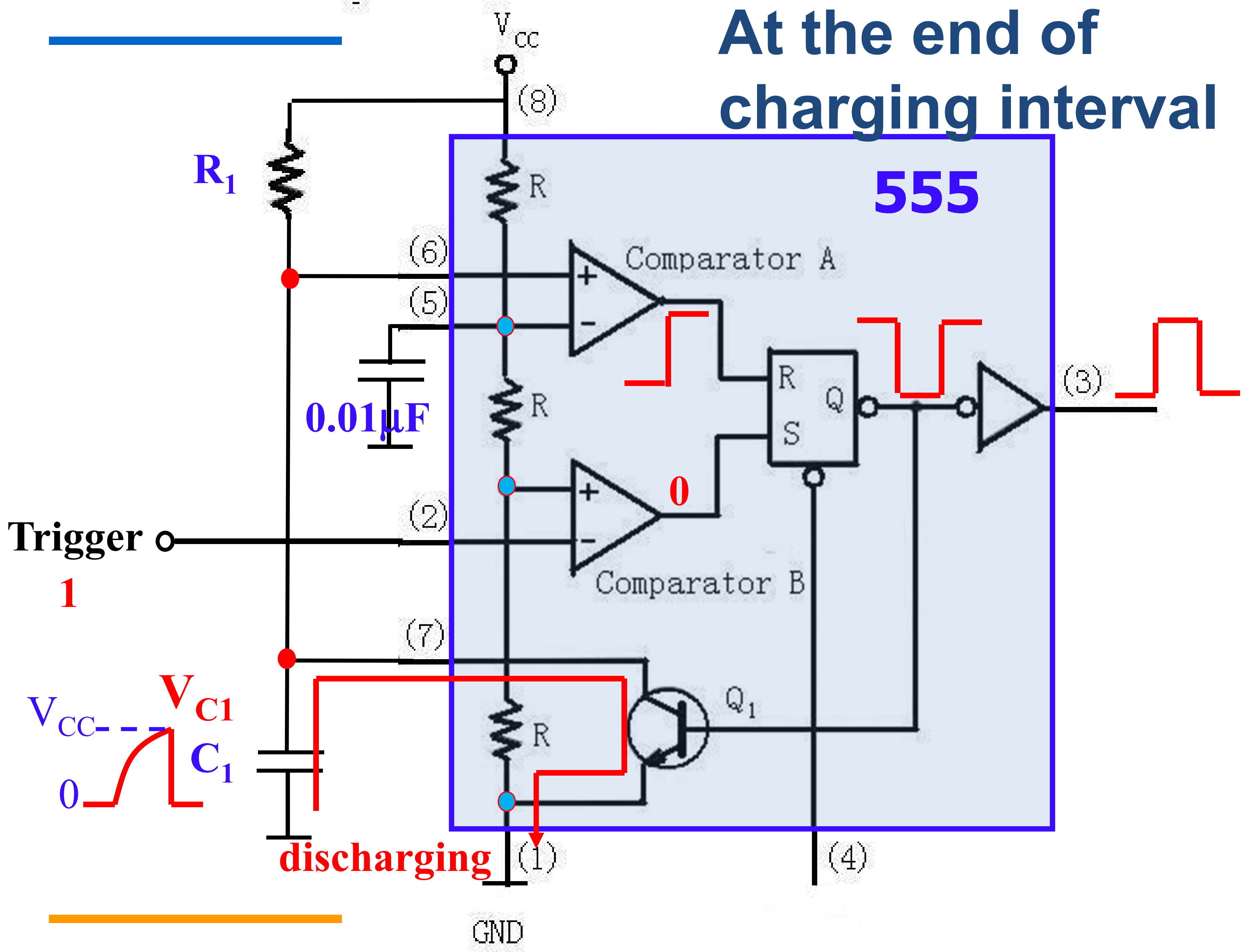
Before Triggering

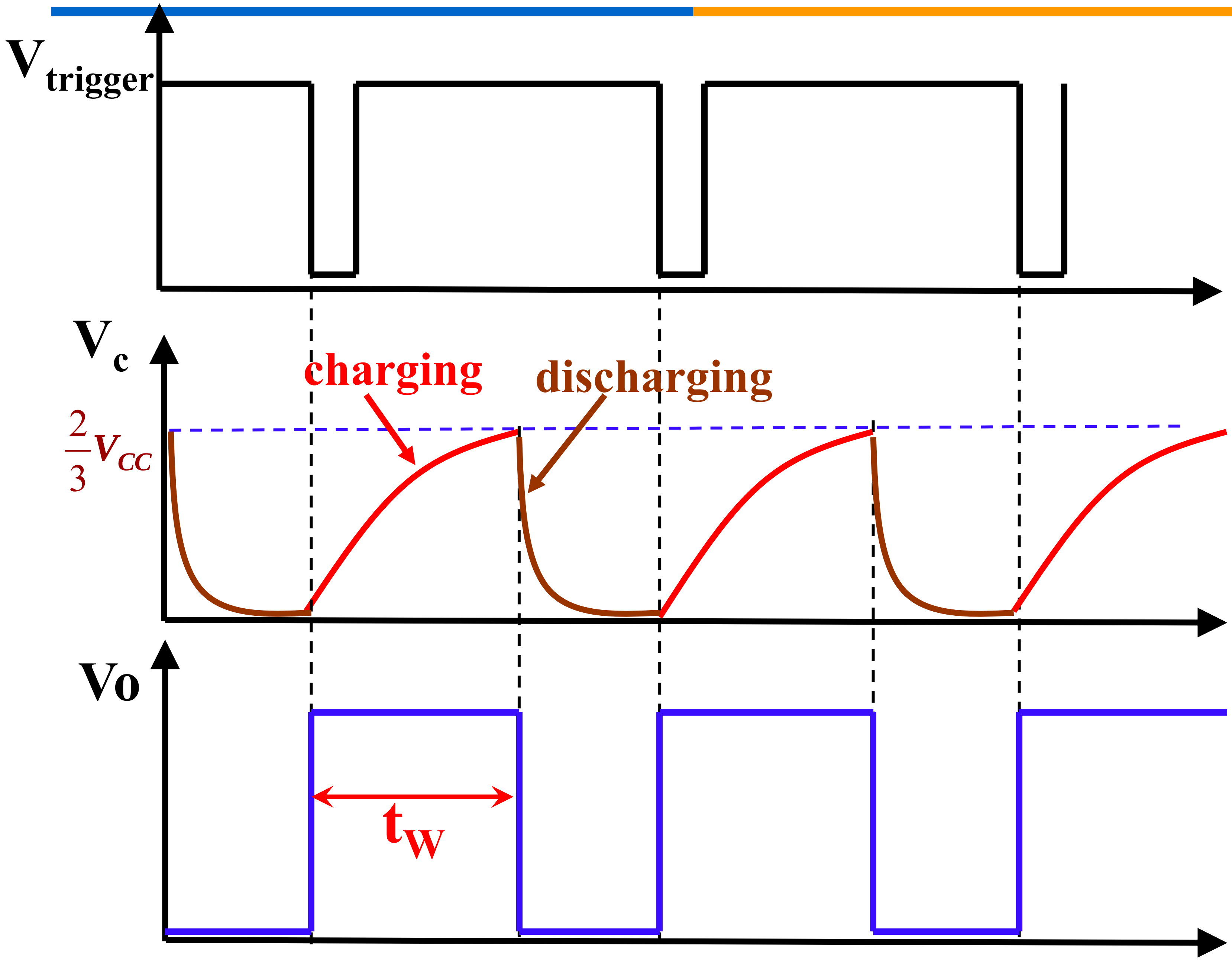


When Triggered



At the end of charging interval





V trigger
V c
charging
discharging
$\frac{2}{3}V_{CC}$
Vo
t_W

$$t_W = R_1 C_1 \ln \frac{V_{CC} - 0}{V_{CC} - \frac{2}{3} V_{CC}}$$

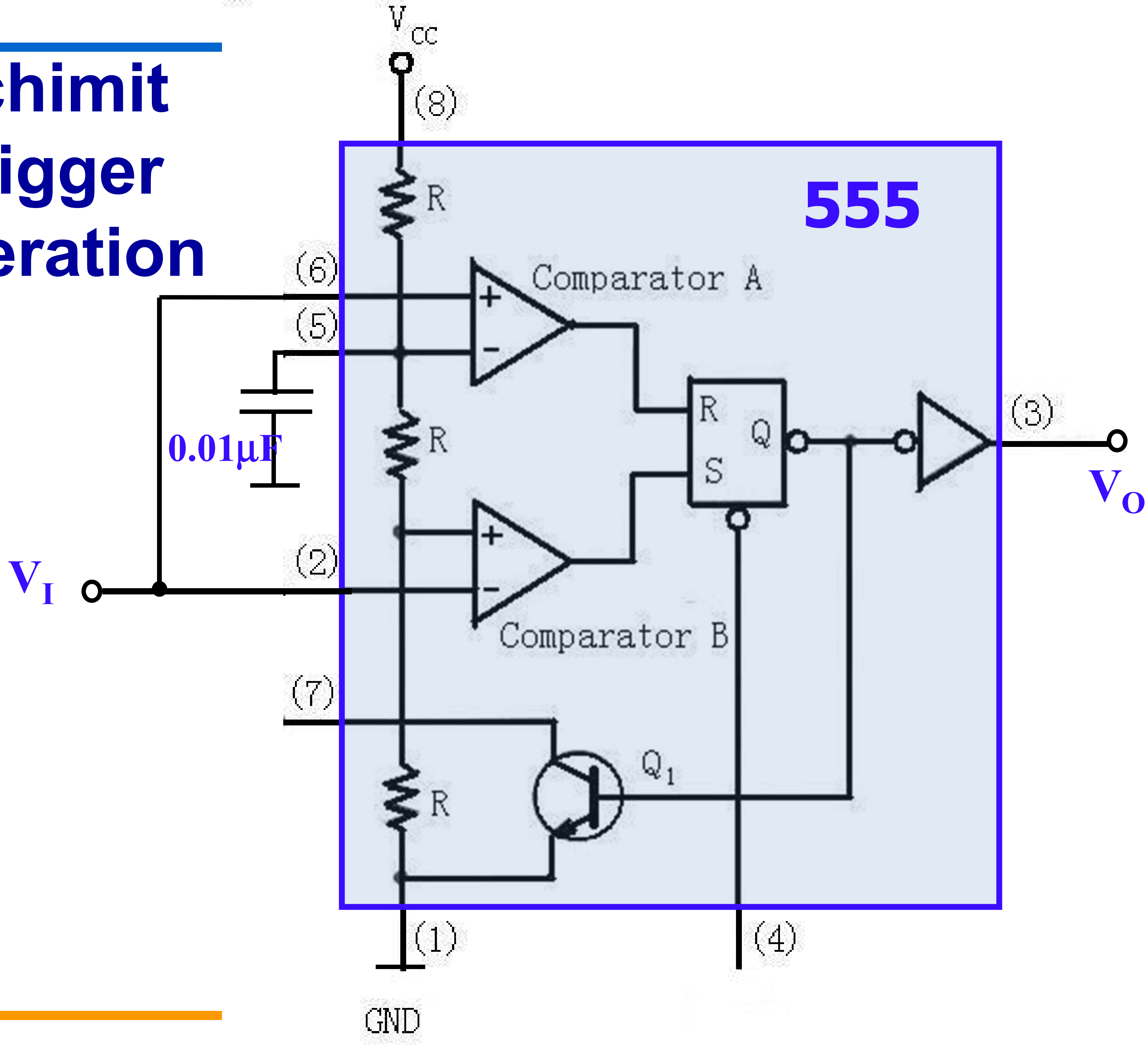
$$= R_1 C_1 \ln 3 \approx 1.1 R_1 C_1$$

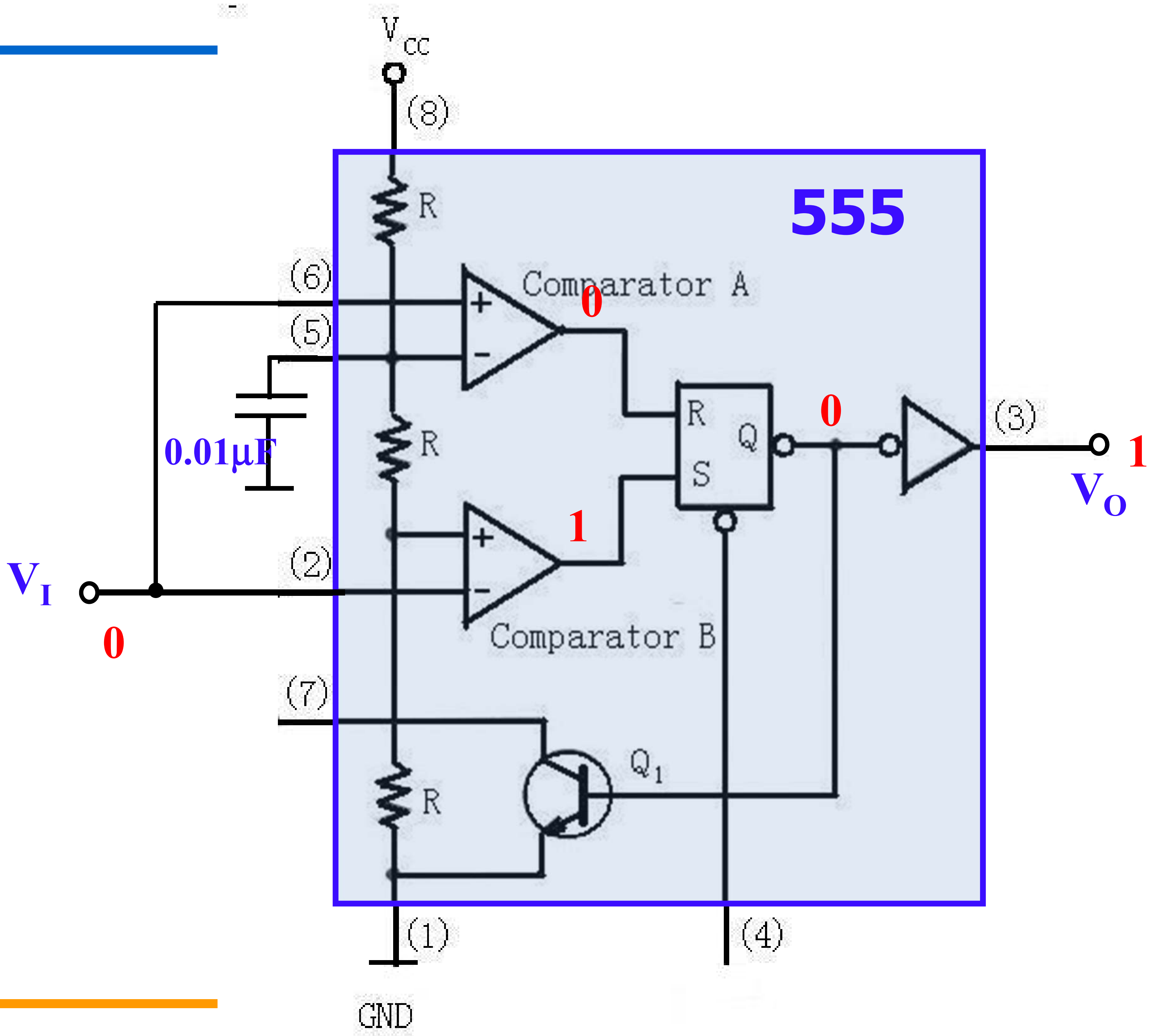
Example

For C_1=0.01μF, determine the value of R_1 for a pulse width of 1ms.

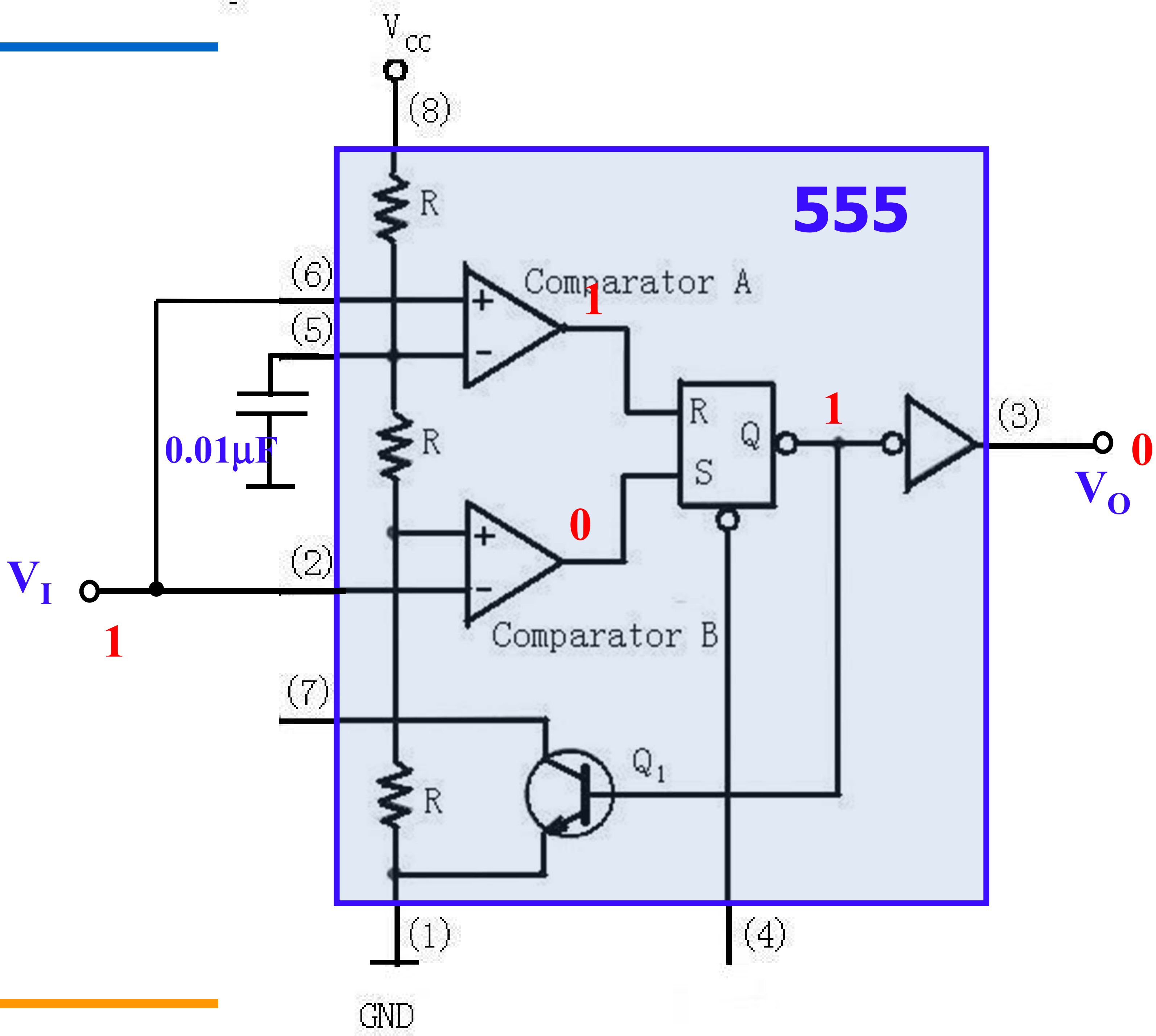
$$\boldsymbol{R}_1 = \frac{\boldsymbol{t}_W}{1.1\boldsymbol{C}_1} = \frac{1\times 10^{-3}}{1.1\times 0.01\times 10^{-6}} \approx 91\boldsymbol{K}\Omega$$

Schimit Trigger Operation

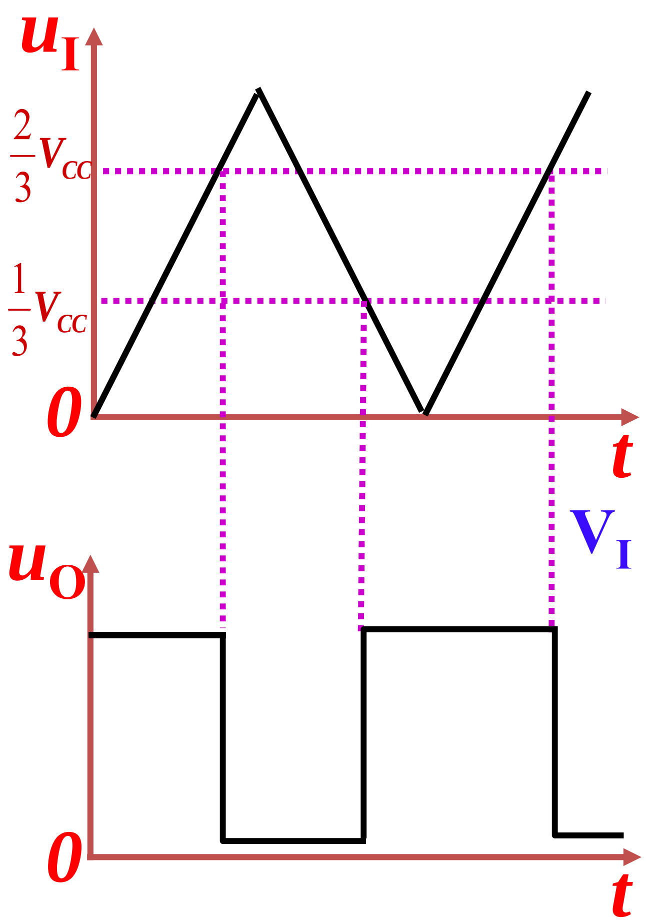




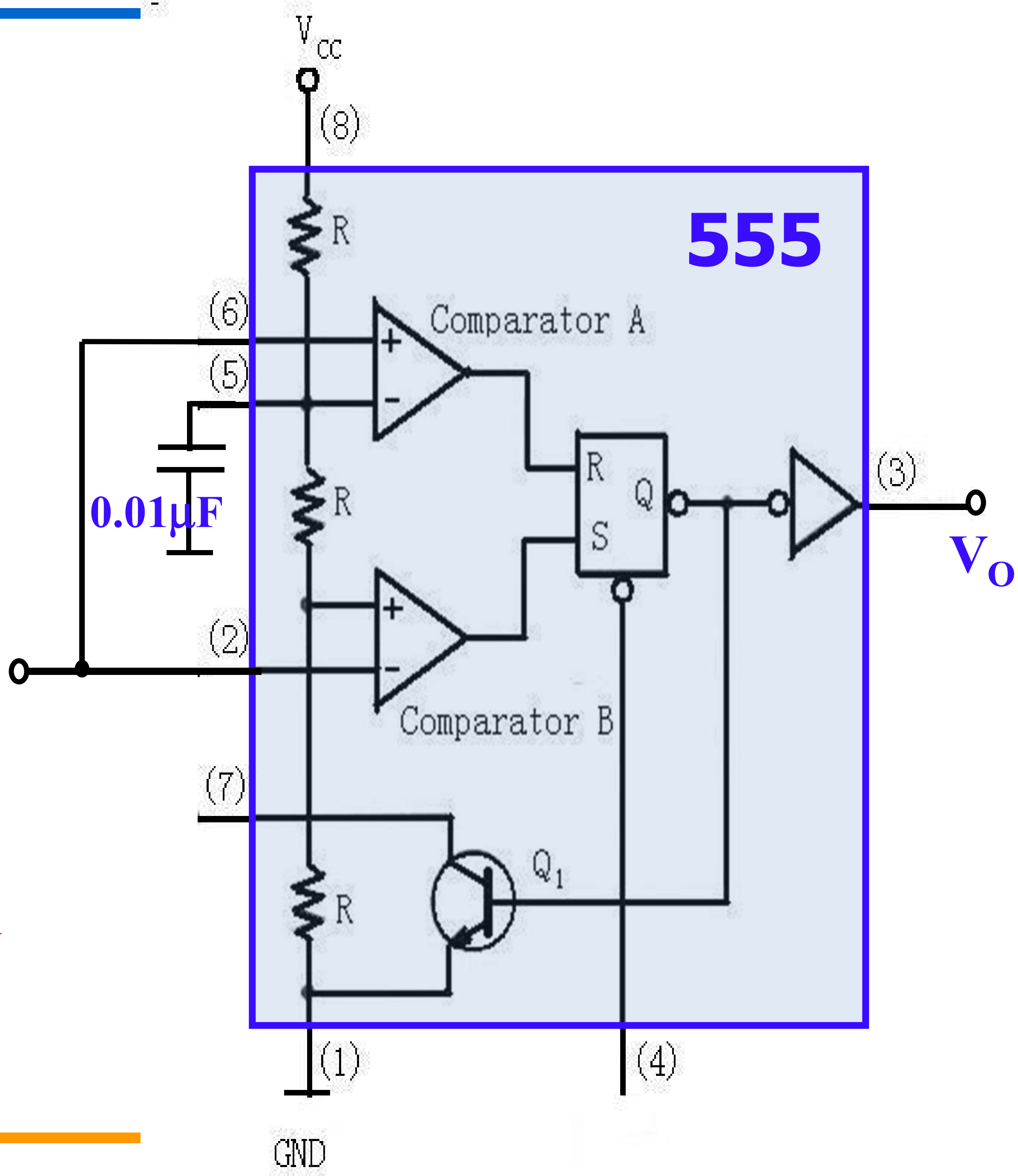
Vcc
(8)
R
555
(6)
Comparator A
0
(5)
R
Q
0
(3)
1
0.01μF
R
S
VO
1
VI
(2)
0
Comparator B
(7)
Q1
R
(1)
(4)
GND



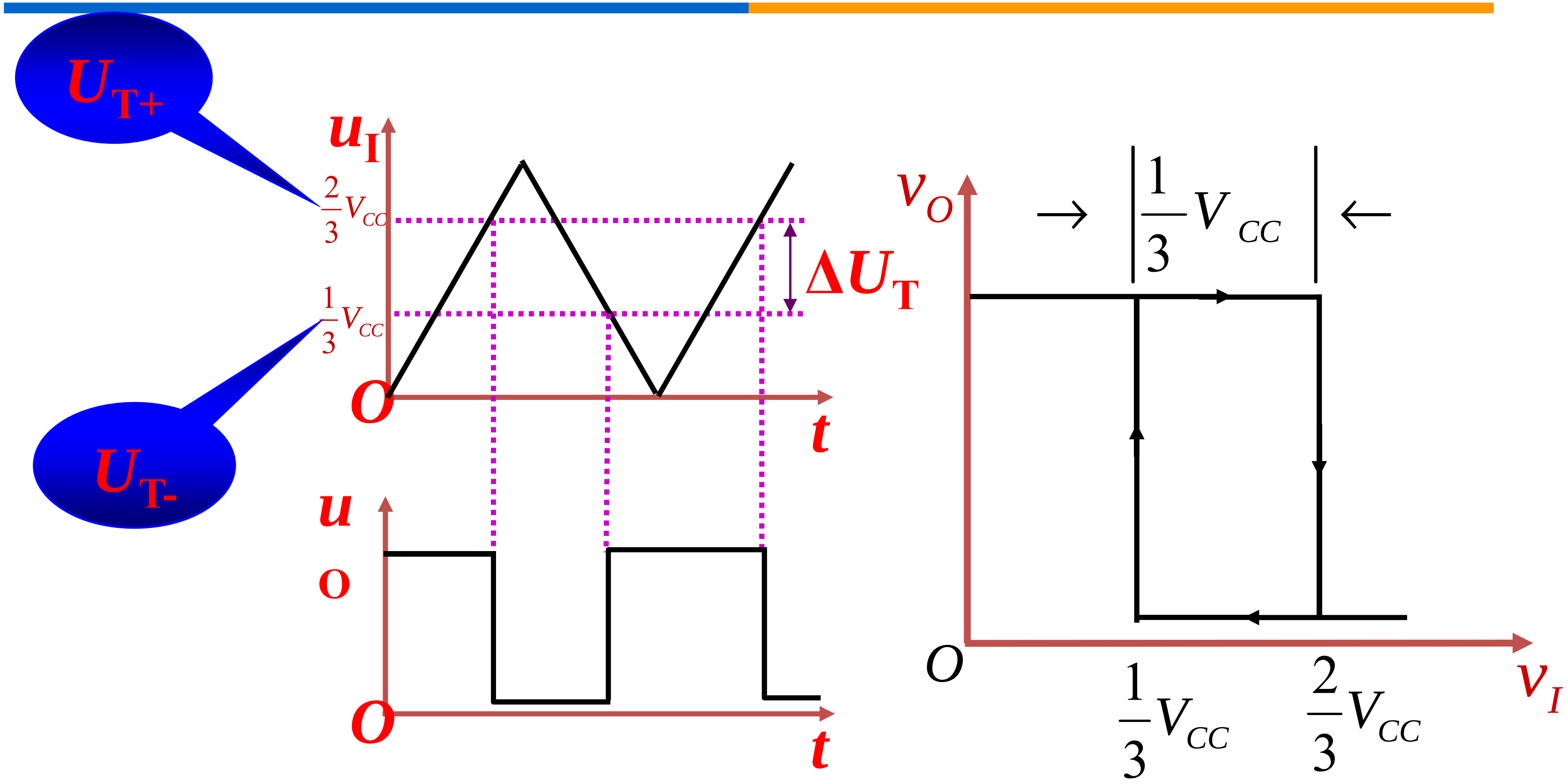
V_{CC}
(8)
R
555
(6)
Comparator A
1
(5)
R
Q
1
(3)
0
V_O
0.01μF
S
R
0
V_I
(2)
1
Comparator B
(7)
Q_1
R
(1)
(4)
GND



u_I
$\frac{2}{3}V_{CC}$
$\frac{1}{3}V_{CC}$
0
t
u_O
0
t



V_{CC}
(8)
R
555
(6)
Comparator A
(5)
0.01μF
R
Q
S
(3)
V_O
V_I
(2)
Comparator B
(7)
Q_1
R
(1)
(4)
GND



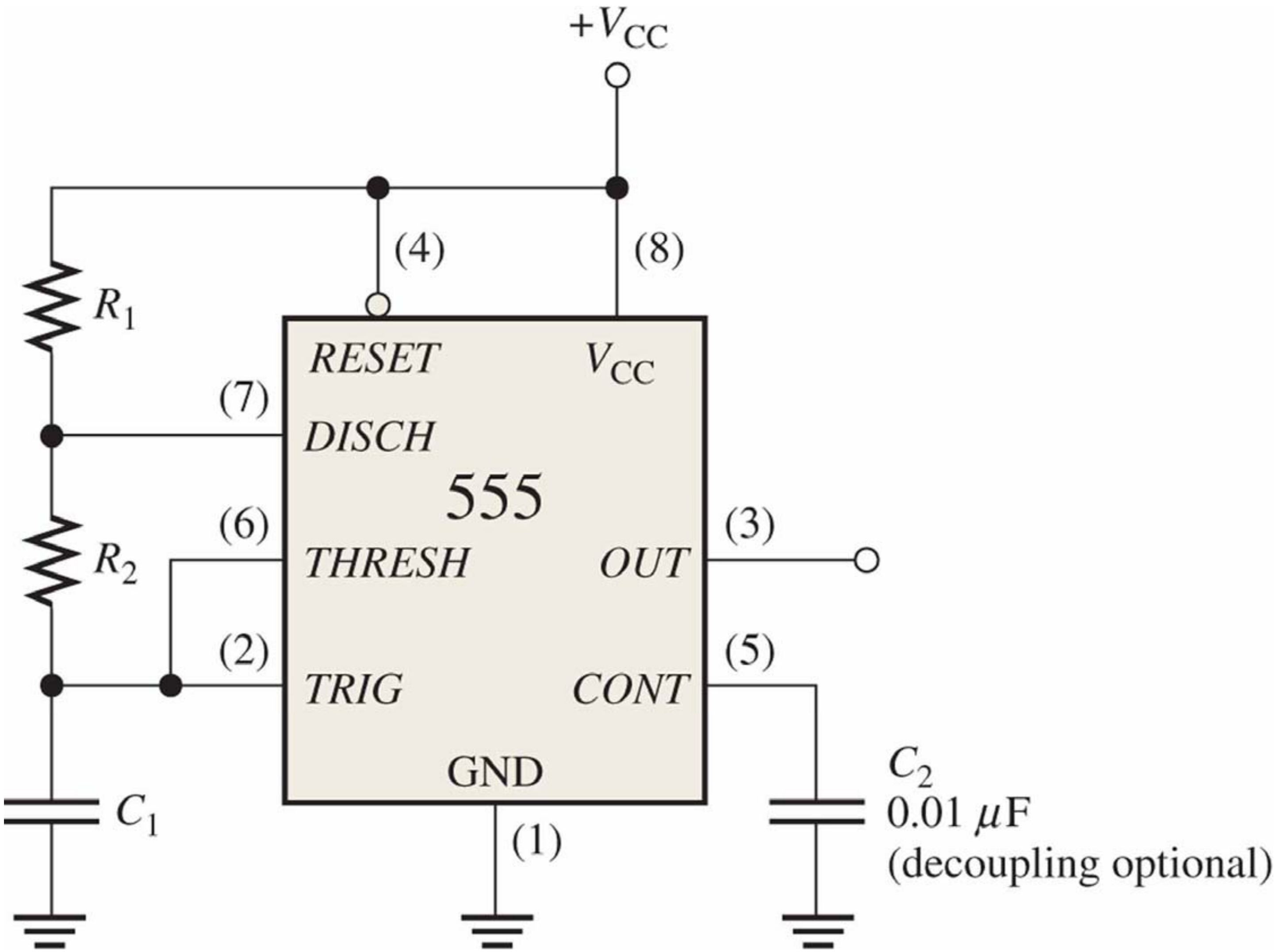
Note: if control voltage V_{CO} (PIN 5) is given, then

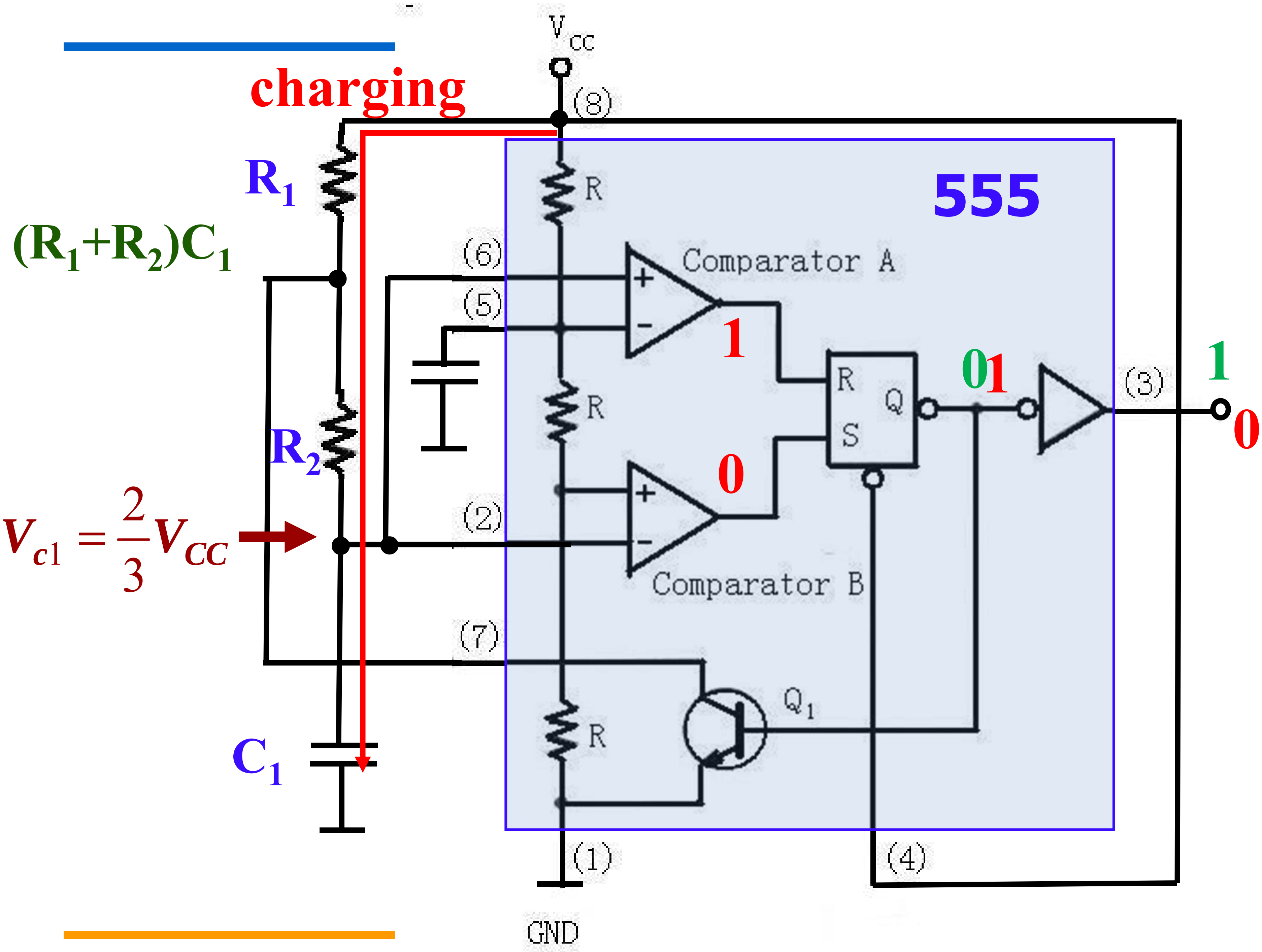
$U_{T+} = V_{CO}$ $\quad U_{T-} = 1/2V_{CO}$ $\quad \Delta U_{T-} = 1/2V_{CO}$

7.8 Astable Multivibrators
多谐振荡器

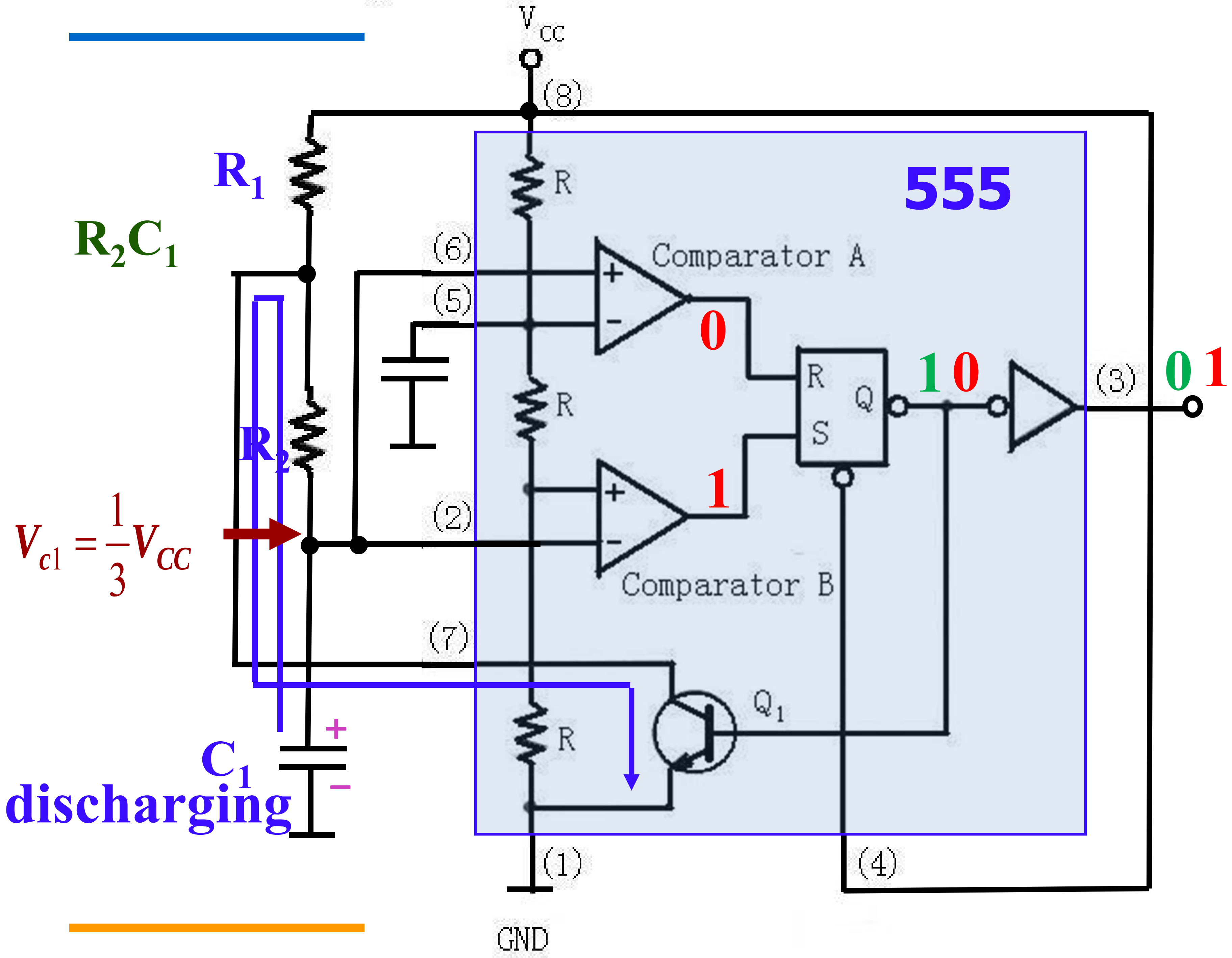
Astable multivibrator devices have no stable states, instead they ***continually switch*** between two unstable states. Consequently, they are used as ***oscillators*** to provide clock signals for timing purposes.

555 Astable Operation

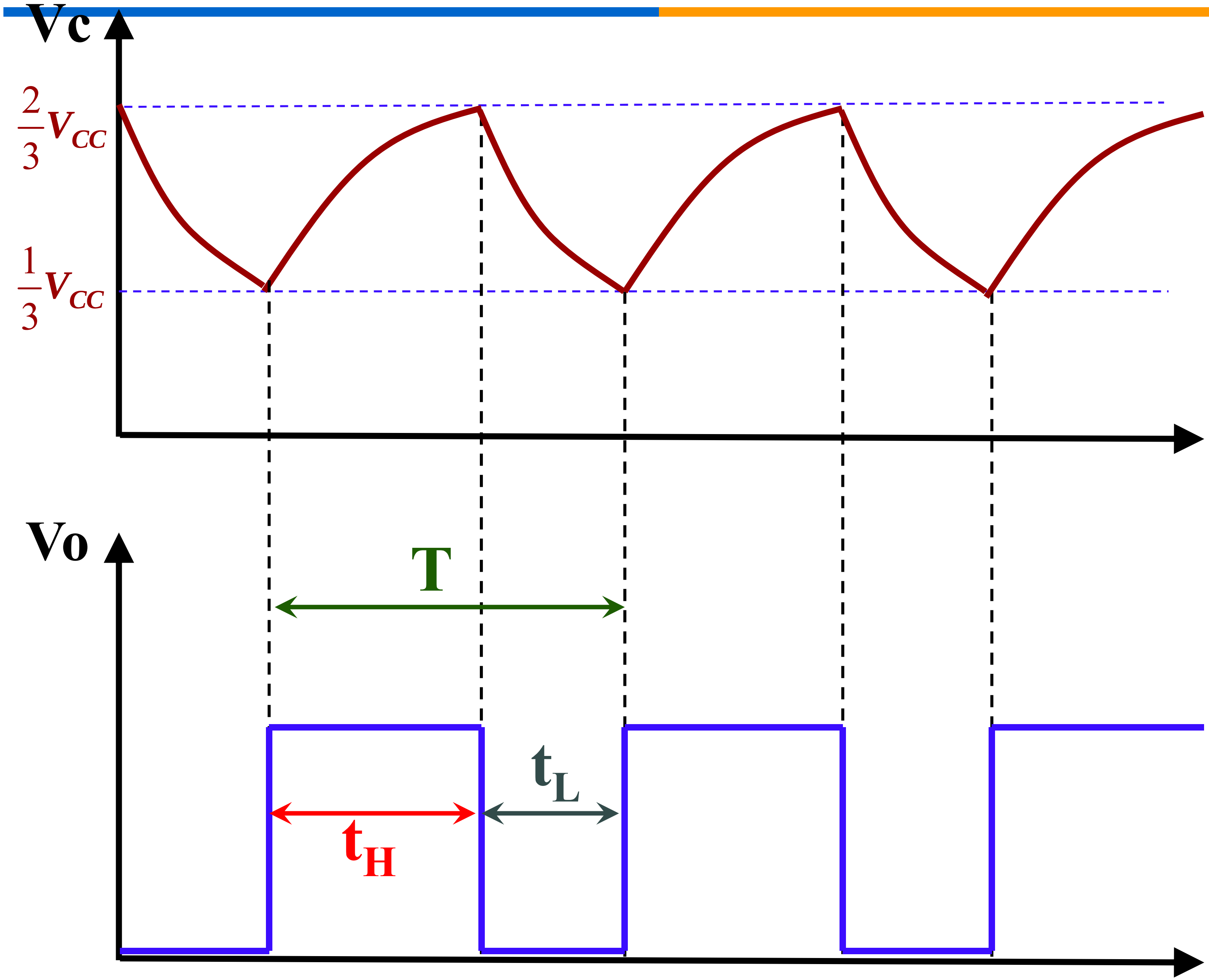




charging
V_{CC}
(8)
R_1
$(R_1+R_2)C_1$
555
R
(6)
Comparator A
(5)
1
R
Q
S
0
01
1
(3)
0
R_2
$V_{c1} = \frac{2}{3}V_{CC}$
(2)
Comparator B
(7)
Q_1
C_1
(1)
(4)
GND



$$V_{c1} = \frac{1}{3} V_{CC}$$


Vc
$\frac{2}{3}V_{CC}$
$\frac{1}{3}V_{CC}$
Vo
T
t_L
t_H

Calculation

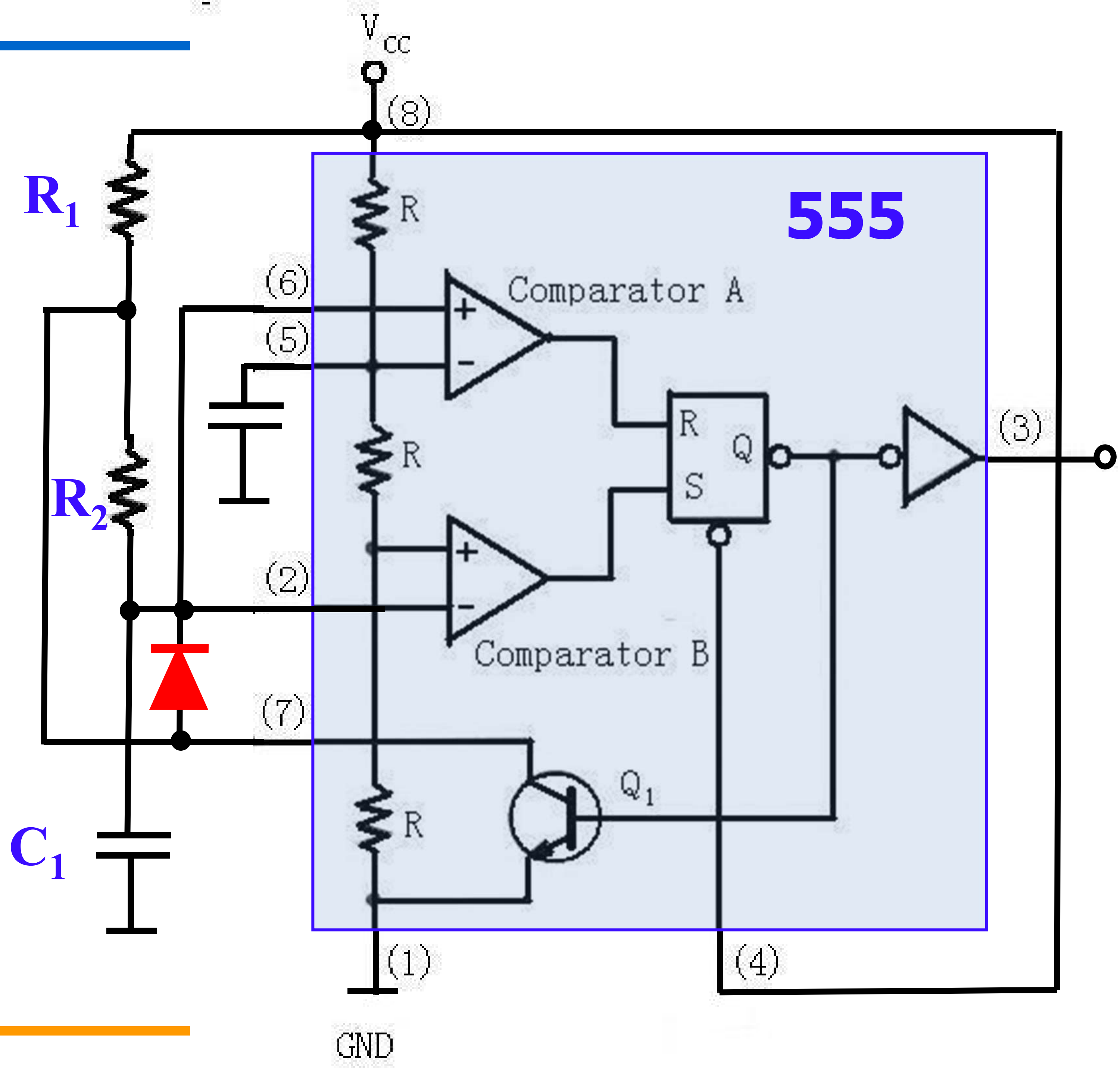
$$T = 0.7(R_1 + 2R_2)C_1$$

$$t_H = 0.7(R_1 + R_2)C_1$$

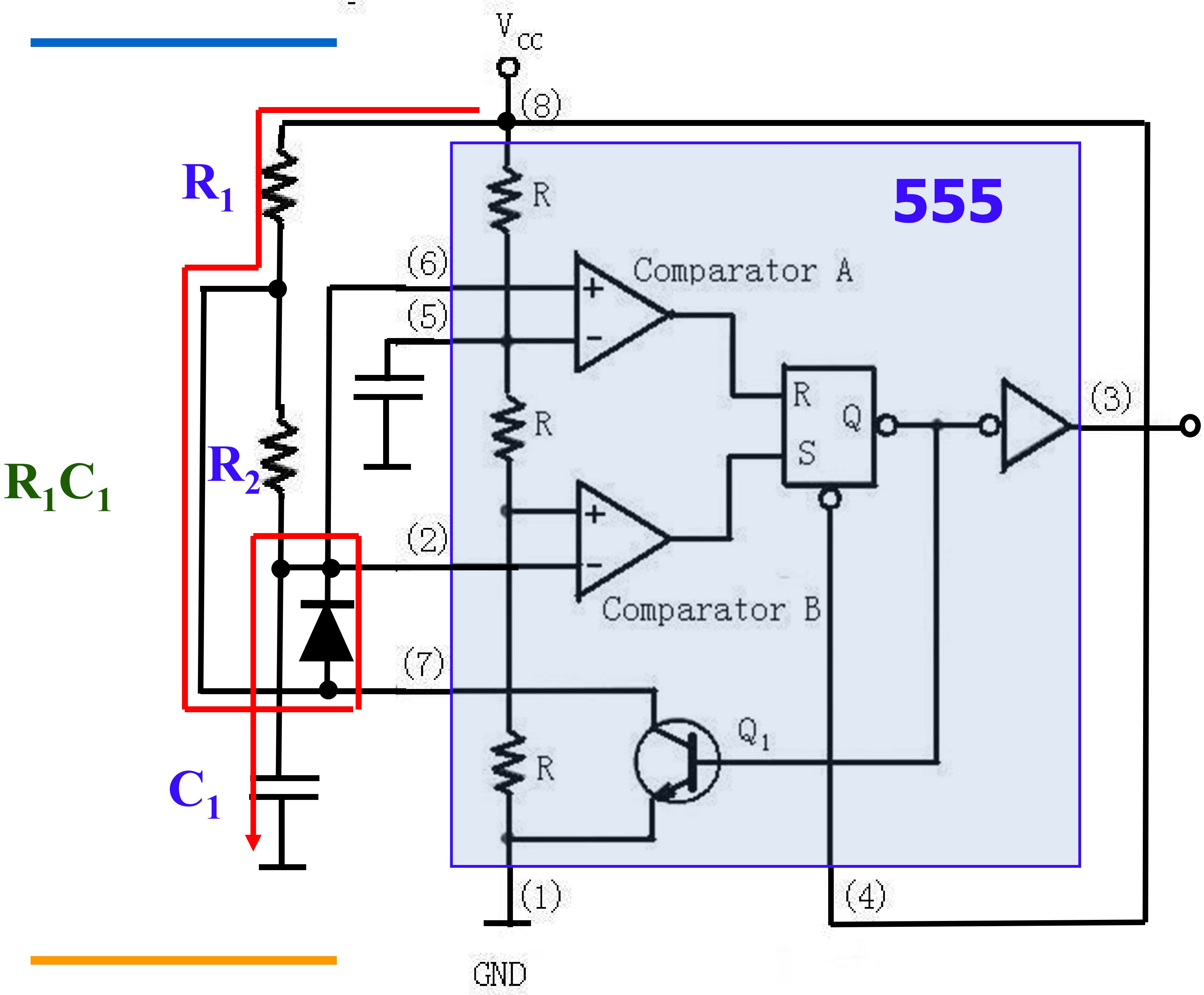
$$f = \frac{1.44}{(R_1 + 2R_2)C_1}$$

$$t_L = 0.7R_2C_1$$

$$Duty\ \ cycle = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100\%$$

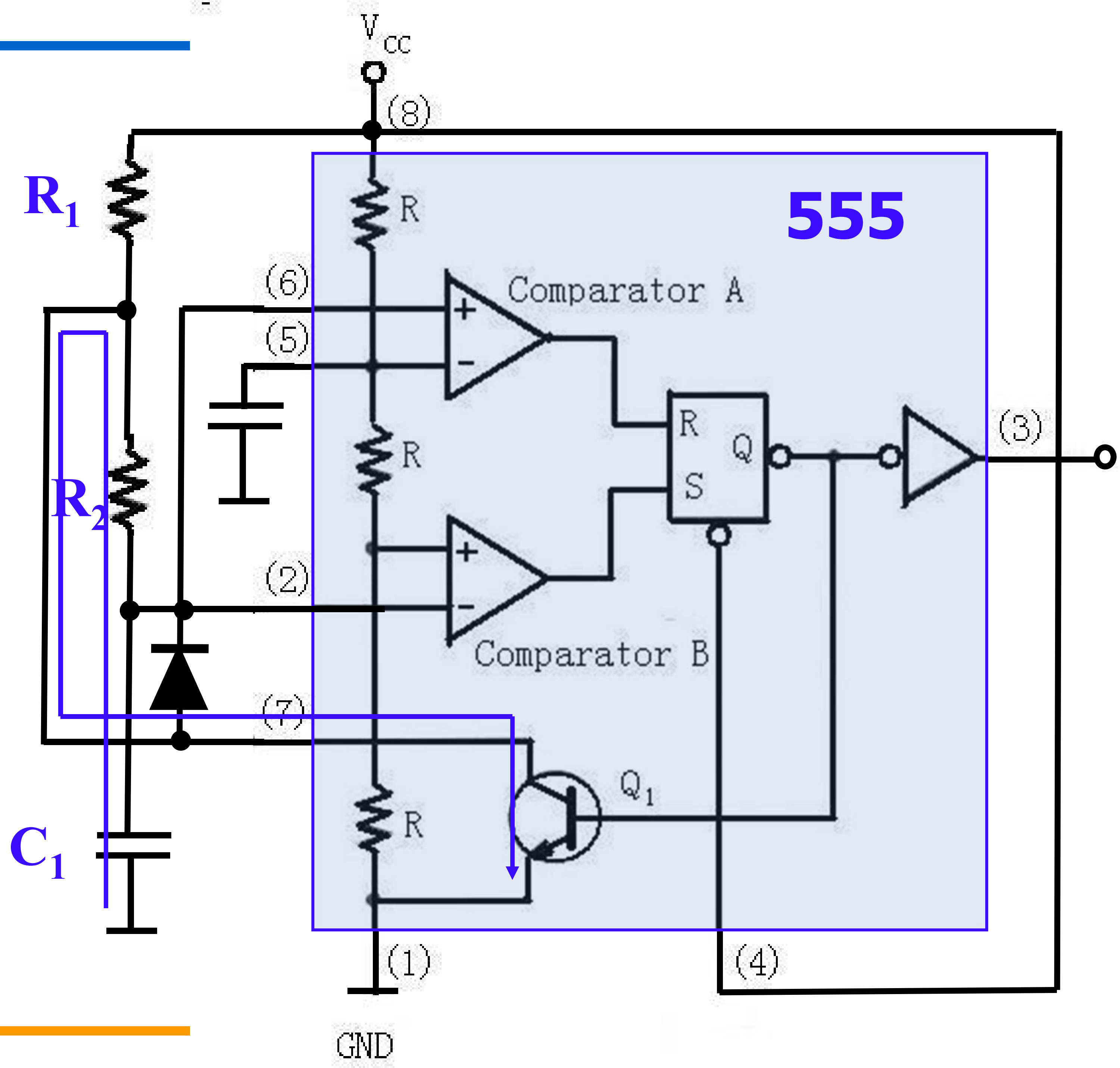


Vcc
(8)
R1
R
555
(6)
Comparator A
(5)
R
Q
S
R
R2
(2)
Comparator B
(7)
Q1
R
C1
(3)
(1)
(4)
GND



V_{CC}
(8)
R_1
555
R
(6)
Comparator A
(5)
R_1C_1
R_2
R
R
Q
S
(3)
(2)
Comparator B
(7)
Q_1
R
C_1
(1)
(4)
GND

R_2C_1



Vcc
(8)
R1
R
555
(6)
Comparator A
(5)
R
Q
S
(3)
R2
R
(2)
Comparator B
(7)
Q1
R
C1
(1)
(4)
GND

Calculation

$$T = 0.7(R_1 + R_2)C_1$$

$$t_H = 0.7R_1C_1$$

$$f = \frac{1.44}{(R_1 + R_2)C_1}$$

$$t_L = 0.7R_2C_1$$

$$Duty\ \ cycle = \frac{R_1}{R_1 + R_2} \times 100\%$$

Homework: Exercise (需要画出电路图和设计公式)

A circuit need a 1Hz clock signal with a duty cycle of 2/3. $R1=40k\Omega$, $C=10\mu F$. Determine the value of R2.

(1) Using the first connection of 555 timer.

(2) Using the second connection of 555 timer.

Quiz

1. The output of a D latch will not change if

   a. the output is LOW

   b. Enable is not active

   c. D is LOW

   d. all of the above

Quiz

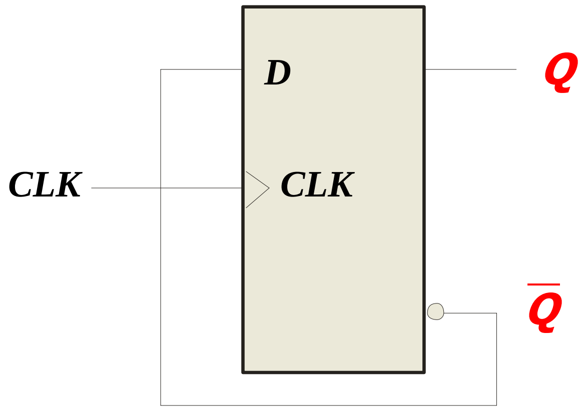
2. The D flip-flop shown will

   a. set on the next clock pulse

   b. reset on the next clock pulse

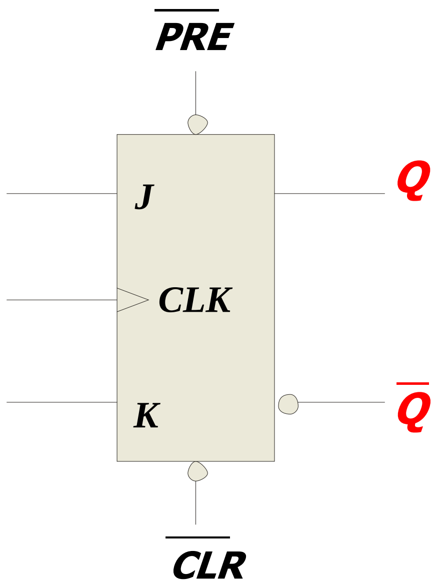
   c. latch on the next clock pulse

   d. toggle on the next clock pulse



Quiz

3. For the J-K flip-flop shown, the number of inputs that are asynchronous is



a. 1

b. 2

c. 3

d. 4

Quiz

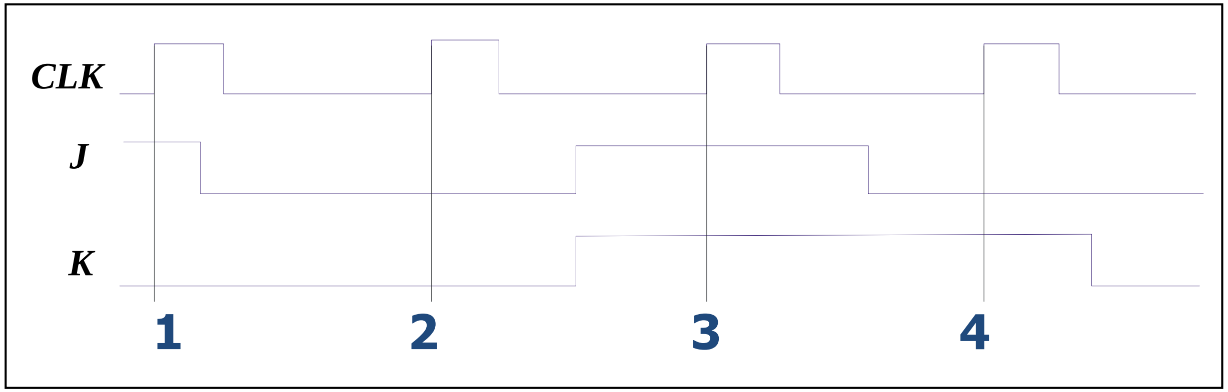
4. Assume the output is initially HIGH on a leading edge triggered J-K flip flop. For the inputs shown, the output will go from HIGH to LOW on which clock pulse?

a. 1

b. 2

c. 3

d. 4



Quiz

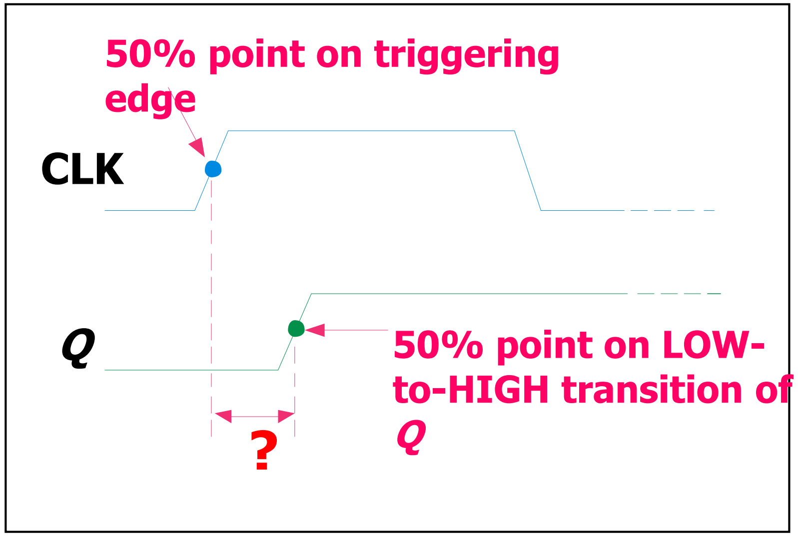
5. The time interval illustrated is called

a. t_{PHL}

b. t_{PLH}

c. set-up time

d. hold time



Quiz

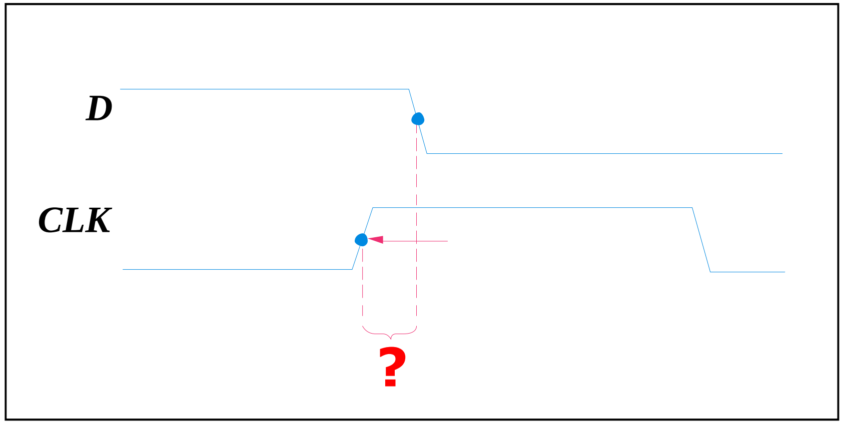
6. The time interval illustrated is called

a. t_{PHL}

b. t_{PLH}

c. set-up time

d. hold time



Quiz

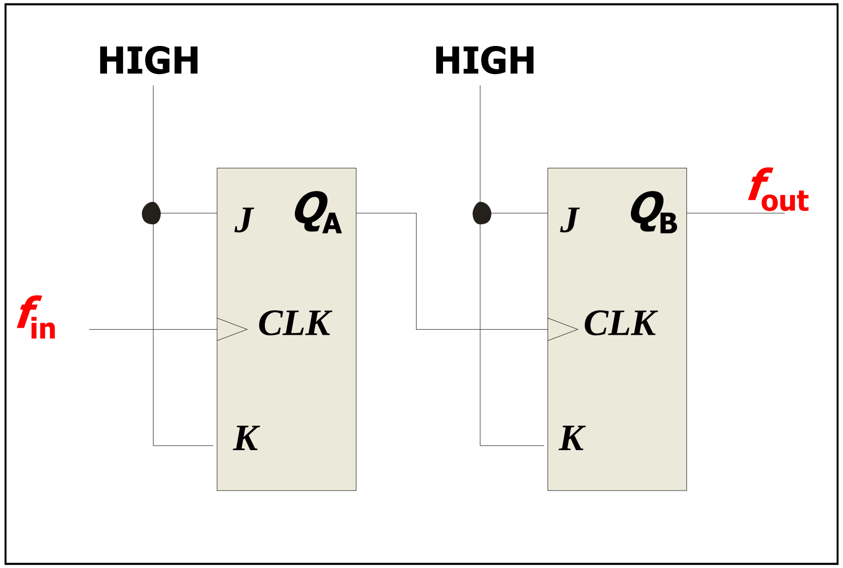
7. The application illustrated is a

   a. astable multivibrator

   b. data storage device

   c. frequency multiplier

   d. frequency divider



Quiz

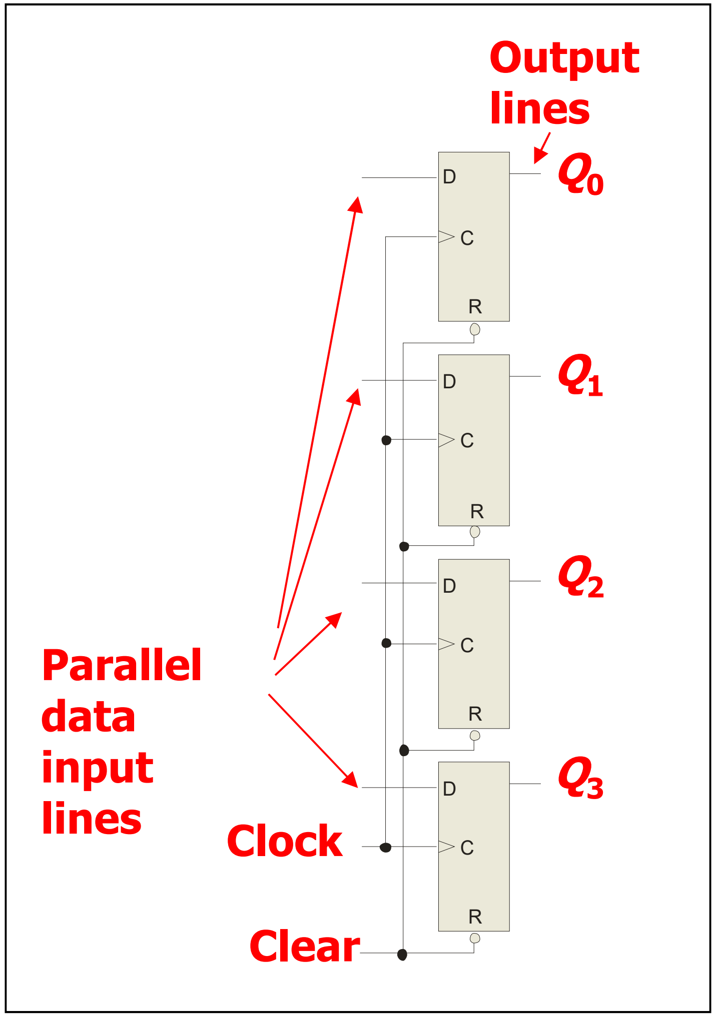
8. The application illustrated is a

a. astable multivibrator

b. data storage device

c. frequency multiplier

d. frequency divider



Quiz

9. A retriggerable one-shot with an active HIGH output has a pulse width of 20 ms and is triggered from a 60 Hz line. The output will be a

a. series of 16.7 ms pulses

b. series of 20 ms pulses

c. constant LOW

d. constant HIGH

Quiz

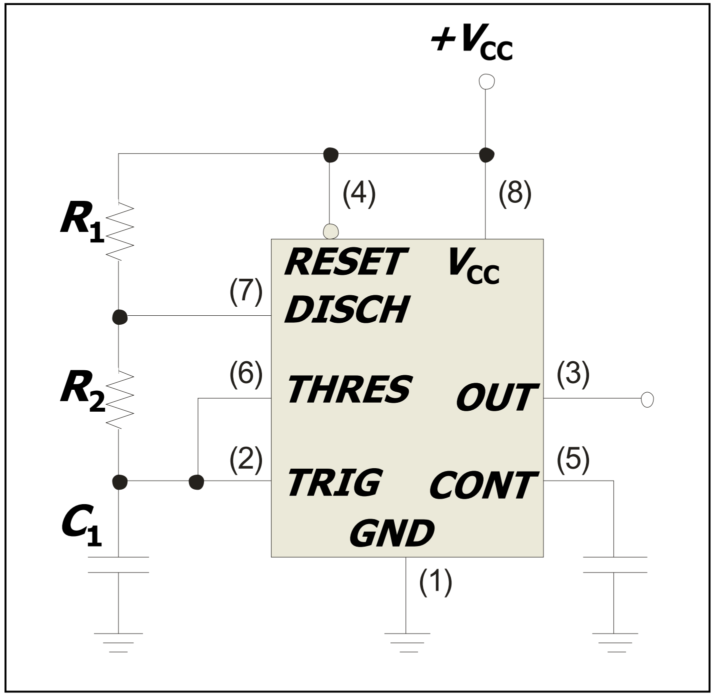
10. The circuit illustrated is a

a. astable multivibrator

b. monostable multivibrator

c. frequency multiplier

d. frequency divider



Homework

- Problems: 1, 2， 6， 7， 12， 16， 25， 29， 31
- Exc1. To achieve a one-shot with a pulse width of approximately 10ms, using a 74121. If select REXT=20KΩ, calculate the capacitance: CEXT=?
- Exc2. A circuit need a 1Hz clock signal with a duty cycle of 2/3. R1=40kΩ, C=10μF. Determine the value of R2.

  (1) Using the first connection of 555 timer.

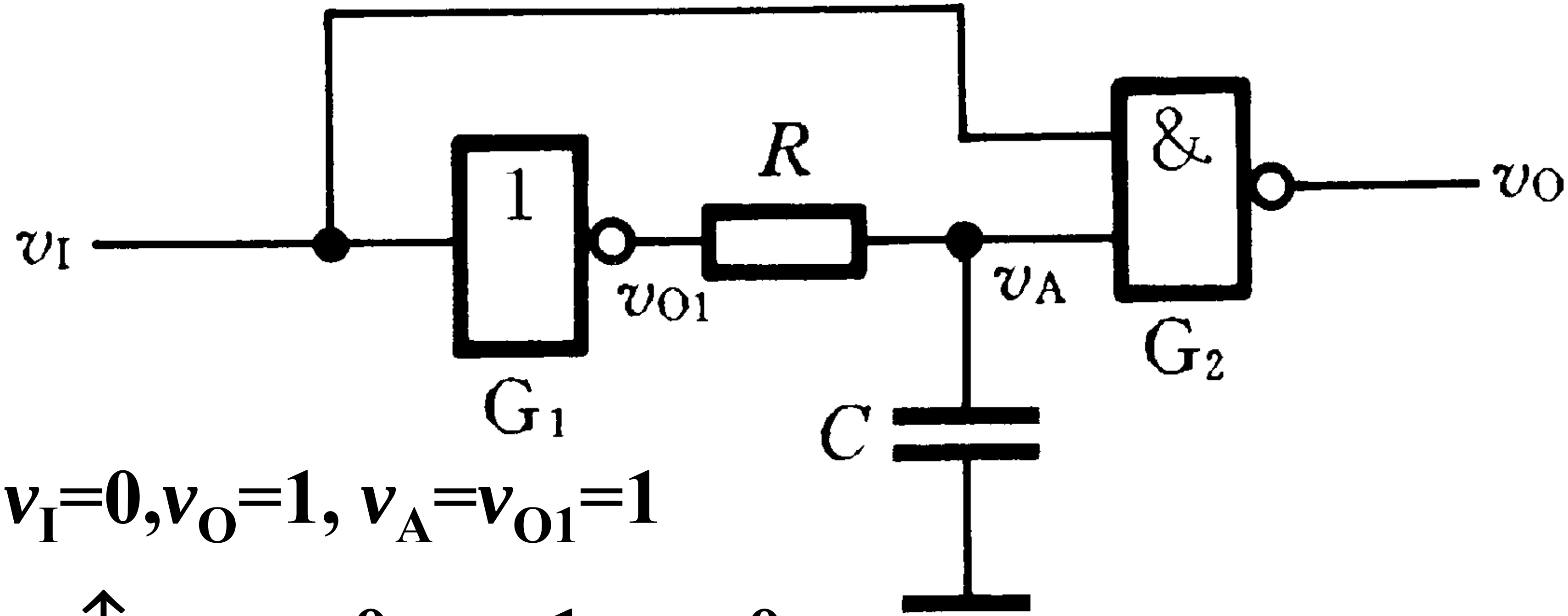
  (2) Using the second connection of 555 timer.

  (需要画出电路图和设计公式)

Answers

1. b	6. d
2. d	7. d
3. b	8. b
4. c	9. d
5. b	10. a

RC Integrator One-Shot



v_I=0,v_O=1, v_A=v_{O1}=1

$v_I\uparrow \rightarrow v_{O1}=0,\ v_A=1,\ v_O=0$

$v_C\downarrow \rightarrow v_{I2}\downarrow \rightarrow v_O\uparrow \rightarrow v_{O1}\uparrow$