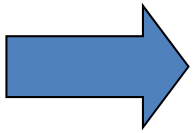
Chapter 7 Flip-Flops and Related Devices

触发器以及相关设备

- Logic circuits
  - Combinational Circuits（组合电路）
  - Sequential Circuits（时序电路）

Basic Block  Flip-Flops

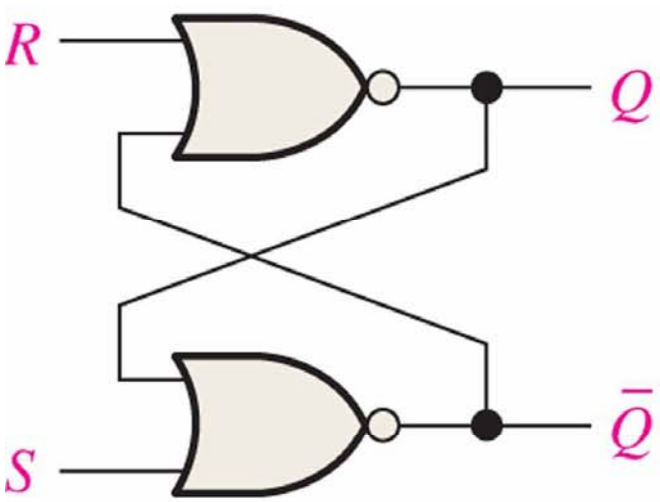
- ***Objectives***
  - Latches（锁存器）
  - Edge-triggered Flip-Flops（边沿触发器）
    - S-R FF
    - D FF
    - J-K FF
    - T FF

7.1 Latches（锁存器）

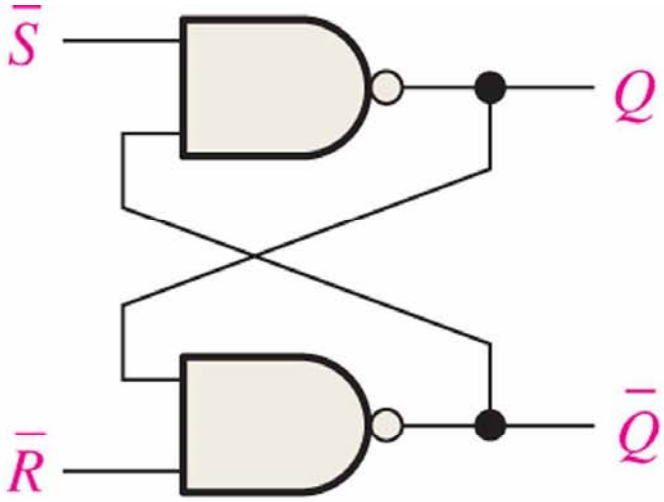
- The ***latch*** is a type of temporary device that has two stable states (***bistable***) and is normally placed in a category separate from that of ***flip-flops***.
- The difference between latches and flip-flops is the method used for changing their states.

- *Latches*
  - S-R (Set-Reset) Latch (SR锁存器)
  - Gated S-R Latch (门控锁存器)
  - Gated D (Data) Latch

7.1.1 S-R (Set-Reset) Latch

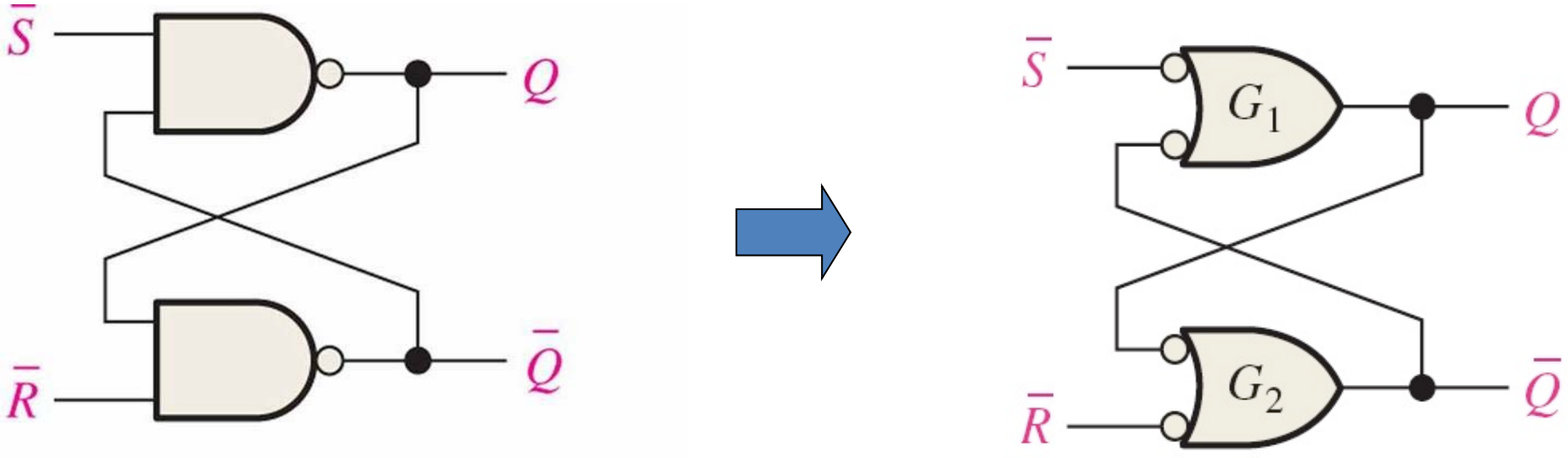


(a) Active-HIGH input S-R latch

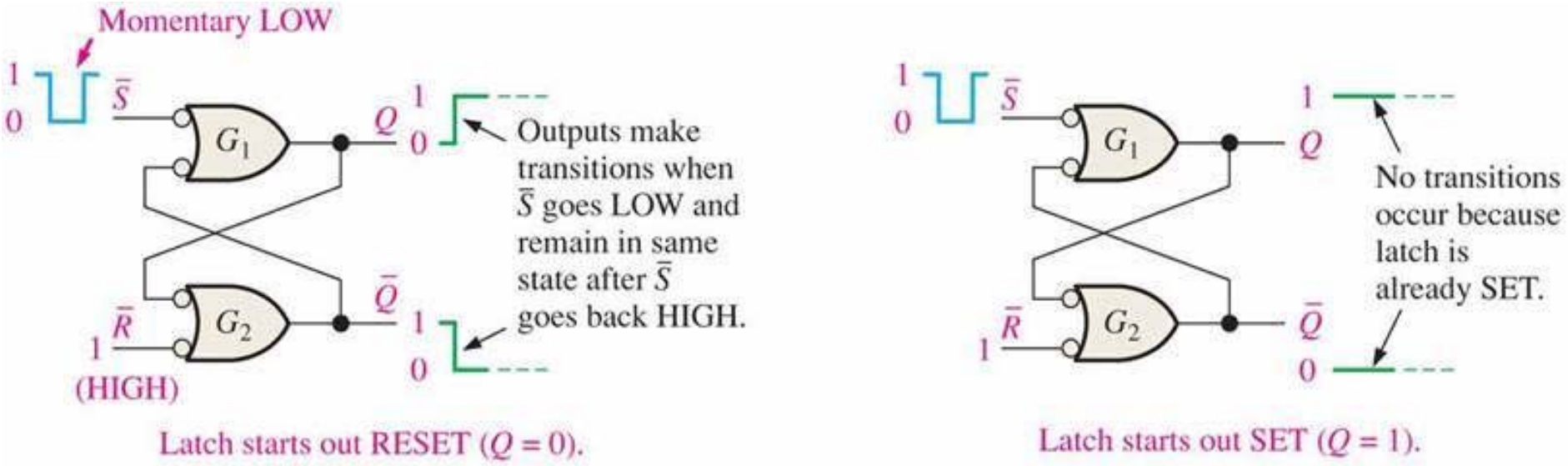


(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

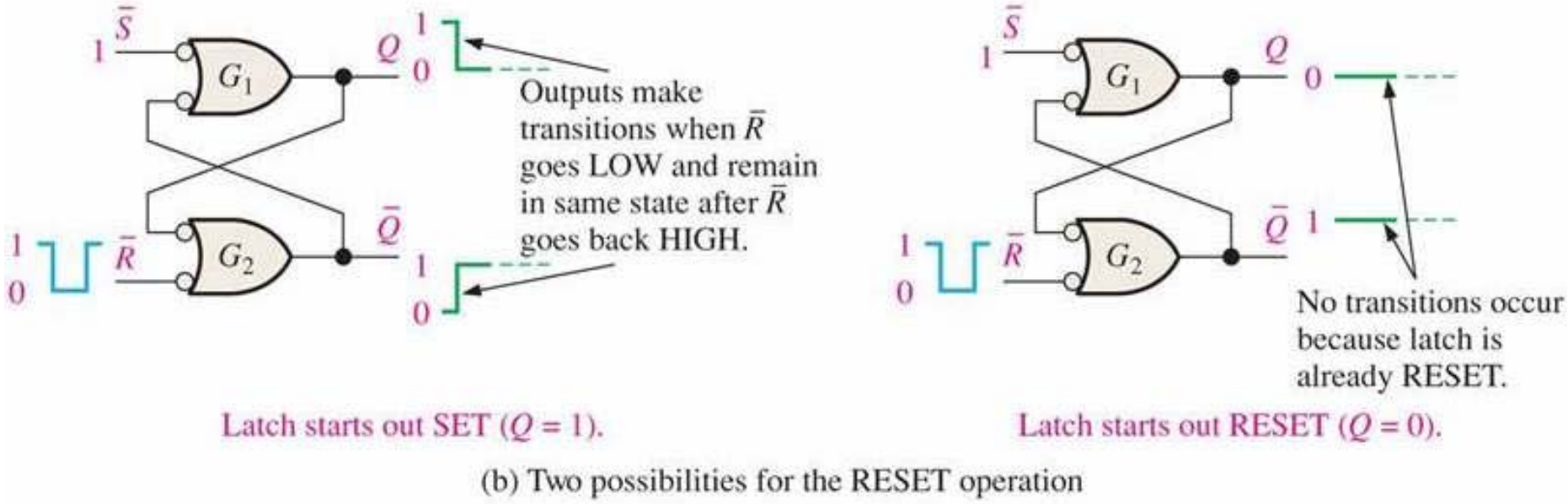
Active-LOW input S-R latch



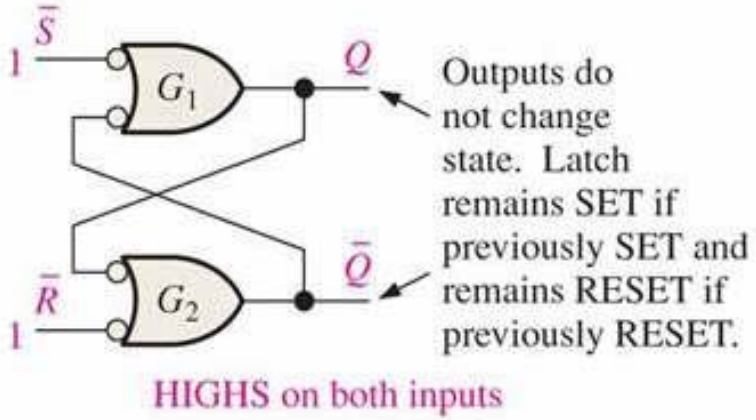
(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch



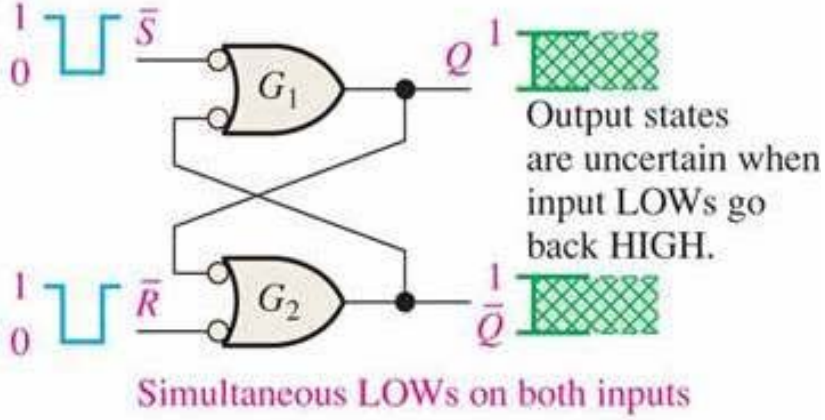
(a) Two possibilities for the SET operation



(b) Two possibilities for the RESET operation



(c) No-change condition

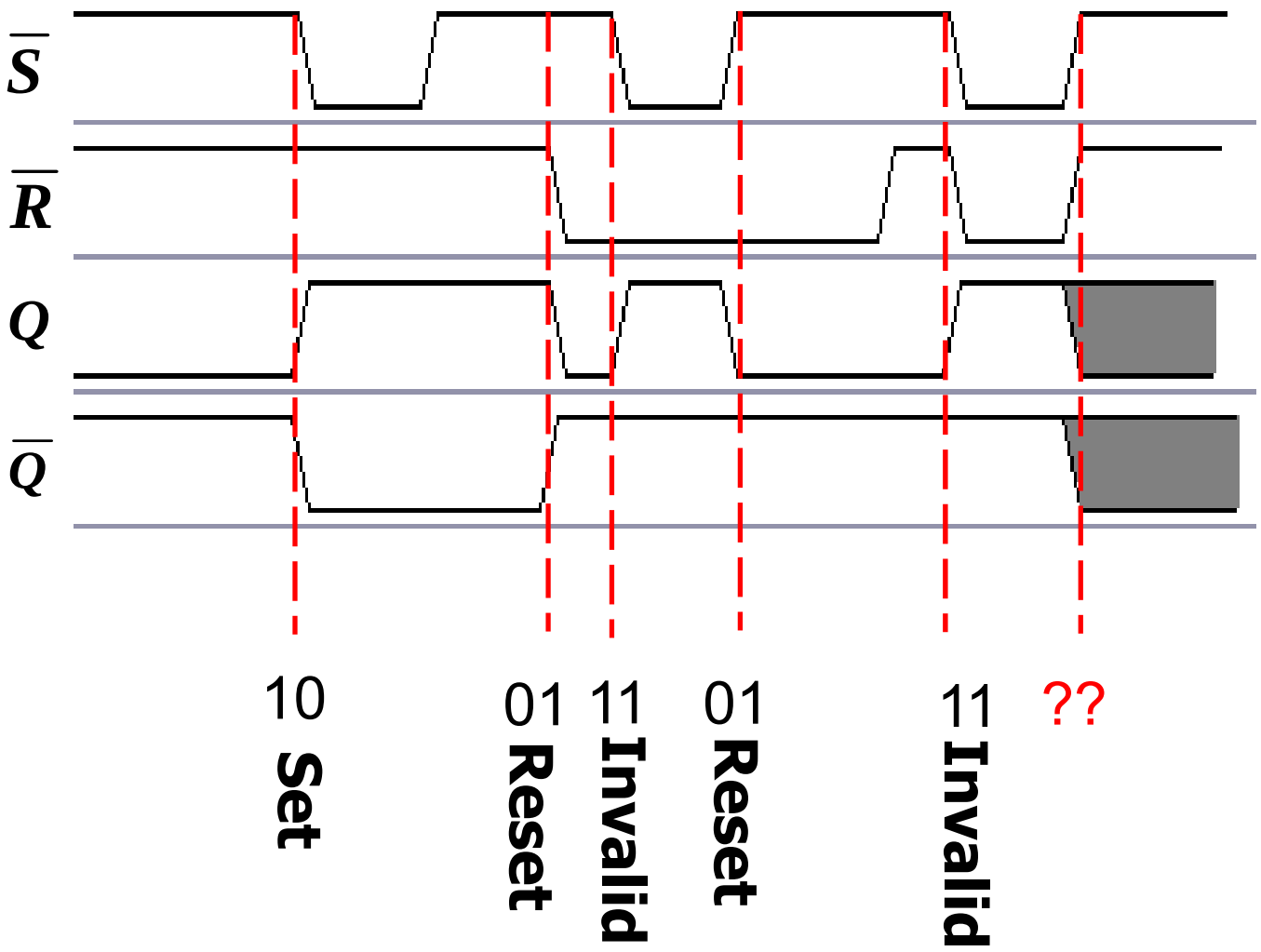


(d) Invalid condition

Truth Table（真值表）

Inputs		Outputs		Comments
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1*	1*	Invalid condition

Timing diagram



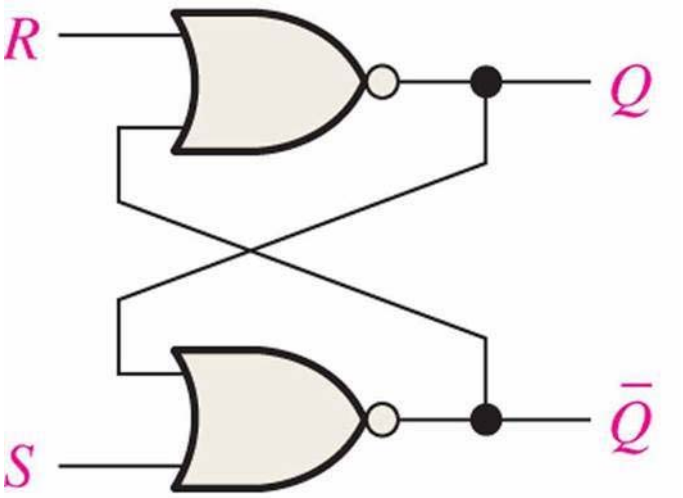
Memory Function

$S=1;\ R=0;\begin{cases} Q=0 \\ \overline{Q}=1 \end{cases}$ “0”, remember “0”

$S=0;\ R=1;\begin{cases} Q=1 \\ \overline{Q}=0 \end{cases}$ “1”, remember “1”

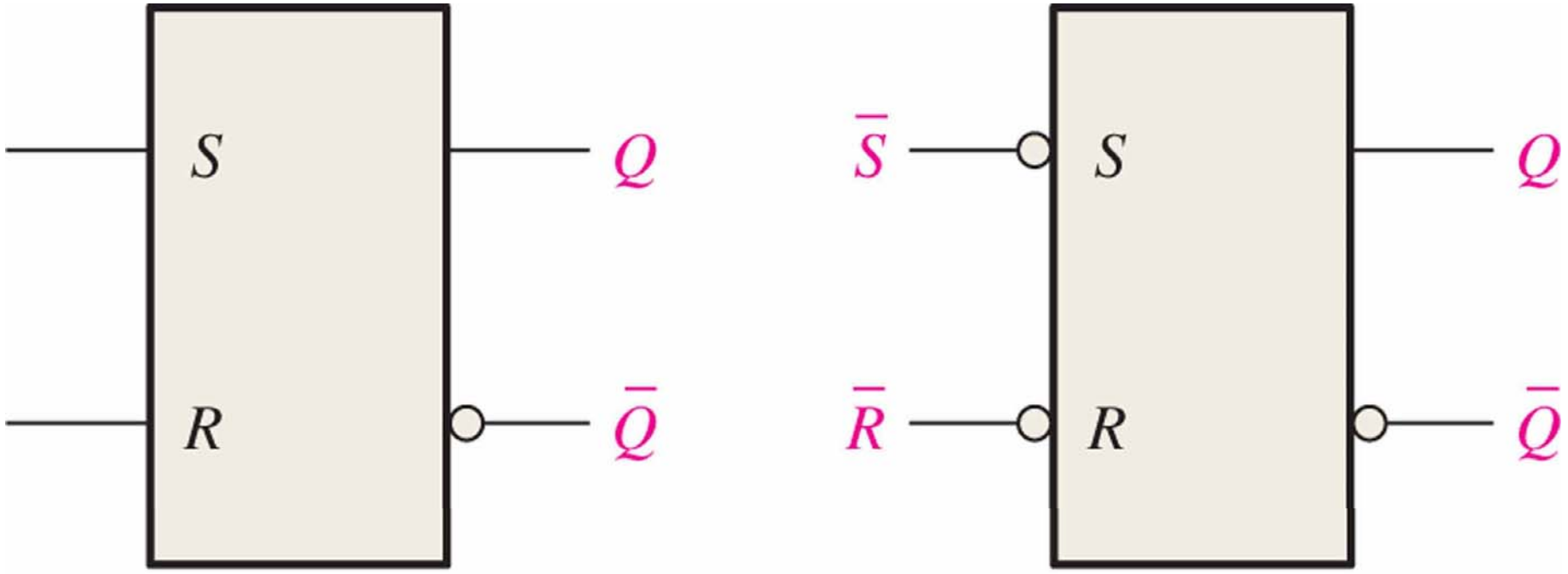
Bi-stable ⇒ **Used to store 1 bit binary number**

Active-HIGH input S-R latch



R	S	Q	$\bar{Q}$
0	0	Q_0	$\bar{Q}_0$
0	1	1	0
1	0	0	1
1	1	0^*	0^*

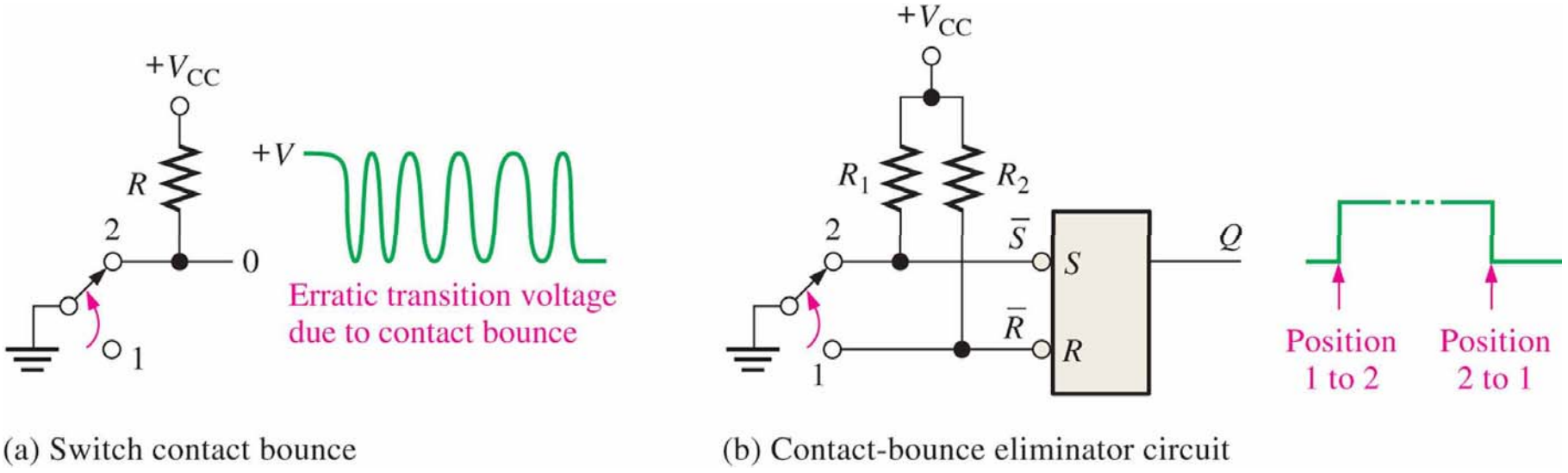
Logic Symbol



(a) Active-HIGH input S-R latch

(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

Application Example



(a) Switch contact bounce

(b) Contact-bounce eliminator circuit

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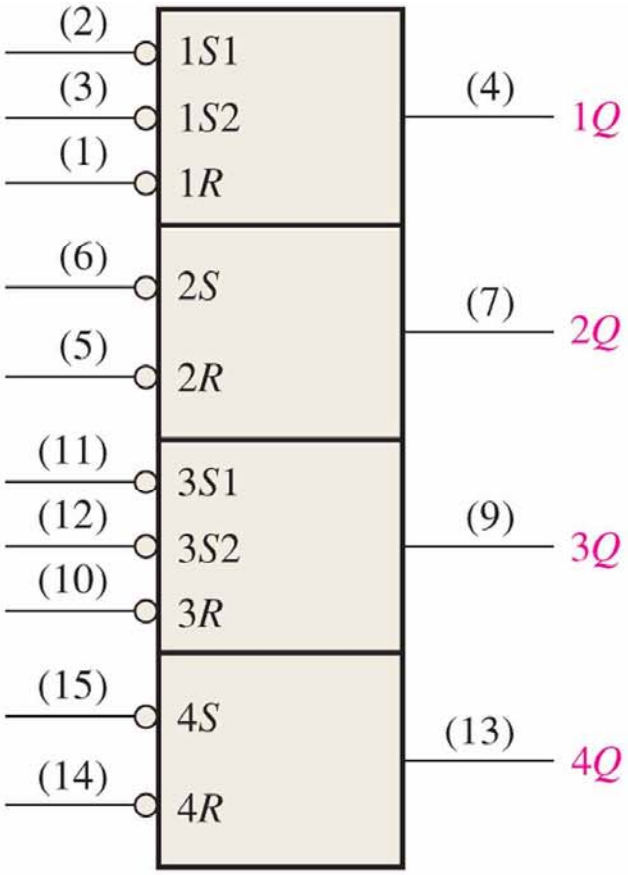
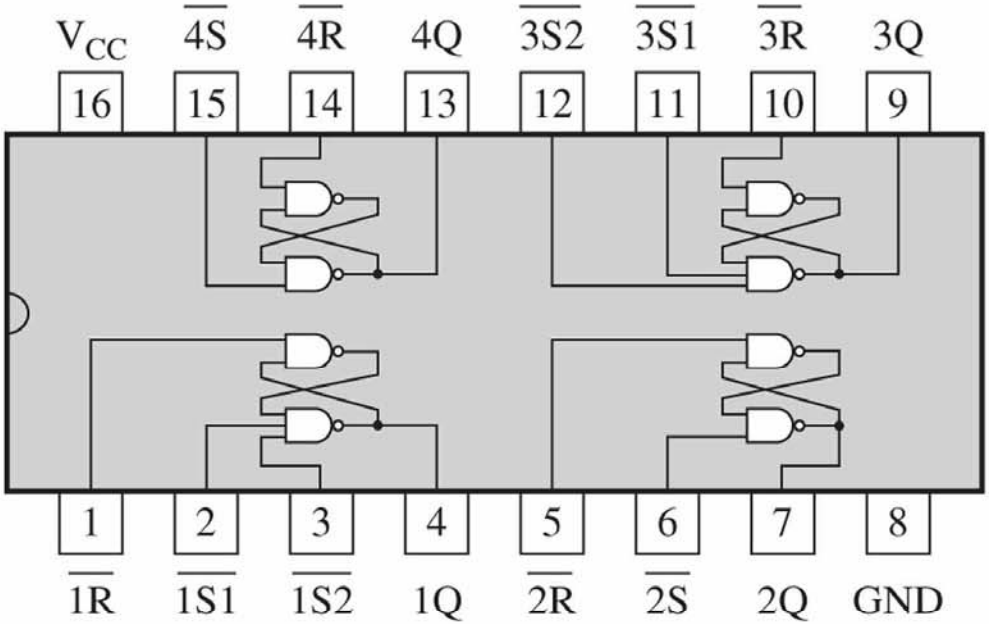


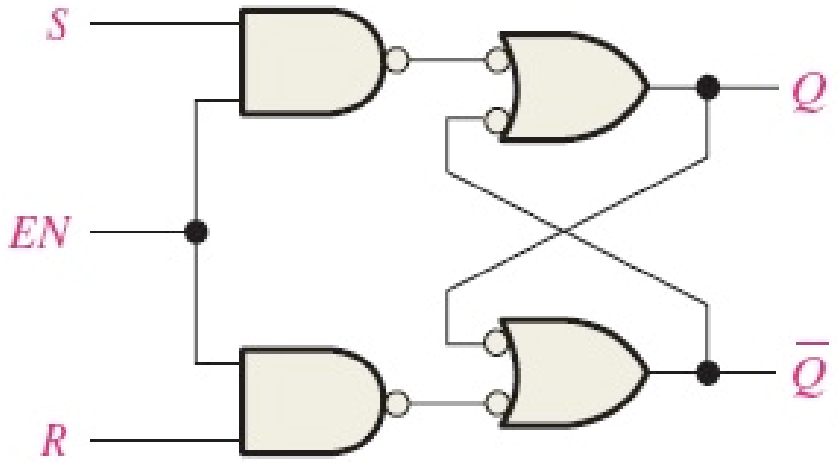
(a) Logic diagram



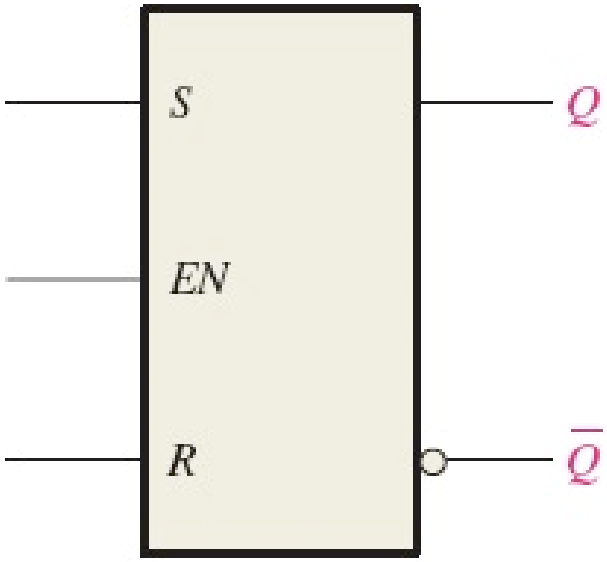
(b) Pin diagram

7.1.2 The Gated S-R Latch（门控S-R锁存器）

EN: control the time when the inputs S and R can control the output. (Level-triggered)

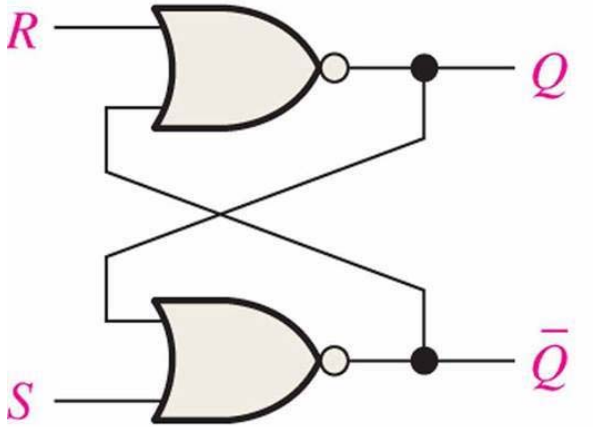


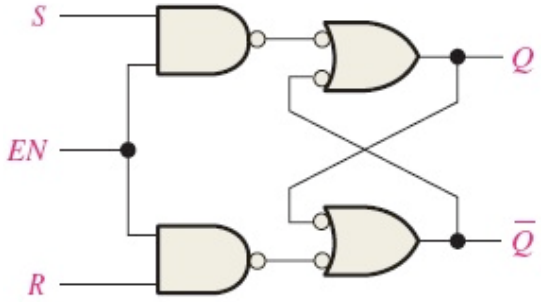
(a) Logic diagram



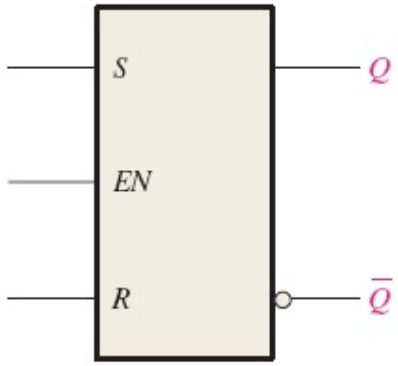
(b) Logic symbol

Comparison





(a) Logic diagram



(b) Logic symbol

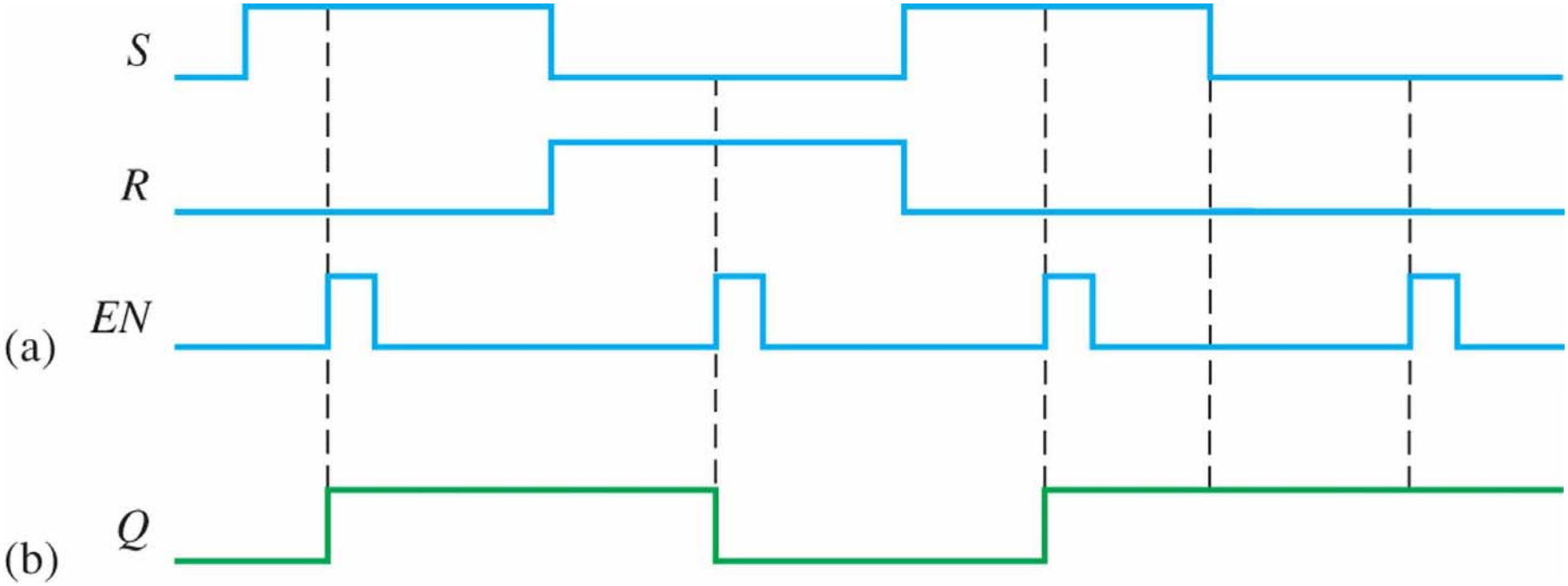
R	S	Q	$\overline{Q}$
0	0	Q_0	$\overline{Q_0}$
0	1	1	0
1	0	0	1
1	1	1^*	1^*

?

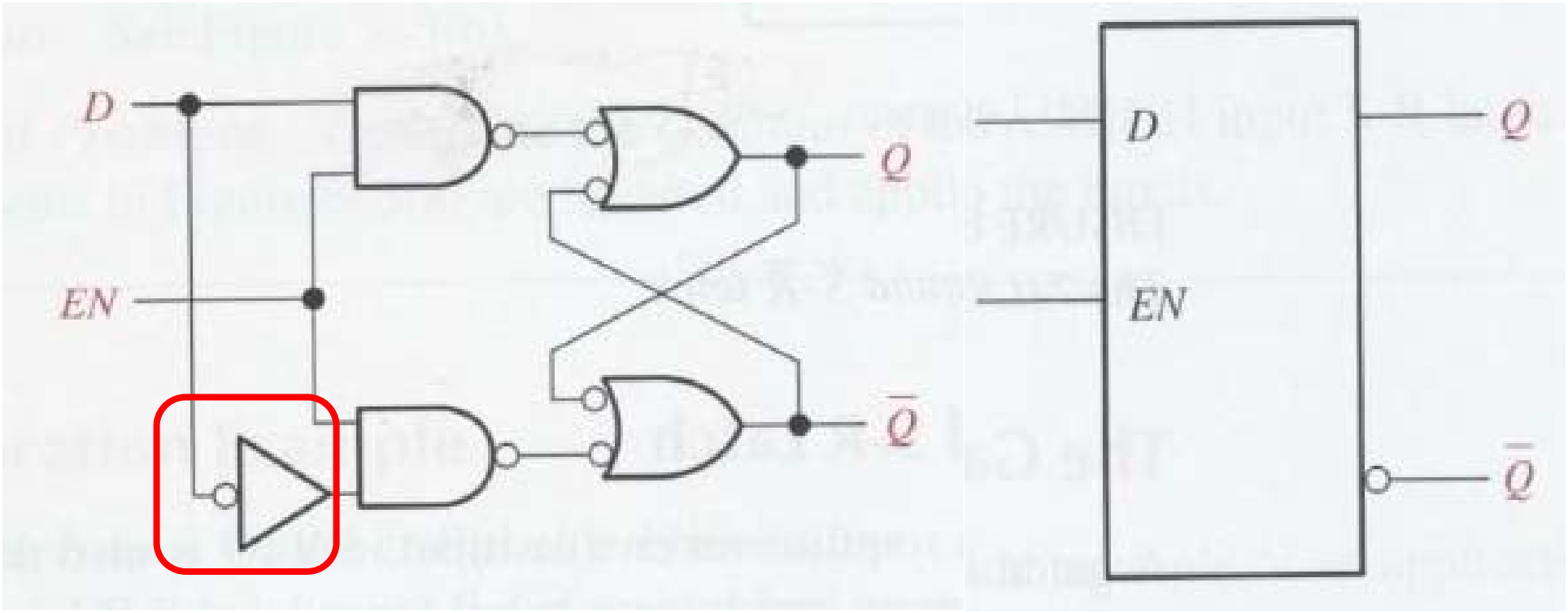
E	R	S	Q	$\overline{Q}$
0	X	X	Q_0	$\overline{Q_0}$
1	0	0	Q_0	$\overline{Q_0}$
1	0	1	1	0
1	1	0	0	1
1	1	1	1^*	1^*

?

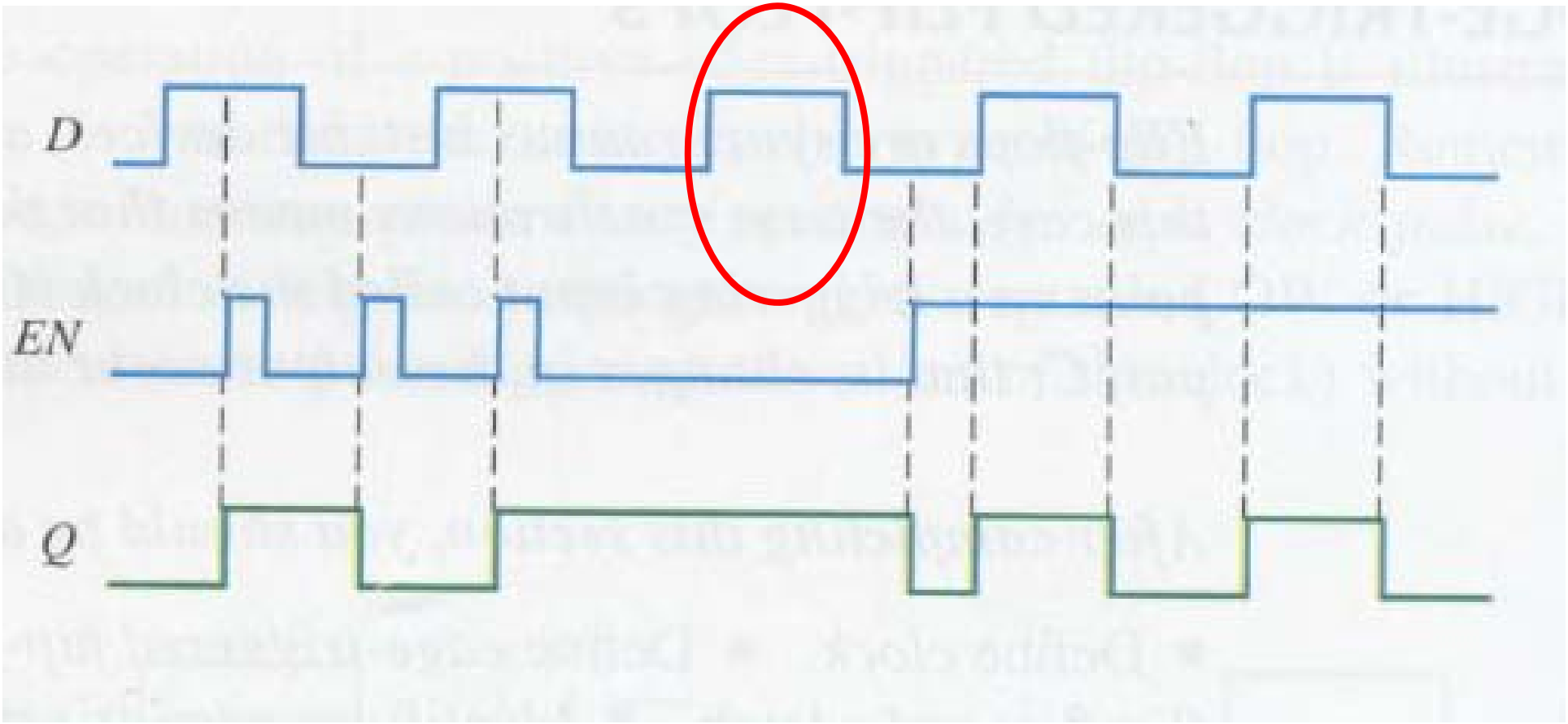
Gated S-R Latch Waveform



7.1.3 The Gated D Latch



Gated D Latch Waveform



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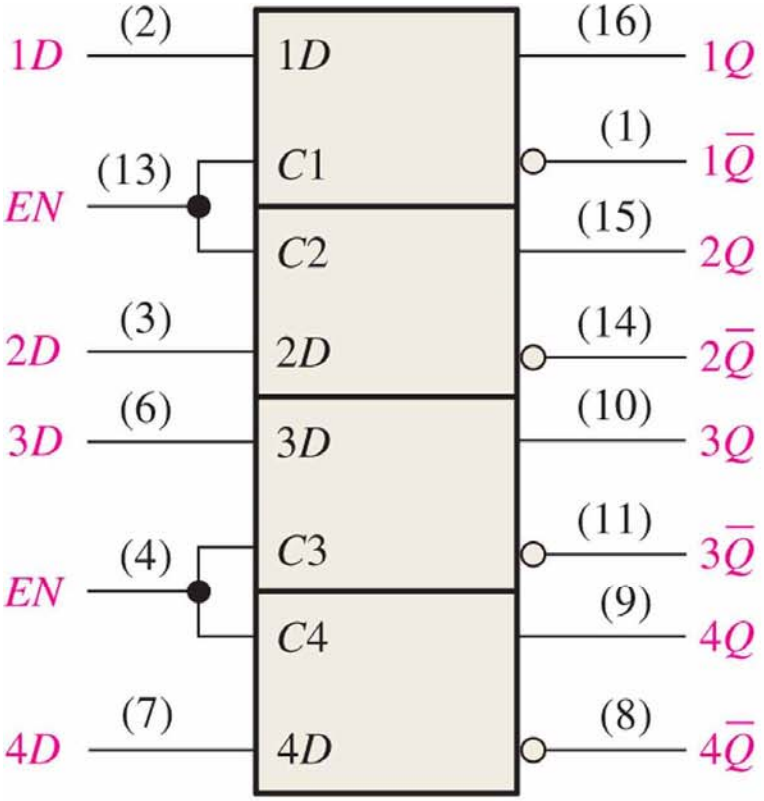

(a) Logic symbol

INPUTS		OUTPUTS		
D	*EN*	*Q*	$\overline{Q}$	COMMENTS
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\overline{Q}_0$	No change

Note: Q_0 is the prior output level before the indicated input conditions were established.

(b) Truth table (each latch)

Application example: Latches for temporary data storage