Chapter 5
Combinational Logic

组合逻辑

Logic circuit

Combinational Logic circuit

(组合逻辑电路：任意时刻的输出仅取决于该时刻的输入，与电路原来的状态无关)

Sequential Logic circuit

(时序逻辑电路：任意时刻的输出取决于该时刻的输入信号以及电路原来的状态)

5.1 Basic Combinational Circuits

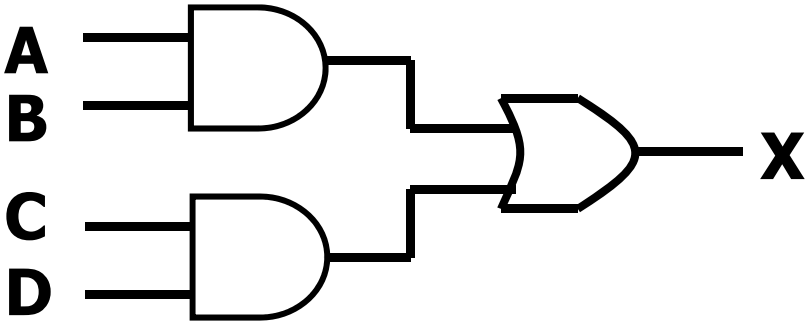
- AND-OR（与-或电路/SOP电路）
- AND-OR-Invert（与-或-非电路/POS电路）
- XOR（异或电路）
- XNOR（同或电路）
- NAND （与非门）
- NOR （或非门）

1 AND-OR Logic

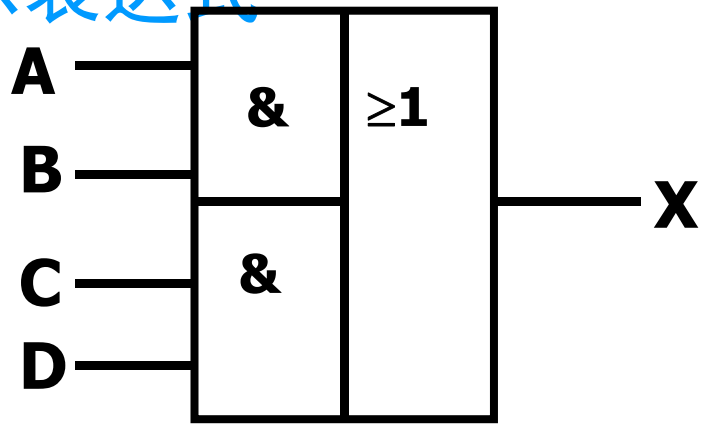
X=AB+CD

An AND-OR circuit directly implements SOP expression, assuming the complements of the variables are available.

与或电路直接实现了SOP的布尔表达式



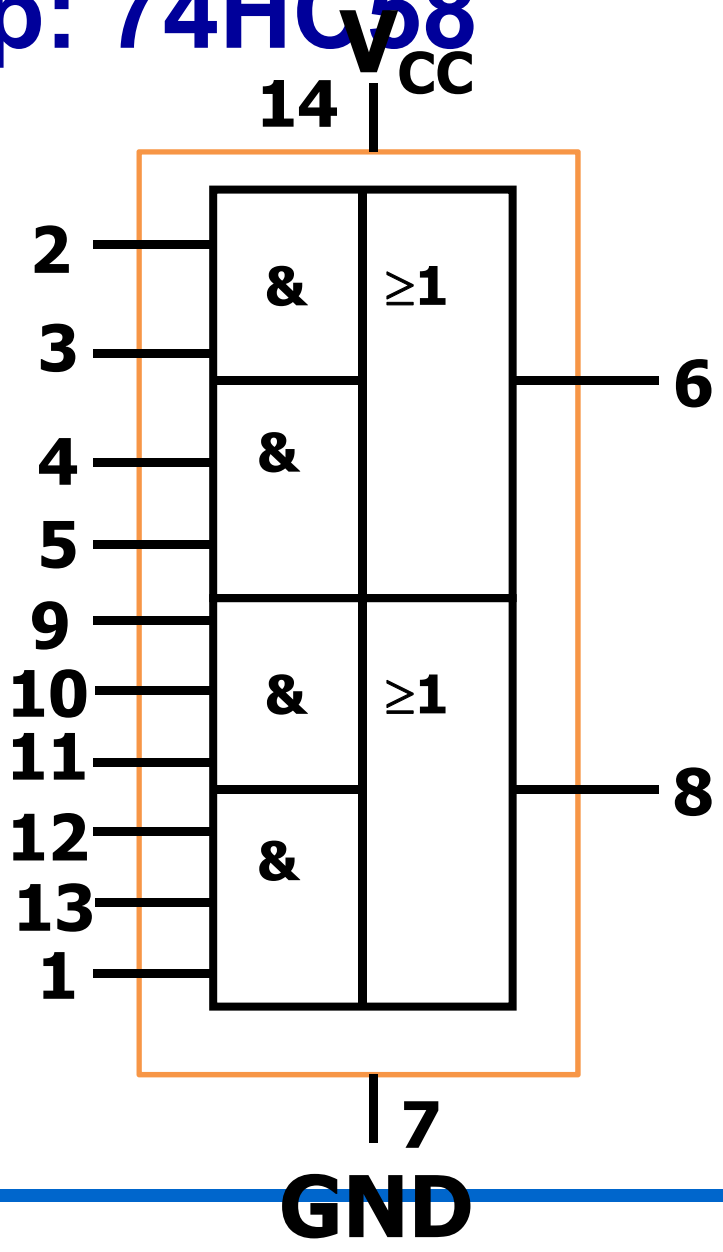
ANSI standard distinctive shape symbols



ANSI standard rectangular outline symbols

Example chip: 74HC58

- 74HC58 (CMOS): dual AND-OR
  - 1 two inputs AND-OR.
  - 1 three inputs AND-OR

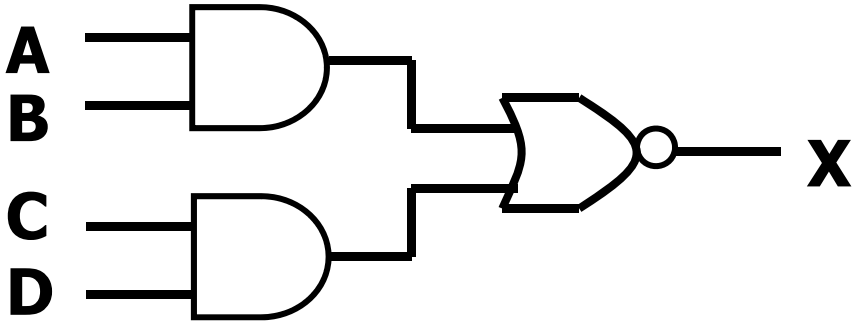


2 AND-OR-Invert Logic

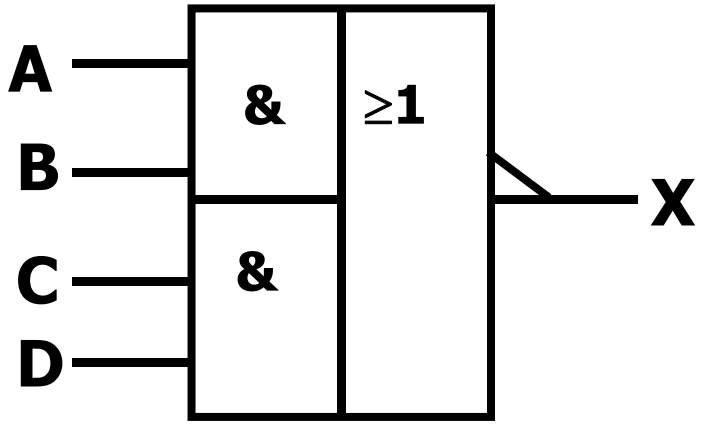
$$X = \overline{AB + CD} = (\overline{A} + \overline{B})(\overline{C} + \overline{D})$$

An AND-OR-Invert can be used to implement ***POS*** expression.

与或非电路直接实现了POS形式的布尔表达式



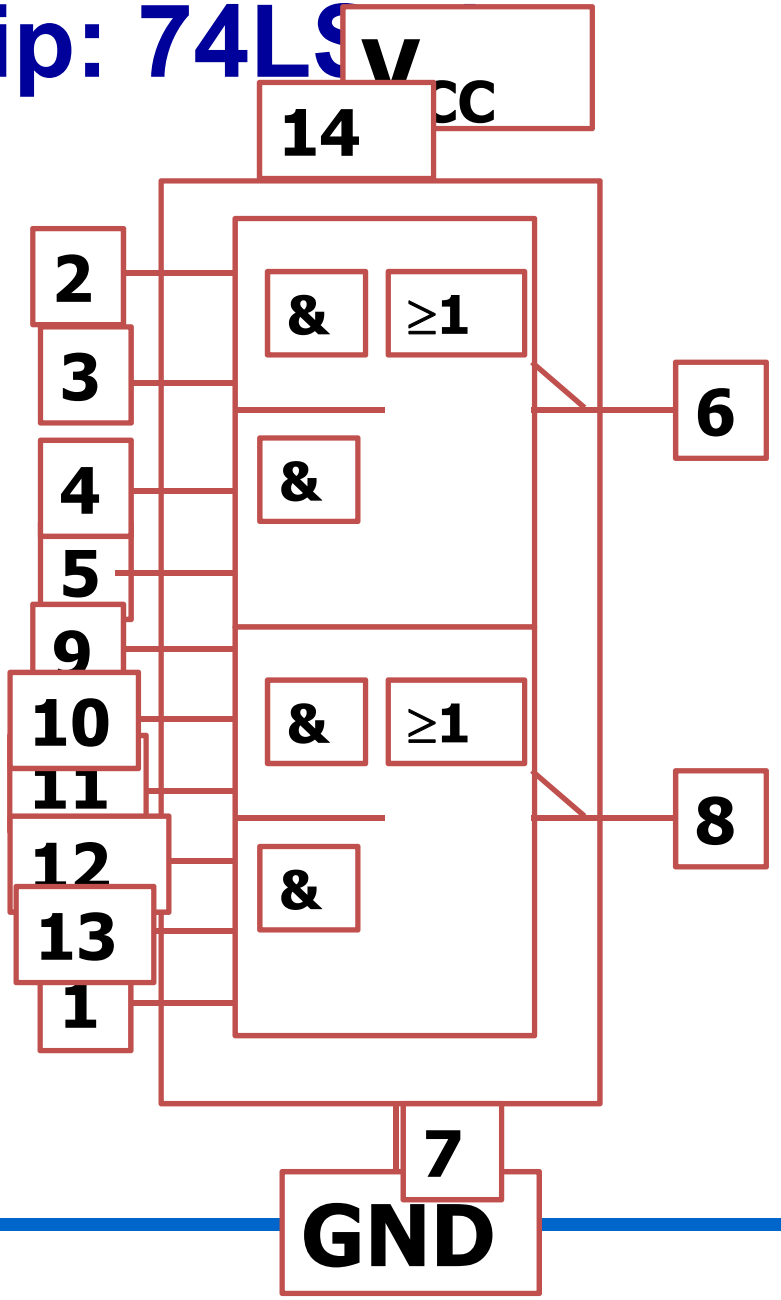
ANSI standard distinctive shape symbols



ANSI standard rectangular outline symbols

Example chip: 74LS

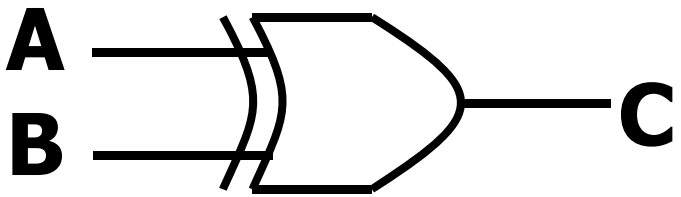
- 74LS51 : dual 2-wide AND-OR-Invert
  - 1 two inputs AND-OR-Invert.
  - 1 three inputs AND-OR-Invert

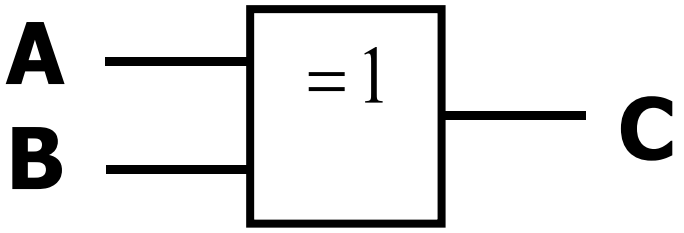


3 Exclusive-OR (XOR)异或

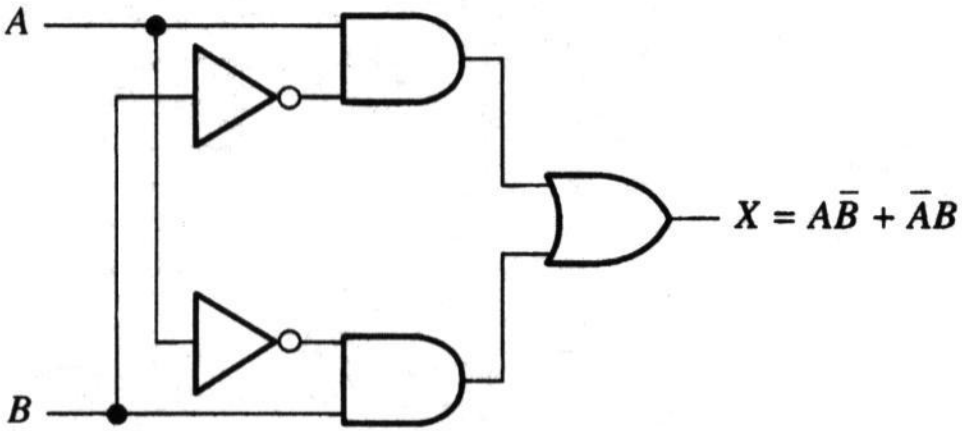
$$X = \overline{A}B + A\overline{B} = A \oplus B$$

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0



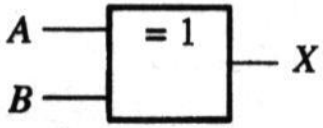


Exclusive-OR logic outputs HIGH only when the two inputs are at opposite levels.



(a) Logic diagram

(b) ANSI distinctive shape symbol



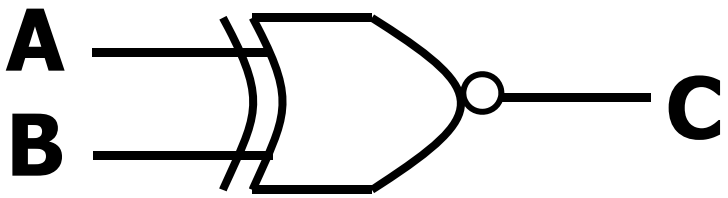
(c) ANSI rectangular outline symbol

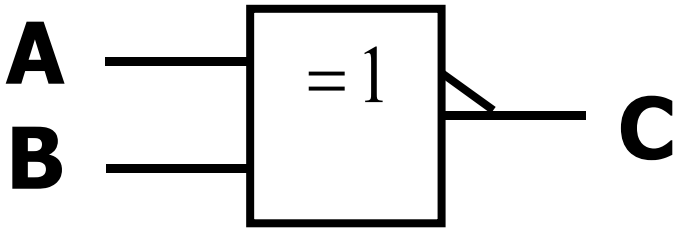
FIGURE 5–7
Exclusive-OR logic diagram and symbols.

4 Exclusive-NOR (XNOR)同或

$$X = AB + \overline{A}\,\overline{B} = \overline{A \oplus B}$$

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1





Exclusive-NOR logic outputs HIGH only when the two inputs are at the same levels.

同或逻辑电路实现：

$$X = \overline{A \oplus B} = \overline{A\overline{B} + \overline{A}B} = \overline{A\overline{B}} \cdot \overline{\overline{A}B} = (\overline{A} + B)(A + \overline{B}) = \overline{A}\,\overline{B} + AB$$

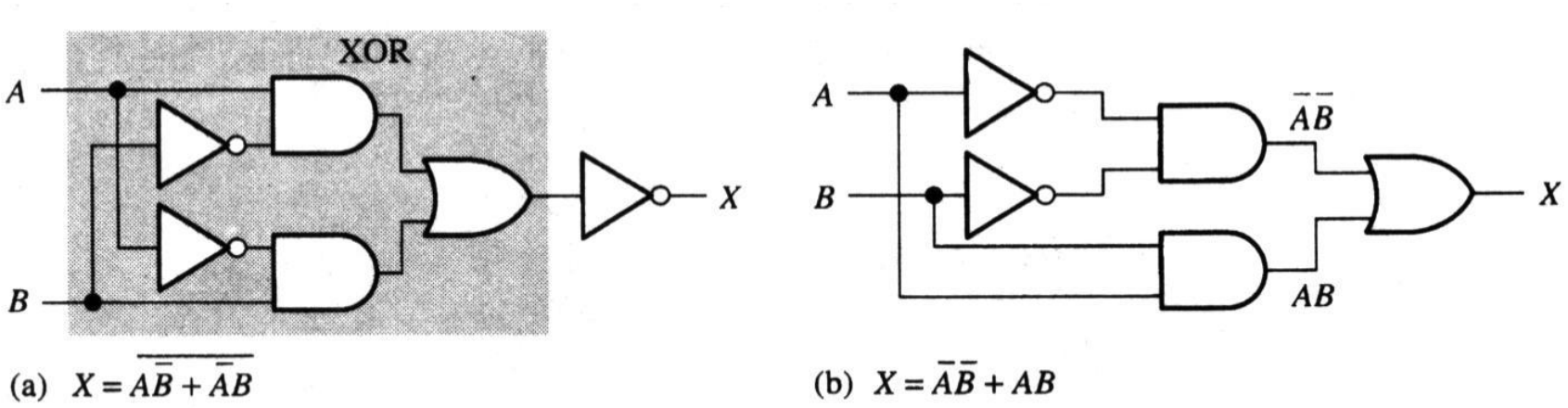
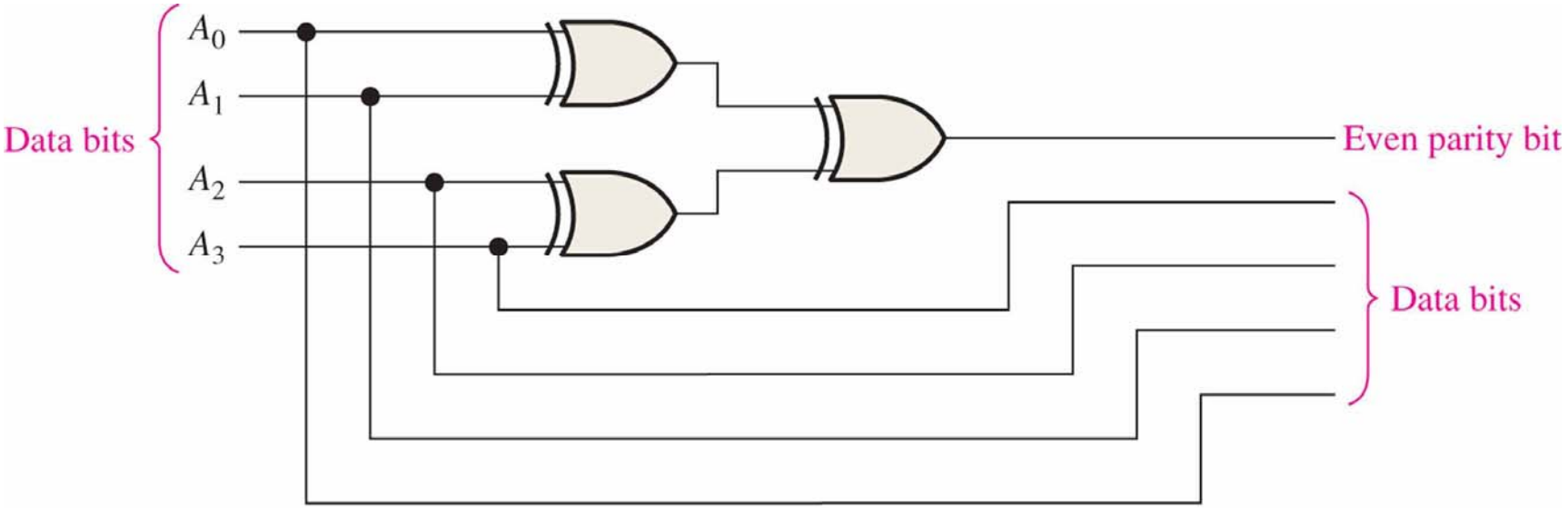


FIGURE 5–8
Two equivalent ways of implementing the exclusive-NOR.

Example: Even-parity check generator



Question: how to design a even-parity checker?

5-2 IMPLEMENTING COMBINATIONAL LOGIC

组合逻辑实现

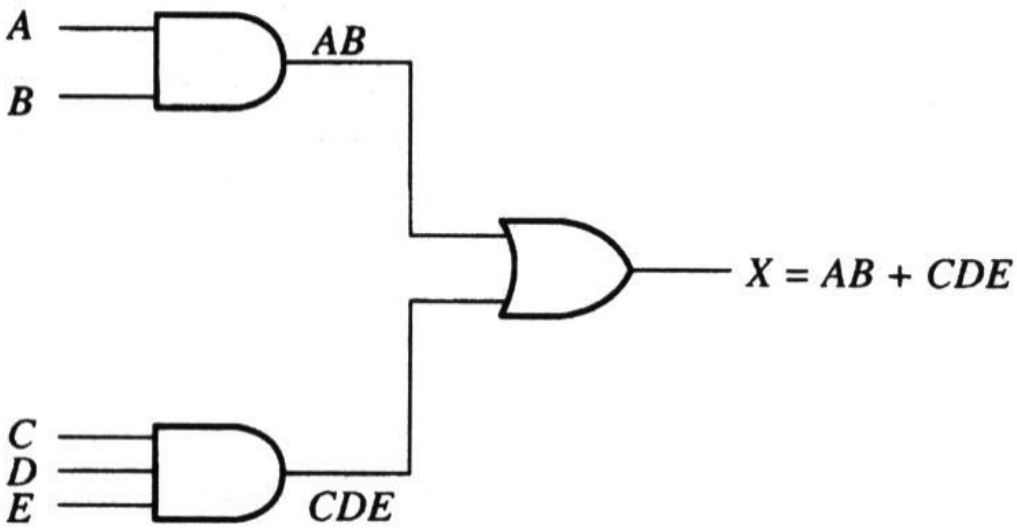
From a Boolean Expression to a Logic Circuit

- Example:

$$X = AB + CDE$$

AND-OR logic

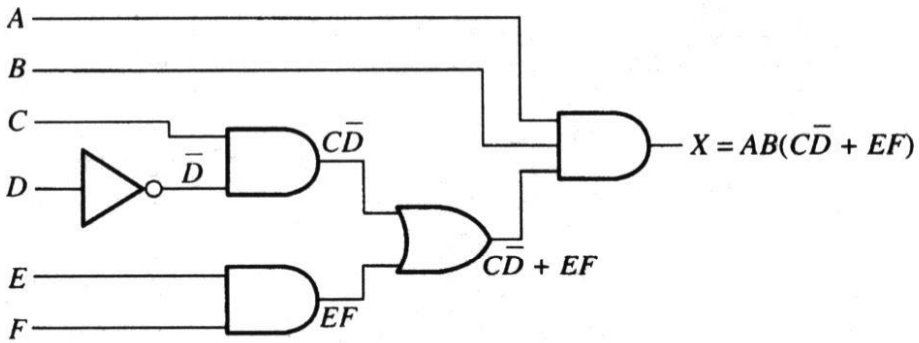
FIGURE 5–9
Logic circuit for X = AB + CDE.



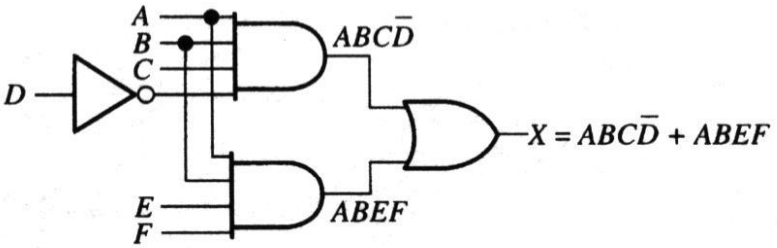
From a Boolean Expression to a Logic Circuit

- Example:

$$X = AB(C\overline{D} + EF)$$



(a)



(b) Sum-of-products implementation of the circuit in part (a)

FIGURE 5–10
Logic circuits for $X = AB(C\overline{D} + EF) = ABC\overline{D} + ABEF$.

From a Truth Table to a Logic Circuit

- Example:

TABLE 5–3

Inputs A	B	C	Output X	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\longrightarrow \overline{A}BC$
1	0	0	1	$\longrightarrow A\overline{B}\,\overline{C}$
1	0	1	0	
1	1	0	0	
1	1	1	0	

$$X = \overline{A}BC + A\overline{B}\,\overline{C}$$

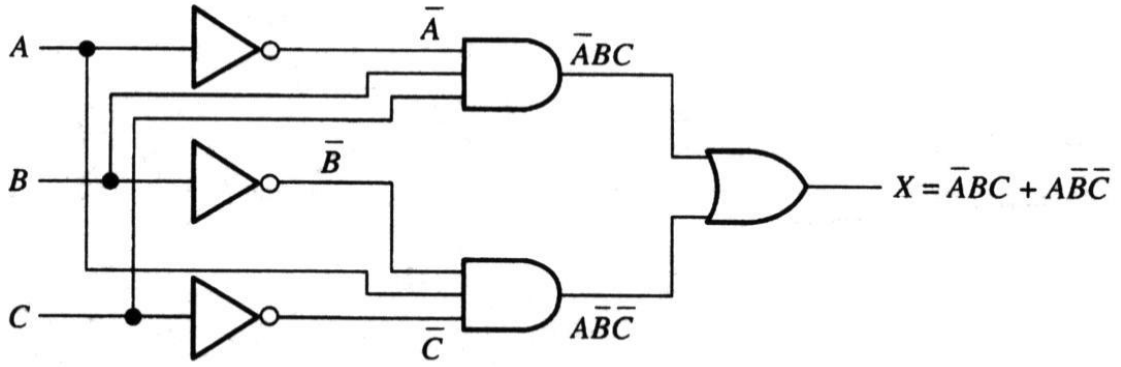
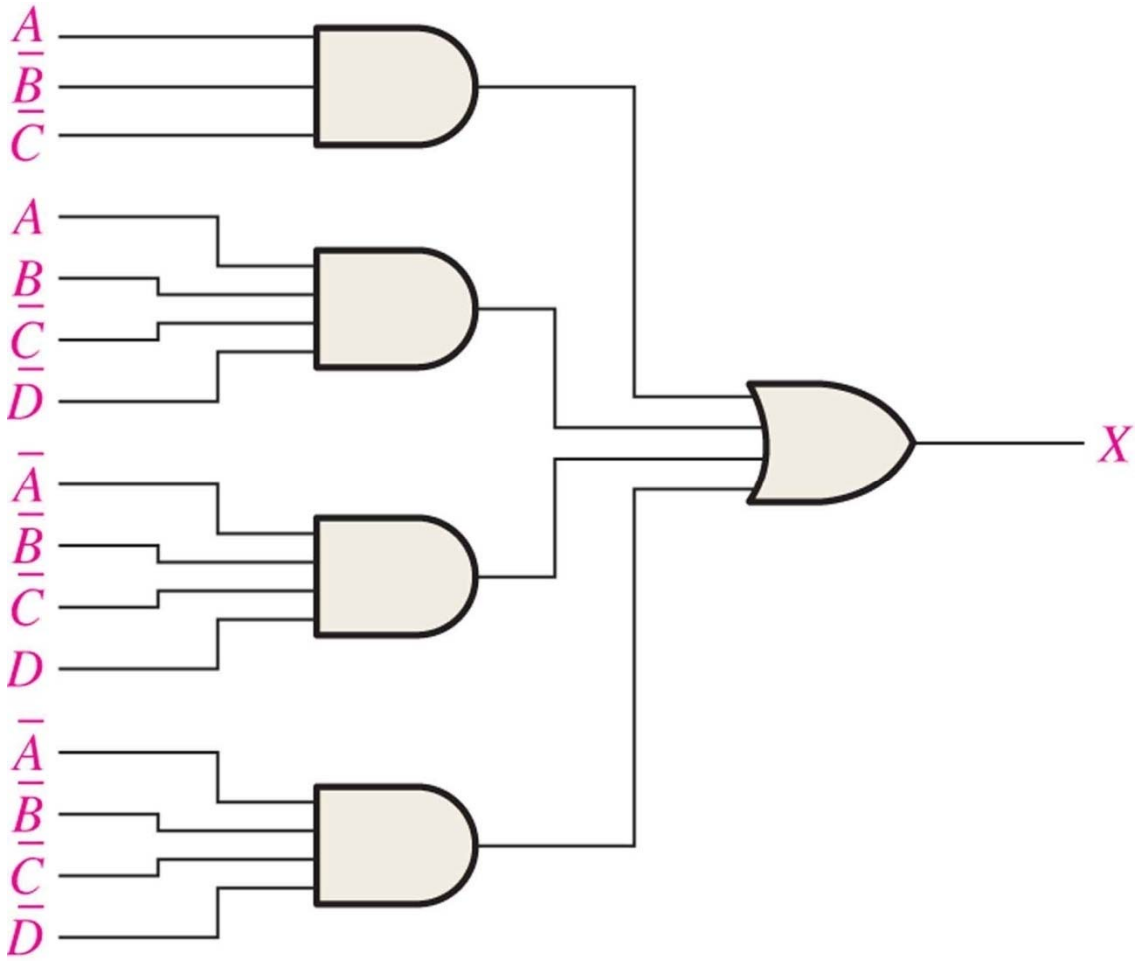


FIGURE 5–11
Logic circuit for $X = \overline{A}BC + A\overline{B}\,\overline{C}$.

Minimize the combinational logic circuit



$$X = A\overline{B}\overline{C} + AB\overline{C}\overline{D} + \overline{A}BCD + \overline{A}BC\overline{D}$$

Transform into standard SOP expression:

$$X = A\overline{B}\overline{C} + AB\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}\overline{C}\overline{D}$$

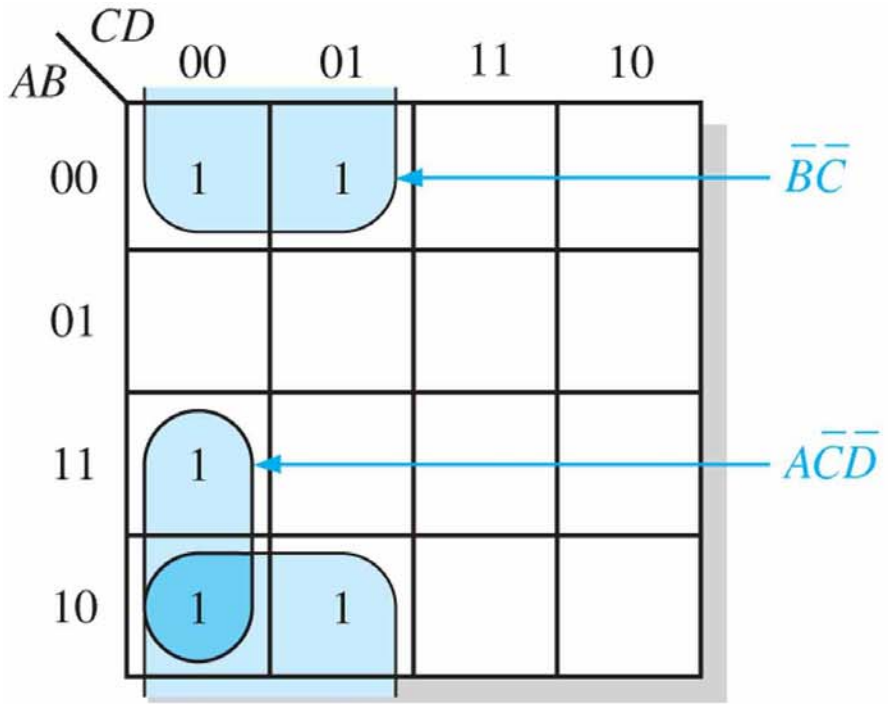
$$X = A\overline{B}\overline{C}\left(D + \overline{D}\right) + AB\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}\overline{C}\overline{D}$$

$$= A\overline{B}\overline{C}D + A\overline{B}\overline{C}\overline{D} + AB\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D$$

$$+ \overline{A}\overline{B}\overline{C}\overline{D}$$

Use Karnaugh map to simplify the circuit:

$$X = A\overline{B}\overline{C}D + A\overline{B}C\overline{D} + AB\overline{C}\overline{D} + \overline{A}B\overline{C}D + \overline{A}BC\overline{D}$$



(a)

$$X = A\overline{B}\overline{C} + \overline{B}\overline{C}$$

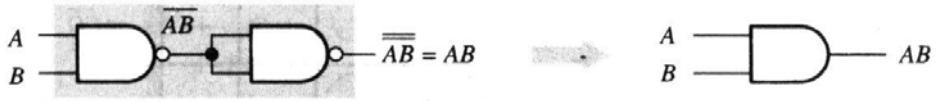
5-3 THE UNIVERSAL PROPERTY OF NAND AND NOR GATES

与非门和或非门的通用特征

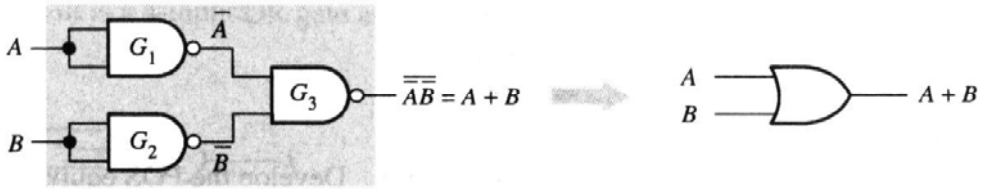
The NAND Gate as a Universal Logic Element

- The NAND gate can be used to produce the NOT, AND, OR, and NOR operations.（与非门可以用来构建非门、与门、或门和或非门）

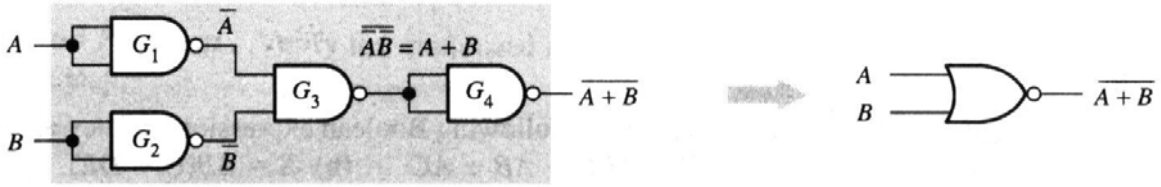
(a) A NAND gate used as an inverter



(b) Two NAND gates used as an AND gate



(c) Three NAND gates used as an OR gate

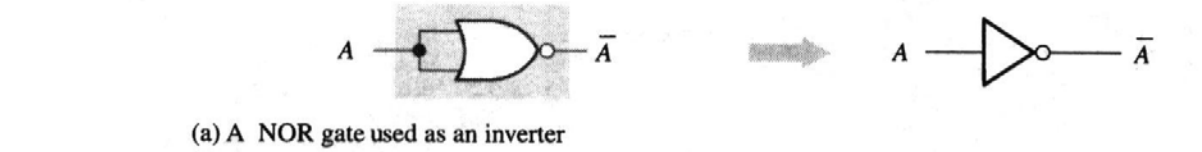


(d) Four NAND gates used as a NOR gate

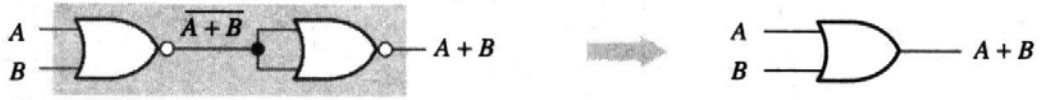
FIGURE 5–18
Universal application of NAND gates.

The NOR Gate as a Universal Logic Element

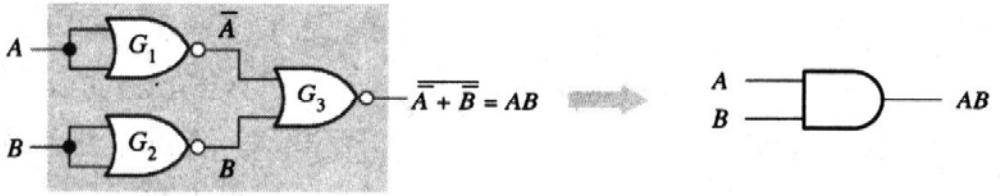
- The NOR gate can be used to produce the NOT, AND, OR, and NAND operations. （与非门可以用来构建非门、与门、或门和与非门）



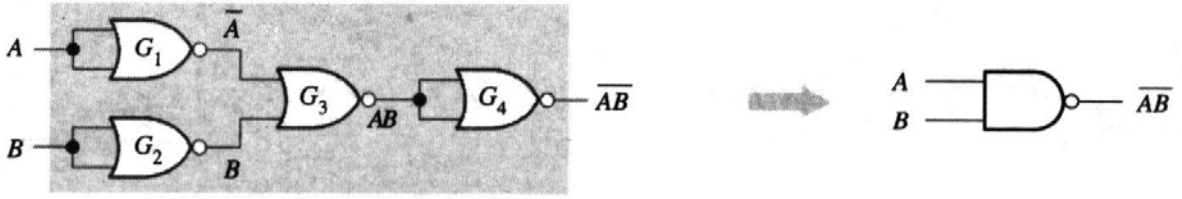
(a) A NOR gate used as an inverter



(b) Two NOR gates used as an OR gate



(c) Three NOR gates used as an AND gate



(d) Four NOR gates used as a NAND gate

FIGURE 5–19

5-4 COMBINATIONAL LOGIC USING NAND AND NOR GATES

使用与非门和或非门的组合逻辑

5 Combinational Logic Using NAND and NOR Gates

- NAND

equivalent

$$\overline{AB} = \overline{A} + \overline{B} \Longrightarrow \text{Negative-OR}$$

- NOR

equivalent

$$\overline{A + B} = \overline{A}\,\overline{B} \Longrightarrow \text{Negative-AND}$$

The ***NAND*** symbol and the ***negative-OR*** symbol are called dual symbols.（与非门与非或门是一对对偶电路）

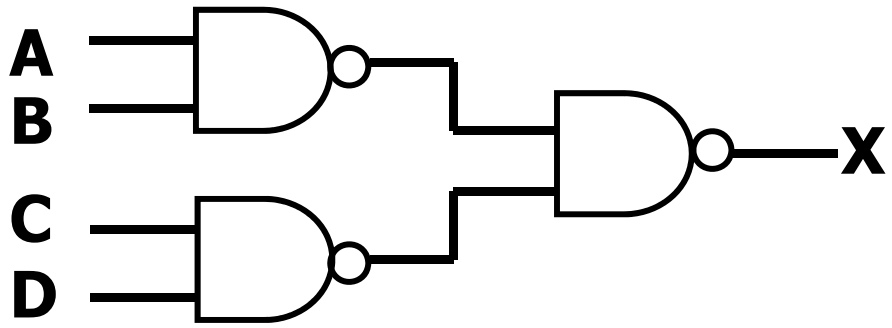
The ***NOR*** symbol and the ***negative-AND*** symbol are called dual symbols.（或非门与非与门是一对对偶电路）

Example: Implementing the following expression using NAND gates:

$$X = AB + CD$$

Solution: $X = AB + CD$

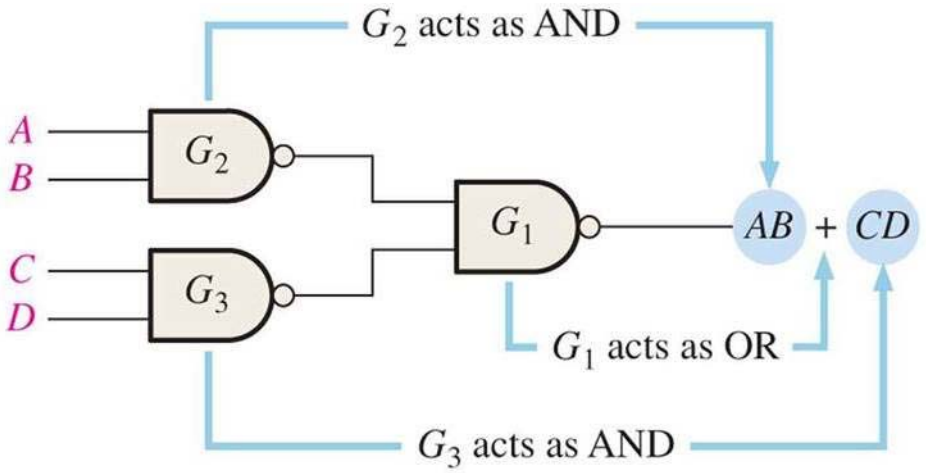
$$= \overline{\overline{AB + CD}} = \overline{\overline{AB} \cdot \overline{CD}}$$



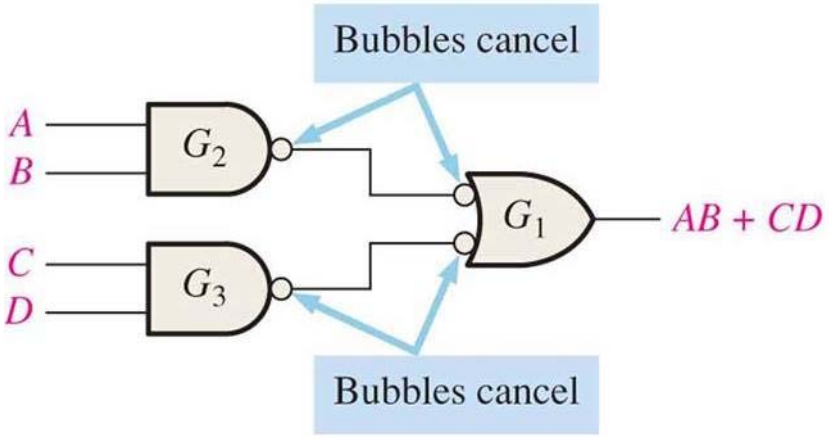
NAND Logic Diagrams Using Dual Symbols

- All logic diagrams using NAND gates should be drawn with each gate represented by either a NAND symbol or the equivalent negative-OR symbol to represent the operations.

- Use the gate symbols in such a way that every connection between a gate output and a gate input is either bubble-to-bubble or nonbubble-to-nonbubble.

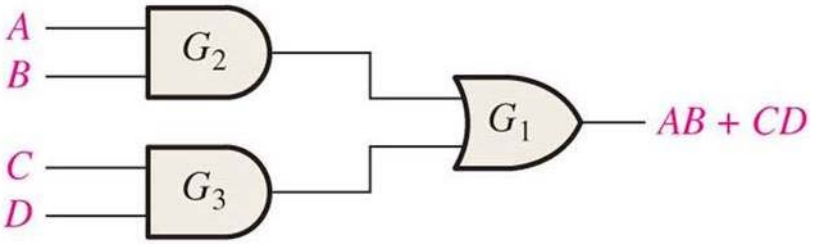


(a) Original NAND logic diagram showing effective gate operation relative to the output expression



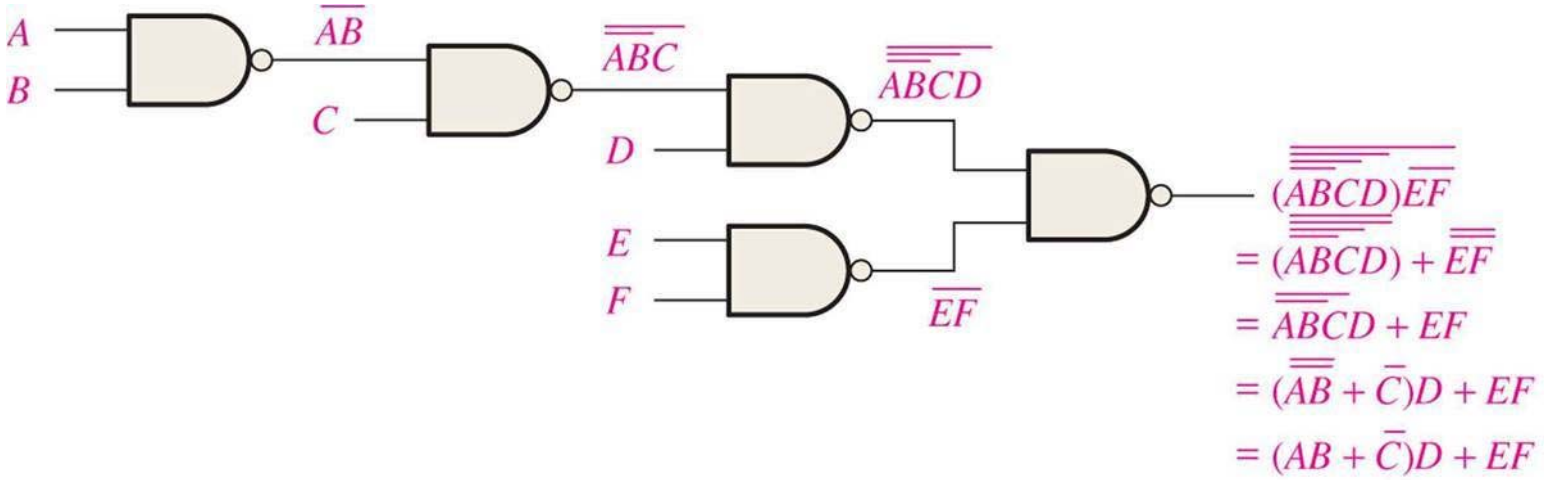
(b) Equivalent NAND/Negative-OR logic diagram

≡

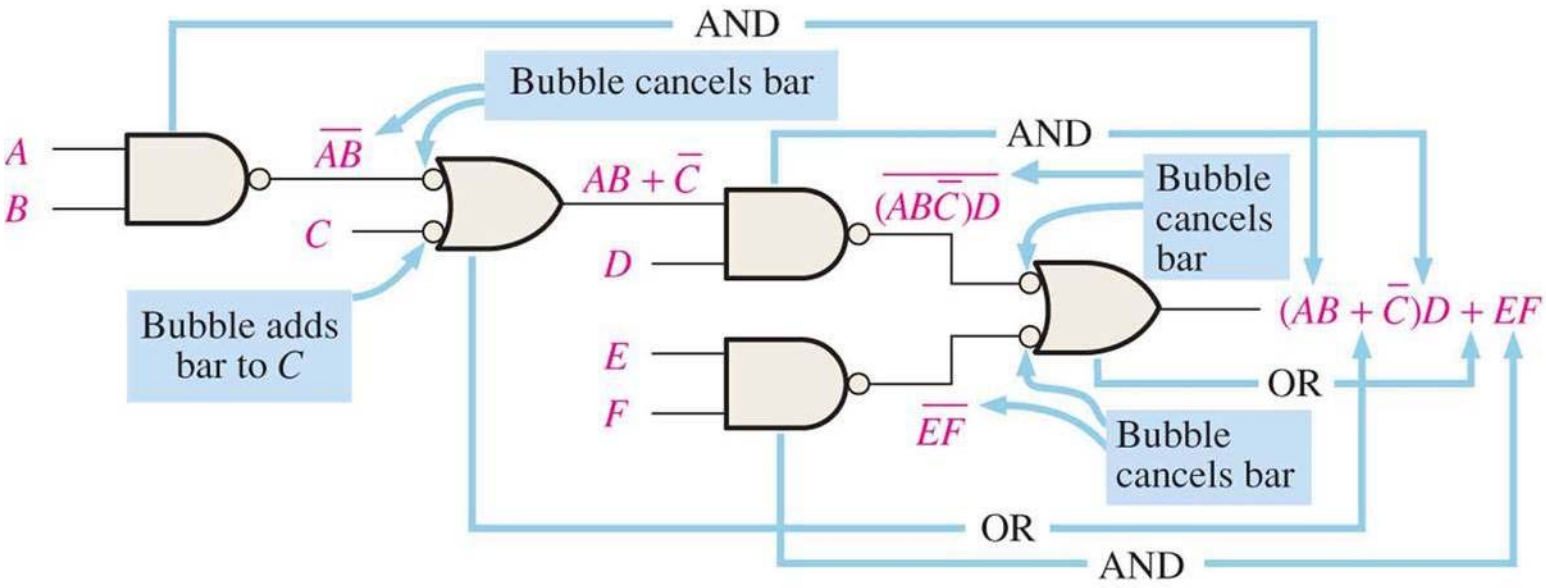


(c) AND-OR equivalent

NAND Logic



(a) Several Boolean steps are required to arrive at final output expression.



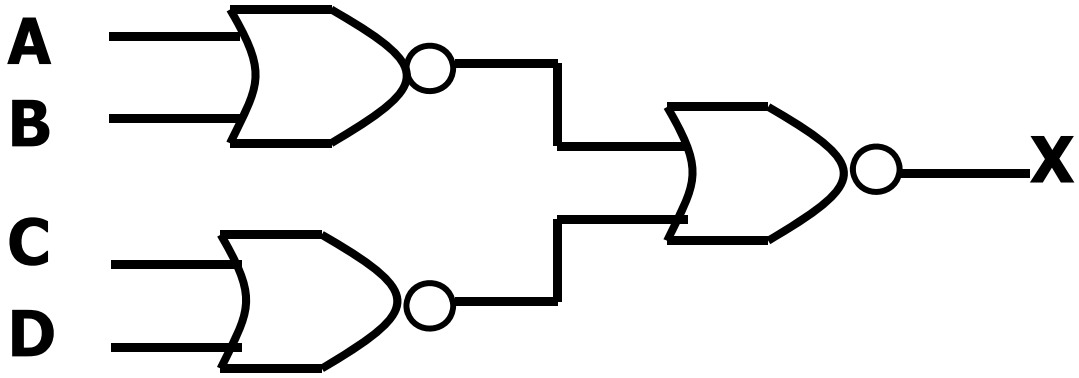
(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

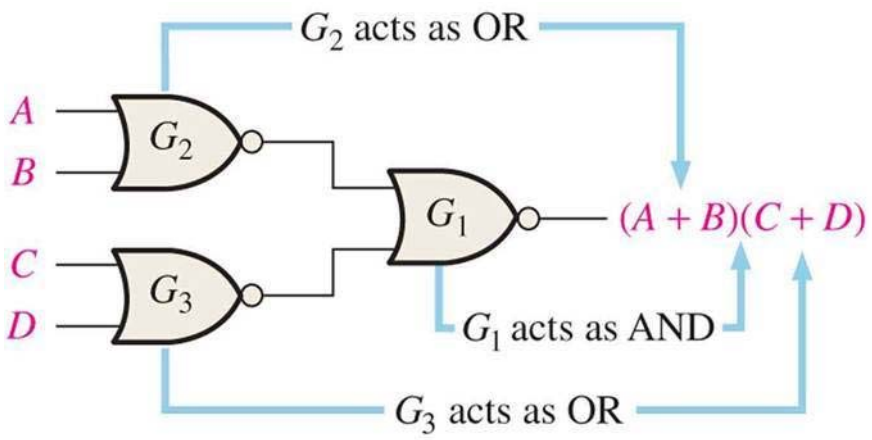
Example: Implementing the following expression using NOR gates:

$$X = (A + B)(C + D)$$

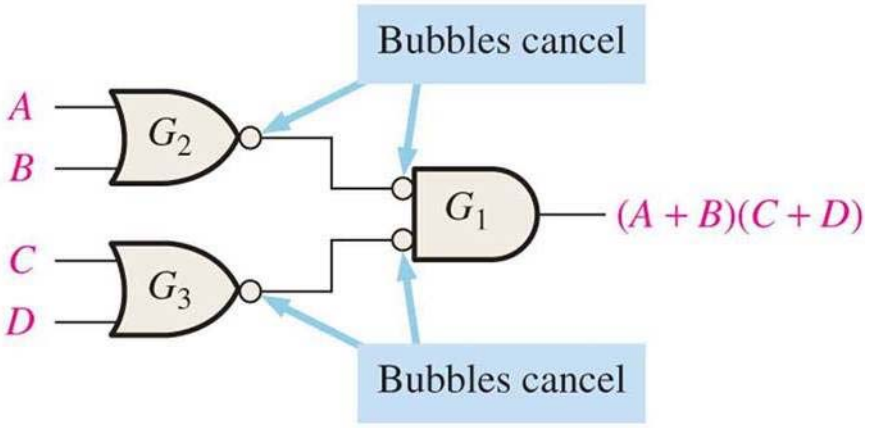
Solution: $X = (A + B)(C + D)$

$$= \overline{\overline{(A + B)(C + D)}} = \overline{\overline{A + B} + \overline{C + D}}$$



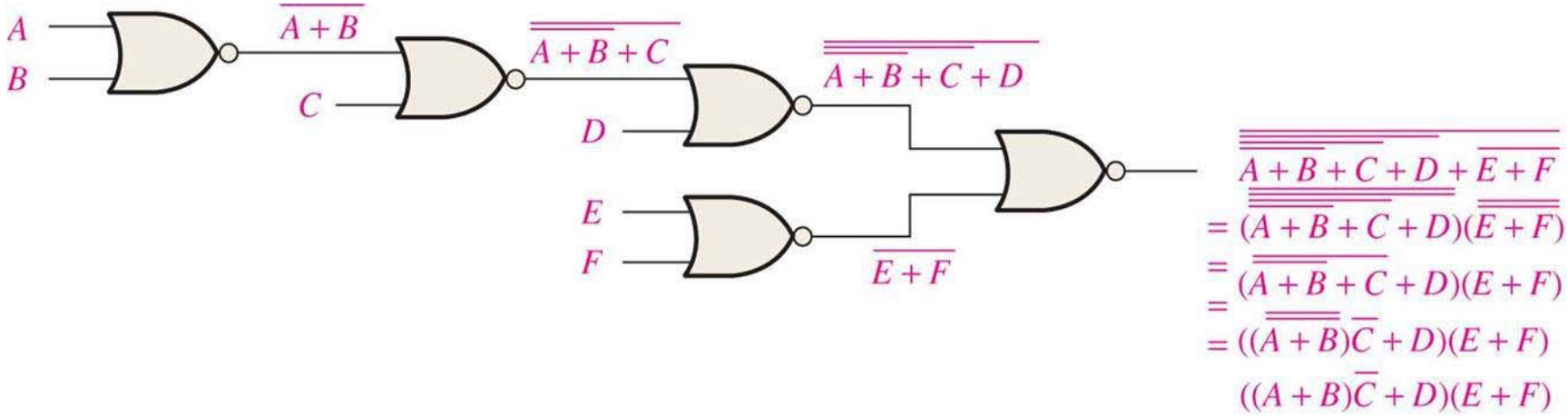

G_2 acts as OR
A
B
C
D
G_2
G_3
G_1
$(A + B)(C + D)$
G_1 acts as AND
G_3 acts as OR

(a)

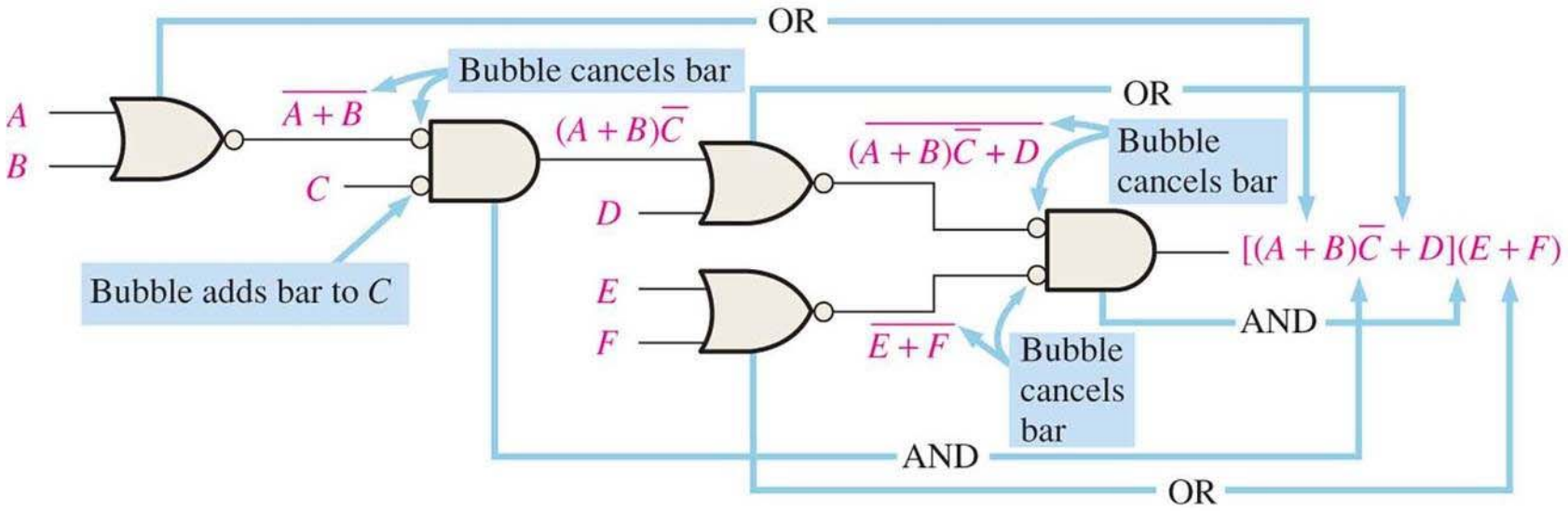

Bubbles cancel
A
B
C
D
G_2
G_3
G_1
$(A + B)(C + D)$
Bubbles cancel

(b)

NOR Logic



(a) Final output expression is obtained after several Boolean steps.



(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

Quiz

1. Assume an SOP expression is $AB + CD$. The equivalent POS expression is

a. $(A + B)(C + D)$

b. $(\overline{A} + B)(\overline{C} + D)$

c. $(\overline{A} + \overline{B})(\overline{C} + \overline{D})$

d. none of the above

Quiz

2. The truth table shown is for

   a. a NAND gate

   b. a NOR gate

   c. an exclusive-OR gate

   d. an exclusive-NOR gate

Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	1

Quiz

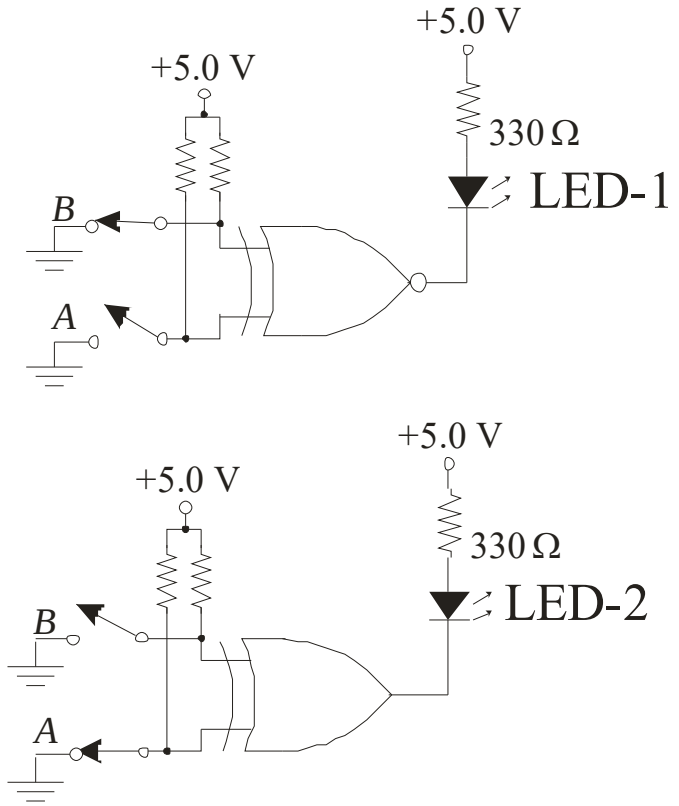
3. An LED that should be ON is

   a. LED-1

   b. LED-2

   c. neither

   d. both



Quiz

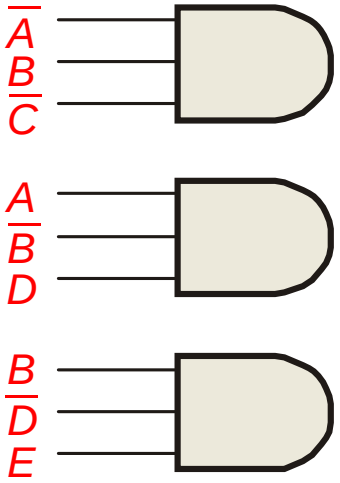
4. To implement the SOP expression $X = \overline{A}B\overline{C} + A\overline{B}D + B\overline{D}E$, the type of gate that is needed is a

a. 3-input AND gate

b. 3-input NAND gate

c. 3-input OR gate

d. 3-input NOR gate



Quiz

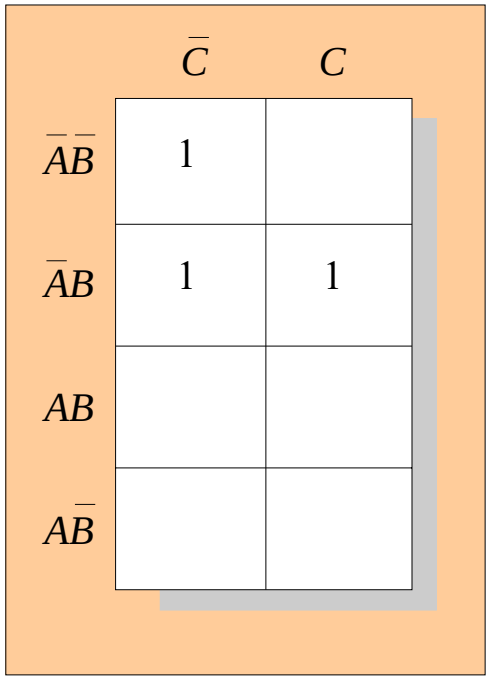
5. Reading the Karnaugh map, the logic expression is

a. $A\overline{C} + \overline{A}\overline{B}$

b. $\overline{A}B + A\overline{C}$

c. $\overline{A}B + B\overline{C}$

d. $\overline{A}B + \overline{A}\overline{C}$



Quiz

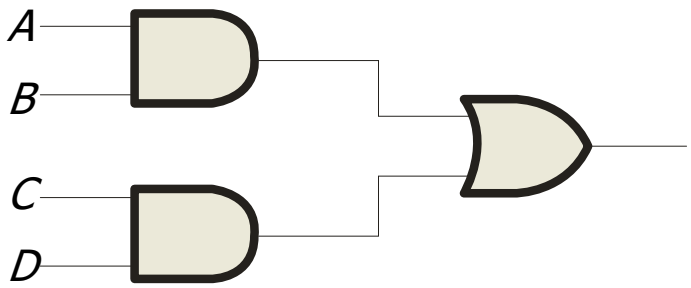
6. The circuit shown will have identical logic out if all gates are changed to

a. AND gates

b. OR gates

c. NAND gates

d. NOR gates



Quiz

7. The two types of gates which are called *universal gates* are

   a. AND/OR

   b. NAND/NOR

   c. AND/NAND

   d. OR/NOR

Quiz

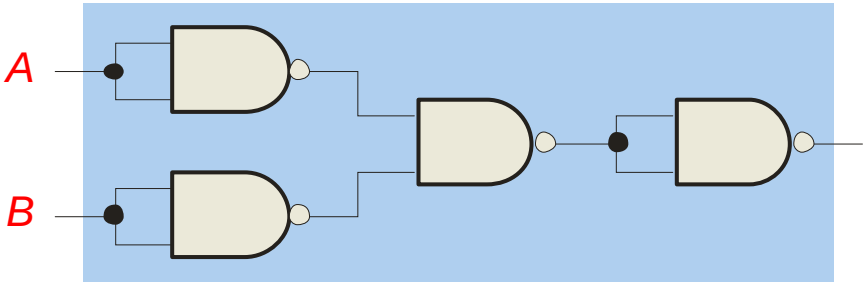
8. The circuit shown is equivalent to an

   a. AND gate

   b. XOR gate

   c. NOR gate

   d. none of the above



Quiz

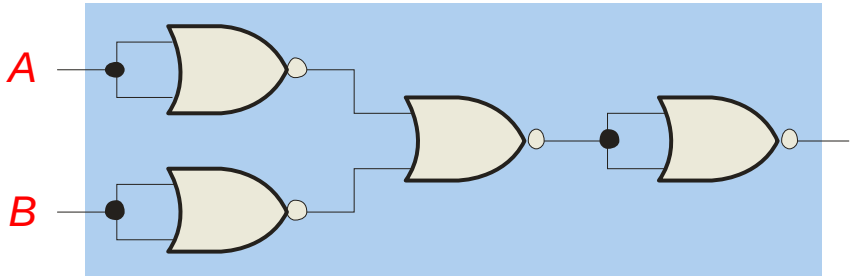
9. The circuit shown is equivalent to

   a. an NAND gate

   b. an XOR gate

   c. an OR gate

   d. none of the above



Quiz

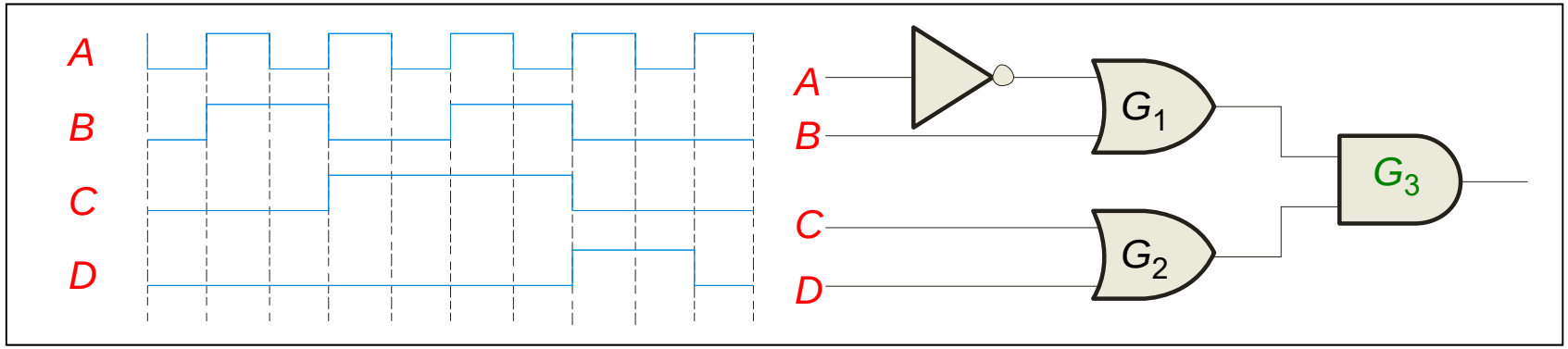
10. During the first *three* intervals for the pulsed circuit shown, the output of

a. G_1 is LOW and G_2 is LOW

b. G_1 is LOW and G_2 is HIGH

c. G_1 is HIGH and G_2 is LOW

d. G_1 is HIGH and G_2 is HIGH



Homework

- 2，6d，8， 11e，12c，13，14
- how to design a even-parity checker?(本章PPT中练习)

Answers

1. b
2. d
3. a
4. c
5. d
6. c
7. b
8. c
9. a
10. c