CHAPTER 6

Functions of Combinational Logic
组合逻辑电路函数

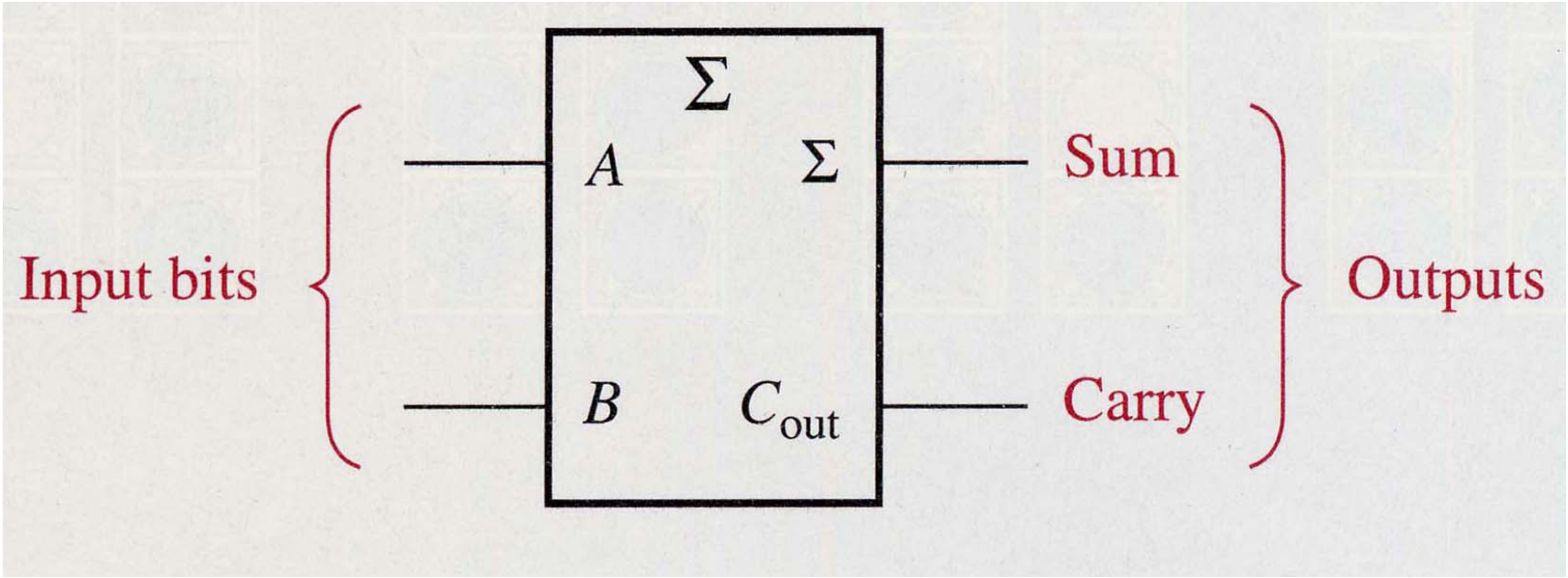
MSI Combinational Logic Circuits

- Adders（加法器）
- Comparator（比较器）
- Decoders（解码器）
- Encoders（编码器）
- Code converters（代码转换器）
- Multiplexer (data selectors)（数据选择器）
- De-multiplexers（多路复用器）
- Parity generators/checkers（奇偶产生/校验器）

1 Adders

- Half-Adder (半加器)
- Full-Adder (全加器)
- Parallel Binary Adder 并行二进制加法器

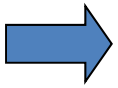
Half-Adder (I)



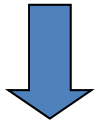
Logic symbol

Half-Adder (II)

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 10$$



A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

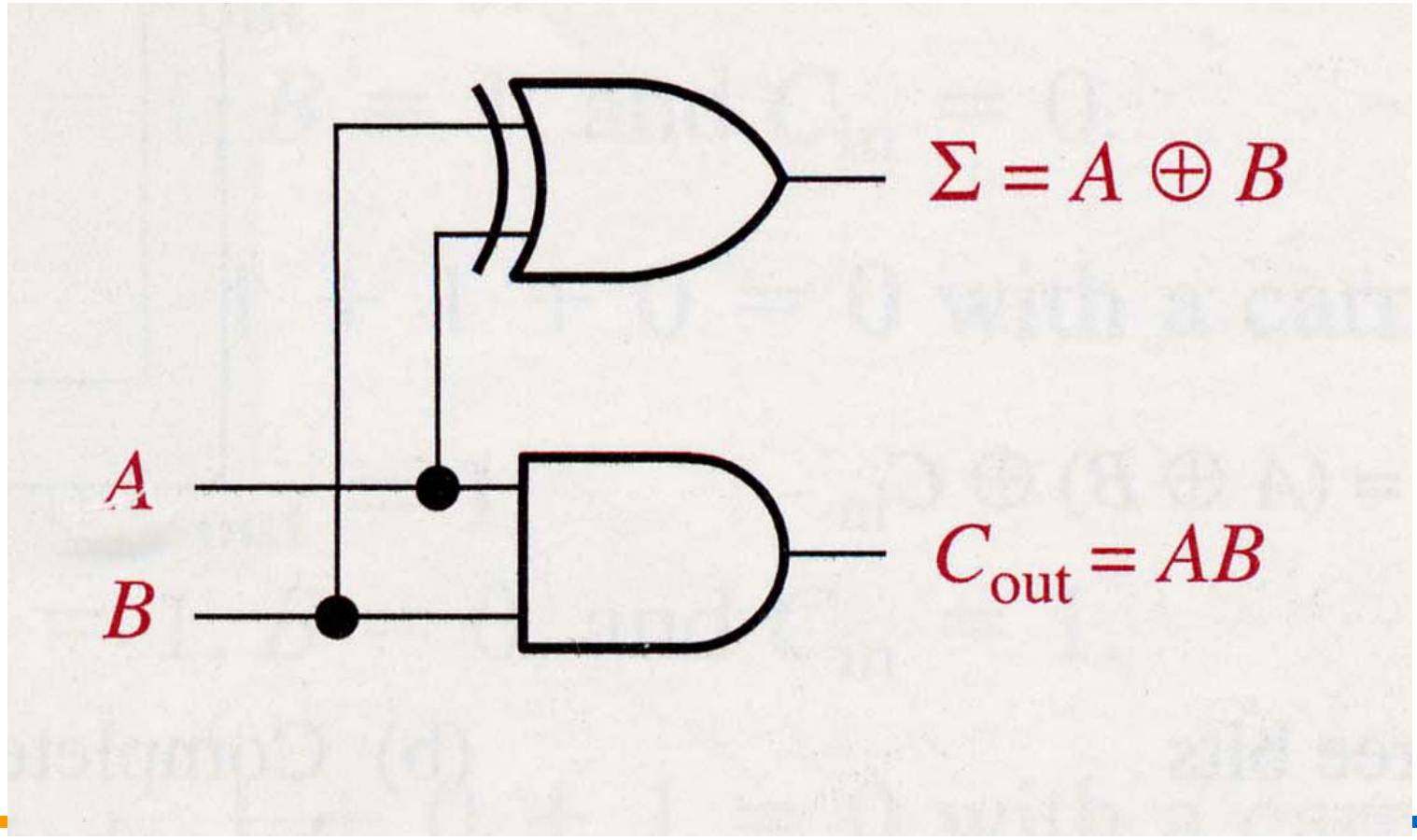


$$\Sigma = A \oplus B$$

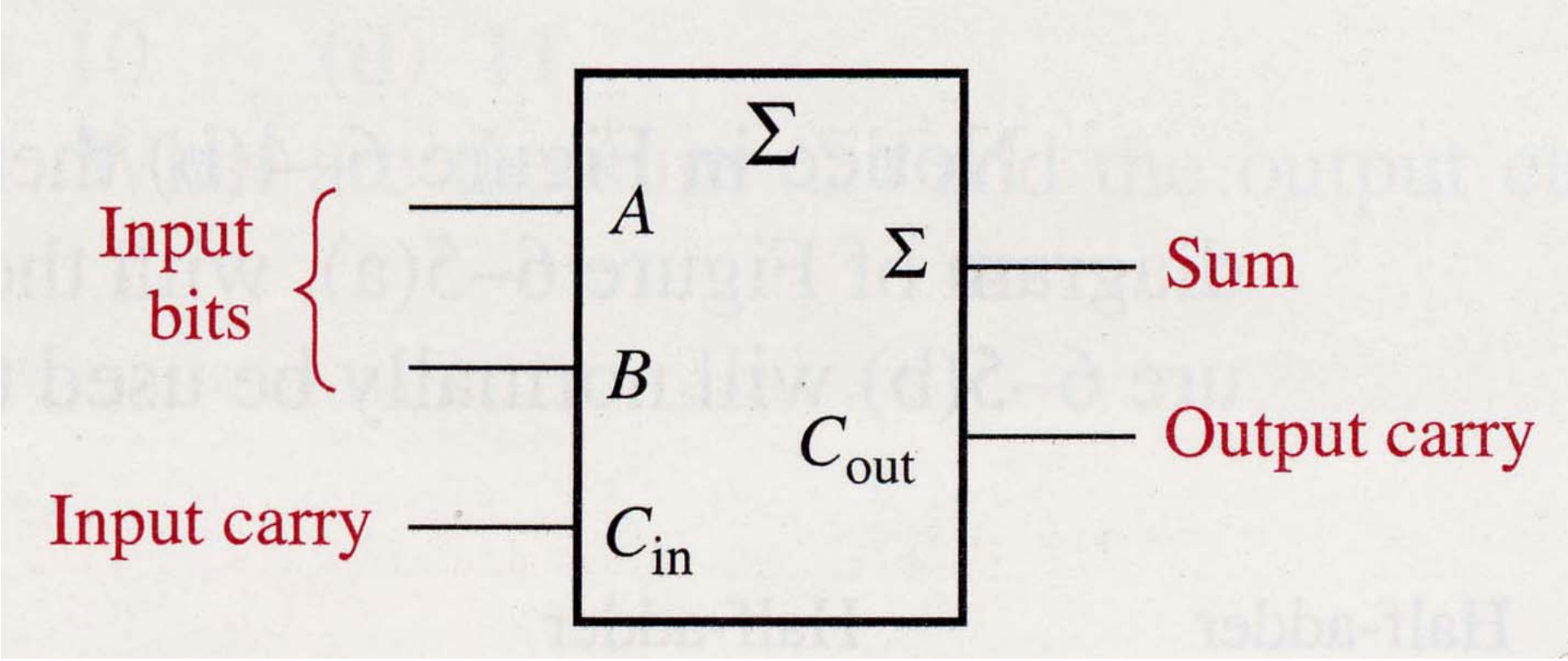
$$C_{out} = AB$$

Half-Adder (III)

Logic diagram



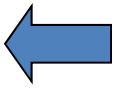
Full-Adder (I)



Full-Adder(II)

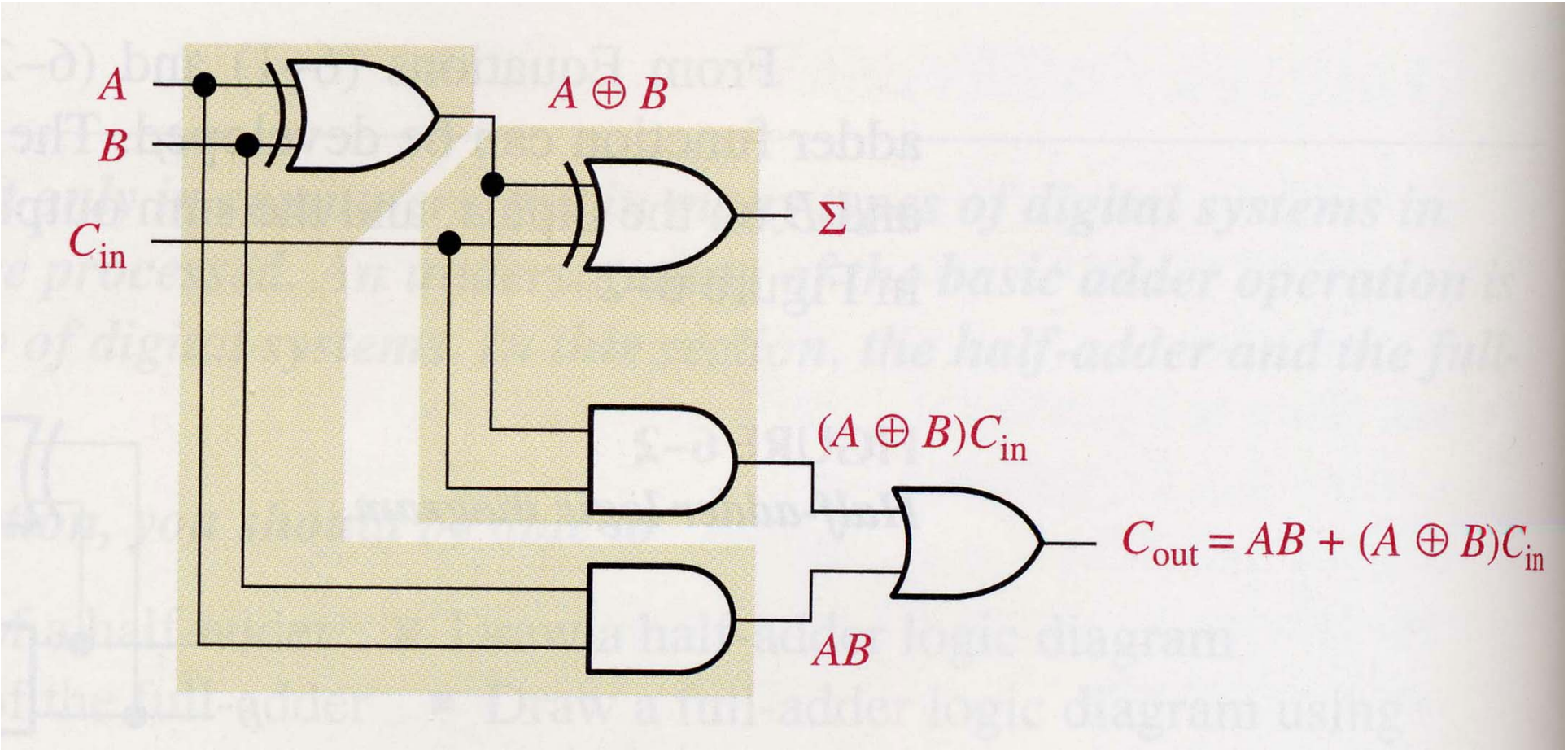
$$\Sigma = (A \oplus B) \oplus C_{in}$$

$$C_{out} = AB + (A \oplus B)C_{in}$$

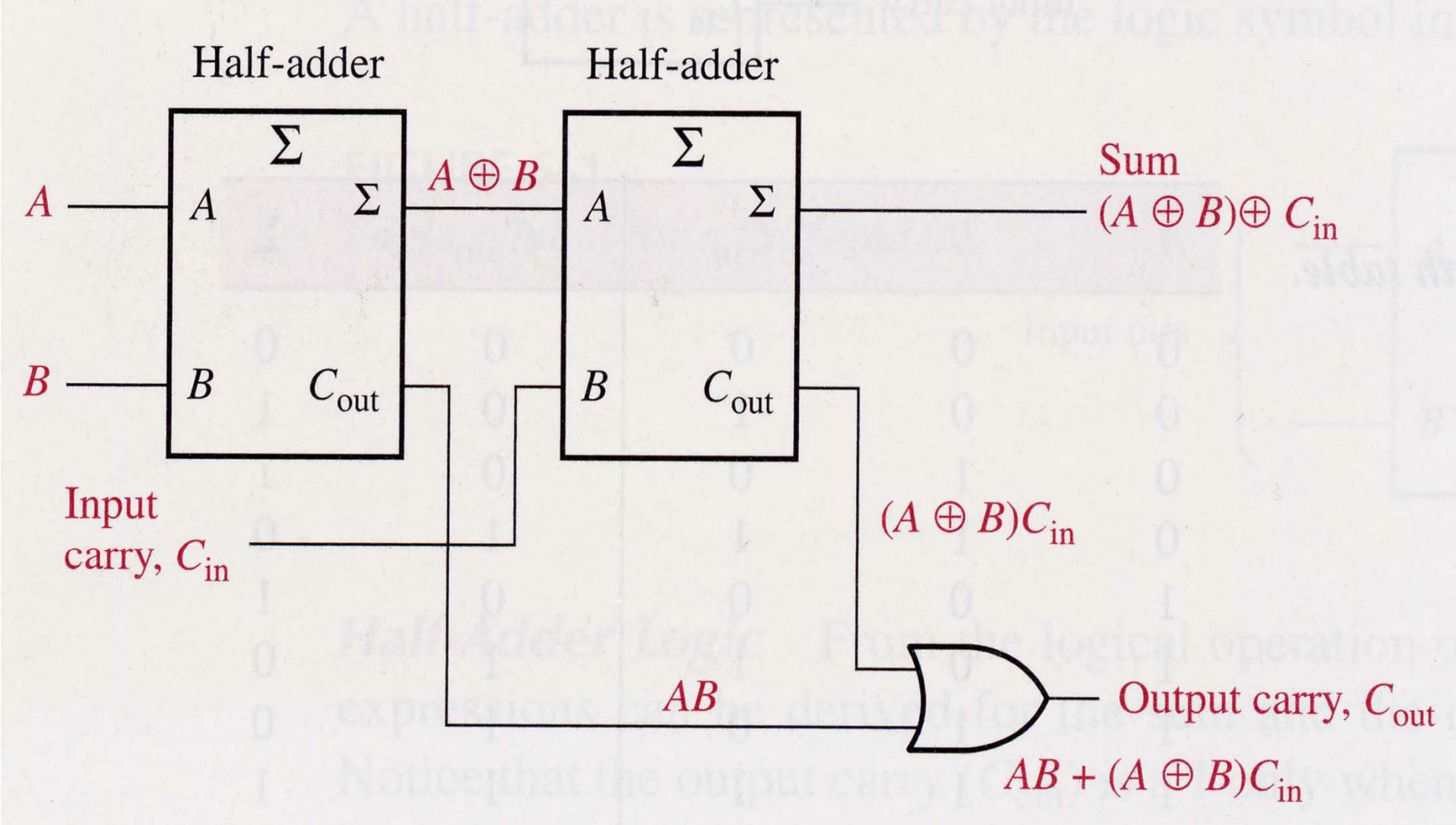


A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Logic Diagram



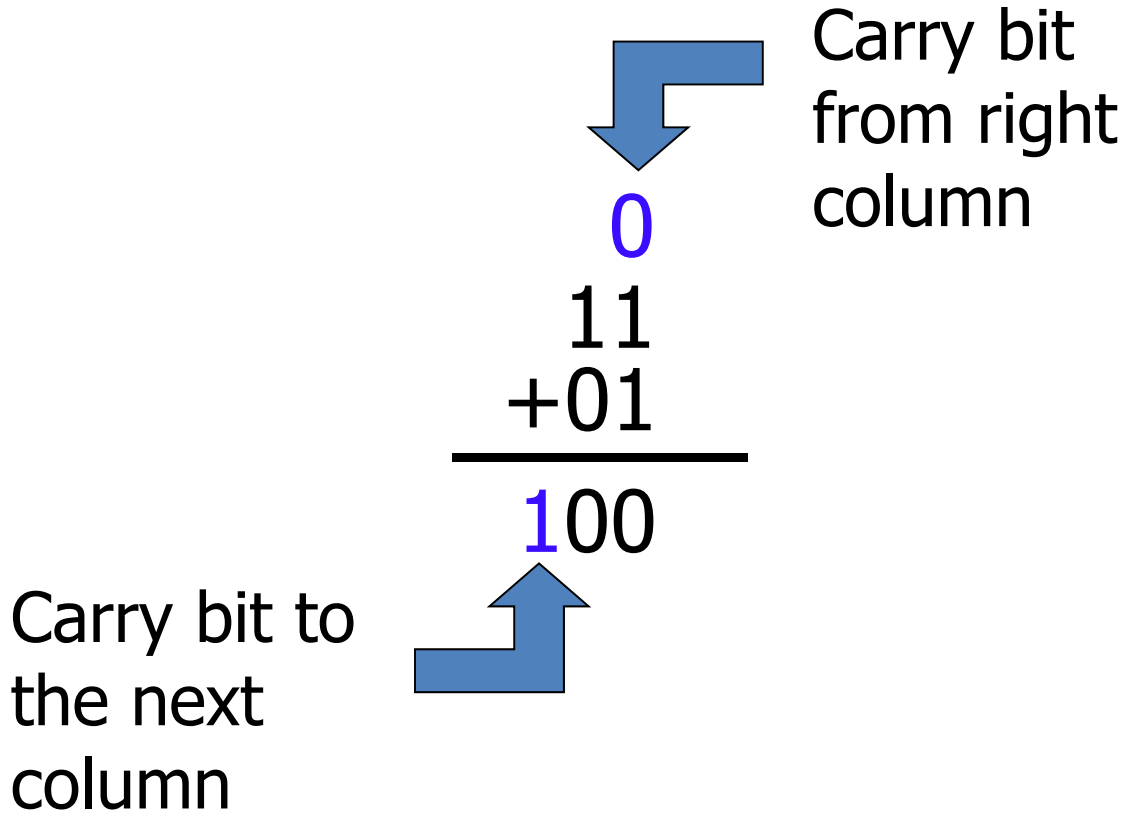
Full-adder implemented with two half-adders.



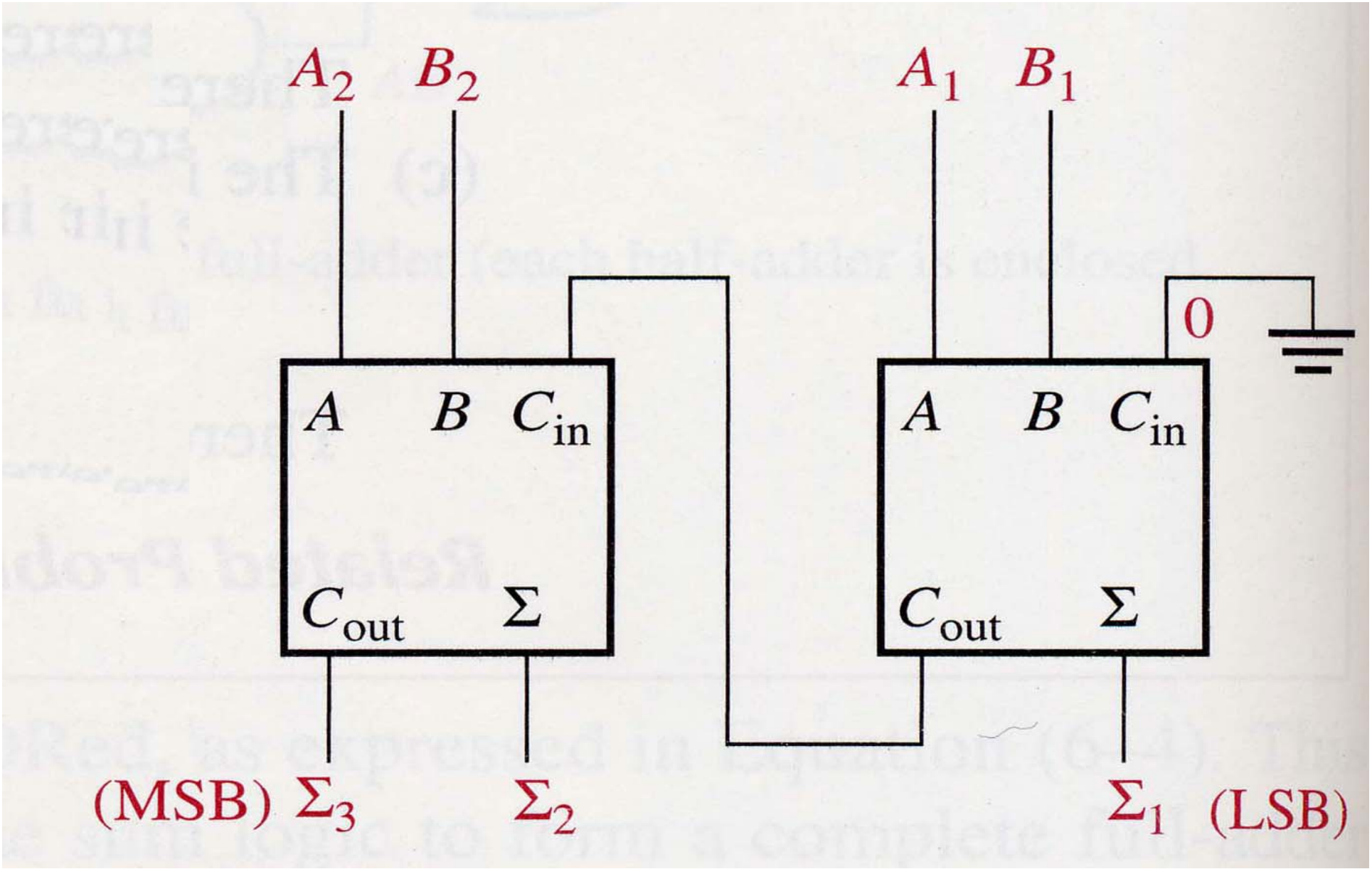
Parallel Binary Adders

- Two or more full-adders are connected to form parallel binary adders.
- A single full-adders is capable of adding two 1-bit binary numbers and an input carry. To add binary numbers with more than one bit, additional full-adders must be used.

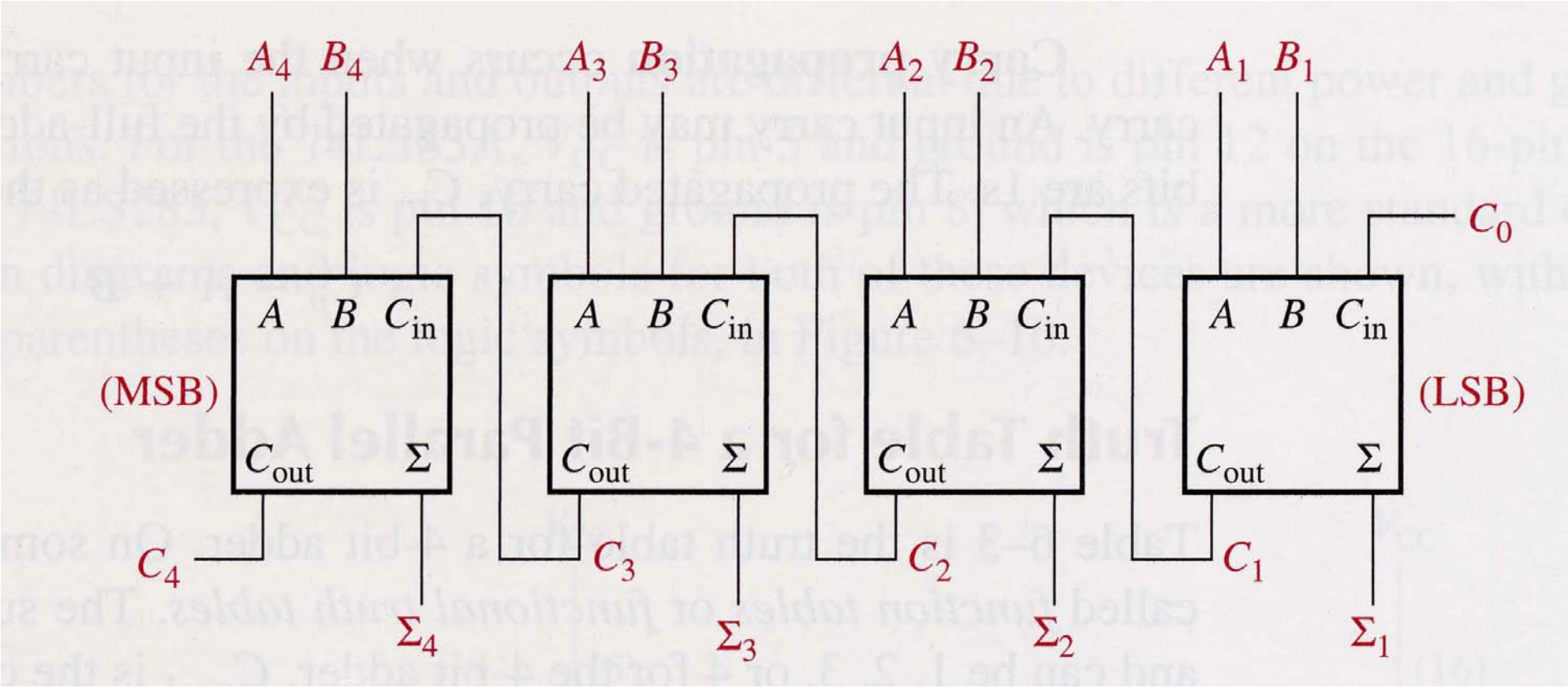
Addition of Two-bit Binary Number



2-bit parallel adder using two full-adders

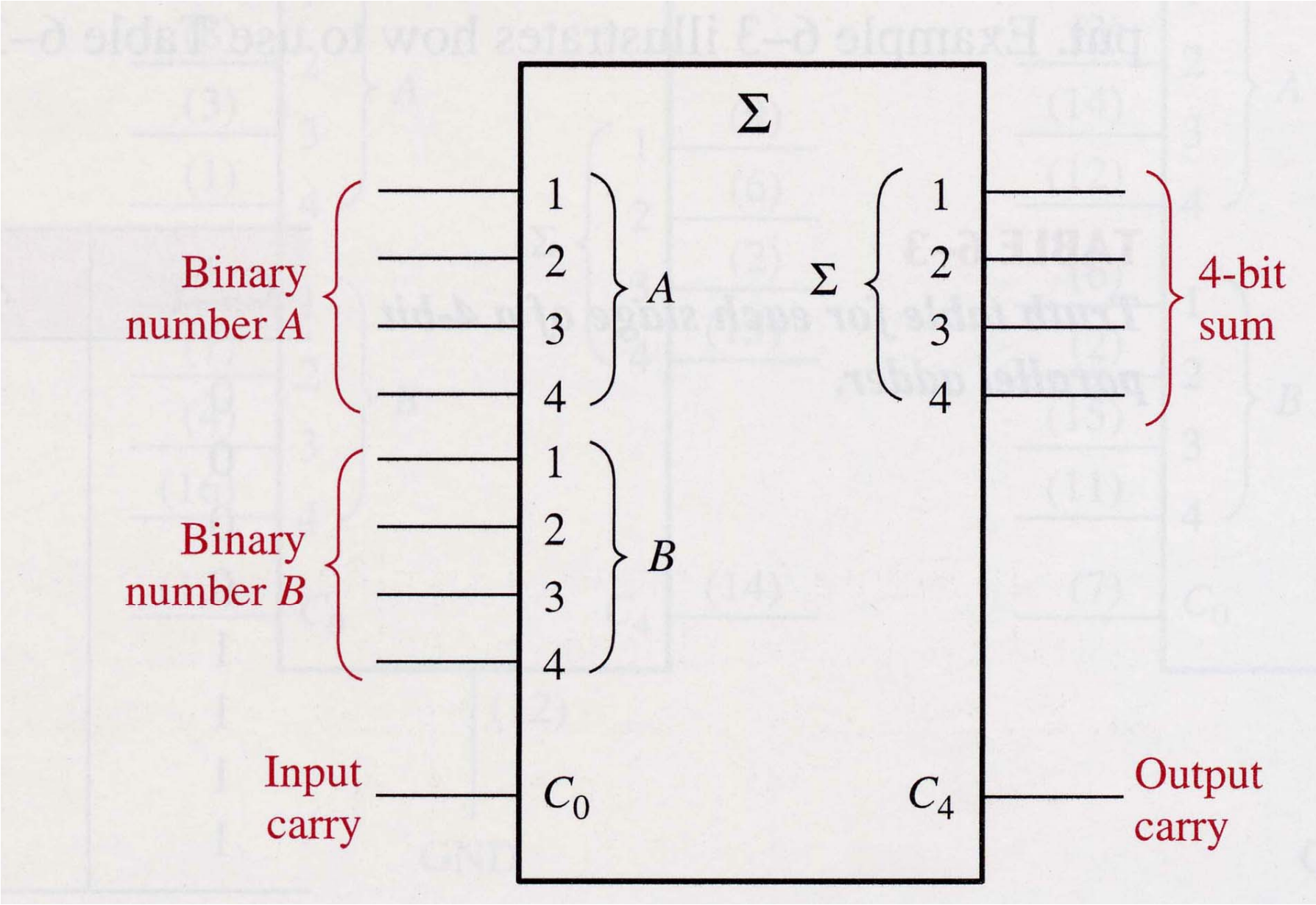


4-bit parallel adder using four full-adders



Block diagram

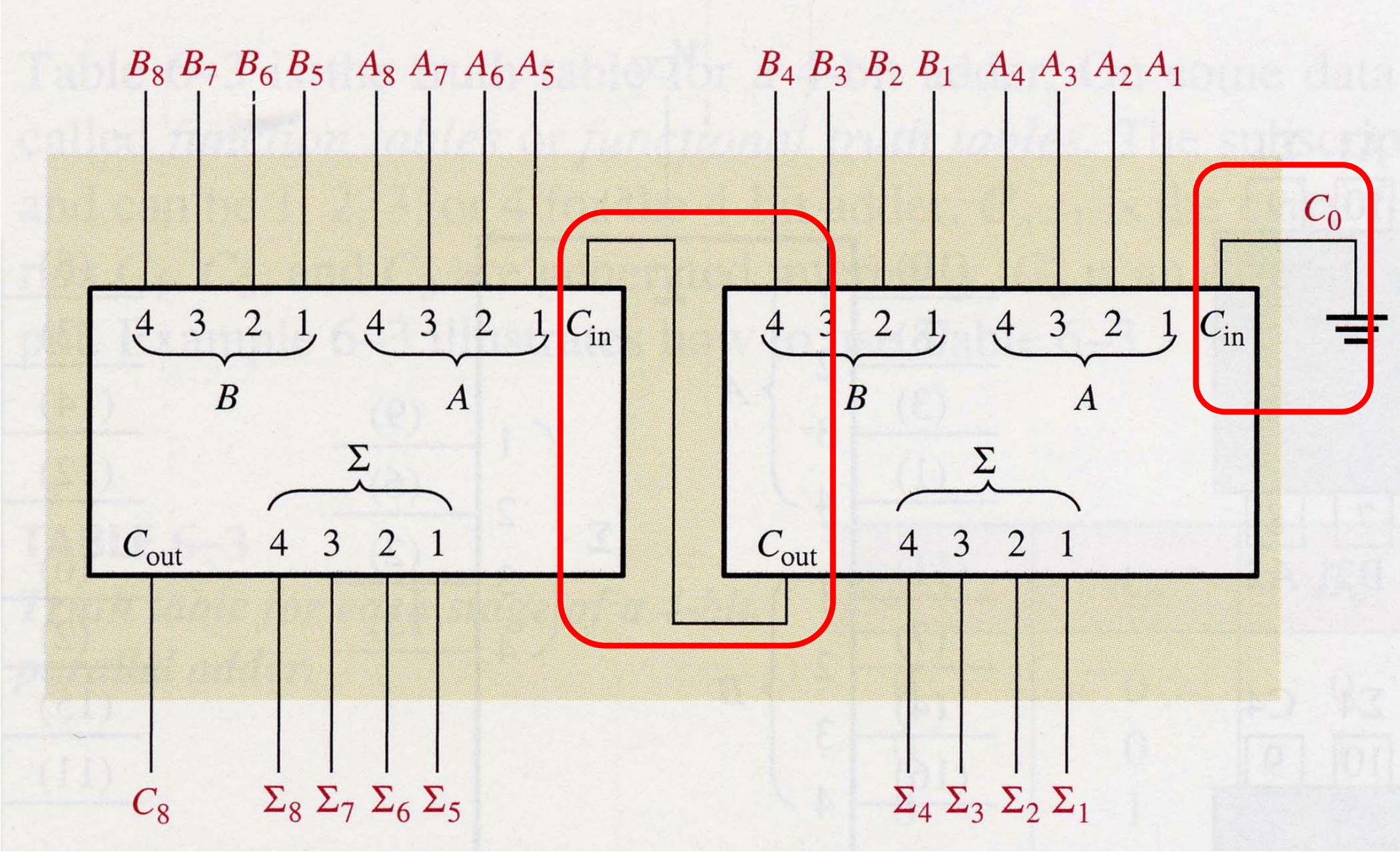
Logic symbol



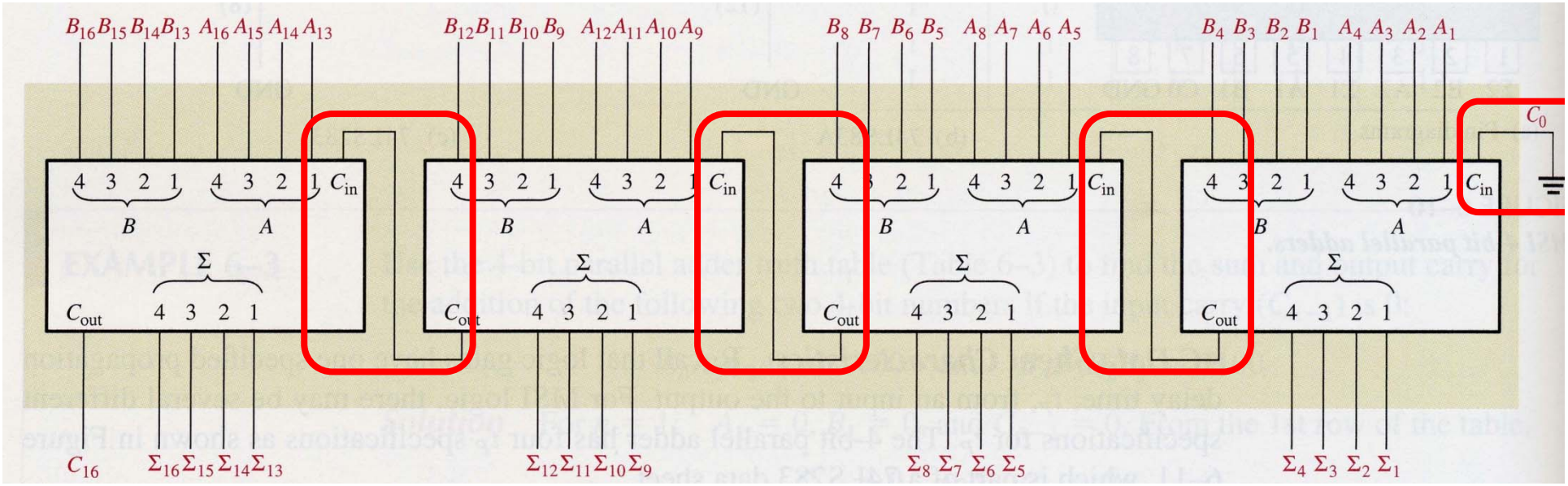
Adder Expansion

- 8-bit adder
- 16-bit adder

8-bit adder


B_8 B_7 B_6 B_5 A_8 A_7 A_6 A_5
B_4 B_3 B_2 B_1 A_4 A_3 A_2 A_1
C_0
4 3 2 1
4 3 2 1
C_{in}
B
A
Σ
C_{out}
C_8
Σ_8 Σ_7 Σ_6 Σ_5
Σ_4 Σ_3 Σ_2 Σ_1

16-bit adder

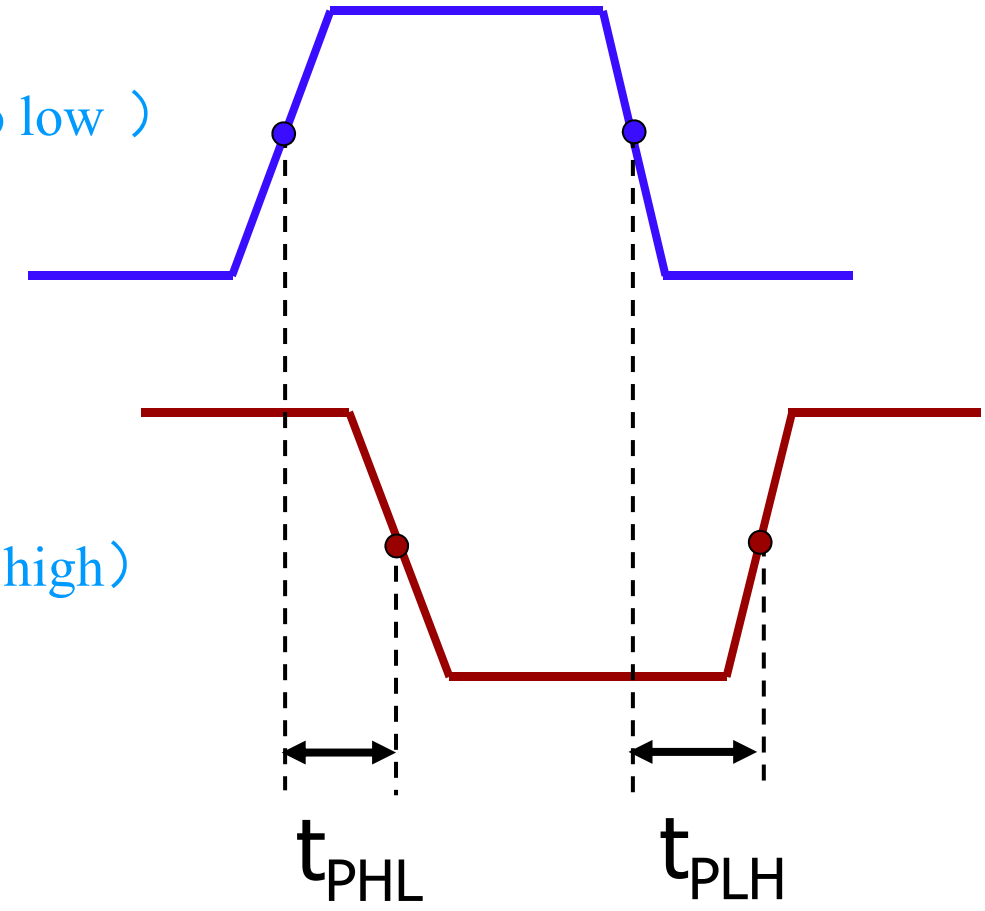

$B_{16}B_{15}B_{14}B_{13}$ $A_{16}A_{15}A_{14}A_{13}$
$B_{12}B_{11}B_{10}B_9$ $A_{12}A_{11}A_{10}A_9$
B_8 B_7 B_6 B_5 A_8 A_7 A_6 A_5
B_4 B_3 B_2 B_1 A_4 A_3 A_2 A_1
C_0
4 3 2 1 4 3 2 1 C_{in}
B A
Σ
C_{out} 4 3 2 1
C_{16}
$\Sigma_{16}\Sigma_{15}\Sigma_{14}\Sigma_{13}$
$\Sigma_{12}\Sigma_{11}\Sigma_{10}\Sigma_9$
Σ_8 Σ_7 Σ_6 Σ_5
Σ_4 Σ_3 Σ_2 Σ_1

Performance Characteristics and Parameters（性能特性与参数）

- *Definition of Propagation Delay Time（传播时延）* t_P: the time interval between a specified reference on the input pulse and a corresponding reference point on the resulting output pulse. （输入脉冲的某一参考电平到输出脉冲的对应参考电平之间的时间间隔）
- The term low speed and high speed（低速与高速）, applied to logic circuits refer to the propagation delay time. The shorter the propagation delay and the higher the frequency at which it can operate. （一个电路的高速与低速的区别通常是指该电路的传播时延参数，传播时延越小，电路速度越快）

Measurement of t_P

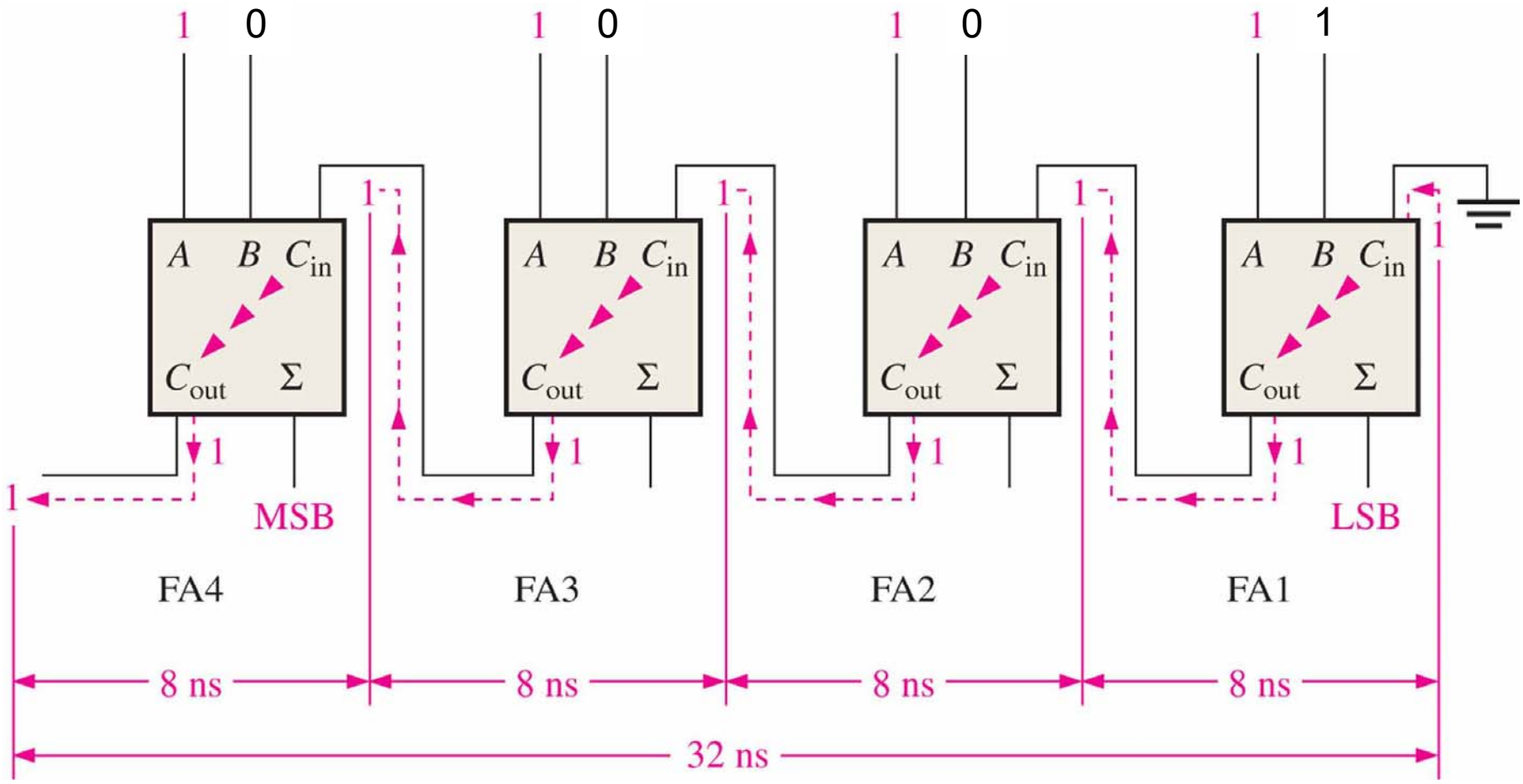
- t_{PHL}（high to low ）
- t_{PLH}（low to high）



Comparison of t_P

	Series	Typical delay time
1	TTL standard-series （TTL标准系列）	11ns
2	TTL F-series（TTL高速系列）	3.3ns
3	CMOS HCT-series （CMOS高速系列）	7ns
4	CMOS AC-series （先进CMOS电路系列）	5ns
5	CMOS ALVC-series	3ns
6	ECL (Emitter Coupled Logic) 射极耦合逻辑（工作在非饱和态）	0.22ns

The disadvantage of Ripple Carry Adder
(级联进位加法器)



Look-ahead carry addition
（超前进位加法器）

- The ***look-ahead carry adder*** anticipates the output carry based on the input bits, and produces the output carry by either ***carry generation*** or ***carry propagation***.

（能够提前预测进位的加法器）

The Look-Ahead Carry Adder (I)
(进位加法器)

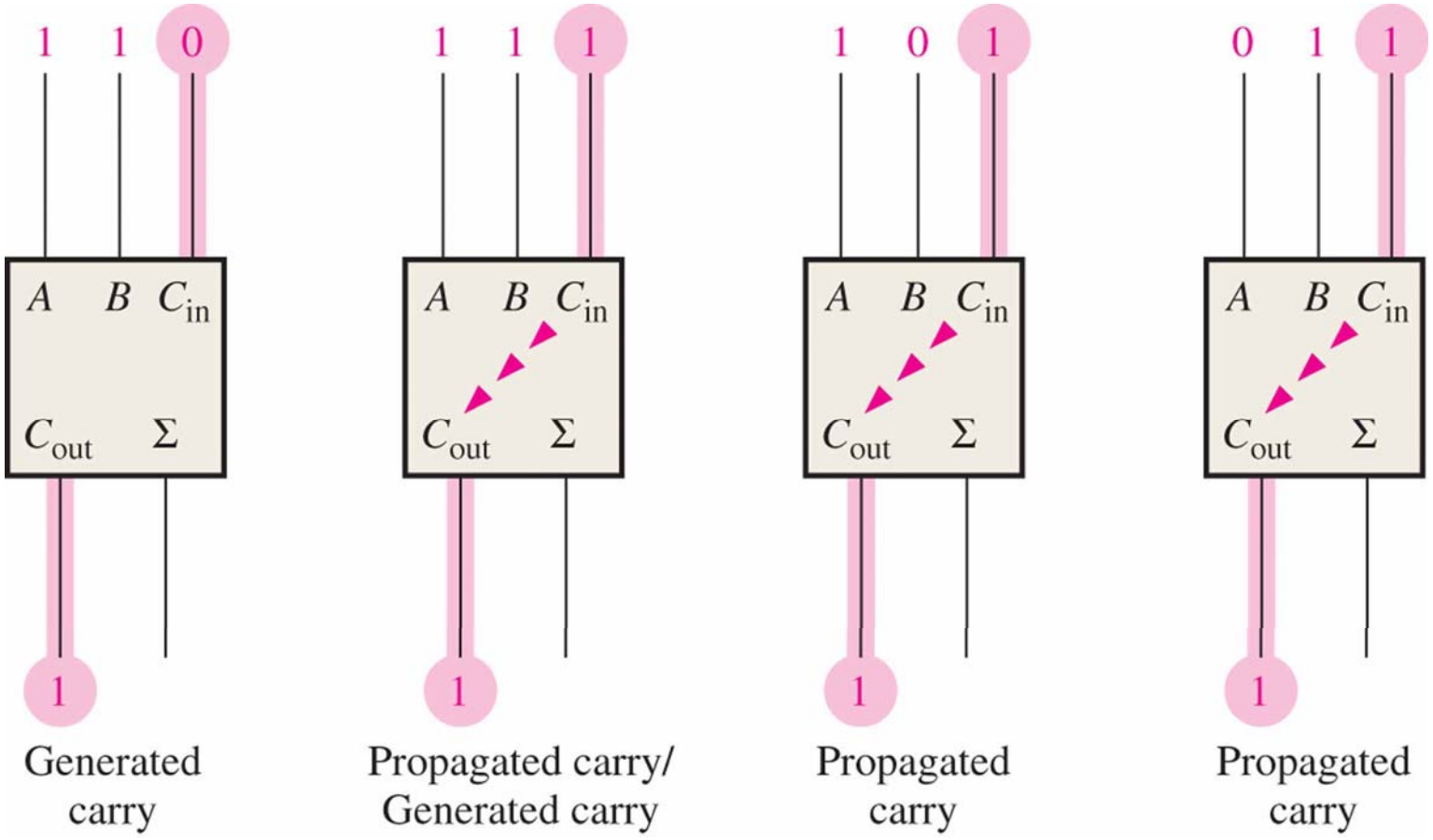
- **Carry generation**（进位产生项）: occurs when an output carry is produced internally by the full adder. That is both input bits are 1s.
- 进位项是由该全加器自身的输入产生，也就是全加器的两个输入都是1的情况

$$C_g\left(\text{or } \text{g}\right) = AB$$

The Look-Ahead Carry Adder (I)
(进位加法器)

- **Carry propagation** （进位传递项）: occurs when the input carry is rippled to become the output carry. An input carry may be propagated by the full-adder when either or both of the input bits are 1s.
- 进位传递项表示该全加器的进位输出是其进位输入传递产生。该情况发生是当输入的两个相加项至少一个为1。

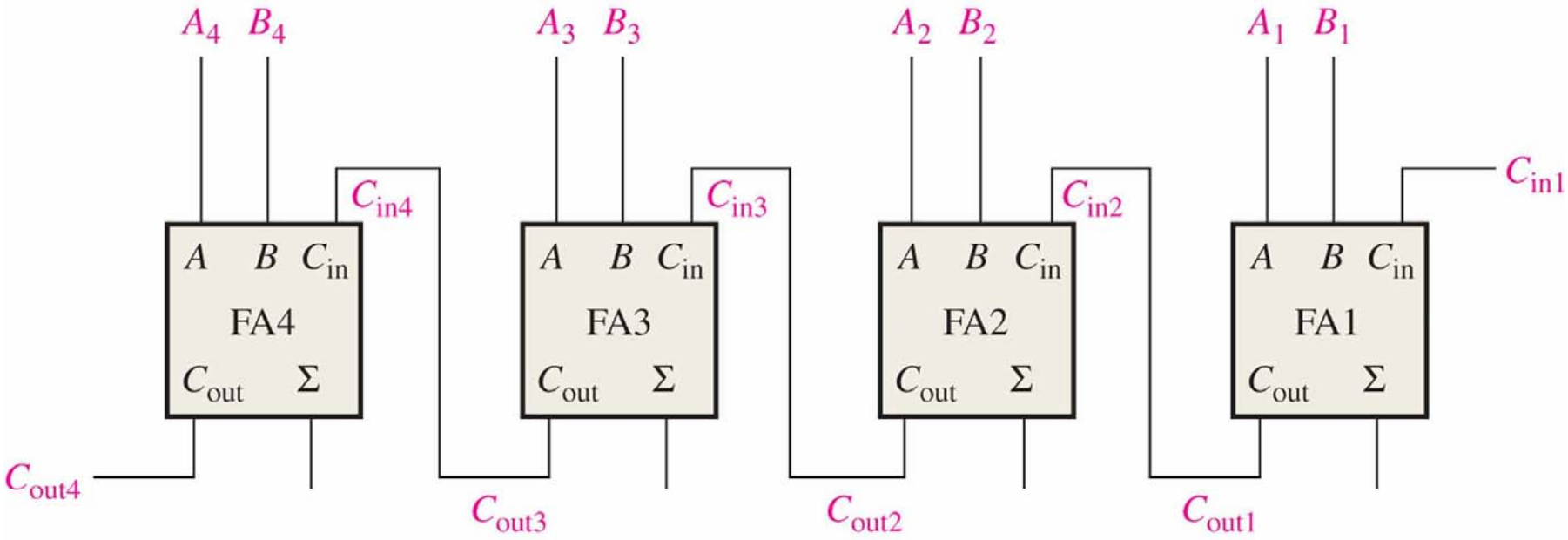
$$C_p\left(\text{or } p\right) = A + B$$



$$C_{out} = C_g + C_p C_{in}$$

$$\left(C_{out} = g + pC_{in}\right)$$

The Look-Ahead Carry Adder (II)



Full-adder 4

$C_{g4} = A_4 B_4$

$C_{p4} = A_4 + B_4$

Full-adder 3

$C_{g3} = A_3 B_3$

$C_{p3} = A_3 + B_3$

Full-adder 2

$C_{g2} = A_2 B_2$

$C_{p2} = A_2 + B_2$

Full-adder 1

$C_{g1} = A_1 B_1$

$C_{p1} = A_1 + B_1$

The Look-Ahead Carry Adder (II)

- **Full-adder 1**: $C_{out} = C_g + C_p C_{in}$
- **Full-adder 2**: $C_{in2} = C_{out1}$

$$\begin{aligned} C_{out2} &= C_{g2} + C_{p2} C_{in2} = C_{g2} + C_{p2} C_{out1} \\ &= C_{g2} + C_{p2} \left(C_{g1} + C_{p1} C_{in1} \right) \\ &= C_{g2} + C_{p2} C_{g1} + C_{p2} C_{p1} C_{in1} \end{aligned}$$

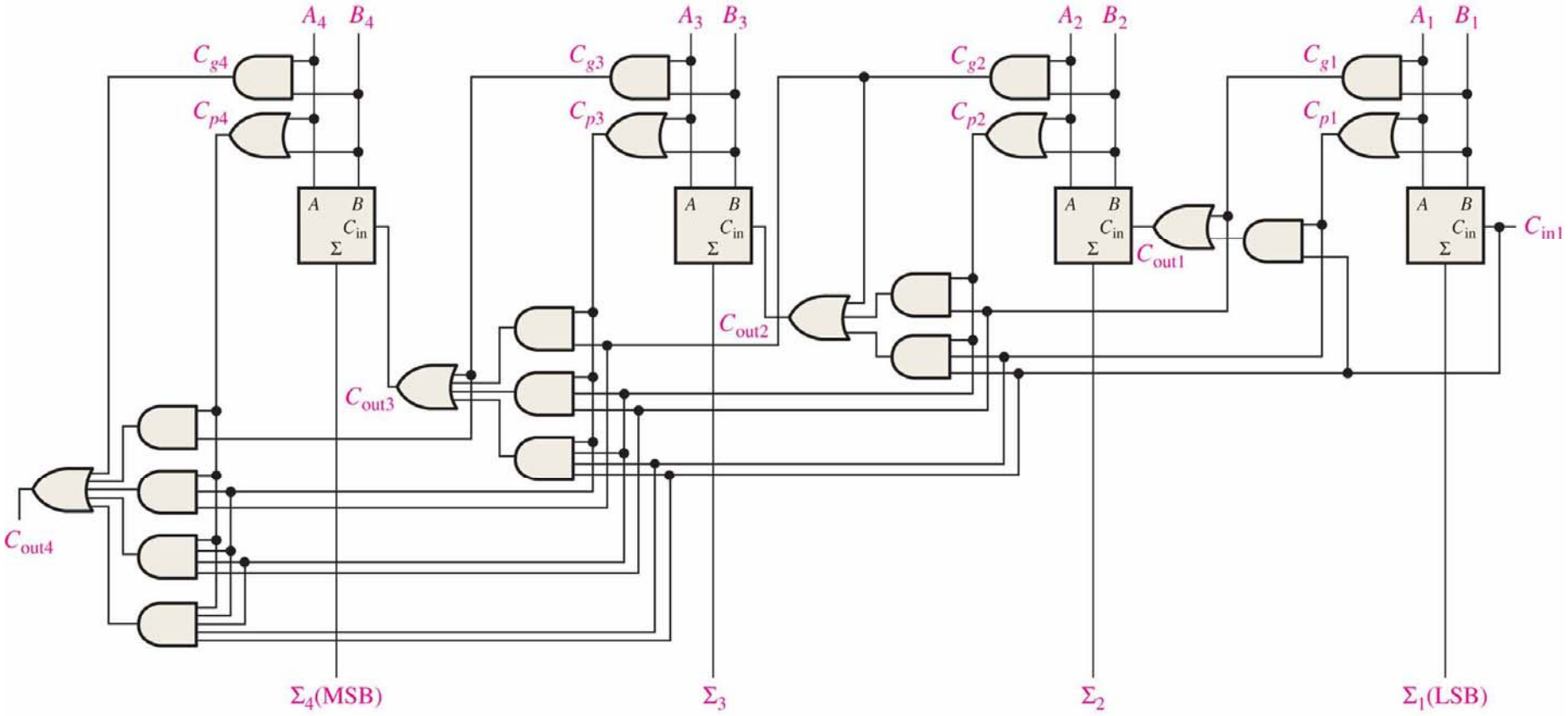
- **Full-adder 3**: $C_{in3} = C_{out2}$

$$\begin{aligned} C_{out3} &= C_{g3} + C_{p3} C_{in3} = C_{g3} + C_{p3} C_{out2} \\ &= C_{g3} + C_{p3} C_{g2} + C_{p3} C_{p2} C_{g1} + C_{p3} C_{p2} C_{p1} C_{in1} \end{aligned}$$

The Look-Ahead Carry Adder (II)

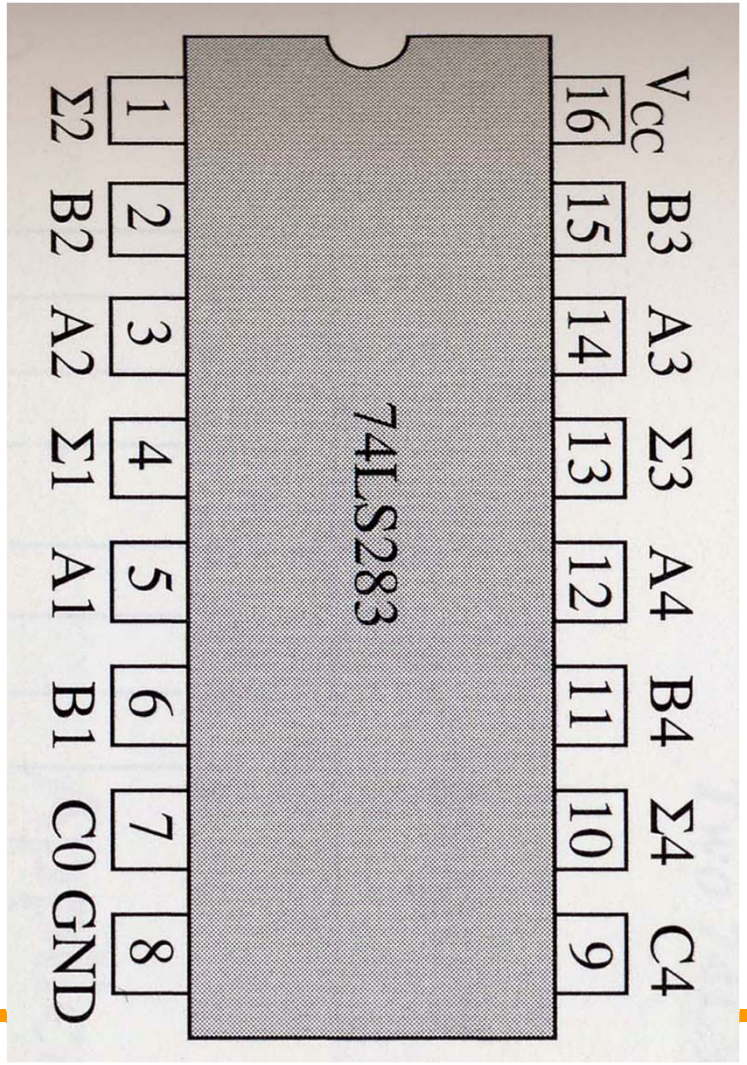
- **Full-adder 4:** $C_{in4} = C_{out3}$

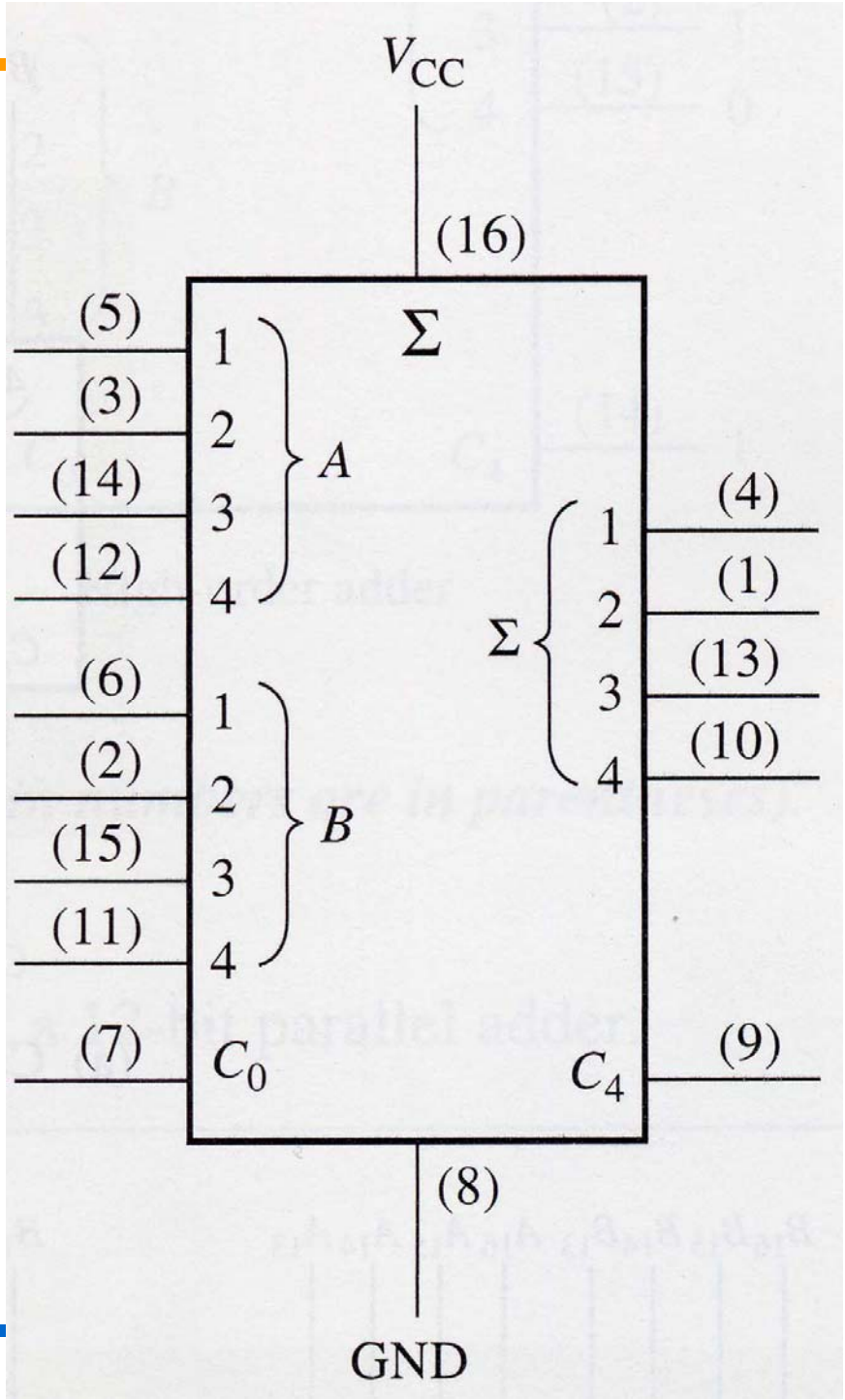
$$C_{out4} = C_{g4} + C_{p4}C_{in4} = C_{g4} + C_{p4}C_{out3}$$
$$= C_{g4} + C_{p4}C_{g3} + C_{p4}C_{p3}C_{g2} + C_{p4}C_{p3}C_{p2}C_{g1} + C_{p4}C_{p3}C_{p2}C_{p1}C_{in1}$$


A_4 B_4
C_{g4}
C_{p4}
A B
C_{in}
Σ
A_3 B_3
C_{g3}
C_{p3}
A_2 B_2
C_{g2}
C_{p2}
A_1 B_1
C_{g1}
C_{p1}
C_{in1}
C_{out1}
C_{out2}
C_{out3}
C_{out4}
Σ_4(MSB)
Σ_3
Σ_2
Σ_1(LSB)

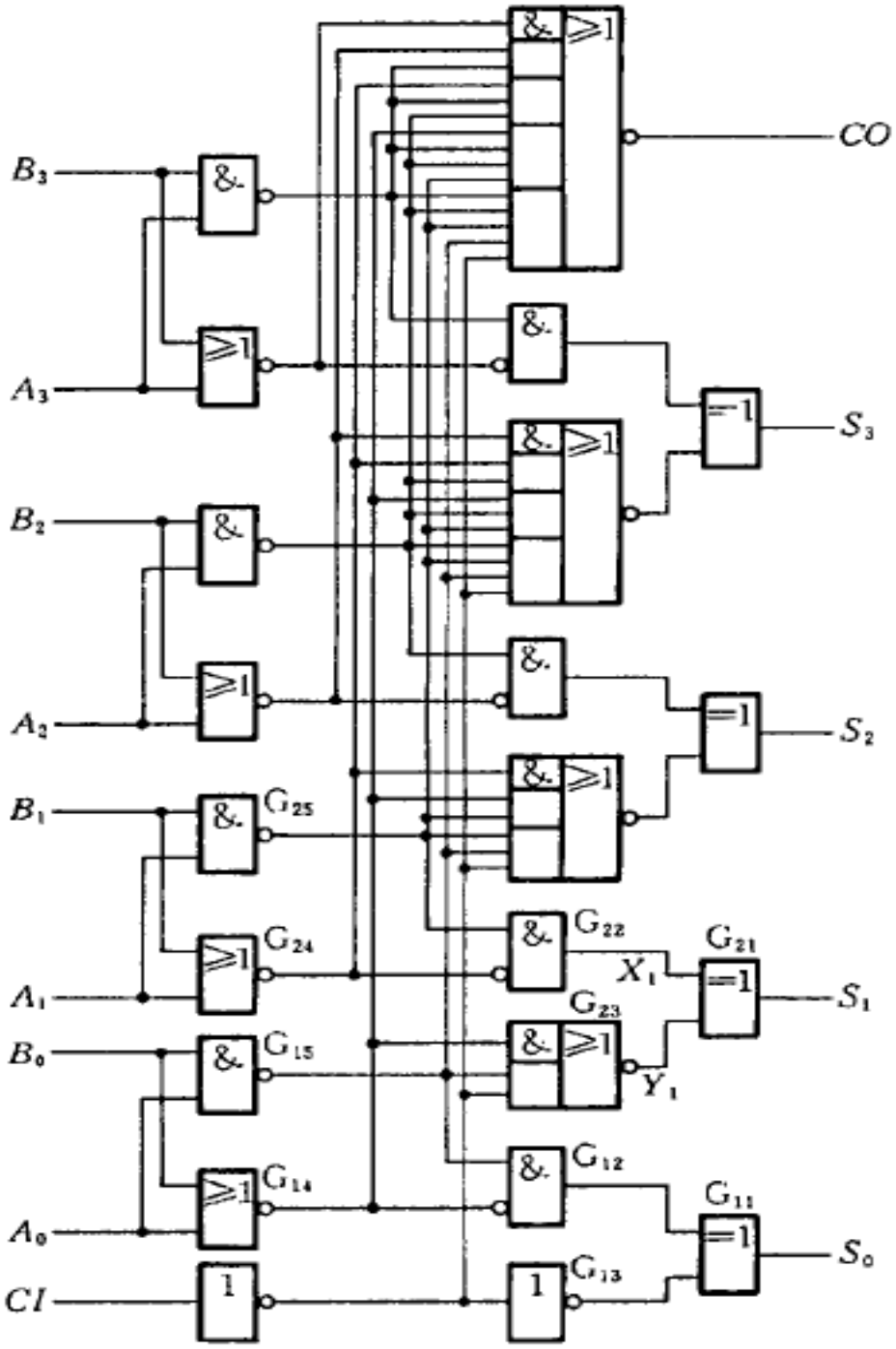
MSI Adders

74LS283





logic diagram of 74LS283



Application Example

A voting system