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DOCUMENT DESCRIPTION

Schematic Checklist for the USB2513B, 36-pin QFN Package

MICROCHIP

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Schematic Checklist for USB2513B

Information Particular for the 36-pin QFN Package

USB Upstream Interface Port 0:

1. USBDP_UP (pin 31), this pin is the USB Upstream channel positive data pin. This pin should be connected directly to pin 3 (D+) on a standard 4-pin, upstream USB connector (Type "B").

2. USBDM_UP (pin 30), this pin is the USB Upstream channel negative data pin. This pin should be connected directly to pin 2 (D-) on a standard 4-pin, upstream USB connector (Type "B").

3. Typical applications will connect pin 4 (Ground) on a standard 4-pin, upstream USB connector (Type "B") directly to digital ground.

4. Pin 1 (VBUS) on the Upstream USB connector can be configured in one of two ways. In Bus-Powered Mode, pin 1 draws +5V power (VBUS) from the Host side and typically powers a +3.3V regulator to power the system. In Self-Powered Mode, pin 1 (VBUS) simply acts as a sensory circuit in order to alert the Hub that a Host is connected.

5. The two metal shield connections on the USB connector should be connected directly to a suitable chassis ground plane.

VBUS_DET Configurations:

Possible VBUS_DET pin (pin 27) connections are dictated by the hardware configuration of the USB link. Possible designs are "Self-Powered Mode", "Self-Powered Permanently Attached Mode" and "Bus-Powered Mode". These three possible configurations are depicted below.

Self-Powered Mode:
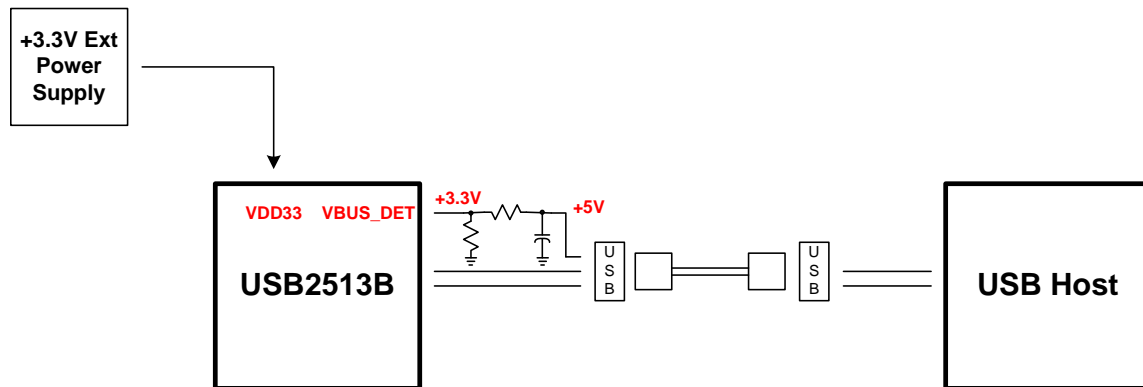
1. In this application, the VBUS_DET pin (pin 27) is driven by a voltage divider circuit that drops the +5V VBUS voltage to +3.3V.

2. For the voltage divider, a series 100K ohm resistor with a 100K ohm resistor to digital ground is recommended.

3. A 1.0 uF capacitor is also recommended on pin 1 (VBUS) of the USB connector.

Self-Powered Permanently Attached Mode:


```
+3.3V Ext
Power
Supply

VDD33    VBUS_DET

USB2513B                    USB Host
```
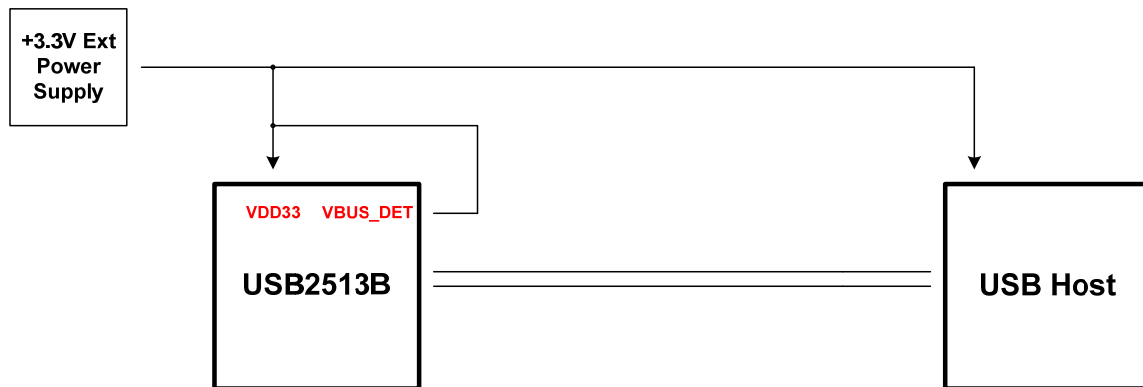
1. In this application, the VBUS_DET pin (pin 27) is driven by the same power rail that powers both the USB2513B and the USB Host.

2. A series resistor (820 ohms to 10K ohms) may be used on the VBUS_DET pin in order to improve susceptibility characteristics.

Bus-Powered Mode:

```
                    +------------------+
                    |  +5.0V-to-       |
                    |  +3.3V           |
                    |  Regulator       |
                    +------------------+

     +-------------------------+                    +----------------+
     |                         |          +5V       |                |
     | VDD33    VBUS_DET       |        U            |                |
     |                         |        S            |                |
     |   USB2513B              |===[ ]  B  [ ]==[ ]  U  ===  USB Host |
     |                         |===                  S               |
     |                         |                     B  ===           |
     +-------------------------+                    +----------------+
```
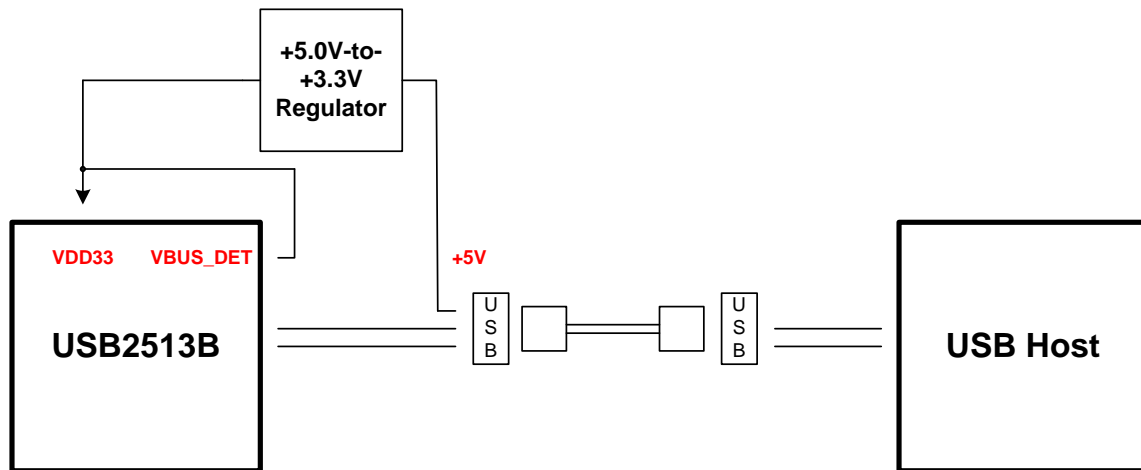
1. Typical Bus-Powered applications will connect pin 1 (VBUS) on a standard 4-pin, upstream USB connector (Type "B") directly to a 2000 mA ferrite bead. This ferrite bead will in turn feed a LDO +5.0V-to-+3.3V voltage regulator to power the USB2513B.

2. We recommend no bulk capacitance be placed on pin 1 (VBUS) of the USB connector in Bus-Powered applications. On the voltage regulator side of the ferrite bead, we recommend limiting the bulk capacitance to 4.7 uF. This should satisfy the 10.0 uF total capacitance to limit in-rush current as required by the USB-IF specification.

3. VBUS_DET (pin 27), this pin detects the state of the supplied upstream power. This pin must be tied to VDD33 when operating in Bus-Powered mode.

4. A series resistor (820 ohms to 10K ohms) may be used on the VBUS_DET pin in order to improve susceptibility characteristics.

USB Downstream Interface Port 1:

1. USBDP_DN1 (pin 2), this pin is the USB Downstream Port 1 channel positive data pin. This pin should be connected directly to pin 3 (D+) on a standard 4-pin, downstream USB connector (Type "A").

2. USBDM_DN1 (pin 1), this pin is the USB Downstream Port 2 channel negative data pin. This pin should be connected directly to pin 2 (D-) on a standard 4-pin, downstream USB connector (Type "A").

3. Typical applications will connect pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A") directly to output of a power distribution switch. This will supply power to the downstream device. Other power distribution schemes are possible; see the latest copy of the USB2513B data sheet for more details on using a poly fuse for USB power distribution.

4. In addition, Microchip recommends the addition of a 150 uF capacitor to be placed on pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A"). This will ensure that the required USB Voltage Drop and Voltage Droop specifications are met for the downstream device.

5. Typical applications will connect pin 4 (Ground) on a standard 4-pin, downstream USB connector (Type "A") directly to digital ground.

6. The two metal shield connections on the USB connector should be connected directly to a suitable chassis ground plane.

7. PRTPWR1 (pin 12), this output pin of the USB2513B is connected to the input enable pin on the USB Port Power Controller for Port 1. PRTPWR1 is an active-high enable signal. When enabled, the USB Port Power Controller will supply +5V VBUS power to pin 1 on the downstream USB connector.

   For this reason, care must be taken when selecting a power distribution switch for the USB2513B. Power distribution switches are available with active high enables or active low enables. Active low enable parts will not work with the USB2513B. The power distribution switch must have an active high enable input and an over-current fault indication active low output.

8. OCS_N1 (pin 13), this input pin samples the Flag (or Over Current Sense) output signal from the power distribution switch for Port 1. An over-current condition is indicated when the signal is low.

USB Downstream Interface Port 2:

1. USBDP_DN2 (pin 4), this pin is the USB Downstream Port 2 channel positive data pin. This pin should be connected directly to pin 3 (D+) on a standard 4-pin, downstream USB connector (Type "A").

2. USBDM_DN2 (pin 3), this pin is the USB Downstream Port 3 channel negative data pin. This pin should be connected directly to pin 2 (D-) on a standard 4-pin, downstream USB connector (Type "A").

3. Typical applications will connect pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A") directly to output of a power distribution switch. This will supply power to the downstream device. Other power distribution schemes are possible; see the latest copy of the USB2513B data sheet for more details on using a poly fuse for USB power distribution.

4. In addition, Microchip recommends the addition of a 150 uF capacitor to be placed on pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A"). This will ensure that the required USB Voltage Drop and Voltage Droop specifications are met for the downstream device.

5. Typical applications will connect pin 4 (Ground) on a standard 4-pin, downstream USB connector (Type "A") directly to digital ground.

6. The two metal shield connections on the USB connector should be connected directly to a suitable chassis ground plane.

7. PRTPWR2 (pin 16), this output pin of the USB2513B is connected to the input enable pin on the USB Port Power Controller for Port 2. PRTPWR2 is an active-high enable signal. When enabled, the USB Port Power Controller will supply +5V VBUS power to pin 1 on the downstream USB connector.

   For this reason, care must be taken when selecting a power distribution switch for the USB2513B. Power distribution switches are available with active high enables or active low enables. Active low enable parts will not work with the USB2513B. The power distribution switch must have an active high enable input and an over-current fault indication active low output.

8. OCS_N2 (pin 17), this input pin samples the Flag (or Over Current Sense) output signal from the power distribution switch for Port 2. An over-current condition is indicated when the signal is low.

USB Downstream Interface Port 3:

1. USBDP_DN3 (pin 7), this pin is the USB Downstream Port 3 channel positive data pin. This pin should be connected directly to pin 3 (D+) on a standard 4-pin, downstream USB connector (Type "A").

2. USBDM_DN3 (pin 6), this pin is the USB Downstream Port 3 channel negative data pin. This pin should be connected directly to pin 2 (D-) on a standard 4-pin, downstream USB connector (Type "A").

3. Typical applications will connect pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A") directly to output of a power distribution switch. This will supply power to the downstream device. Other power distribution schemes are possible; see the latest copy of the USB2513B data sheet for more details on using a poly fuse for USB power distribution.

4. In addition, Microchip recommends the addition of a 150 uF capacitor to be placed on pin 1 (VCC) on a standard 4-pin, downstream USB connector (Type "A"). This will ensure that the required USB Voltage Drop and Voltage Droop specifications are met for the downstream device.

5. Typical applications will connect pin 4 (Ground) on a standard 4-pin, downstream USB connector (Type "A") directly to digital ground.

6. The two metal shield connections on the USB connector should be connected directly to a suitable chassis ground plane.

7. PRTPWR3 (pin 18), this output pin of the USB2513B is connected to the input enable pin on the USB Port Power Controller for Port 3. PRTPWR3 is an active-high enable signal. When enabled, the USB Port Power Controller will supply +5V VBUS power to pin 1 on the downstream USB connector.

   For this reason, care must be taken when selecting a power distribution switch for the USB2513B. Power distribution switches are available with active high enables or active low enables. Active low enable parts will not work with the USB2513B. The power distribution switch must have an active high enable input and an over-current fault indication active low output.

8. OCS_N3 (pin 19), this input pin samples the Flag (or Over Current Sense) output signal from the power distribution switch for Port 3. An over-current condition is indicated when the signal is low.
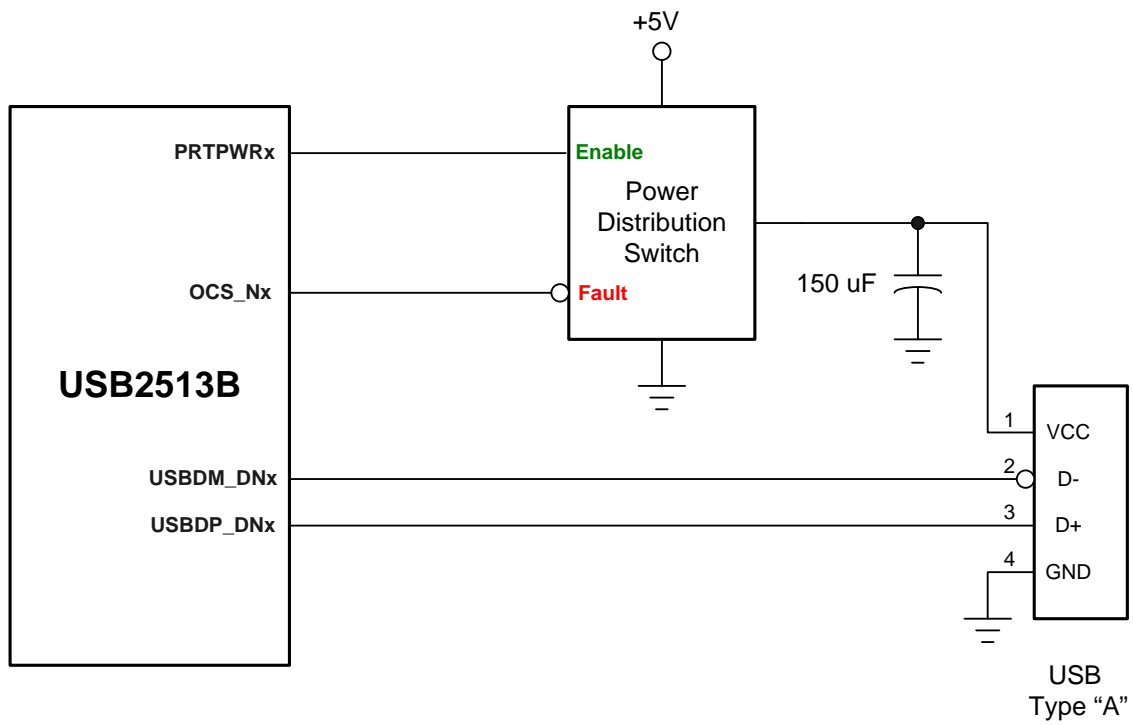
+5V

PRTPWRx   Enable

Power
Distribution
Switch

OCS_Nx   Fault

USB2513B

150 uF

1   VCC

USBDM_DNx   2   D-

USBDP_DNx   3   D+

4   GND

USB
Type "A"

Figure 1 – Typical USB2513B USB Downstream Port Application

+3.3V Power Supply Connections:

1. The digital supply (VDD33) pins on the USB2513B QFN are 15 & 23. They require a connection to +3.3V.

2. Each VDD33 power pin should have one .01 μF (or smaller) capacitor to decouple the USB2513B. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (VDDA33) pins on the USB2513B QFN are 5, 10, 29 & 36. They require a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. Each VDDA33 pin should have one .01 μF (or smaller) capacitor to decouple the USB2513B. The capacitor size should be SMD_0603 or smaller.
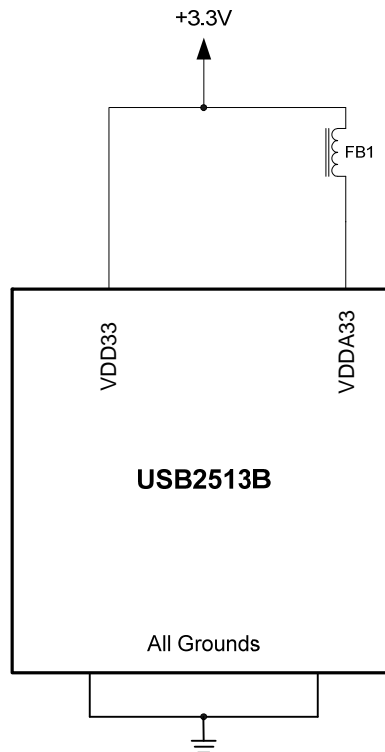

Figure 2 - +3.3V Power Supply Connections

CRFILT:

1. CRFILT (pin 14), this pin provides bypassing for the +1.2V core regulator. The pin requires a 0.01 μF decoupling/bypass capacitor. The capacitor should be located as close as possible to pin 14 without using vias. In addition, pin 14 requires a bulk capacitor placed as close as possible to pin 14. The bulk capacitor must have a value of at least 0.1 μF, and have an ESR (equivalent series resistance) of no more than 2.0 Ω. Microchip recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

   Caution: Even though both are +1.2V levels, **Do Not Connect** CRFILT to PLLFILT.

   Caution: This +1.2V supply is for internal logic only and USB2513B use only. **Do Not** power other external circuits or devices with this supply.

PLLFILT:

1. PLLFILT (pin 34), this pin provides bypassing for the second +1.2V regulator. The pin requires a 0.01 μF decoupling/bypass capacitor. The capacitor should be located as close as possible to pin 34 without using vias. In addition, pin 34 requires a bulk capacitor placed as close as possible to pin 34. The bulk capacitor must have a value of at least 0.1 μF, and have an ESR (equivalent series resistance) of no more than 2.0 Ω. Microchip recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

   Caution: Even though both are +1.2V levels, **Do Not Connect** PLLFILT to CRFILT.

   Caution: This +1.2V supply is for internal logic only and USB2513B use only. **Do Not** power other external circuits or devices with this supply.
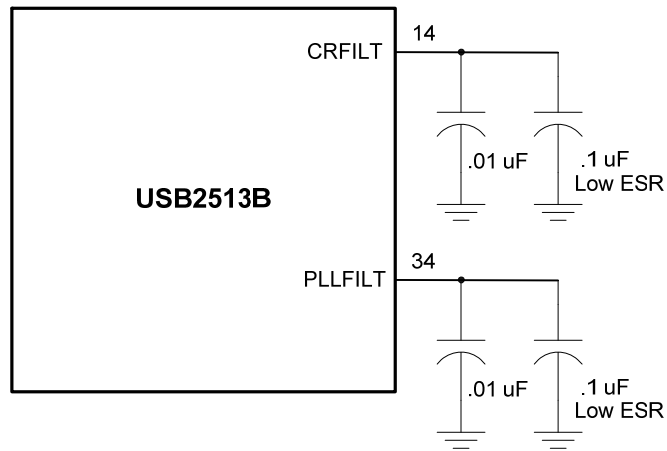
Figure 3 - USB2513B +1.2V Power Connections

Ground Connections:

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the USB2513B QFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the USB2513B must be connected directly to a solid, contiguous digital ground plane.

2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our USB products.

Crystal Connections:

1. A 24.000 MHz crystal must be used with the USB2513B QFN. For exact specifications and tolerances refer to the latest revision USB2513B data sheet.

2. XTALIN (pin 33) on the USB2513B QFN is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XTALOUT (pin 32) on the USB2513B QFN is the clock circuit output. This pin requires a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, the additional external 1.0M Ω resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the USB2513B SQFN.

EEPROM Interface:

1. Enhanced OEM configuration options can be loaded into the USB2513B via the use of an optional external serial I^{2}C EEPROM. Otherwise, the USB2513B will use it's default register values.

2. SCL (pin 24) on the USB2513B QFN connects to the external I^{2}C EEPROM's serial clock pin.

3. SDA (pin 22) on the USB2513B QFN connects to the external I^{2}C EEPROM's serial data pin.

4. Be sure to select a 2-wire style 2K I^{2}C EEPROM that is organized for 256 x 8-bit operation.

5. The hub will read the external EEPROM for configuration data and then attach to the upstream USB host. The hub does not have the capacity to write to the external EEPROM.

SMBus Interface:

1. Enhanced OEM configuration options can also be loaded into the USB2513B via the USB2513B being configured as an SMBus Slave. The Microchip hub can then be configured by an external processor (Master) via the SMBus interface. This strategy is also optional and otherwise, the USB2513B will use it's default register values.

2. SMBCLK (pin 24) on the USB2513B QFN connects to the external SMBus Master's serial clock pin.

3. SMBDATA (pin 22) on the USB2513B QFN connects to the external SMBus Master's serial data pin.

4. The hub waits indefinitely for the SMBus code load to complete and only appears as a newly connected device on USB after the code load is complete. The hub's SMBus acts as a slave-only SMBus device.

5. The 7-bit slave address is 0101100b. The hub will not respond to the general call address of 0000000b.

RBIAS Resistor:

1. RBIAS (pin 35) on the USB2513B QFN should connect to digital ground through a 12.0K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded USB Physical device.

Required External Pull-ups/Pull-downs:

1. SMBCLK (pin 24) requires a 10.0K ohm pull-up resistor (VDD33) in order to guarantee proper operation in SMBus mode.

2. SMBDATA (pin 22) requires a 10.0K ohm pull-up resistor (VDD33) in order to guarantee proper operation in SMBus mode.

Configuration Straps:

1. All configuration strap values are latched in on Power-On Reset and System Reset (if enabled). For more detailed information of each bit and functionality, consult the latest version of the USB2513B data sheet. Input configuration strap options are disabled in SMBus and I^2C EEPROM modes.

2. CFG_SEL1, CFG_SEL0 (pins 25 & 24), these two straps configure the operating mode of the USB2513B. These pins have no internal terminations and must be terminated with the use of external resistors. Either pin can be driven low with an external 100.0K Ω resistor to digital ground or a 10.0K Ω resistor to VDD33. They should not be left floating. The possible modes are as follows:

Mode Configuration Straps	
CFG_SEL[1..0]	**Description**
00	**Default Configuration** Strap Options Enabled, Self-Powered Operation Enabled, Individual Power Switching & Individual Over-Current Sensing
01	**SMBus Slave Configuration** Strap Options Disabled, All Registers Configured Over SMBus
10	**Default Configuration** Strap Options Enabled, Bus-Powered Operation Enabled, Individual Power Switching & Individual Over-Current Sensing
11	**I^2C EEPROM Configuration** Strap Options Disabled, All Registers Configured By I^2C EEPROM

3. NON_REM1, NON_REM0 (pins 22 & 28), these two straps configure the presence of permanently attached (non-removable) devices on the downstream ports of the USB2513B. These pins have no internal terminations and must be terminated with the use of external resistors. Either pin can be driven low with an external 100.0K Ω resistor to digital ground or a 10.0K Ω resistor to VDD33. They should not be left floating. The possible modes are as follows:

NON_REMx Mode Configuration Straps	
NON_REM[1..0]	**Description**
00	All Downstream Ports Are Removable
01	Port 1 Is Non-Removable (Permanently Attached)
10	Port 1 & Port 2 Are Non-Removable (Permanently Attached)
11	Port 1, Port 2 & Port 3 Are Non-Removable (Permanently Attached)

4. **Design Note:** For Removable / Non-Removable cases, there are three configurations:

   A. If a port has a USB connector exposed to the consumer, it is Removable.

   B. If a port does not have a USB connector and never has a device connected, it should be disabled.

   C. If a port does not have a USB connector but usually has a device connected (Permanently Attached), it should be configured as Non-Removable. It is OK for this device to periodically reset and detach.

5. **Design Note:** Describing the Downstream Ports accurately in a USB design as far as Removable / Non-Removable is concerned is important with regards to USB Compliance testing implications. When the USB compliance software runs, it will check for various port functionality (like the ability to wake the device up upon device attach, ability of not to wake up when this function is disabled, etc, etc). This is done by instructing the person who conducts the test to plug-unplug a regular USB mouse to ports under test, multiple times. If the design has embedded devices permanently attached to some ports and they are not declared as "non-removable", the software will assume that these ports are "user accessible", and will wait for operator to plug-unplug the test mouse into it, which obviously will be impossible. So, the test will time-out and fail, failing the entire certification. If your Removable ports are described as Non-Removable at the time of testing, the software will flag the discrepancy between test declarations and descriptors, and the certification will also fail. It is recommended that the design engineer accurately describe the system (Removable / Non-Removable) if USB compliance is important. Some designs may require re-ordering of the USB ports in the schematic to accomplish this.

6. LOCAL_PWR (pin 28), this input configuration strap is **only** operational when Dynamic Power Switching is Enabled. A USB register write is required to enable Dynamic Power Switching in the hub. See the data sheet for more details. The LOCAL_PWR pin, when enabled, configures the hub for either Bus-Powered operation or Self-Powered operation. The settings are as follows:

    0 = Bus-Powered (Hub gets all it's from the Upstream USB VBUS)
    1 = Self-Powered

    See the latest version of the USB2513B data sheet for complete details.

7. PRT_DIS_P1 (pin 2) and PRT_DIS_M1 (pin 1), if input configuration strap options are enabled, these two pins enable / disable the Down Stream Port 1 on the Hub. The two terminations should be referenced to VDD33. Both pins must be terminated in the same manner; the settings are as follows:

    0 = Port 1 Enabled (No External Terminations Added)
    1 = Port 1 Disabled (10.0K Ω Added to Both Pins)

    See the latest version of the USB2513B data sheet for complete details.

8. PRT_DIS_P2 (pin 4) and PRT_DIS_M2 (pin 3), if input configuration strap options are enabled, these two pins enable / disable the Down Stream Port 2 on the Hub. The two terminations should be referenced to VDD33. Both pins must be terminated in the same manner; the settings are as follows:

    0 = Port 1 Enabled (No External Terminations Added)
    1 = Port 1 Disabled (10.0K Ω Added to Both Pins)

    See the latest version of the USB2513B data sheet for complete details.

9. PRT_DIS_P3 (pin 7) and PRT_DIS_M3 (pin 6), if input configuration strap options are enabled, these two pins enable / disable the Down Stream Port 3 on the Hub. The two terminations should be referenced to VDD33. Both pins must be terminated in the same manner; the settings are as follows:

> 0 = Port 1 Enabled (No External Terminations Added)
> 1 = Port 1 Disabled (10.0K Ω Added to Both Pins)

See the latest version of the USB2513B data sheet for complete details.

10. BC_EN1 (pin 12), if input configuration strap options are enabled, this pin enables / disables the battery charging protocol on Downstream Port 1. When supporting the battery charging protocol, the hub also supports external port power controllers. The battery charging protocol enables a device to draw the currents per the USB battery charging specification. The termination should be referenced to VDD33. The settings are as follows:

> 0 = Battery Charging Feature Is Not Supported Port 1 (internal PD)
> 1 = Battery Charging Feature Is Supported Port 1 (10.0K Ω Added)

See the latest version of the USB2513B data sheet for complete details.

11. BC_EN2 (pin 16), if input configuration strap options are enabled, this pin enables / disables the battery charging protocol on Downstream Port 2. When supporting the battery charging protocol, the hub also supports external port power controllers. The battery charging protocol enables a device to draw the currents per the USB battery charging specification. The termination should be referenced to VDD33. The settings are as follows:

> 0 = Battery Charging Feature Is Not Supported Port 2 (internal PD)
> 1 = Battery Charging Feature Is Supported Port 2 (10.0K Ω Added)

See the latest version of the USB2513B data sheet for complete details.

12. BC_EN3 (pin 18), if input configuration strap options are enabled, this pin enables / disables the battery charging protocol on Downstream Port 3. When supporting the battery charging protocol, the hub also supports external port power controllers. The battery charging protocol enables a device to draw the currents per the USB battery charging specification. The termination should be referenced to VDD33. The settings are as follows:

> 0 = Battery Charging Feature Is Not Supported Port 3 (internal PD)
> 1 = Battery Charging Feature Is Supported Port 3 (10.0K Ω Added)

See the latest version of the USB2513B data sheet for complete details.

13. **Design Note:** The USB2513B supports the USB Battery Charging Specification Revision 1.1 for Charging Downstream Ports (CDP). When configured for Battery Charging Mode, the PRTPWR[3..1] pin behavior is different than Non-Battery Charging mode operation. Also, when configured for CDP, the +5V VBUS supply and the Port Power Controller / Over-Current Protection device(s) must be able to support 1.5 amps of power; so device selection is important. When not supporting Battery Charging, the +5V VBUS rail and PPC / OCP devices need only to be rated for 0.8 amps of power. See the latest USB2513B data sheet for more details on this subject.

Miscellaneous:

1. RESET_N (pin 26), is an active-low reset input. This signal resets all logic and registers within the USB2513B. A hardware reset (RESET_N assertion) is required following power-up. Please refer to the latest copy of the USB2513B data sheet for reset timing requirements. Microchip does not recommend the use of an RC circuit for this required pin reset. A reset generator / voltage monitor is one option to provide a proper reset. Better yet, for increased design flexibility, a controllable reset (GPIO, dedicated reset output) should be considered. In this case, Microchip recommends a push-pull type output (not an open-drain type) for the monotonic reset to ensure a sharp rise time transition from low-to-high.

2. HS_IND (pin 25), this pin indicates the Upstream Port speed connection. See the latest version of the USB2513B data sheet for complete details.

> 0 = Hub Is Connected At Full Speed (12 Mbit/s)
> 1 = Hub Is Connected At High Speed (480 Mbit/s)

3. SUSP_IND (pin 28), this pin indicates the USB State of the USB2513B. See the latest version of the USB2513B data sheet for complete details.

> 0 = Hub Is Unconfigured **Or** Configured And In USB Suspend Mode
> 1 = Hub Is Configured And Is Active (Not In Suspend)

4. TEST (pin 11), this pin must be tied directly to digital ground in order to ensure proper operation.

5. Incorporate a large SMD resistor (SMD_1210) to connect the USB chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

6. Be sure to incorporate enough bulk capacitors (4.7 - 22µF caps) for each power plane.

USB2513B QFN QuickCheck Pinout Table:

Use the following table to check the USB2513B QFN shape in your schematic.

	USB2513B QFN		
Pin No.	Pin Name	Pin No.	Pin Name
1	USBDM_DN1 / PRT_DIS_M1	19	OCS_N3
2	USBDP_DN1 / PRT_DIS_P1	20	NC
3	USBDM_DN2 / PRT_DIS_M2	21	NC
4	USBDP_DN2 / PRT_DIS_P2	22	SDA / SMBDATA / NON_REM1
5	VDDA33	23	VDD33
6	USBDM_DN3 / PRT_DIS_M3	24	SCL / SMBCLK / CFG_SEL0
7	USBDP_DN3 / PRT_DIS_P3	25	HS_IND / CFG_SEL1
8	NC	26	RESET_N
9	NC	27	VBUS_DET
10	VDDA33	28	SUSP_IND / LOCAL_PWR / NON_REM0
11	TEST	29	VDDA33
12	PRTPWR1 / BC_EN1	30	USBDM_UP
13	OCS_N1	31	USBDP_UP
14	CRFILT	32	XTALOUT
15	VDD33	33	XTALIN / CLKIN
16	PRTPWR2 / BC_EN2	34	PLLFILT
17	OCS_N2	35	RBIAS
18	PRTPWR3 / BC_EN3	36	VDDA33
37		EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package	

Notes:

USB2513B QFN Package Drawing:
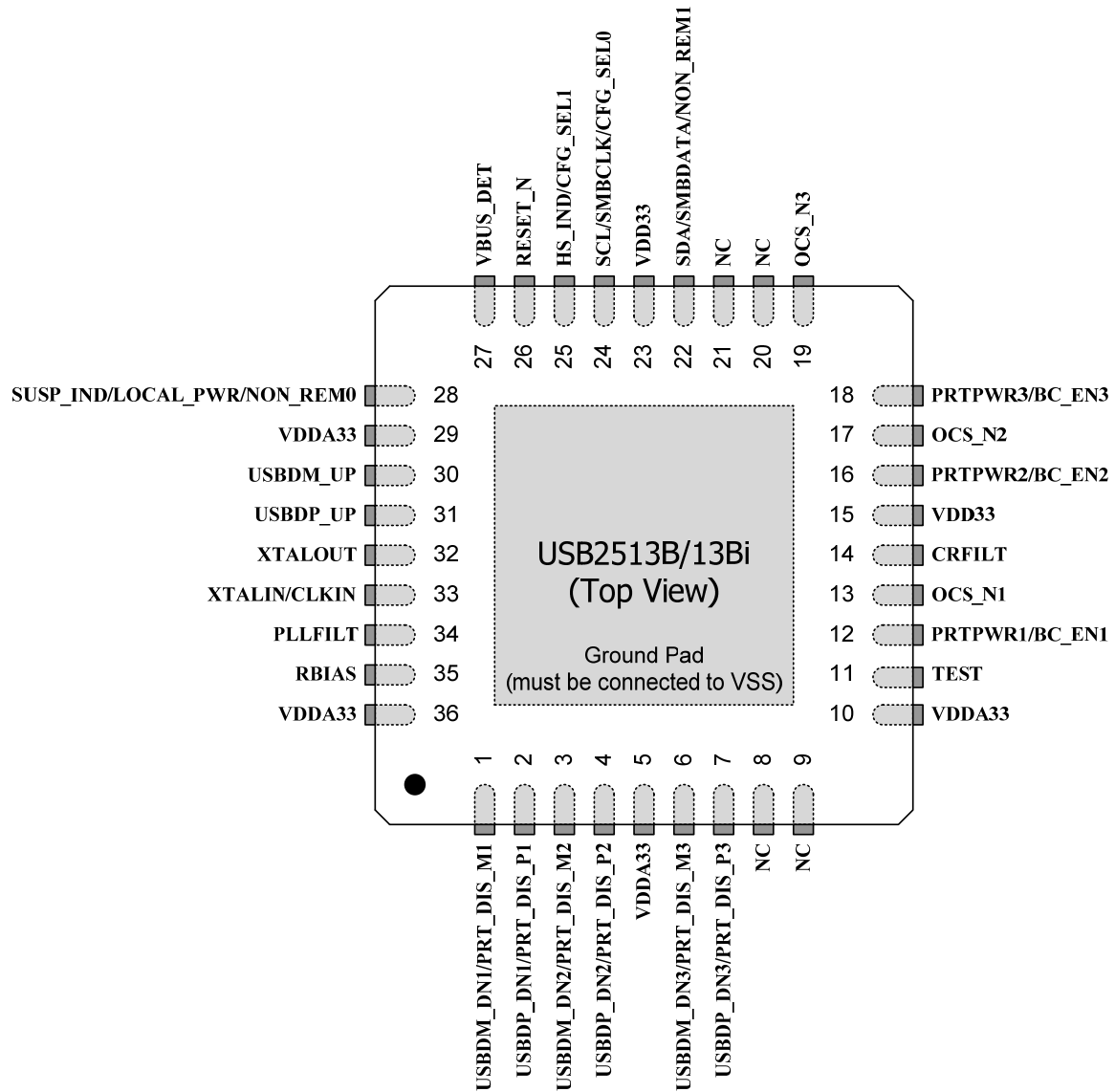
Indicates pins on the bottom of the device.

Reference Material:

1. Microchip USB2513B Data Sheet; check web site for latest revision.

2. Microchip USB2514B CEB Schematic, Assembly EVB-USB2514; check web site for latest revision.

3. Microchip USB2514B CEB PCB, Assembly EVB-USB2514; order PCB from web site.

4. Microchip USB2514B CEB PCB Bill of Materials, Assembly EVB-USB2514; check web site for latest revision.

5. CEB stands for Customer Evaluation Board.

6. Microchip USB2514B Reference Design, check web site for latest revision.

7. Microchip Reference Designs are schematics only; there are no associated PCBs.