Computer Science and Engineering 431
Computer Architecture
Fall 2015

Course Project

Distributed: Nov 3, 2015 **Due:** Dec 14, 2015 **Points**: 45

In this SimpleScalar final project you are going to construct your own set of experiments to try to find the "best" design. This can be a team-of-two project or, only with prior permission from me, an individual project. Of course, I will expect more experimentation from a team project than from an individual project.

Your **baseline** datapath is a single instruction, in-order issue, pipelined datapath with predict-not-taken branch prediction.

```
sim: command line: /home/software/simplesim/simplesim-3.0/sim-outorder
-fastfwd 500000 –max:inst 2500000 –fetch:ifqsize 1 –fetch:speed 1
–fetch:mplat 3 –bpred nottaken –bpred:ras 0 –decode:width 1
–issue:width 1 –issue:inorder true –issue:wrongpath false –ruu:size 4
–lsq:size 2 –res:ialu 1 –res:imult 1 –res:fpalu 1 –res:fpmult 1
–res:memport 2 -cache:il1 il1:1024:8:1:r -cache:il2 dl2
-cache:dl1 dl1:1024:8:1:r -cache:dl2 ul2:2048:16:2:r -itlb:16:4096:4:r
–dtlb:32:4096:4:r –cache:dl1lat 1 –cache:il1lat 1 –cache:dl2lat 5
-cache:il2lat 5 –mem:lat 90 10 –mem:width 8
```

The baseline system memory hierarchy settings are il1:1024:8:1:r and dl1:1024:8:1:r (8KB direct mapped L1 caches with 1 word (8B) blocks (remember this is a 64 bit/word machine), random replacement policy), ul2:2048:16:2:r (a unified 64KB 2-way set associative L2 cache with 2 word (16B) blocks), memory latency = 90 cycles for the first and 10 for the rest (so 100 cycles for 2 word (16B) blocks). Settings not specified in the above config file should their default value.

Your assignment is to experiment with the datapath and memory hierarchy design to come up with the "best" performing design(s) in term of two geometric means of the execution time ([IC x clock_cycle_time]/IPC), one for the four integer benchmarks and one for the two floating point benchmarks. It could be that the best performing design for the integer benchmarks is different than the one for the floating point benchmarks. The IC (instruction's (*committed*) count) for each benchmark is a constant (2,500,000). Thus you will be trying to optimize `sim_IPC` and the clock cycle time. The clock cycle time is determined by the issue width and datapath type: static single issue (baseline), static superscalar (SS), or dynamic superscalar (SS) as follows:

Static, issue width (baseline) = 1 means a 100 ps clock cycle
Static, issue width = 2 means a 115 ps clock cycle
Static, issue width = 3 means a 130 ps clock cycle
Static, issue width = 4 means a 145 ps clock cycle

Dynamic, issue width = 2 means a 125 ps clock cycle
Dynamic, issue width = 4 means a 160 ps clock cycle
Dynamic, issue width = 8 means a 195 ps clock cycle

Other setting constraints are as follows:

1. The il1 block size must match the ifq size (e.g., for the baseline machine the ifqsize is set to 1 word (8B) so the il1 block size is also set to 8B). The dl1 should have the same block size as your il1.
2. The ul2 block size must be at least twice your il1 (dl1) block size with a maximum ul2 block size of 128B. Your ul2 must be at least as large as il1+dl1 in order to be inclusive.
3. The il1 sizes and il1 latencies are linked as follows (the same linkages hold for the dl1 size and dl1 latency):
   il1 = 8 KB (baseline, minimum size) means il1lat = 1
   il1 = 16 KB means il1lat = 2
   il1 = 32 KB means il1lat = 3
   il1 = 64 KB (maximum size) means il1lat = 4
   The above are for direct mapped caches. For 2-way set associative add an additional cycle of latency to each of the above; for 4-way (maximum) add two additional cycles.
4. The ul2 sizes and ul2 latencies are linked as follows:
   ul2 = 64KB (baseline, minimum size) means ul2lat = 5
   ul2 = 128 KB means ul2lat = 6
   ul2 = 256 KB means ul2lat = 7
   ul2 = 512 KB means ul2 lat = 8
   ul2 = 1024 KB (1 MB) (maximum size) means ul2lat = 9
   The above are for 2-way set associative caches. For 4-way set associative add one additional cycle of latency to each of the above; for 8-way add two additional cycles; for 16-way (maximum) add three additional cycles; for direct mapped subtract 1 cycle.
5. All other settings are yours to play with, except
   bpred can be any of the supported schemes except NOT perfect (as perfect cannot be implemented and is just provided in SimpleScalar as a way to tell how close to perfect one of the implementable schemes is)
   mplat is fixed at 3 (default)
   fetch:speed ratio of no more than 4
   ifqsize can be set to a maximum of 16 words (64B)
   decode:width less than or equal to your fetch:ifqsize

the total number of imult+ialu and fpalu+fpmult no more than twice the issue width (so for an issue width of 1, you can have imult+ialu <=2 and fpalu+fpmul <=2)

mem:width (memory bus width) can be either 8B (default) or 16B

memport can be set to a maximum of 2 (default)

mem:lat is fixed at 90 + 10 cycles

tlb:lat is fixed at 30 (default), page size 4096 (default), maximum tlb sizes of 256 entries for itlb and 512 entries for dtlb

bpred:ras maximum size of 16 entries (8 is default)

bpred:btb of 1024 sets, 4 way associative maximum (512,4 is default)

ruu:size no more than 8 times the issue width (so a maximum of 64 (must be a power of two))

lsq:size no more than 4 times the issue width (so a maximum of 32 (must be a power of two))

Your report for the course Project is due (submitted through the Angel dropbox) by midnight the first day of Finals Week, December 14. But you should begin thinking **now** about your plan for experimentation. What series of experiments are you going to run and why? In what order? Without careful thought you could end up running thousands of experiments, many of which will not be useful.

The report should be a minimum of 6, maximum of 10 for individual projects (maximum of 15 for team projects) typed, single space pages in 12 point font for text and tables. Include a cover page on your report (not included in the page count above) that lists team member names and the IPC and execution time (in usec) for the baseline machine for `mcf` and `milc`, the IPC and execution time for your "best" design(s) for `mcf` and `milc` (the best design might be different for `mcf` and `milc`), and the execution time geometric means for the integer and floating point benchmarks for your "best" design(s) overall. The report should be accompanied up a minimum of 4 graphs or bar charts (minimum of 6 for team projects) (included in the page count above) that defend your choice of settings for your "best" performing design(s). As an appendix to your report (so not included in the page count given above), include the configuration files for your baseline and for your "best" designs for `mcf` and `milc`. Also submit them as four separate files (report, baselineconfig, bestmcfconfig, bestmilcconfig) in the Angel dropbox for the Project.

Points will be assigned for best performing design(s), comprehensiveness in experimentation, following the guidelines, clarity, style, neatness (and spelling, grammar, ...).