Student Name:			_ Student ID:				
COMPUTER ORGANIZATION & ARCHITECTURE							
MID-TERM 1 (2013-2014)							
MAX MARKS: 15	5		TIME: 1 HR				
Q1. Answer the follow	wing:		(2)				
addressable? b) How many m	nemory bytes will b	pe required to sto the following va	a 2M X 32 memory if the memory is wordare the 8085 instruction CALL 6400H? alues loaded into its memory locations: (3)				
	Address	Data]				
	800	900	-				
	900	1000					
		1000	-				
	1000	500					
	•••						
	1100	600					
	1600	700					
a) LOAD IMMIb) LOAD DIREc) LOAD INDII	EDIATE 800 CT 800 RECT 900 umulator contents		on of the following instruction: lowing 8085 instructions are being executed (all (3)				

	A	S	Z	CY
MVI A, 80H				
ORA A				
OKA A				
RAR				

PLEASE TURN OVER

Q4. Consider a computer with identical interpreters at levels 1, 2 and 3. It takes an interpreter n instructions to fetch, examine and execute one instruction. A level 1 instruction takes k nanoseconds to execute. How long does it take for an instruction at levels 2 and 3? (1)	
Level 2:	
Level 3:	
Q5. Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program. Computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much? (3)	
Q6. Suppose a program runs in 100 seconds on a computer, with the multiply operations responsible for 80 seconds of this time. How much do I have to improve the speed of multiplication if I want my program to run three times faster? (3)	