THE LNM INSTITUTE OF INFORMATION TECHNOLOGY, JAIPUR

COMPUTER ORGANIZATION & ARCHITECTURE

END-TERM (2013-2014)

MAX MARKS: 100 **TIME: 3 HRS**

Q1. Fill in the blanks: [1 x 11=11]

a) Distributing data over multiple disks in RAID is called _____

b) A single layer blu-ray disk can hold about _____ GB of data.

c) Modems that can transmit in one direction only at a given time are called _____

d) Devices which can initiate bus transfers are called _____

e) The set of pages that a program is actively and heavily using is called the _____

f) A program that generates page faults frequently and continuously is said to be _____

g) Operations that have two operands and produce one result are called _____operations

h) A register pointing to the base of the local stack frame is called _____

i) The acronym AGP stands for _____

j) An LCD display screen consists of two parallel glass plates containing a sealed volume of _____

k) The depressions in the substrate of a CD are called _____

Q2. The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with 4 fields: an opcode field; a mode field to specify 1 of 7 addressing modes; a register address field to specify 1 of 60 registers; and a memory address field. Assume an instruction is 32 bits long. Answer the following: [1 x 5=5]

a) How large must the mode field be?

b) How large must the register field be?

c) How large must the address field be?

d) How large is the opcode field?

e) What is the maximum number of instructions that can be there in the instruction set?

Q3. Write the data path flow for the instruction LOAD R1, 312(R2). Assume that each internal register *R* in the microprocessor has two control signals, R_{in} and R_{out}. The input registers for the ALU are *X* and *Y* and the output register is *Z*. [5]

Q4. Check for data hazard in the following set of instructions for a 5-stage pipeline and possible ways of avoiding it: [2+3=5]

ADD R1, R2, R3

XOR R6, R1, R4

SUB R7, R6, R1

Q5. Assume a 2^{20} byte memory: [2+2=4]

a) What are the lowest and highest addresses if memory is byte-addressable?

b) What are the lowest and highest addresses if memory is word-addressable, assuming a 16-bit word?

Q6. Suppose we wish to evaluate the following expression: [5]

$Z = A / (B \times C \times (D + E))$

Write a program to evaluate the above arithmetic statement using a stack organized computer with zero-address instructions (so only pop and push can access memory).

Q7. Suppose a computer using direct mapped cache has 2^{32} words of main memory and a cache of 1024 blocks, where each cache block contains 32 words. [1+6+4=11]

a) How many blocks of main memory are there?

b) What is the format of a memory address as seen by the cache, that is, what are the sizes of the tag, block, and word fields (assume that byte is not referenced in memory address)?

c) To which cache block will the memory reference $000063FA_{16}$ map?

Q8. A digital camera has a resolution of 3000 x 2000 pixels, with 3 bytes/pixel for RGB color. The manufacturer of the camera wants to be able to write a JPEG image at a 5x compression factor to the flash memory in 2 sec. What data rate is required? [4]

Q9. For a certain program, 2% of the code accounts for 50% of the execution time. Compare the following three strategies with respect to programming time and execution time. Assume that it would take 100 man-months to write it in C, and that assembly code is 10 times slower to write and four times more efficient. [6]

a) Entire program in C.

b) Entire program in assembler.

c) First all in C, then the key 2% rewritten in assembly language.

Q10. A computer with a five-stage pipeline deals with conditional branches by stalling for the next three cycles after hitting one. How much does stalling hurt the performance if 20% of all instructions are conditional branches? Ignore all sources of stalling except conditional branches. [4]

Q11. Write short notes on: [5 x 8=40]

a) Assembler
b) Trap
c) Memory hierarchy
d) DMA
e) 2-level Daisy chain bus arbitration
f) Co-routines
g) External fragmentation
h) Instruction location counter