LNMIIT
The LNM Institute of Information Technology

Electronics II

Mid Semester Exam 1

Date: 25th February 2015 **Time: 90 Minutes** **Max Marks. 40**

Notes: If not mentioned, then use second approximation of diode for problem solving.
Marks of each question are mention against it.
Assumptions made should be written clearly.

Q.1: Design a voltage divider biased Common Emitter configuration BJT amplifier with following specifications. Ic(sat) = 10mA, VCC = 15V , Q point at center of load-line and βdc = 100. [5]

Q.2: Design a two input OR gate using silicon diodes. You can use current limiter resistors with a maximum value of 10kΩ. Explain the working and justify the values of resistors used. [5]

Q.3: For the circuit shown in figure 1, find the labeled node voltages for β =100. [5]

Q.4: For the circuit given in figure 2, find the value of resistor R, so that V_o = 2.7V. Assume that the diodes available have 0.7 Volts drop at 1mA and that ΔV = 0.1V/decade change in current. [5]

Q.5: In figure 3, what is the value of load voltage (Across 1.5kΩ) for each of these cases? [5]
A: Zener diode shorted B: Zener diode open C: Series resistor open D: Load resistor shorted [5]

Q.6: For the circuit given in figure 4, find the current flowing in each resistor and each diode. [5]

Q.7: Analyze the circuit given in figure 5 and find out the values of r_e, I_E, V_C, V_E, A_v, f_{Lc1}, f_{Lc2}, f_{ui}, and f_{uo}. Given Cbc = Cbe = 10pF and βdc = 100. Thus find out 3dB bandwidth of amplifier. [10]

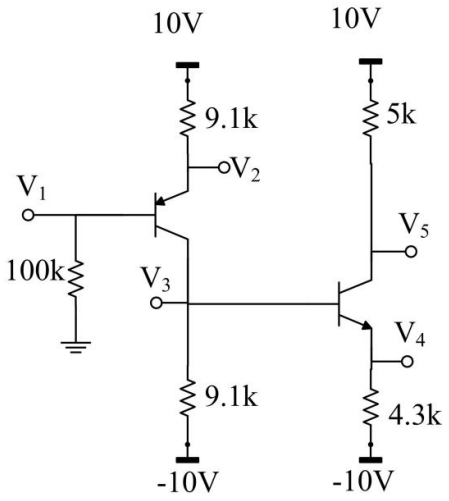

Figure 1

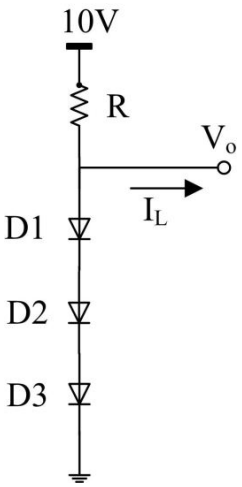

Figure 2

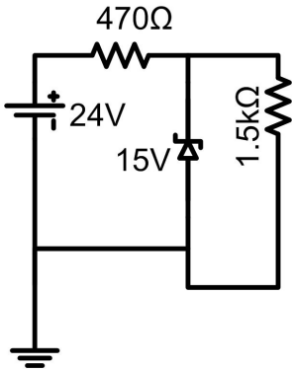

Figure 3

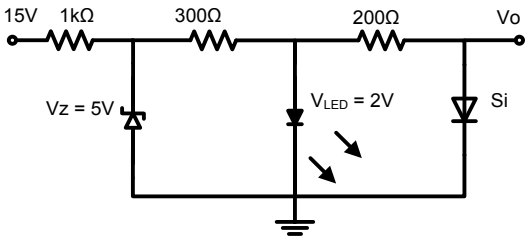

Figure 4

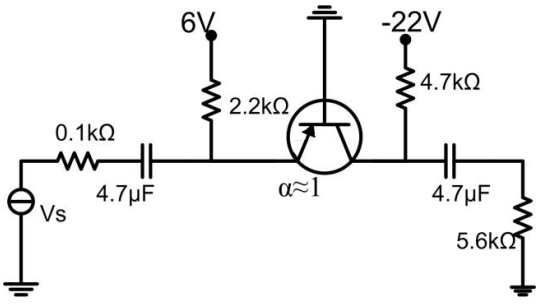

Figure 5