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THE LNM INSTITUTE OF INFORMATION TECHNOLOGY

B.TECH. 4th SEMESTER (2015-16)

COMPUTER ORGANIZATION & ARCHITECTURE, ENDTERM EXAM

MAX MARKS: 100 **TIME: 3 HOURS**

Q1. Fill in the blanks: (10*1=10)

a) The hardware which determines potential data hazards in a pipelined architecture is called _____.

b) The Hamming distance between 10010 and 10101 is _____.

c) An optical mouse has an LED and a _____ on the bottom.

d) A system with frequent page faults is said to be _____

e) A 64kB of cache can be organized as _____ cache lines of 64 bytes each.

f) A device that produces an image line by line is called a _____ device.

g) Distributing data over multiple drives in RAID is called _____

h) _____ modems can transmit data in both directions at the same time.

i) In a digital camera, the film is replaced by a rectangular array of _____ that are sensitive to light.

j) In CYMK colour printers, the inks used are cyan, yellow, magenta and _____

Q2. What do the following acronyms stand for? (5*1=5)

a) SIMD b) BIOS c) MMU d) LCD e) PSW

Q3. State two differences between: (5*2=10)

a) RISC and CISC b) Macros and procedures c) Virtual memory implementations using paging and segmentation d) Interrupts and traps e) Synchronous and asynchronous buses

Q4. Discuss a two-level centralized bus arbitration system. (5)

Q5. Assume that for a process, x and y are stored in a memory segment whose base address is in register R5. x is at offset 20 and y is stored in the next word. z is to be stored at memory address whose base address is in register R2 and offset is 30. Assume a byte addressable memory and a 32-bit machine.

For the C statement $z = x * y$

a) Write the equivalent assembly language instructions and indicate the addressing modes being used in each. (8)

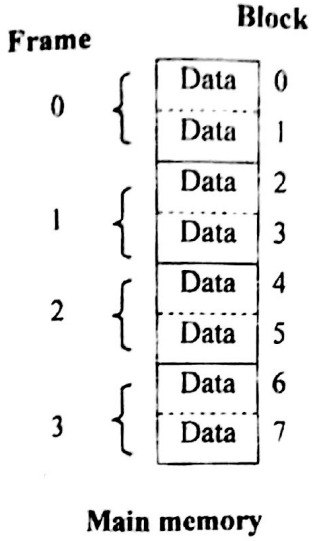
b) For any two assembly language instructions in your program (must be of different types, ex. data movement and arithmetic), write the corresponding microinstructions. (5+5)

Q6. Given a virtual memory system, a 2-way set associative cache and a page table for a process **P**. Assume cache blocks of 8 words and page size of 16 words. In the system below, main memory is divided into blocks and two blocks equal one page frame. (DO NOT give objective answers. Show the working.)

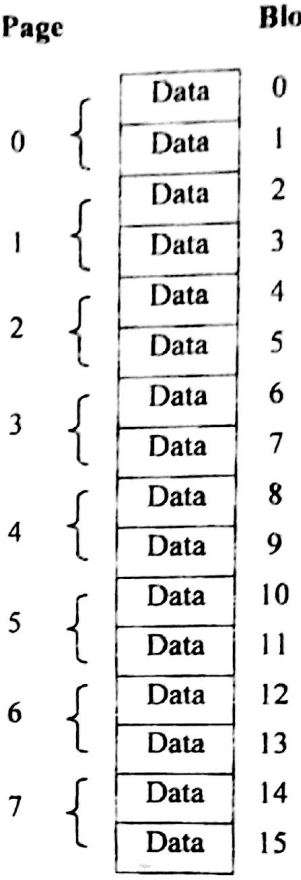
Cache Capacity = 32 words.

	Frame	Valid
0	3	1
1	0	1
2	-	0
3	2	1
4	1	1
5	-	0
6	-	0
7	-	0

Page Table



Main memory



Virtual memory for Process P

a) How many bits are there in a virtual address of process **P**? (2)

b) How many bits are there in the physical address? (2)

c) Determine the translation of virtual address 18_{10} into physical address. (5)

d) Determine the number of cache hits and misses if the following sequence of memory addresses is accessed:

49, 59, 50, 62, 3, 10, 17, 22

Show the status of cache at each step. (16)

e) Compute the hit ratio. (2)

Q7. Use the information in the following table to answer the question below:

Processor	Clock rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	1.5 GHz	1	2	3	4
P2	2 GHz	2	2	2	2

Given a program with 10^6 instructions, divided into instruction classes as follows: 10% class A, 20% class B, 50% class C and 20% class D, which implementation is faster? (5)

Q8. Consider the following sequence of instructions being executed in a 5-stage pipeline having separate instruction and data caches. The pipeline stages are IF, ID, EX, OF, WB (in this order).

```
LOOP: ADDI R12, R12, 4
      LW R8, 40(R12)
      ADD R9, R9, R8
      ADDI R11, R11, -1
      CMP R11, R0
      BNE LOOP
```

a) Identify the different types of pipeline hazards. (5)

b) Determine the stages where pipeline needs to be stalled to correctly execute the instruction sequence. (5)

c) Can operand forwarding help reduce the hazards? Show how. (5)

d) Can you suggest any reordering of instructions that would reduce the number of bubbles. Show how. (5)