The LNM Institute of Information Technology

Computer Science & Engineering

Computer Organization and Architecture

Exam Type: End-Term

Start new question on new page

Attempt all questions in sequence

Please be precise while writing your answer

Time: 180 Minutes **Date:** 29-Nov-2018 **Max. Marks:** 100

Q1. A machine has a 32-bit architecture, with 1-word long instructions. It has 50 registers, each of which is 32 bits long. It needs to support two types of instructions. There are 40 Type I instructions, which have an immediate operand and two register operands. Type II instructions are load/store instructions having two register operands, out of which one register specifies the memory address. (5+2+3+1=11)

a) Assuming that the immediate operand in Type I instructions is an unsigned integer, what is the maximum value of the immediate operand?

b) How many maximum Type II instructions are possible?

c) Assuming word addressable memory, what is the maximum size of memory that can be addressed?

d) What is the kind of memory addressing being used in Type II instructions?

Q2. Suppose we are working with an error-correcting code that will allow all single-bit errors to be corrected for memory words of length 7. We have already calculated that we need 4 check bits. Code words are created according to the Hamming algorithm presented in the text. We now receive the following code word:

1 0 1 0 1 0 1 1 1 1 0

Assuming even parity, is this a legal code word? If not, according to our error-correcting code, where is the error? (5)

Q3. Given a byte-addressable memory of 2048 bytes consisting of several interleaved 64 Byte* 8 RAM chips, show how the memory address will be interpreted? (5)

Q4. A computer has a 256 KByte, 4-way set associative, write back byte-addressable data cache with block size of 32 Bytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. What is the size of the cache tag directory in bits? (7)

Q5. In a byte-addressable machine we divide the virtual address as follows: (2+5+4+2=13)

Virtual page number (12 bits)	Offset (8 bits)

a) What is the page size in such a system?

b) What is the size of a page table (in bytes) for a process that has 256K of physical memory? Assume there are no valid/invalid/other information bits.

c) Consider a segment of the page table as given below, where will logical address 2700 map to in the physical memory?

d) Where will logical address 2500 map to?

Virtual page	Page number	Valid bit (Valid:1, Invalid:0)
8	15	1
9	200	0
10	82	1

Q6. Consider a disk with the following characteristics: (6+3=9)
Average seek time = 8 msec, Average rotational delay= 3 msec, Spindle speed= 10,000 rpm
Sectors/track= 170 sectors, Sector size= 512 bytes

a) What is the average time to read one sector?
b) What is the time taken to read a file sequentially if the file occupies 100 tracks?

Q7. List the differences between Sub-routine and interrupt-service -routine? Explain precisely with example. (4)

Q8. Write the sequence of steps that take place when the processor receives an interrupt in vectored interrupt scheme. (5)

Q9. Assume that propagation delay along the bus and through the ALU are 0.3 and 2 ns respectively. The setup time for the register is 0.2 ns. (4+4)

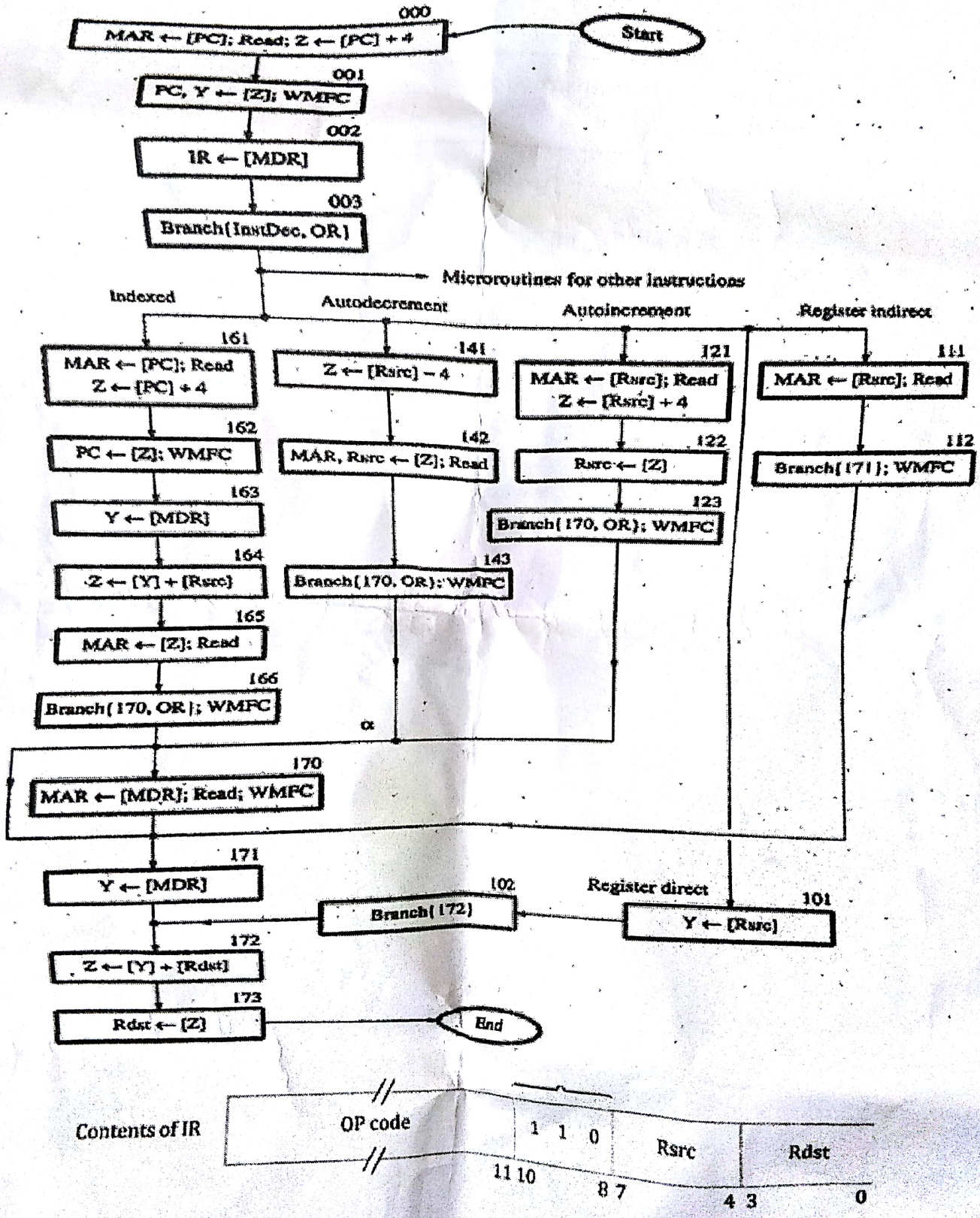
a. What should be the clock period for the single internal bus system to execute following Micro-routine.
b. Assume clock period is C and memory access time is T, calculate total time required to execute following Micro-routine in terms of C and T.

1 PC_{out}, MAR_{in}, Read, Select4,Add, Z_{in}
2 Z_{out}, PC_{in}, Y_{in}, WMFC
3 MDR_{out}, IR_{in}
4 $R3_{out}$, MAR_{in}, Read
5 $R1_{out}$, Y_{in}, WMFC
6 MDR_{out}, SelectY, Add, Z_{in}
7 Z_{out}, $R1_{in}$, End

Q10. Multiply using Booth Algorithm. A=010111, B=110110. (8)

Q12. Assume that 25 percent of the dynamic count of the instructions executed on a computer are branch instructions. Delayed branching is used, with two delay slots. If six stage pipeline is used, estimate the gain in performance if the compiler will be able to use 85 percent of the first delay slots and 20 percent of second delay slot. (10)

Q13. Study the flowchart carefully and answer the following questions. (10+5)



For the instruction **"ADD RSrc, RDst"** the 10^{th} 9^{th} and 8^{th} bits of the **"IR "**show the addressing mode of the source register where 110 indicates indexed addressing mode.

A. The part of the micro-routine is given below. Complete the micro-routine till the next micro-branch?

Address (octal)	Microinstruction
000	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}
001	Z_{out}, PC_{in}, Y_{in}, WMFC
002	MDR_{out}, IR_{in}
003	μBranch {μPC ← 101 (from Instruction decoder); $\mu PC_{5,4} \leftarrow [IR_{10,9}]$; $\mu PC_3 \leftarrow [\overline{IR_{10}}] \times [\overline{IR_9}] \times [IR_8]$}

B. If the autodecrement path is to be followed in the flowchart what should be the value of $IR_{10,9,8}$.