THE LNM INSTITUTE OF INFORMATION TECHNOLOGY

DIGITAL SYSTEMS

(II Semester, 2017-18)

Time: 90 minutes **Maximum Marks: 25**

Q1. Perform BCD addition of decimal numbers 267 and 534. (2)

Q2. Convert the decimal number 987.87 to hexadecimal number system up to 4-decimal places. Represent the leftmost digit of the resultant hexadecimal number into binary and obtain its gray code. (2+1)

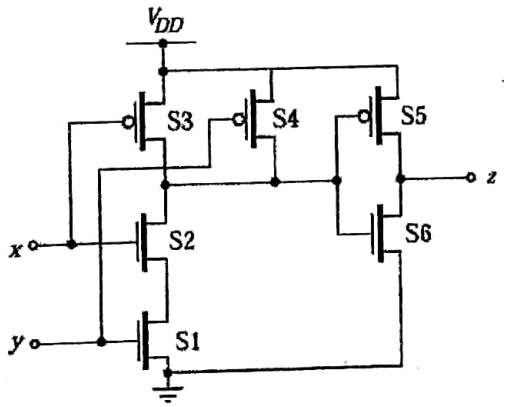
Q3. Convert the following switching expression as sum of minterms:

$$F = (a + b.c').c + b'$$

(Here, b' and c' represents the complement of b and c respectively).

Design the gate network for the resulting expression using {NAND} universal set. (2+2)

Q4. Following CMOS circuit implements the AND gate logic. Design the CMOS circuit for OR gate logic? (3)



Q5. Following are the functional specification for a gate network

$$Input: x \in \{2,3,4,...,12\}$$

$$Output: z \in \{0,1\}$$

$$Function: z \in \begin{cases} 1 & if \sum x_i = 2; \text{ i.e. number of 1's are two} \\ 0 & otherwise \end{cases}$$

(a) Design a minimal two-level gate network using the K-map in the sum of product form? (3)

(b) Analyse the characteristics for the designed gate network in above part? (3)

(c) Re-design the network to meet the Fan-in requirement of the gate, that is described as two for each gate? (2)

(d) Is the size of re-designed network is higher than the minimal one? If yes, how it can be reduced? (2)

Gate type	Fan-in	t_{pLH} (ns)	t_{pHL} (ns)	Load factor (standard load)	Size (equivalent gates)
AND	2	0.15+0.037L	0.16+0.017L	1.0	2
AND	3	0.20+0.038L	0.18+0.018L	1.0	2
AND	4	0.28+0.039L	0.21+0.019L	1.0	3
OR	2	0.12+0.037L	0.20+0.019L	1.0	2
OR	3	0.12+0.038L	0.34+0.022L	1.0	2
OR	4	0.13+0.038L	0.45+0.025L	1.0	3
NAND	2	0.05+0.038L	0.08+0.027L	1.0	1
NOR	2	0.06+0.075L	0.07+0.016L	1.0	1
Buffer	1	0.15+0.006L	0.19+0.003L	2.0	4

Q6. Determine the output waveform of the logic circuit in the below Figure (a). Assume that all gates have a propagation delay of 5 ns. The timing diagram in Figure (b) has a 5-ns resolution. (3)