LNMIIT
The LNM Institute of Information Technology

ELECTRONICS AND COMMUNICATION DEPARTMENT
The LNMIIT, JAIPUR
Digital Circuits and Systems (Code: DCS)

October 3, 2017

Time: 90 Minites — *Mid Sem Examination Solution* — Maximum Marks: 30

Section I:

Q1. (a) If the numbers (+992) and (+78) are in signed magnitude format, convert the numbers to signed-10's complement form and show that $SUM1 = -SUM2$, where $SUM1 = (+992) - (+78)$ and $SUM2 = (-992) + (+78)$.

[1+1+1]

Solution: Number of required digits, in this case, is five since the sum of these two numbers are four digit number and one digit required for the sign digit. Hence, these numbers can be written as:

$+992 \rightarrow 00992$ and $+78 \rightarrow 00078$ and then the 10's complement form as: $99999 - 00992 + 1 = 99008$ and $99999 - 00078 + 1 = 99922$, respectively. **[1]**

$SUM1 = (+992) - (+78)$
$SUM1 = 00992$+10's complement of (00078)
$SUM1 = 00992 + 99922$
$SUM1 = 100914$, after discarding end carry $SUM1 = 00914 = +914$ **[1]**

similarly for $SUM2$
$SUM2 = (-992) + (+78)$
$SUM2 =$10's complement of $(00992) + 00078$
$SUM2 = 99008 + 00078$
$SUM2 = 99086$, no carry so we need to take 10's complement back $-ve$ sign, that is:
$SUM2 = -($10's complement of 99086$) = -(99999 - 99086 + 1) = -(00914) = -(+914) = -SUM1$ **[1]**

(b) Make a table listing two different self complimenting codes, if inputs are (A, B, C, D).

[2+2]

Solution: A necessary condition for a self-complimenting code is that the sum of its weights should be 9, e.g. in Excess-3 code $8+4+2+1+3 = 18 = 1+8 = 9$, in 631-1 code $6+3+1-1 = 9$ and in 2421 code $2+4+2+1 = 9$. Examples are: **[2] marks for each code**.

Decimal Digit	Excess-3 Code	631-1 Code	2421 Code
0	0011	0011	0000
1	0100	0010	0001
2	0101	0101	0010
3	0110	0111	0011
4	0111	0110	0100
5	1000	1001	1011
6	1001	1000	1100
7	1010	1010	1101
8	1011	1101	1110
9	1100	1100	1111

You were required to make a table listing all 16 combinations for (A, B, C, D) inputs. To verify your solution take a number such as $1011 = 5$ in 2421 code. Complement of 1011 is $0100 = 4$ in 2421 code, which is complement of 5, thus 2421 code is self-complementing.

Q2. (a) If $F = x + y$, find its dual F_d and prove that F_d is an identity element with respect to $(+)$ operator and F is another identity element with respect to $(.)$ operator. *Hint: $a + 0 = a$ and $a.1 = a$ where 0 is an identity element with respect to $(+)$ operator and 1 is an identity element with respect to $(.)$ operator, respectively.*

[1+1+1]

Solution: Dual F_d of F is: $F_d = x.y$ **[1]**
Based on the hint $a + 0 = a$ and $a.1 = a$ lets calculate $F + F_d$ and $F.F_d$.
$F + F_d = x + y + x.y$
$F + F_d = x + x.y + y + x.y = x.(1 + y) + y.(1 + x) = x.1 + y.1 = x + y$
$F + F_d = F$ comparing with $a + 0 = a$, F_d is an identity element with respect to $(+)$ operator. **[1]**

Similarly for $F.F_d$
$F.F_d = (x + y).(x.y) = x.x.y + x.y.y = x.y + x.y = x.y$
$F_d.F = F_d$ comparing with $a.1 = a$, F is an identity element with respect to $(.)$ operator. **[1]**

(b) Prove also from part (a) that $F + F' = 1$ and $F.F' = 0$.

[1+1]

Solution: Complement of F, that is $F' = (x + y)' = x'y'$
Then,
$F+F' = x+y+x'y' = x+x'y'+y+x'y' = (x+x')(x+y')+(x'+y)(y+y') = x+y'+x'+y = (x+x')+(y+y') = 1$ **[1]**

similarly,
$F.F' = (x + y)(x'y') = xx'y' + x'yy' = 0$ **[1]**
Bonus marks, if you have written correctly theorem's and/ or postulate's names used.

Q3. X and Y are the input of a circuit which produces Difference D (of $X - Y$) and Borrow B as outputs. Implement the circuit using minimum $2 : 1$ multiplexers.

[1+2]

Solution: One mark for the table and two marks for the circuit. Digital circuit can be design in two ways.

X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

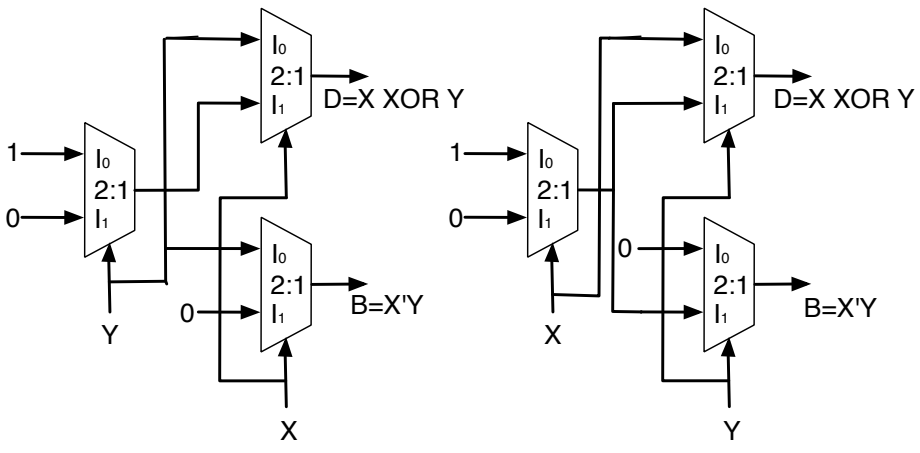

Figure 1:
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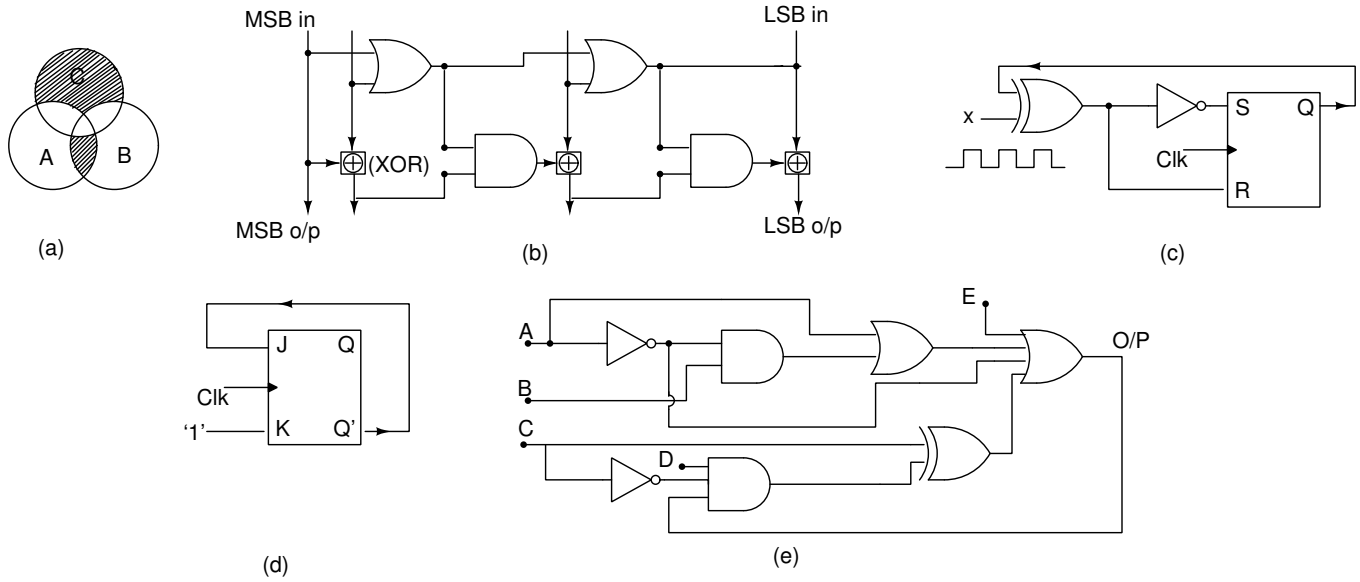

Figure 2: Refer for section II

Section II:

1. An 8 bit ripple carry adder is to be realized using some full adders FA (all identical) and half adderes HA (all identical). The worst case carry and sum propogation of full adder is 12ns and 15ns, respectively. The worst case carry and sum propogation of half adder is 10ns and 15ns, respectively. Calculate the worst case delay (in ns) of best design of 8 bit adder using these FAs and HAs only. [03]

   Solution: Best solution with 7 FAs and 1 HA

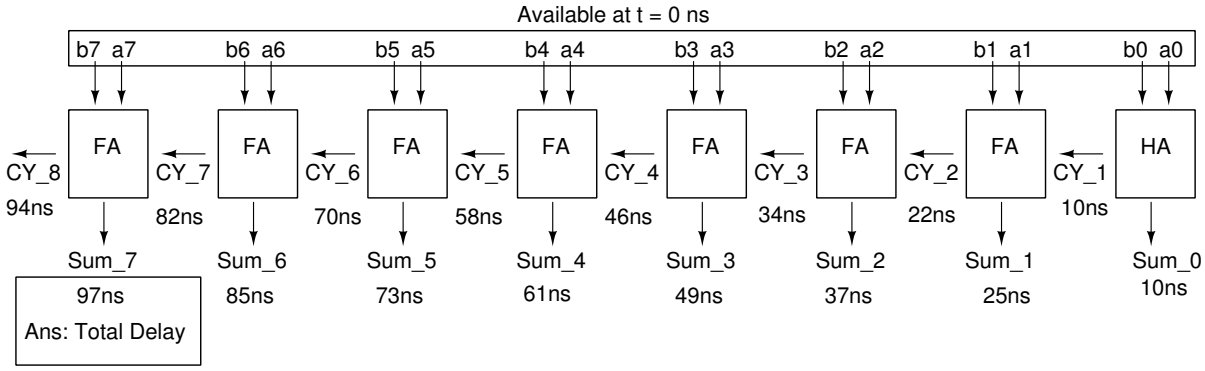

Figure 3:

2. X and Y are the input of a circuit which produces Differene D (of X−Y) and Borrow B as outputs. Implement the circuit using minimum 2:1 multiplexers. [02]

   Solution: Best solution with 3 - 2:1 Mux

X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

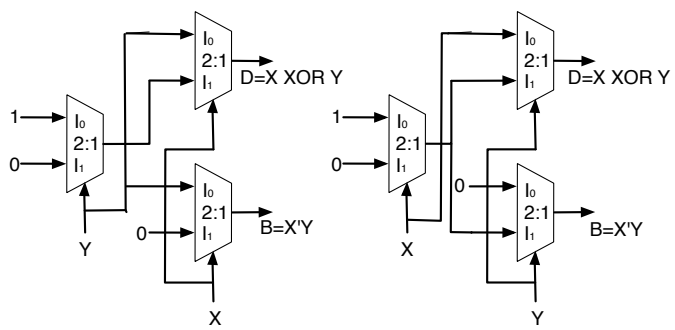

Figure 4:

3. Consider the circuit shown in the Fig. 1(c) and find the expression for next state Q+ as a function of x and Q. [02]
   Solution: Ans: $Q_{n+1} = Q_n$ XNOR X

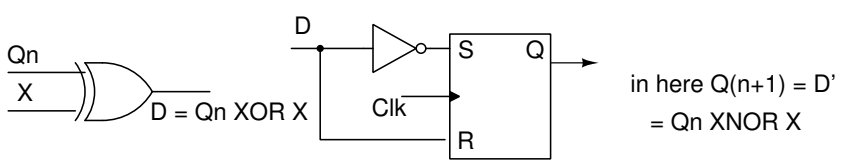

Figure 5:

4. Design a JK flip-flop using D flip-flop and some other gates. [02]

   Solution:

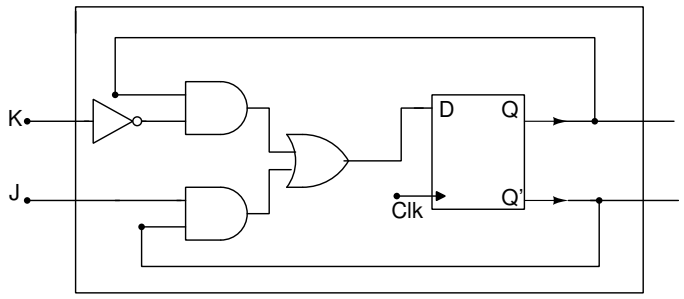

Figure 6:

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5. Whether the circuit shown i Fig. 1(e) is sequential or not (consider all gates as ideal with zero propogation delay) ? Prove your answer with reasoning. [02]

   Solution: Although circuit has a feedback element in its architecture but as explain in the Fig. 6 the output is always stuck at '1' means does not follow any input sequence. Hence, this circuit can not be classify as sequential circuit.

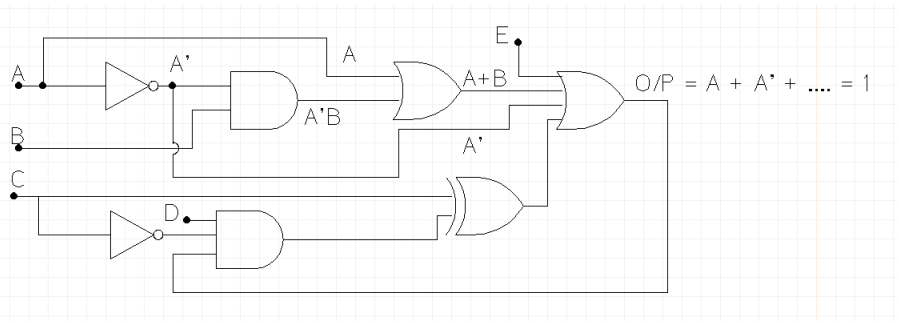

Figure 7:

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6. In the circuit (shown in Fig. 1(d)) JK flip-flop has J and K as inputs and Q and Q' as outputs. It is configured as J = Q' (means Q' is connected to the input J) and K = '1'. Initially flip-flop is cleared and then FF is clocked with 6 clock pulses. Calculate the sequence at the output Q for these 6 clock pulses (in the answer MSB should belongs to the value of Q corrrosponds to 6th clock pluse and LSB should belongs to the value of Q corrosponds to 1st clock pulse). [03]

   Solution: From 6 to 1 = sequence is 010101 as explained in Fig. 7

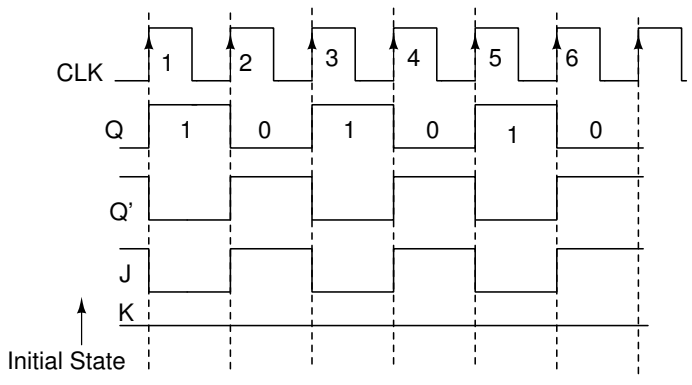

Figure 8:

Section III - SET B - Objective Questions - with 25% negative marking:

1. Correct hamming code for a binary code $D_4D_3D_2D_1 = 1101$ (Hint - even parity check and p_0 bit is at the extreme left in the hamming code):
   (a) 0 1 1 0 0 1 1 (b) 0 1 0 1 1 0 1 (c) 0 0 1 0 0 1 1 (d) 0 1 0 0 1 0 0 (e) 0 0 1 1 0 0 1. [01]
2. In SR latch racing condition occurs for input conditions which are (latch is enabled in all cases) (a) S = R ='1' followed by S = R = '0' (b) S = R ='0' followed by S = R = '1' (c) when S = R ='1' (d) S = R ='1' followed by any other input combination (e) S = R = '0' followed by any other input combination. [0.5]
3. For output Q_n of J-K flip flop to have a transition from '0' to '1' (with the edge of the clock pulse), the value of the inputs J and K are , respectively (a) '1' and X (don't care) (b) '0' and X (c) X and '1' (d) X and '0' (e) '1' and '0'. [0.5]
4. Booloean expression for the shaded area shown in Fig. 1(a) is: (a) AB + B'C' (b) AB + B'C' + A'B' (c) ABC' + A'B'C + A'B'C (d) A'B'C + ABC' (e) ABC + AB'C'. [0.5]
5. The circuit shown in Fig. 1(b) converts . (a) BCD to Binary (b) Binary to Excess-3 (c) Binary to Grey (d) Grey to Binary (e) Grey to Excess-3. [0.5]

Answer Sheet:

1. (a) 2. (a) 3. (a) 4. (c) ABC' + A'B'C + A'B'C and (d) A'B'C + ABC' (as in SET B) 5. (d)