END-SEM EXAM (May 7, 2018) MAX. MARKS: 45

COURSE: DIGITAL SYSTEMS MAX. TIME: 3 Hrs

***Note: NO DOUBTS!!** (If required, make and state your assumptions)*

Q1. Using postulates of Boolean algebra and the theorems, prove $BC + A'B' + A'C' = ABC + A'$ *[2 marks]*

Q2. Following pairs of 8-bit vectors $\underline{x}$ and $\underline{y}$ representing integers in the two's complement system.

(a) X= 10110110 Y=01100111

(b) X=10101010 Y=11110001

Obtain the (x+y) and (x-y) using two's complement arithmetic? Also describe the values of conditions OVF (Over flow), ZERO, SIGN? *[2 marks]*

Q3. With a suitable example, explain how a buffer can be used to reduce the propagation delay of a gate network? *[2 marks]*

Q4. A combinational system has four inputs *a, b, c, d* and one output *y*. The output *y* is 1 if and only if the number represented by (*a, b, c, d*) in binary code is prime. Design a minimal two-level network to implement this system, using Quine-McCluskey minimization method (0 and 1 are not prime). *[6 marks]*

Q5. For a sequential system described using the given state table description

(a) Determine the minimal state table and draw the state diagram? *[4 marks]*

(b) Design the sequential system for the minimised state description using JK Flipflop? *[6 marks]*

(PS: Present state, NS: Next State)

PS	x=a	x=b	x=c	x=d
A	D,1	C,0	B,1	F,1
B	C,0	F,1	E,1	B,0
C	B,1	A,0	D,1	F,1
D	G,0	F,1	E,1	B,0
E	C,0	A,1	D,1	E,0
F	C,1	F,1	D,0	H,0
G	D,1	A,0	B,1	F,1
H	B,1	C,0	B,1	F,1
	NS , z			

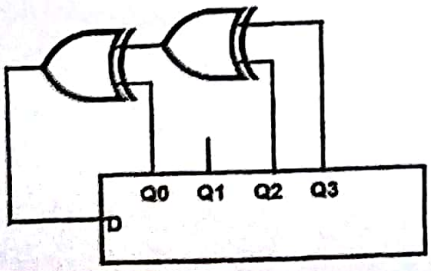
Q6. Implement the following function using cascade network *[2+2 marks]*

F (a, b, c, d) = one-set (1, 3, 6, 7, 9, 11, 14)

(a) of Multiplexers (4:1) (b) of decoder (2:4) and one OR gate

Q7. Compare two different approaches (coincident and tree decoding) of decoder network in terms of resources, delay, and load factor at input and output side? *[4 marks]*

Q8. A 4-bit right shift register is initialized to values 1000 for (*Q0, Q1, Q2, Q3*). The input (*D*) to the register is derived from *Q0, Q2,* and *Q3* as shown in the figure. Write down the sequence generated by the circuit till its repetition? *[2 marks]*



Q9. Design a sequential system which has an input *I*= {0,1} and produces output *z*=1 when pattern (101011) occurs five times. (Hint: Design the system in two modules: pattern recognizer and counter) *[4 marks]*

Q10. Design a network using Modulo-8 binary counter, decoder and SR flipflop to produce the different timing signals with different duty cycles? *[4 marks]*

(a) duty cycle= 25% (b) duty cycle=75%

Q11. For the given function design the simple execution graph and explain how it can be modified to reduce the cost of system and to reduce the timing parameters? *[5 marks]*

```
While{
        Read a, b, c, d, x
        Z1=a+b+c+d
        If(x=0)
        {
                Z2=(a+b)*c
        }
        Else
        {
                Z2=(a+b)*(c+d)
        }
}
```