THE LNM INSTITUTE OF INFORMATION TECHNOLOGY

COMPUTER ORGANIZATION & ARCHITECTURE

MID-TERM 2 (2013-2014)

MAX MARKS: 15 **TIME: 1 HR**

Q1. Answer the following: [4]

a) 1M Byte memory consists of ____ RAM chips with size 256K x 1 bit.

b) The number of bits in the tag field if the main memory contains *n* blocks and cache contains *m* blocks is ___.

c) In *k*-way associative mapping, it becomes direct mapping if *k* = ____.

d) If memory has an access time of 100ns, access time of the cache memory is 40ns with 80% hit ratio, then the effective access time of the CPU is _____.

Q2. Design a 5 x 3 bit RAM cell. [3]

Q3. Suppose we are working with an error-correcting code that will allow all single-bit errors to be corrected for memory words of length 7. We have already calculated that we need 4 check bits, and the length of all code words will be 11. Code words are created according to the Hamming algorithm. We now receive the following code word: [3]

1 0 1 0 1 0 1 1 1 1 0

Assuming even parity, is this a legal code word? If not, according to our error-correcting code, where is the error?

Q4. Consider a machine with 16-bit instructions and 16 registers. Using **expanding opcode** method, encode the following instructions: [2]

- 15 instructions with 3 addresses
- 14 instructions with 2 addresses
- 31 instructions with 1 address
- 16 instructions with 0 addresses

Q5. Suppose that we have a virtual address space of 2^8 words for a given process and physical memory of 4 page frames. Assume also that page frames are 32 words in length. Some pages from the process have been brought into main memory. Figure illustrates the current state of the system. [3]

Page Table

Page	Frame no.	Valid bit
0	2	1
1	-	0
2	-	0
3	0	1
4	1	1
5	-	0
6	-	0
7	3	1

Map virtual address 13_{10} to a physical address.