

Digital Circuits and Systems

End Semester Exam

Date: 26th Nov 2013

Time: 180 Minutes

Max Marks. 80

Notes: Use don't care conditions wherever you can. Minimum network solved with don't care conditions would result in full marks.

Assumptions made should be written clearly.

1: Design a combinational circuit with 3 inputs A, B and C which would provide you A', B' and C'. You can use unlimited number of AND and OR gates, only two NOT gates and no other gate. Explain the logic with truth table and prove that your solution works. [10]

2: Design a sequential system that works as a three-bit prime number generator. It would generate the sequence 0 and 7 that are prime numbers. If $Q_2Q_1Q_0$ is the state vector then design the system using JK flip flop for Q_2 , T flip flop at Q_1 and D flip flop at Q_0 position and external logic gates. [10]

3: Consider an input integer n in the range 0 to 15. $A = 3n \bmod 16$ and $B = 7n \bmod 16$ are two function vectors. To link the vector A and B a combinational system is needed to convert an integer in A to an integer in B. Design such a system using:

A. One 8 input MUX and one XOR gate. [7]

B. One 4 input decoder and one 16 input encoder. [3]

4: Implement a binary Full adder using only and minimum number of 2x1 MUXes. [5]

5: Analyze the sequential circuit given in figure 1. It has one input Clk and 3bit output variable $Q = Q_1Q_2Q_3$. Assuming that initially $Q = 000$, write down the value of Q for 10 cycles of input clock. [5]

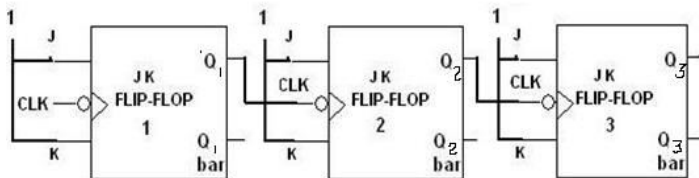


Figure 1

6: Design a mod 16 even number counter using only a register and 4 bit binary adder. [5]

7: Design a minimal 2 level network for the function $F(A, B, C, D) = \sum m(5, 7, 13, 15)$. [5]

8: Implement a 64 to 6 line encoder using 8 to 3 encoders and OR gates only. [5]

9: Analyze the circuit shown in figure 2 and obtain high level description of the system assuming vector $z = (z_2, z_1, z_0)$ represents an integer. [5]

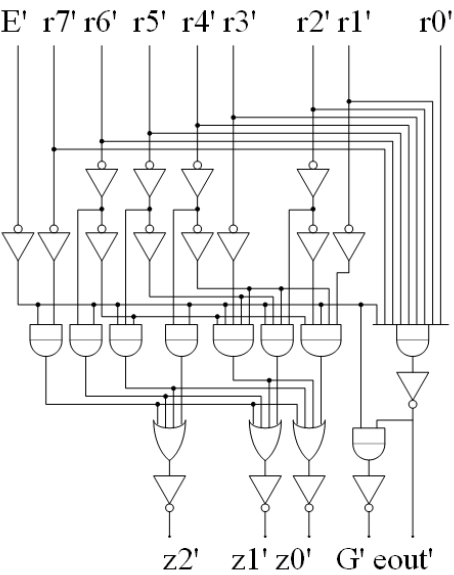


Figure 2

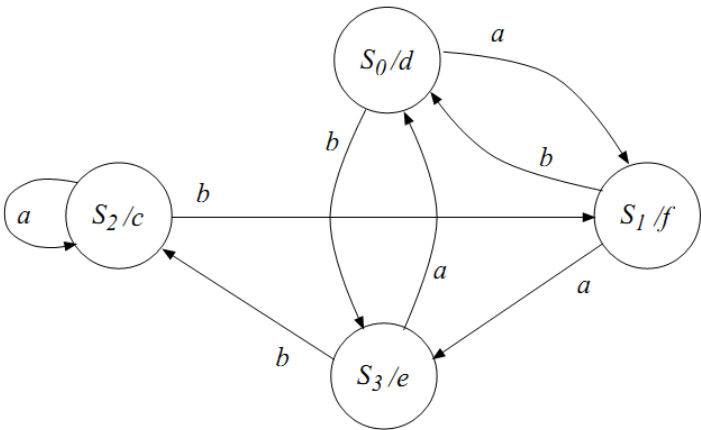


Figure 3

10: Analyze the state diagram in Figure 3 and design the corresponding sequential network. [5]

11: Analyze the circuit given in figure 4. This system implements a state machine with 7 states S_0 to S_6 with $Q_2Q_1Q_0$ vector representing corresponding binary values of state names.(i.e 010 represents S_2 and so on) and external input x . Draw the corresponding state diagram. [5]

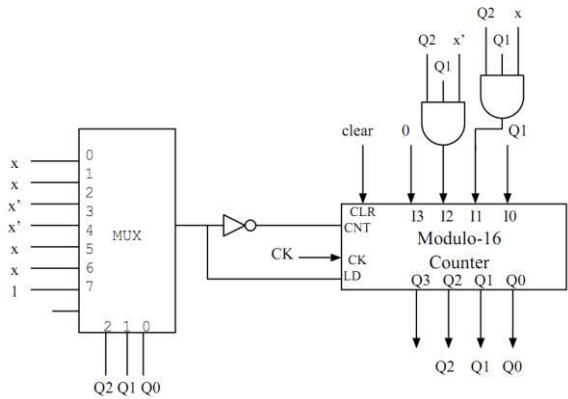


Figure 4

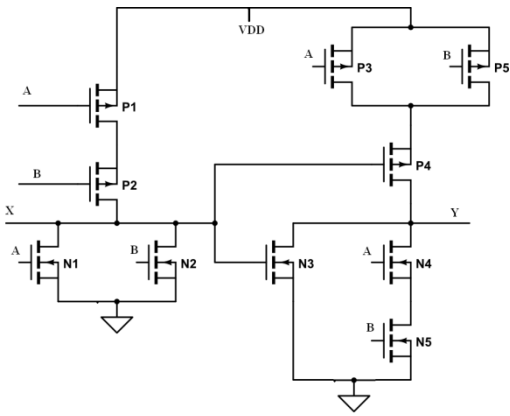


Figure 5

12: Implement the function $F(A, B, C) = A \text{ XOR } B \text{ XOR } C$ using minimum number of transistors. [5]

13: Analyze the circuit given in Figure 5 and find out the logic gates being implemented at X and Y. [5]