THE LNM INSTITUTE OF INFORMATION TECHNOLOGY

COA MID-TERM (2017-2018, I)

MAX MARKS: 30 **TIME: 90 MINS**

Q1. Consider a single-address machine. Suppose the locations in memory contain the following:

Memory address	Instruction
2000	LDA 5000
2004	ADD 5100
2008	STORE 5100
2012	HLT
5000	724
5100	006

a) Show, **with reasons**, the contents of the IR, PC, MAR, MDR, ACC and memory location 5100 at the conclusion of instruction at memory address 2004. (Assume that the next fetch-decode-execute cycle is about to begin and its address has been forwarded by the PC). (6)

b) Draw the data-path showing relevant registers which will help in execution of instruction at memory address 2004. (2)

Q2. In a computer system, the memory contains the values shown below:

Address	Value
1000	1400
...	...
1100	400
...	...
1200	1000
...	...
1300	1100
...	...
1400	1300

Assume R1 is the implied register in the indexed addressing mode and contains value 200.

Suppose we have the instruction "Load R5, 1000" where first operand is the destination and second operand specifies source. Determine the effective memory address and actual value loaded into R5 for the following addressing modes: (1*3=3)

a) Direct
b) Indirect
c) Indexed

Q3. Consider a 32-bit processor with 64 registers and an instruction set of size 12. Each instruction has five distinct fields, namely opcode, two source register identifiers, one destination register identifier, and a 12-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion (i.e. from an address that is a multiple of 4). If a program has 100 instructions, what is the amount of memory consumed by the program? (4)

Q4. Suppose I want to use 12-bit floating point representation (1 bit for sign, 5 bits for exponent and 6 bits for mantissa) while following IEEE standard.

d) What should be the value of p in "excess-p"? (1)
e) Represent 0.125 and -0.27 in this format. (2+2)
f) Perform addition of above two numbers and normalize the result using truncate (chopping) method. (3)
g) Calculate the error of normalization. (1)

Q5. A machine has 31 registers, 1024 memory addresses (and assume it is completely available for user program) with 32-bit words.

a) Expand the opcode to incorporate 31 three-address instructions (both sources are memory operands; destination is a register reference to register or indirect mode with a bit to specify mode) and 64 two-address instructions (both source and destination are memory operands). (4)

b) If this machine accepts only zero-address instructions and memory is word addressable, how many maximum zero-address instructions can the memory store? (2)