LNMIIT
The LNM Institute of Information Technology

Electronics II
End Term Exam

Date: 29th April 2014 | Time: 180 Minutes | Max Marks. 50

Notes: If not mentioned, then you can ignore I_B in problem solving.
If not mentioned, use first approximation for diodes.
Assumptions made should be written clearly.

Q.1: The input voltage to the circuit in **Figure 1** is Vs = 12sinωt V. Determine the output across 3kΩ resistor and plot it for two clock cycles accurately. [5]

Q.2: Analyze the circuit given in **Figure 3**. Let R2 = 2kΩ. V1 and V2 can have two different values, 2V and 8V. Assume that forward bias diode have 0.7 drop. This circuit should work as logic OR gate. Determine the range of R1 for which this circuit would work fine. (hint, consider all 4 operation and find range of R1) [5]

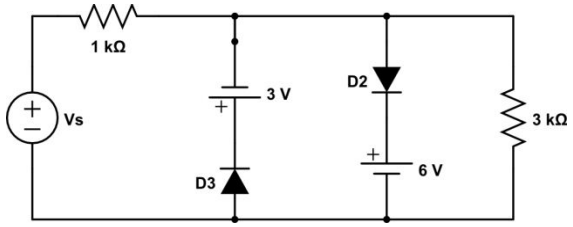

Figure 1

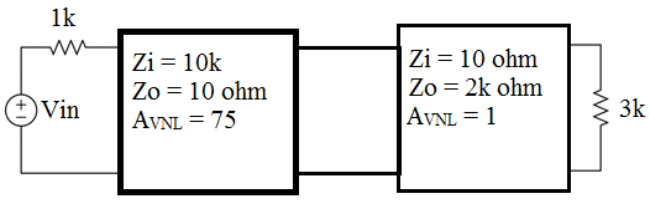

Figure 2

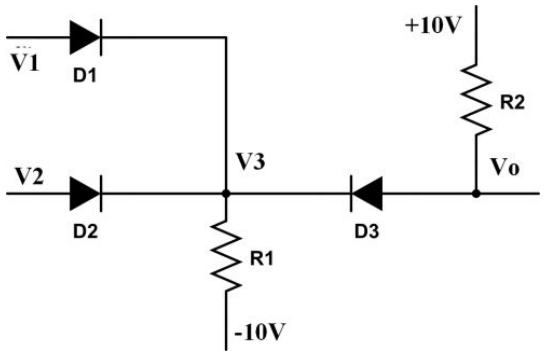

Figure 3

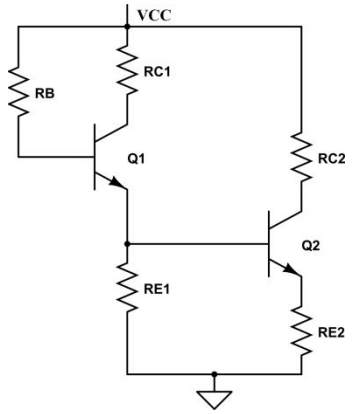

Figure 4

Q.3: Design a pulse width modulator using NE555. If the value of R is 2kΩ, C is 5nF and V_{CC} = 12V then find out the minimum and maximum width that can be produced by this modulator. Also write down a suitable frequency of the triggering pulse. [5]

Q.4: For the circuit given in **Figure 4**, RB = 230kΩ, RE1 = 400Ω, RE2 = 0Ω, RC1 = RC2 = 100Ω and VCC = 6V. Find out the values of I_{C1}, I_{C2}, V_{CE1} and V_{CE2} given that β for both BJTs = 100. [5]

Q.5: Consider the cascaded amplifier system given in **Figure 2**. A_{vNL} represents voltage gain of amplifier without any load. Find out the voltage gain of first stage with load (A_{V1}) and second stage (A_{V2}). If input voltage is 50mV, then find out the output voltage (across 3kΩ resistor) value as well. [5]

Q.6: (a). Write down the Barkhausen stability criterion? [1]

(b). For the transistor Colpitts oscillator of **Figure 5** and the following circuit values, calculate the oscillation frequency: $L = 100\ \mu H$, $C_1 = 0.005\mu F$ and $C_1 = 0.01\mu F$. [2]

(c). Calculate the oscillation frequency for the transistor Hartley circuit of **Figure 6** and the following circuit values: $L_1 = 750\mu H$, $L_2 = 750\mu H$, $M = 150\mu H$, and $C = 150pF$. [2]

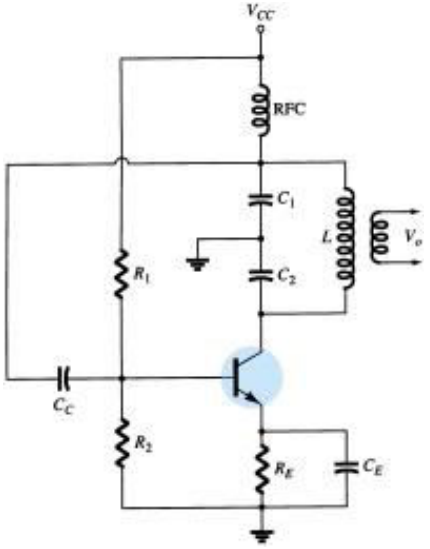

Figure 5

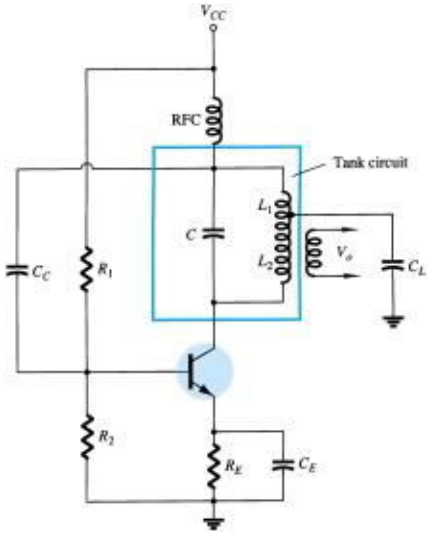

Figure 6

Q.7: Prove that the percentage ripples of the half-wave and full-wave rectifiers are 121% and 48%, respectively. [5]

Q.8: Draw the circuit diagram of the *Improved Series Regulator* (two-transistor regulator) and explain the operation using KVL/KCL equation(s)? [5]

Q.9: Explain all five parameters of a practical filter (to be concise in your answers) indicate all of these parameters with their region in the *Gain* vs. *Frequency* plot. [5]

Q.10: Design a 4th order active Low Pass Butterworth Filter (LPF) for given specification: [5]

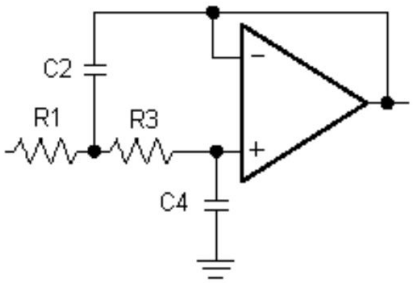

Figure 7: 2nd order LPF

Transfer function of 2nd order LPF $= \dfrac{R1R3}{s^2(C2C4)+sC4(R1+R3)+R1R3}$, where $s = a \pm jb$

Butterworth pole locations:

Order	**Real** $(-a)$	**Imaginary** $(\pm jb)$
4	0.9239 0.3827	0.3827 0.9239

Assume resistors value 2kΩ and design the filter for response with a roll off frequency of 5kHz.