

EE168 Lab 4

Tutorial Continued

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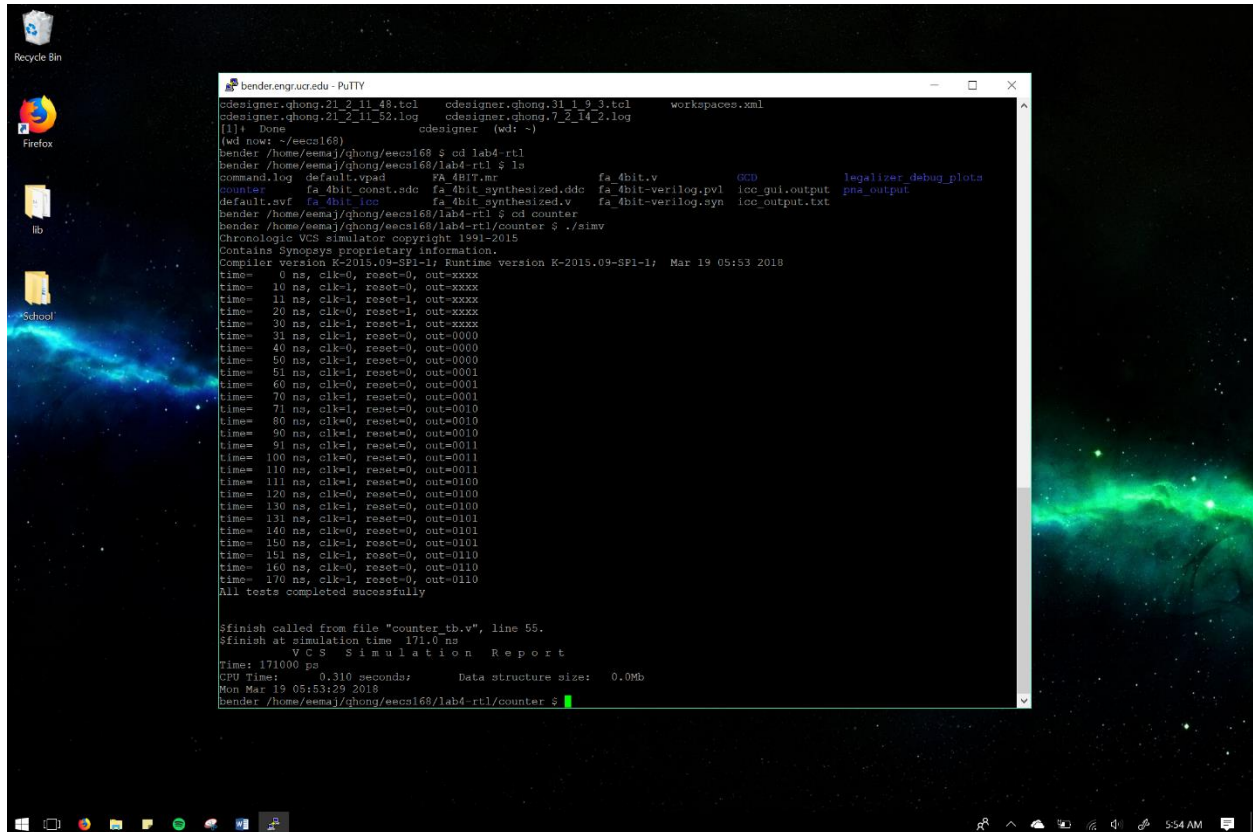
861 210 810

NetID- qhong004

ENGR- qhong

Introduction

Images



The screenshot shows a Linux desktop with a dark theme and a space-themed wallpaper. On the left, there is a sidebar with icons for Recycle Bin, Firefox, lib, and School. The terminal window, titled 'bender.engr.ucr.edu - PuTTY', displays the following text:

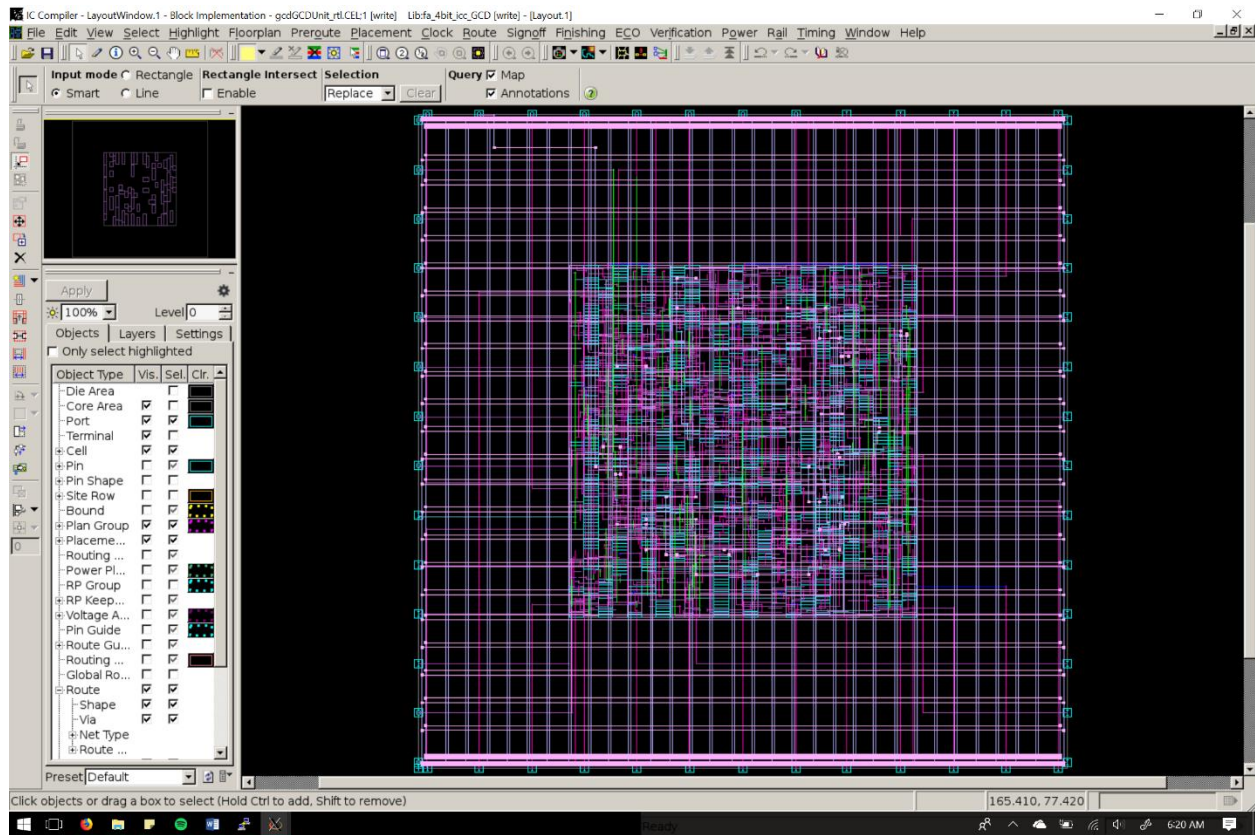
```
cdesigner.qhong.21_2_11_48.tcl cdesigner.qhong.31_1_9_3.tcl workspaces.xml
cdesigner.qhong.21_2_11_52.log cdesigner.qhong.7_2_14_2.log
[1]: Done cdesigner (wd: ~)
[wd now: /seec168]
bender /home/seec168/qhong/seec168 $ cd lab4-rtl
bender /home/seec168/qhong/seec168/lab4-rtl $ ls
command.log default.vpad fa_4bit.mr fa_4bit.v GCD legalizer_debug_plots
counter fa_4bit_count.sdc fa_4bit_synthesized.ddc fa_4bit-verilog.pvl ico_gui_output pna_output
default.svf fa_4bit_ico fa_4bit_synthesized.v fa_4bit-verilog.syn ico_output.txt
bender /home/seec168/qhong/seec168/lab4-rtl $ cd counter
bender /home/seec168/qhong/seec168/lab4-rtl/counter $ ./simv
Chronologic VCS simulator copyright 1991-2015
Contains Synopsys proprietary information.
Compiler version K-2015.09-SP1-1; Runtime version K-2015.09-SP1-1; Mar 19 05:53 2018
time= 0 ns, clk=0, reset=0, out=xxxx
time= 10 ns, clk=1, reset=0, out=xxxx
time= 11 ns, clk=1, reset=1, out=xxxx
time= 20 ns, clk=0, reset=1, out=xxxx
time= 30 ns, clk=1, reset=1, out=xxxx
time= 31 ns, clk=1, reset=0, out=0000
time= 40 ns, clk=0, reset=0, out=0000
time= 50 ns, clk=1, reset=0, out=0000
time= 51 ns, clk=1, reset=0, out=0001
time= 60 ns, clk=0, reset=0, out=0001
time= 70 ns, clk=1, reset=0, out=0001
time= 71 ns, clk=1, reset=0, out=0010
time= 80 ns, clk=0, reset=0, out=0010
time= 90 ns, clk=1, reset=0, out=0010
time= 91 ns, clk=1, reset=0, out=0011
time= 100 ns, clk=0, reset=0, out=0011
time= 110 ns, clk=1, reset=0, out=0011
time= 111 ns, clk=1, reset=0, out=0100
time= 120 ns, clk=0, reset=0, out=0100
time= 130 ns, clk=1, reset=0, out=0100
time= 131 ns, clk=1, reset=0, out=0101
time= 140 ns, clk=0, reset=0, out=0101
time= 150 ns, clk=1, reset=0, out=0101
time= 151 ns, clk=1, reset=0, out=0110
time= 160 ns, clk=0, reset=0, out=0110
time= 170 ns, clk=1, reset=0, out=0110
All tests completed successfully

$finish called from file "counter_tb.v", line 55.
$finish at simulation time 171.0 ns
VCS $ i m u l a t i o n R e p o r t
Time: 171000 ps
CPU Time: 0.310 seconds; Data structure size: 0.0Mb
Mon Mar 19 05:53:29 2018
bender /home/seec168/qhong/seec168/lab4-rtl/counter $
```

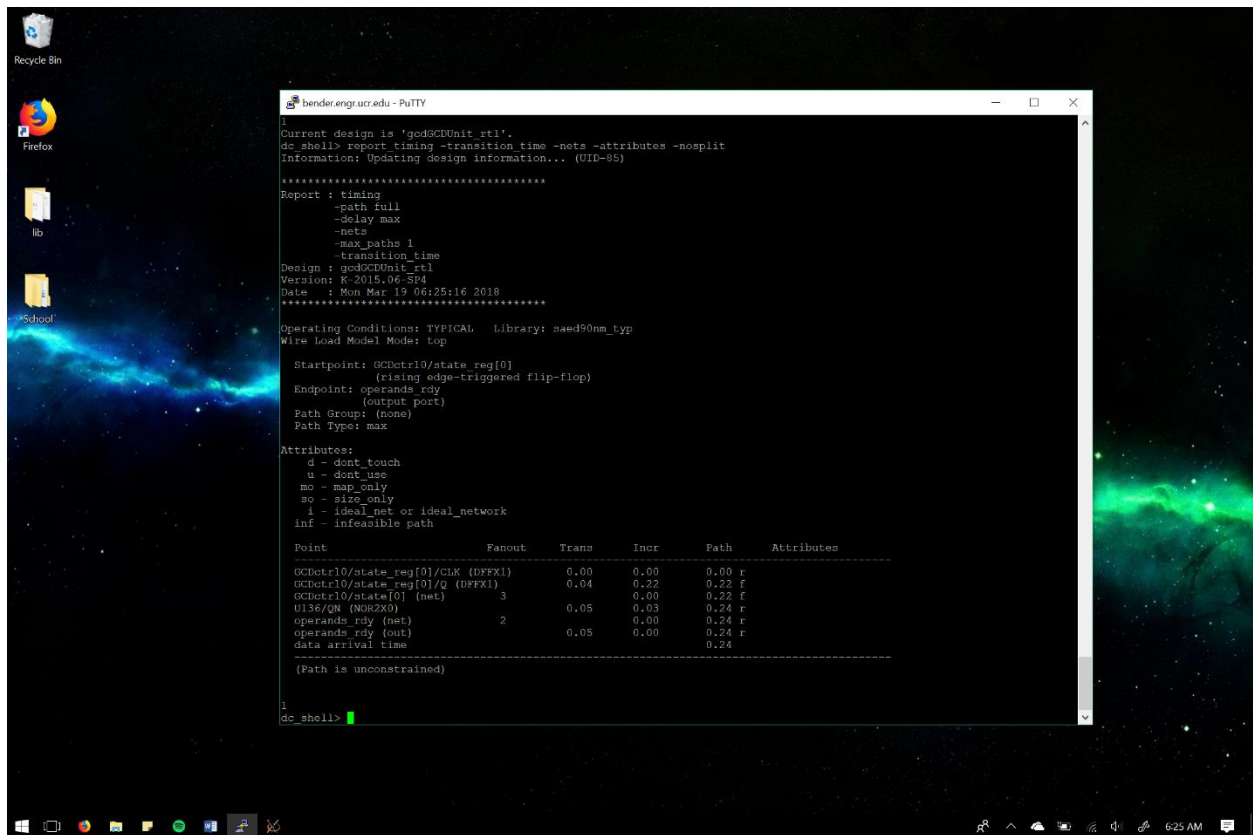
Sim result of Counter



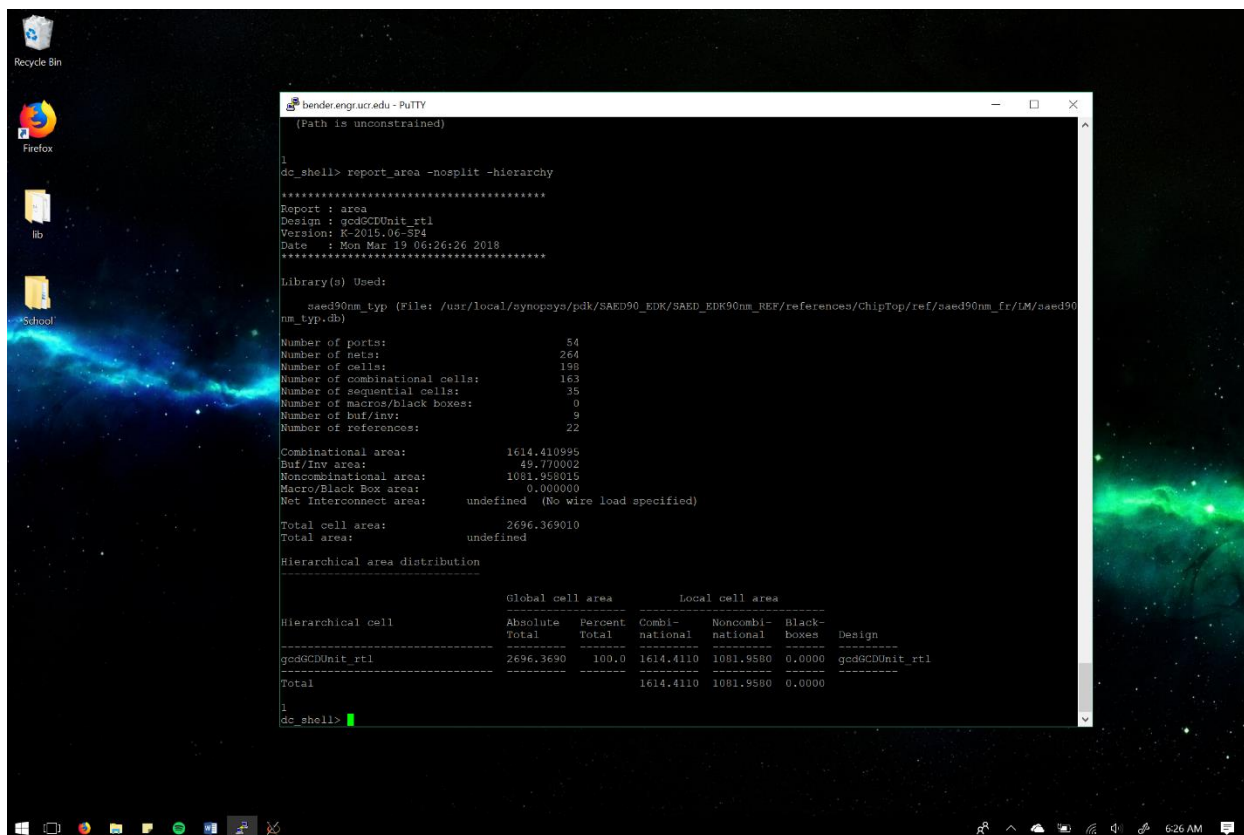
Result of gate level for 4bit Full adder



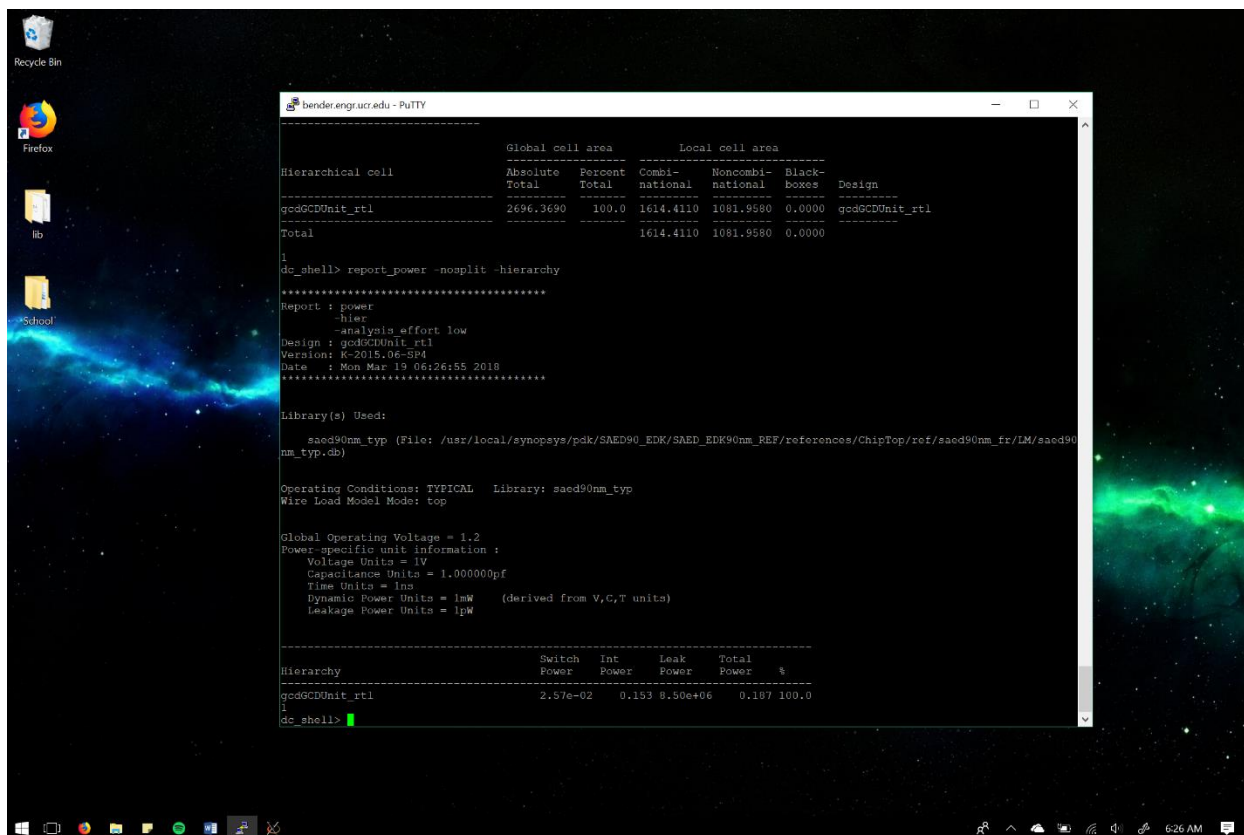
Final layout for GCD (Fig 51)



Timing Report



Area Report



Power Report


```
Recycle Bin
Firefox
lib
School

bender.engr.ucr.edu - PuTTY
gdcgcdunit_rtl 2.57e-02 0.153 8.50e+06 0.187 100.0

dc_shell> report_reference -nosplit -hierarchy

*****
Report : reference
Design : gdcgcdunit_rtl
Version: K-2015.06-SP4
Date : Mon Mar 19 06:27:37 2018
*****

Attributes:
b - black box (unknown)
bo - allow boundary optimization
d - dont_touch
mo - map_only
h - hierarchical
n - noncombinational
r - removable
s - synthetic operator
u - contains unmapped logic

Reference Library Unit Area Count Total Area Attributes
-----
AND2X1 saed90nm_typ 7.445000 1 7.445000
AO21X1 saed90nm_typ 10.138000 1 10.138000
AO221X1 saed90nm_typ 12.502000 4 51.608002
AO222X1 saed90nm_typ 14.746000 20 294.920006
DFFABX1 saed90nm_typ 32.256001 32 1032.192017 n
DFFX1 saed90nm_typ 24.882999 2 49.765999 n
FACD2X1 saed90nm_typ 29.490999 11 324.400991 r
INVX0 saed90nm_typ 5.530000 9 49.770002
ISOLANDX1 saed90nm_typ 7.373000 4 29.492001
ISOLORX1 saed90nm_typ 7.387000 4 29.548000
MUX21X1 saed90nm_typ 11.059000 4 44.236000
NAND2X0 saed90nm_typ 5.443000 47 255.820992
NAND3X0 saed90nm_typ 7.373000 17 125.341002
NAND4X0 saed90nm_typ 8.294000 3 24.881999
NOR2X0 saed90nm_typ 5.530000 7 38.710001
NOR3X0 saed90nm_typ 8.294000 2 16.587999
NOR4X0 saed90nm_typ 9.216000 4 36.863998
OQ21X1 saed90nm_typ 9.216000 3 27.647999
OQ22X1 saed90nm_typ 11.059000 19 210.121000
OQ221X1 saed90nm_typ 12.802000 1 12.802000
OR4X1 saed90nm_typ 10.152000 1 10.152000
XNOR2X1 saed90nm_typ 13.824000 1 13.824000
-----
Total 22 references 2696.369010
1
dc_shell>
```

Reference Report

```
Recycle Bin
Firefox
lib
School

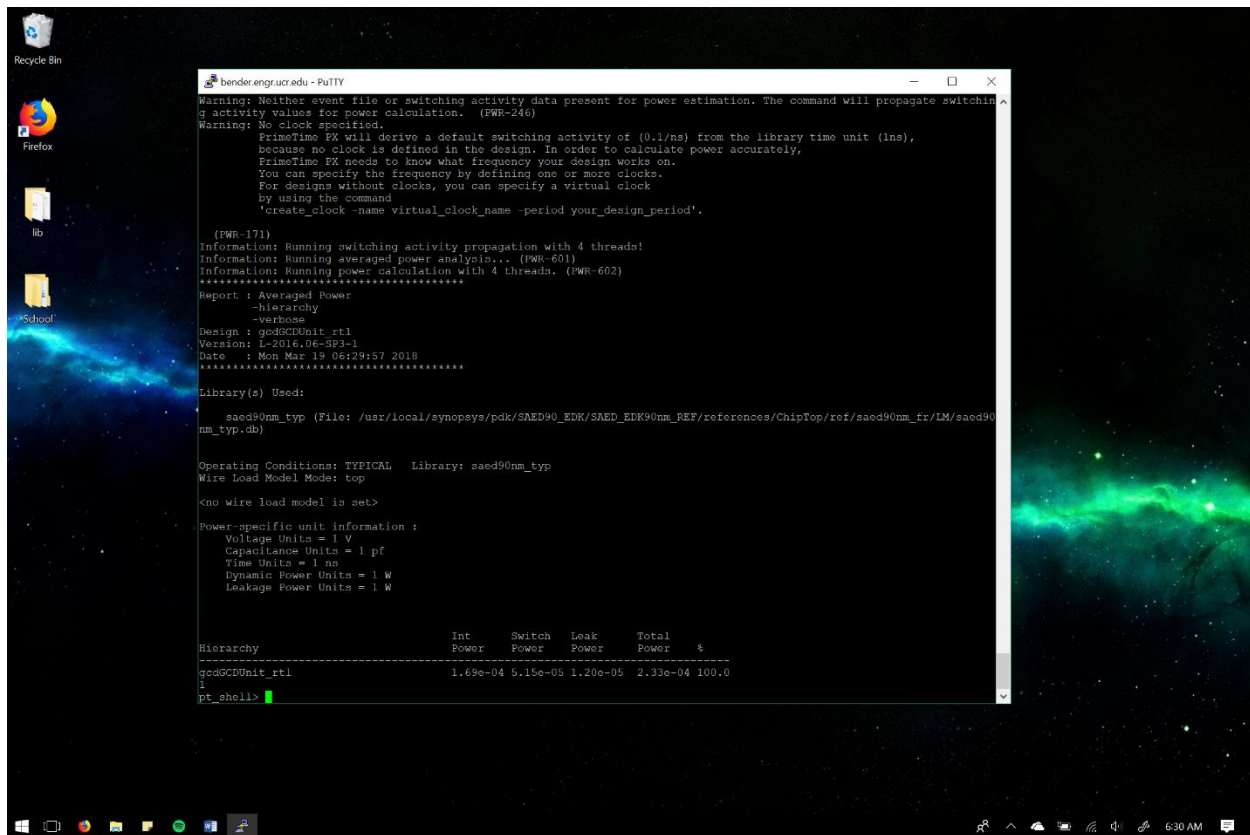
bender.engr.ucr.edu - PuTTY
DW1X1      saed90nm_typ  24.862999  2  49.763999 n
FADDX1     saed90nm_typ  29.496999  11 324.400991 r
INVX0      saed90nm_typ  5.530000   9  49.770002
ISOLANDX1  saed90nm_typ  7.373000   4  29.492001
ISOLGEX1   saed90nm_typ  7.387000   4  29.548000
MEX22X1    saed90nm_typ  11.059000  4  44.236000
NAND2X0     saed90nm_typ  5.443000  47 255.820992
NAND3X0     saed90nm_typ  7.373000  17 125.341002
NAND4X0     saed90nm_typ  8.294000   3  24.881999
NOR2X0      saed90nm_typ  5.530000   7  39.710001
NOR3X0      saed90nm_typ  8.294000   2  16.587999
NOR4X0      saed90nm_typ  9.216000   4  36.863998
OAX1X1      saed90nm_typ  9.216000   3  27.647999
OAX2X1      saed90nm_typ  11.059000  19 210.121000
OAX21X1     saed90nm_typ  12.902000   1  12.902000
OR4X1       saed90nm_typ  10.152000   1  10.152000
XNOR2X1     saed90nm_typ  13.824000   1  13.824000
-----
Total 22 references 2696.369010
l
dc_shell> report_resources -nosplit -hierarchy
*****
Report : resources
Design : godgcd0nit_rtl
Version: K-2015.06-SP4
Date   : Mon Mar 19 06:28:04 2018
*****

Resource Report for this hierarchy in file ./god_dpath.v

| Cell      | Module      | Parameters | Contained Operations |
|-----|-----|-----|-----|
| sub_x_2   | DW01_sub    | width=16   | GCDdpath0/sub_45 (god_dpath.v:45) |
| lt_x_3    | DW_cmp      | width=16   | GCDdpath0/lt_51 (god_dpath.v:51) |
|-----|-----|-----|-----|

Implementation Report
|-----|-----|-----|-----|
| Cell      | Module      | Current    | Set      |
|-----|-----|-----|-----|
| sub_x_2   | DW01_sub    | apparch (area) |         |
| lt_x_3    | DW_cmp      | apparch (area) |         |
|-----|-----|-----|-----|
l
dc_shell>
```

Resource Report



```
bender.engr.ucr.edu - PuTTY
Warning: Neither event file or switching activity data present for power estimation. The command will propagate switching activity values for power calculation. (PWR-246)
Warning: No clock specified.
PrimeTime EX will derive a default switching activity of (0.1/ns) from the library time unit (1ns), because no clock is defined in the design. In order to calculate power accurately, PrimeTime EX needs to know what frequency your design works on.
You can specify the frequency by defining one or more clocks.
For designs without clocks, you can specify a virtual clock by using the command
'create_clock -name virtual_clock_name -period your_design_period'.

[PWR-171]
Information: Running switching activity propagation with 4 threads!
Information: Running averaged power analysis... (PWR-601)
Information: Running power calculation with 4 threads. (PWR-602)
*****
Report : Averaged Power
        -hierarchy
        -verbose
Design : gcdGCDUnit_rtl
Version: I-2016.06-SP3-1
Date   : Mon Mar 19 06:29:57 2018
*****

Library(s) Used:

    saed90nm_typ (File: /usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/saed90nm_ft/LM/saed90nm_typ.db)

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: top

<no wire load model is set>

Power-specific unit information :
Voltage Units = 1 V
Capacitance Units = 1 pf
Time Units = 1 ns
Dynamic Power Units = 1 W
Leakage Power Units = 1 W

Hierarchy                                     Int      Switch  Leak     Total
Power      Power      Power      Power
-----
gcdGCDUnit_rtl                             1.69e-04 5.15e-05 1.20e-05 2.33e-04 100.0
1
pt_shell>
```

Primetime Power Report

Conclusion

I did not encounter any problems