EE168 Lab 4
Tutorial Continued

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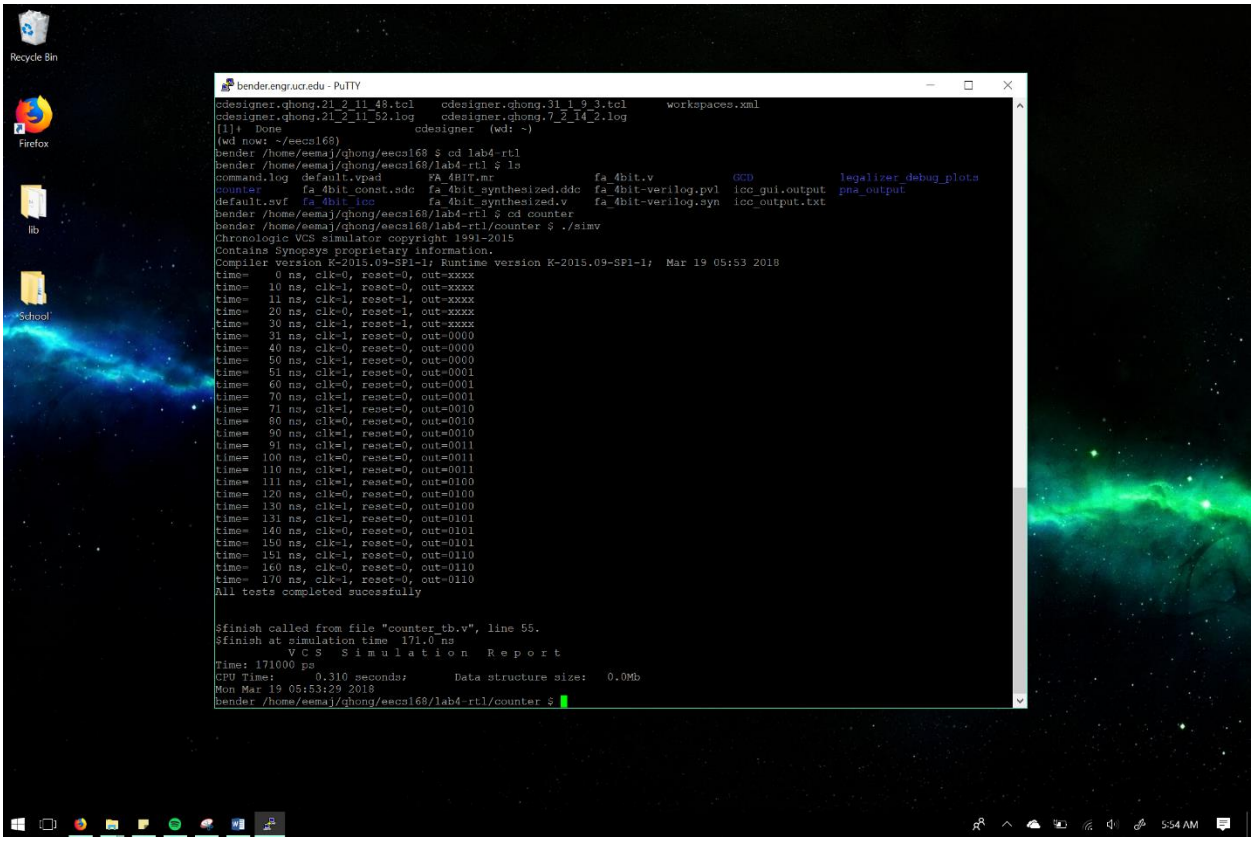
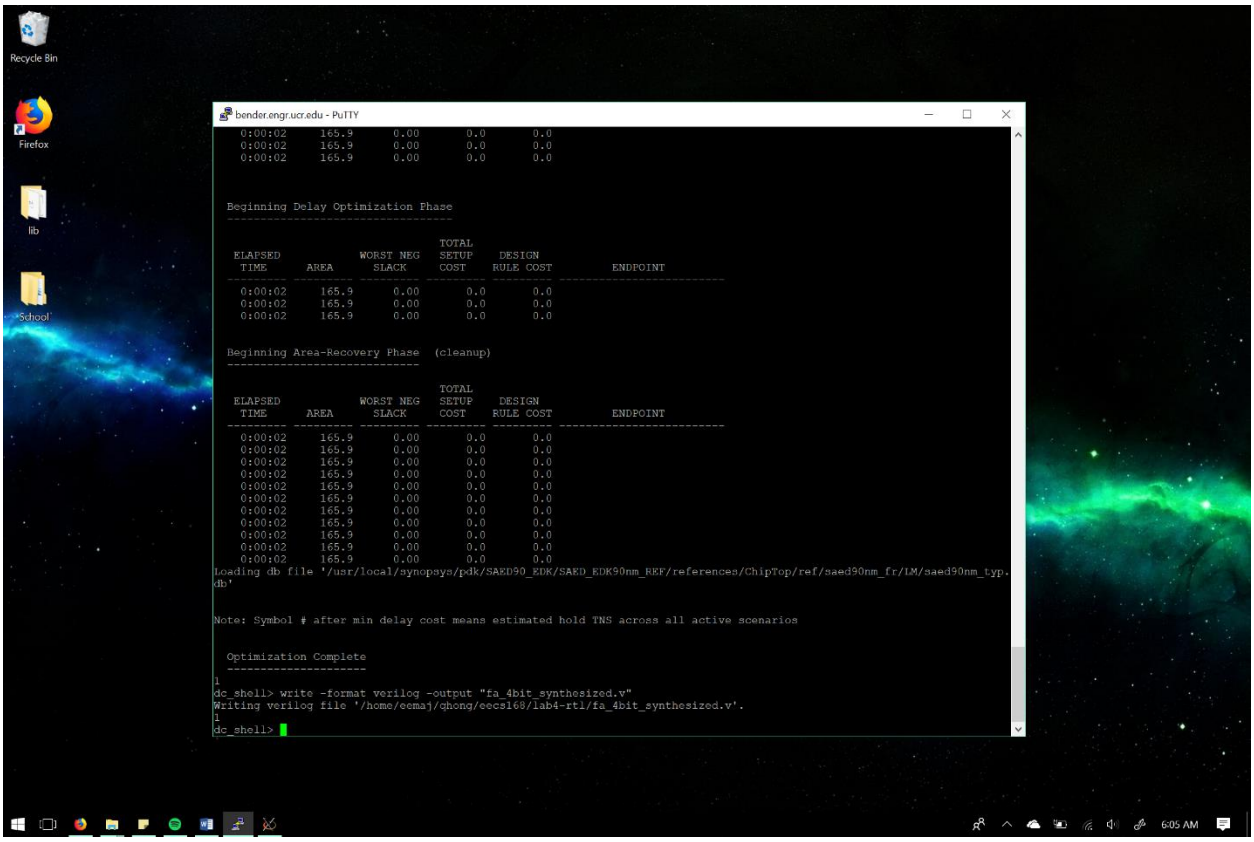
Introduction

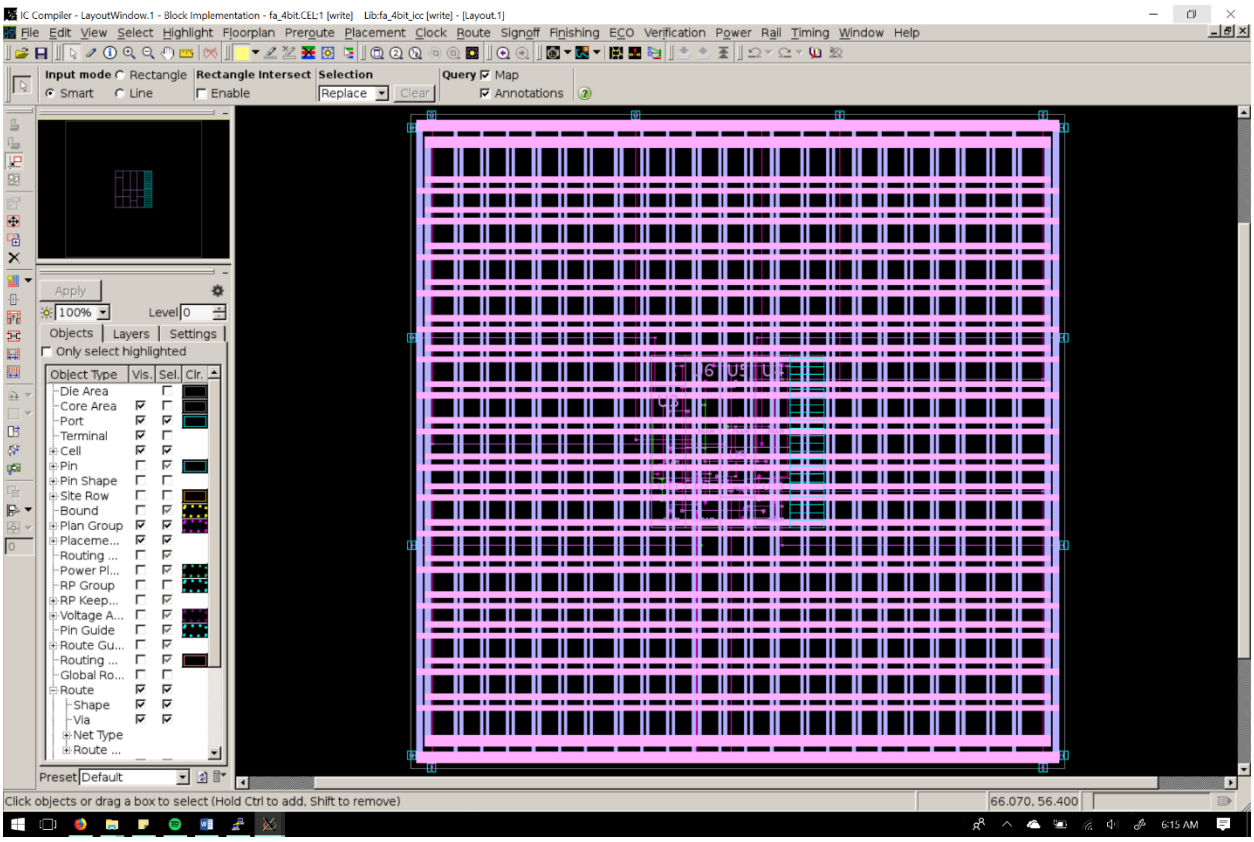
Images



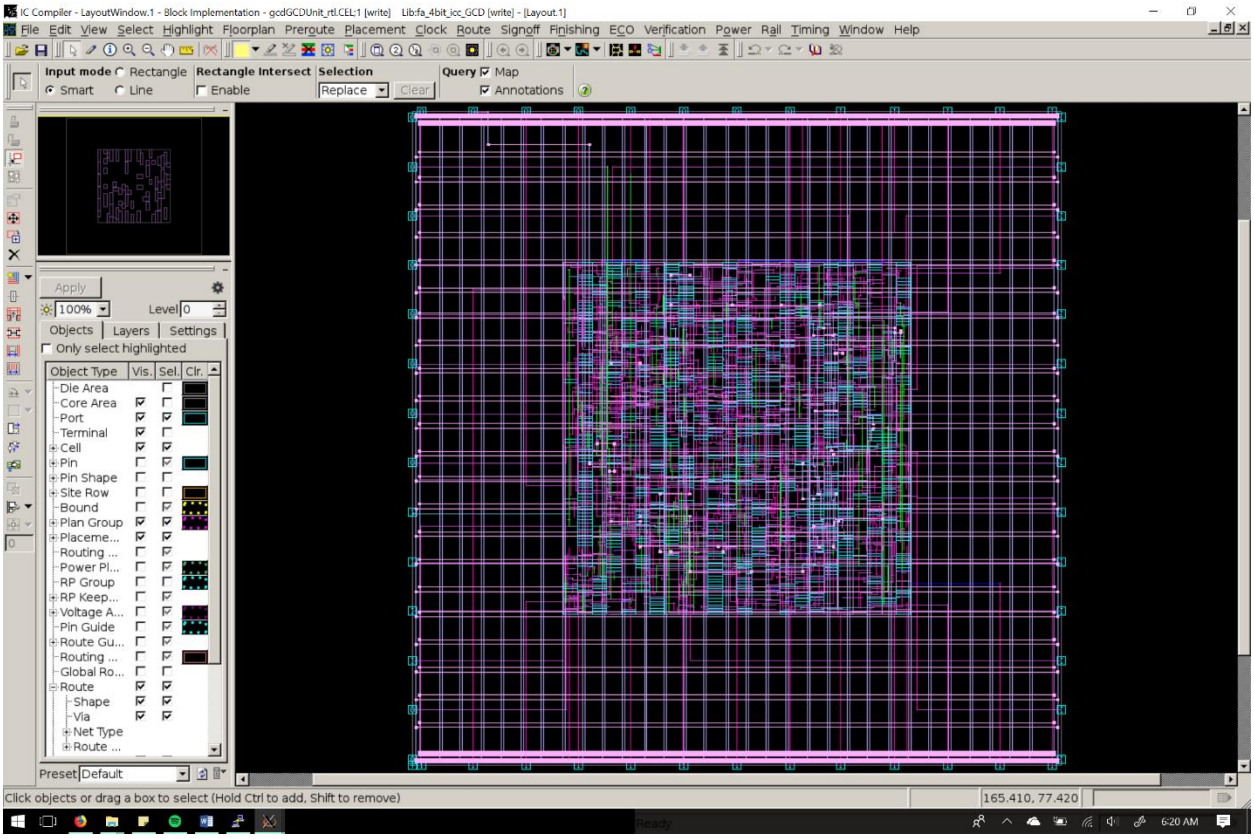
Sim result of Counter



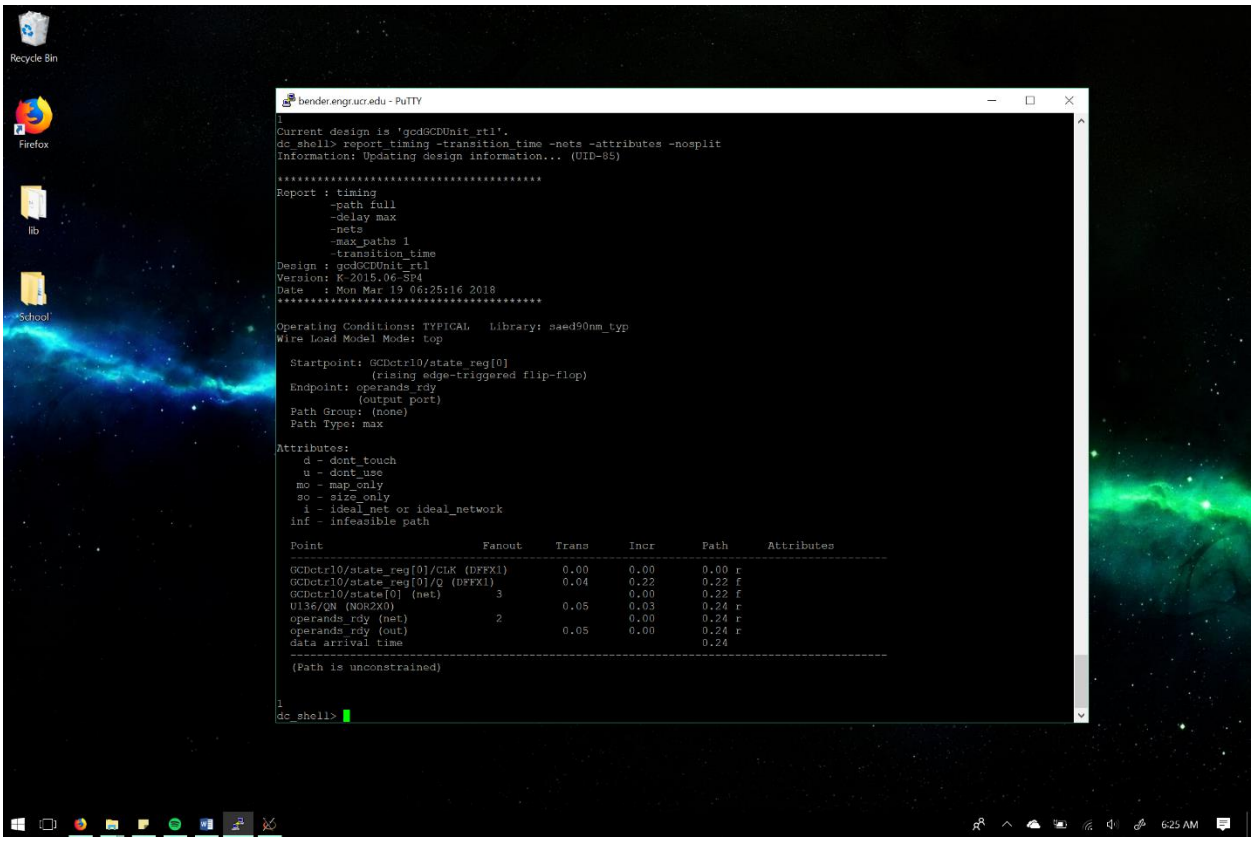
Result of gate level for 4bit Full adder



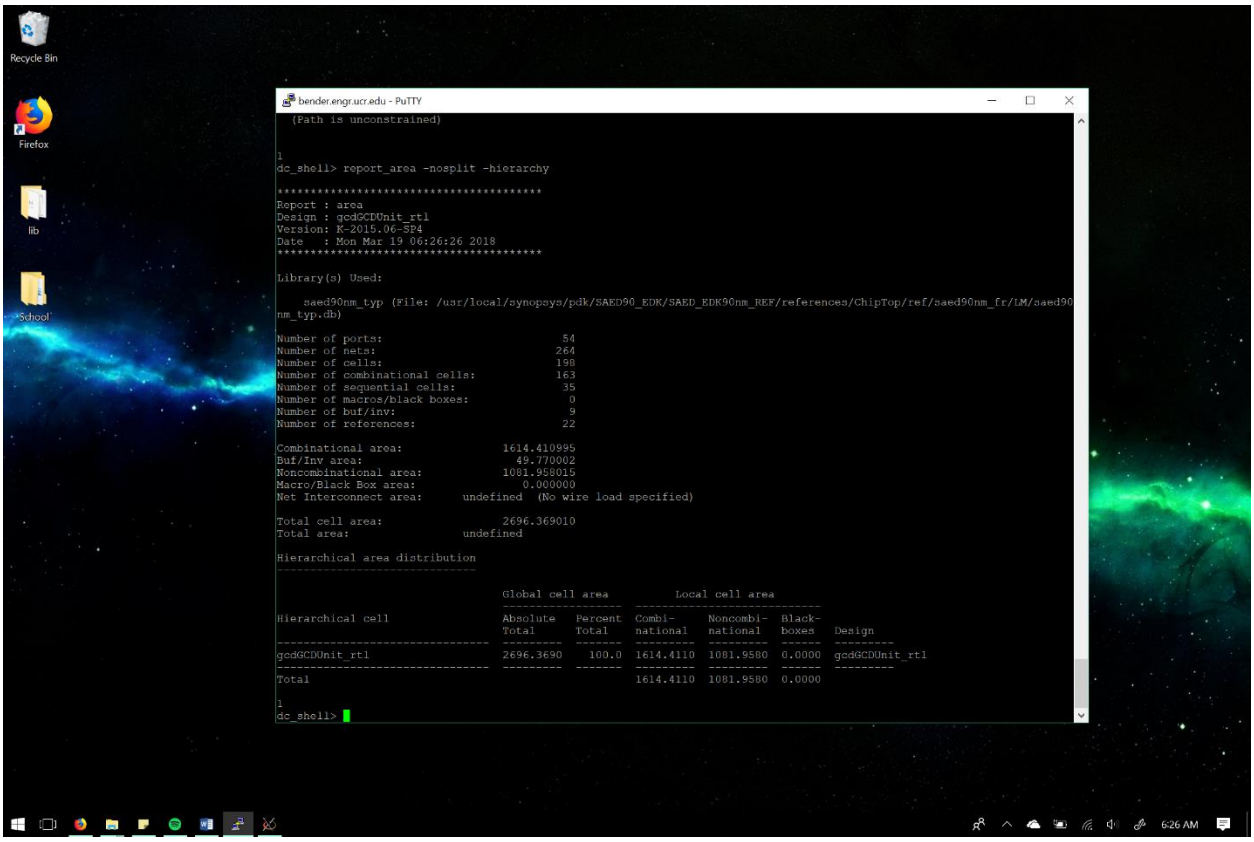
Final layout for 4-bit adder (Fig 49)



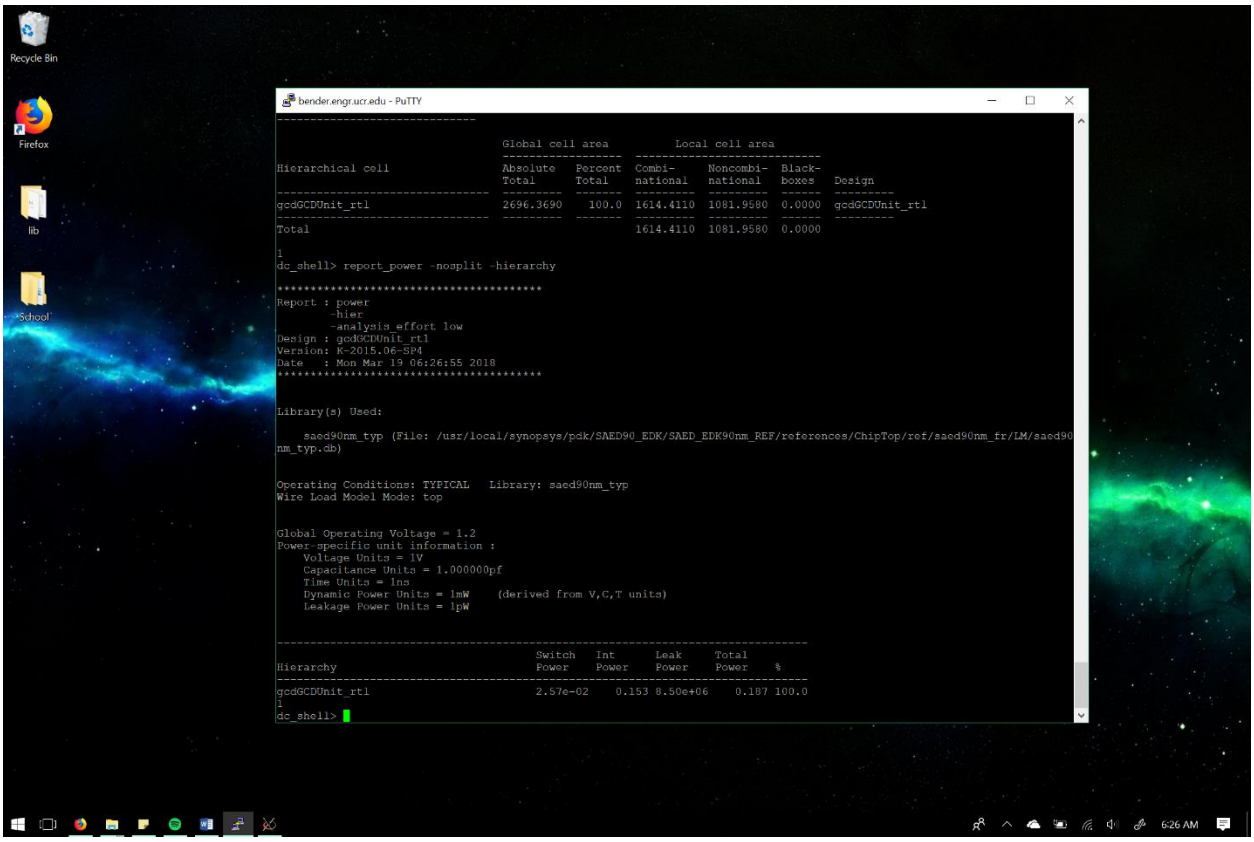
Final layout for GCD (Fig 51)



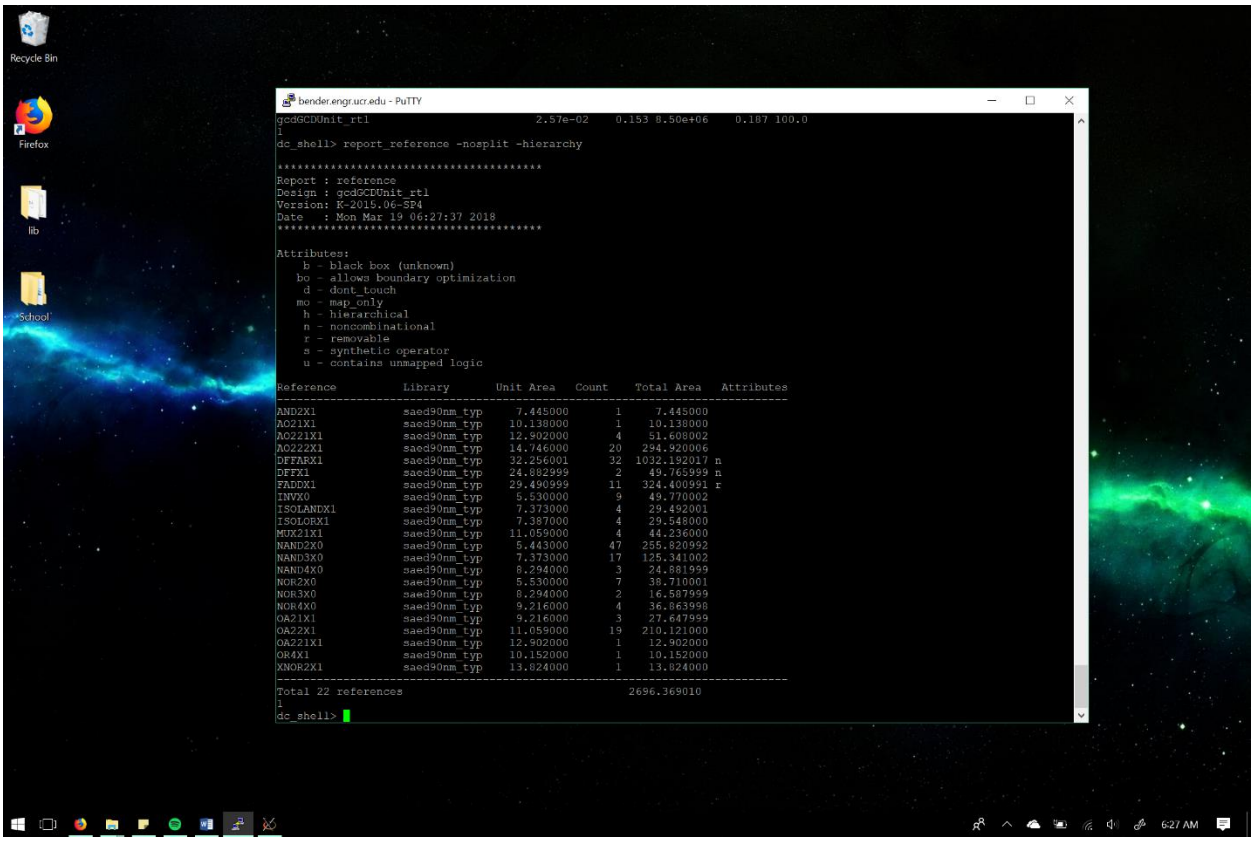
Timing Report


Recycle Bin
Firefox
lib
School
bender.engr.ucr.edu - PuTTY
(Path is unconstrained)
1
dc_shell> report_area -nosplit -hierarchy
****
Report : area
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date : Mon Mar 19 06:26:26 2018
****
Library(s) Used:
saed90nm_typ (File: /usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/saed90nm_fr/LM/saed90nm_typ.db)
Number of ports: 54
Number of nets: 264
Number of cells: 198
Number of combinational cells: 163
Number of sequential cells: 35
Number of macros/black boxes: 0
Number of buf/inv: 9
Number of references: 22
Combinational area: 1614.410995
Buf/Inv area: 49.770002
Noncombinational area: 1081.958015
Macro/Black Box area: 0.000000
Net Interconnect area: undefined (No wire load specified)
Total cell area: 2696.369010
Total area: undefined
Hierarchical area distribution
Global cell area
Local cell area
Hierarchical cell
Absolute Total
Percent Total
Combi-national
Noncombi-national
Black-boxes
Design
gcdGCDUnit_rtl 2696.3690 100.0 1614.4110 1081.9580 0.0000 gcdGCDUnit_rtl
Total 1614.4110 1081.9580 0.0000
1
dc_shell>
6:26 AM

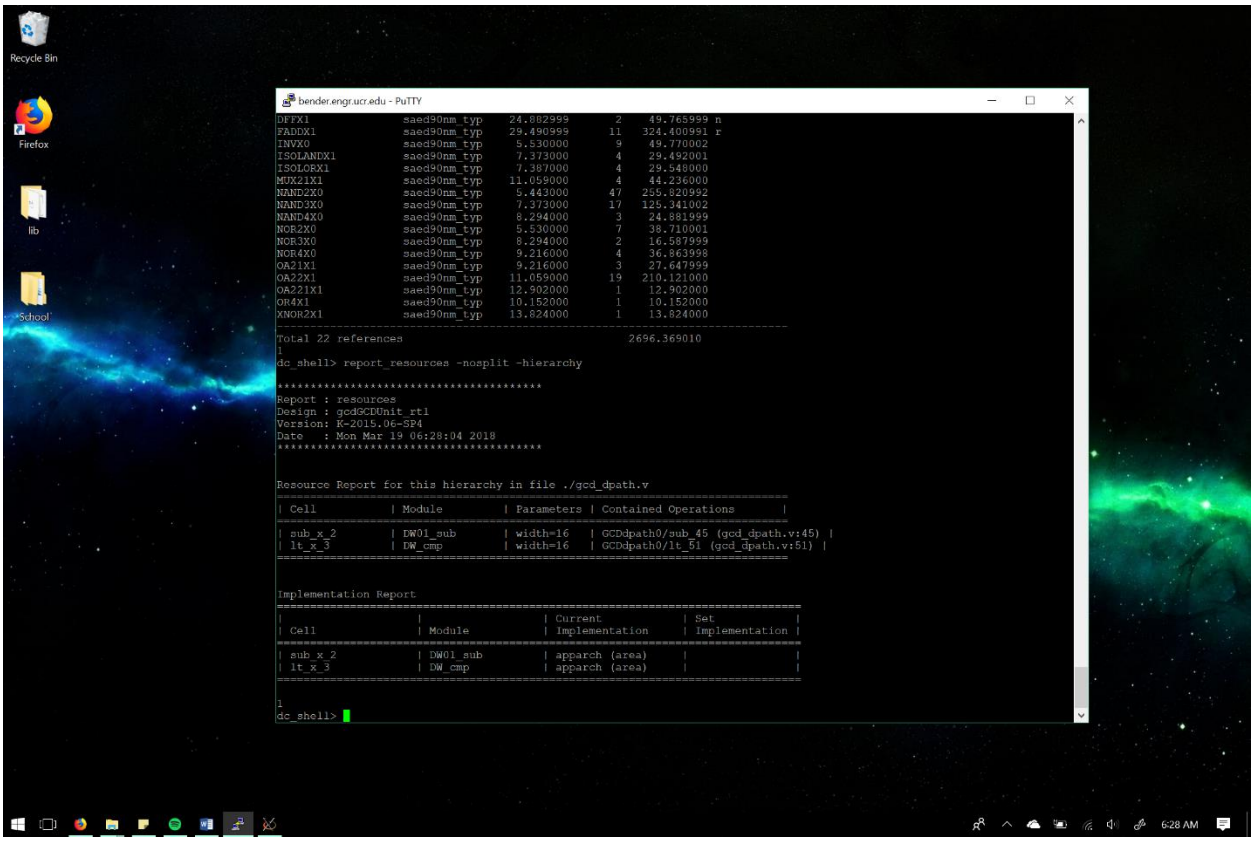
Area Report



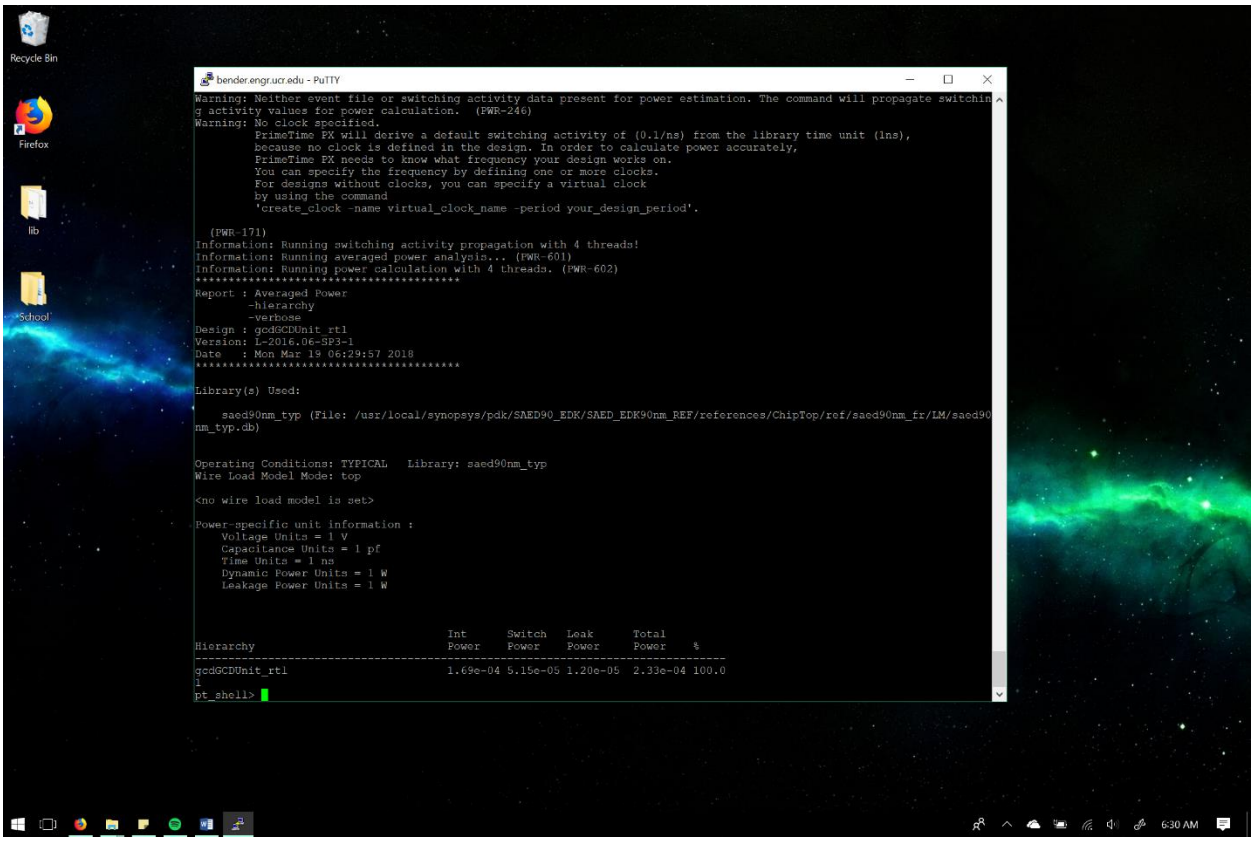
Power Report



Reference Report



Resource Report



Primetime Power Report

Conclusion

I did not encounter any problems