Jeffery Xu, 1832975
Simon Chen, 1832768
Cynthia Li, 1839952

EE 331 Lab
Experiment 4

1. Introduction

This document is a report on the observation of the behavior of the CD4007 CMOS integrated circuit. The information is provided in the following format. In section 2, the data for all 3 procedures are presented in order. In procedure 1, we use the E-mode MOSFET driver with resistor load to set up a simple inverter design. Procedure 2 is similar to procedure 1 but with the addition of a JFET to the load. In procedure 3, we simulate and observe the behavior of a CMOS inverter circuit. In section 3, results are analyzed and questions regarding the procedures are addressed. Finally, in Section 4, overall results are discussed and conclusions are made.

2. Data

2.1 E-mode MOSFET driver with resistor load

In procedure 1, we utilize one NMOS inside the CD4007 chip and connect a resistor to set up a resistor load MOSFET driver circuit. Then, we sweep the Vin from 0V to 5V and test the circuit with 1K Ohm, 4.7k Ohm and 20K Ohm resistors to observe the VTC under different resistance. Finally, we need to compare and analyze the results and decide which resistance is better for logic gates in part 3.

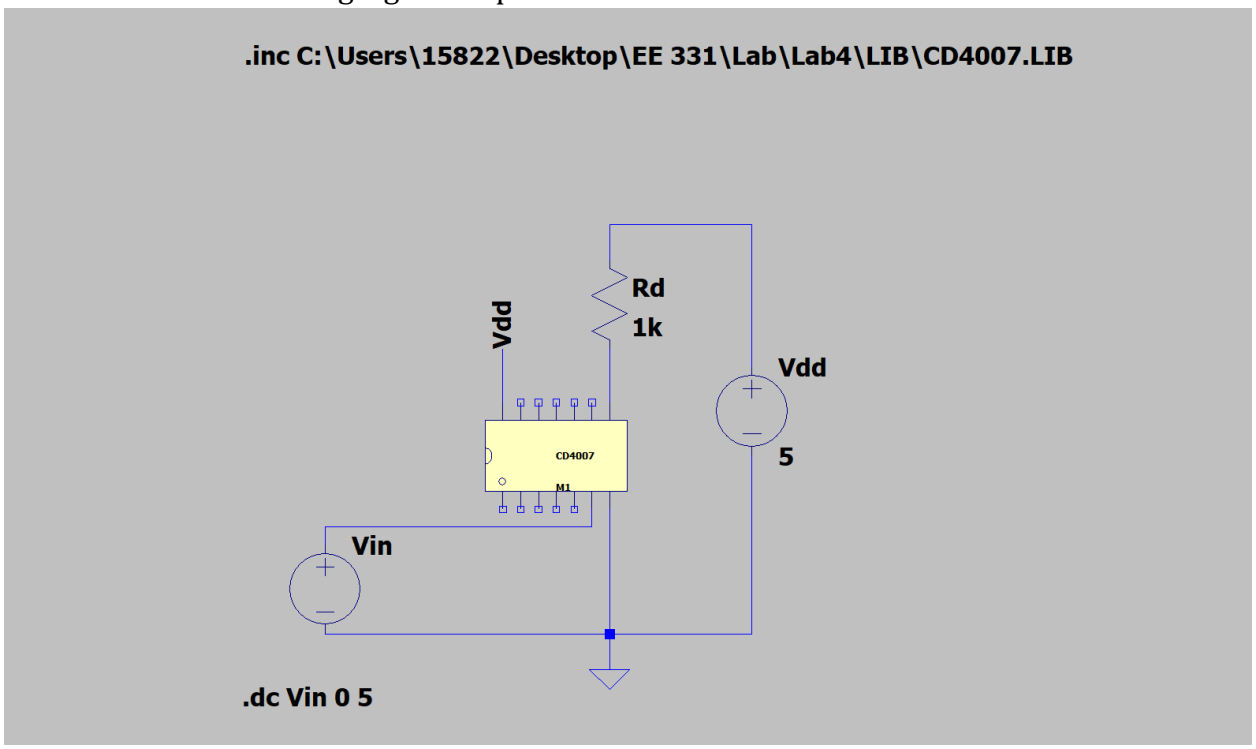

Fig. 1 Procedure 1 Schematics

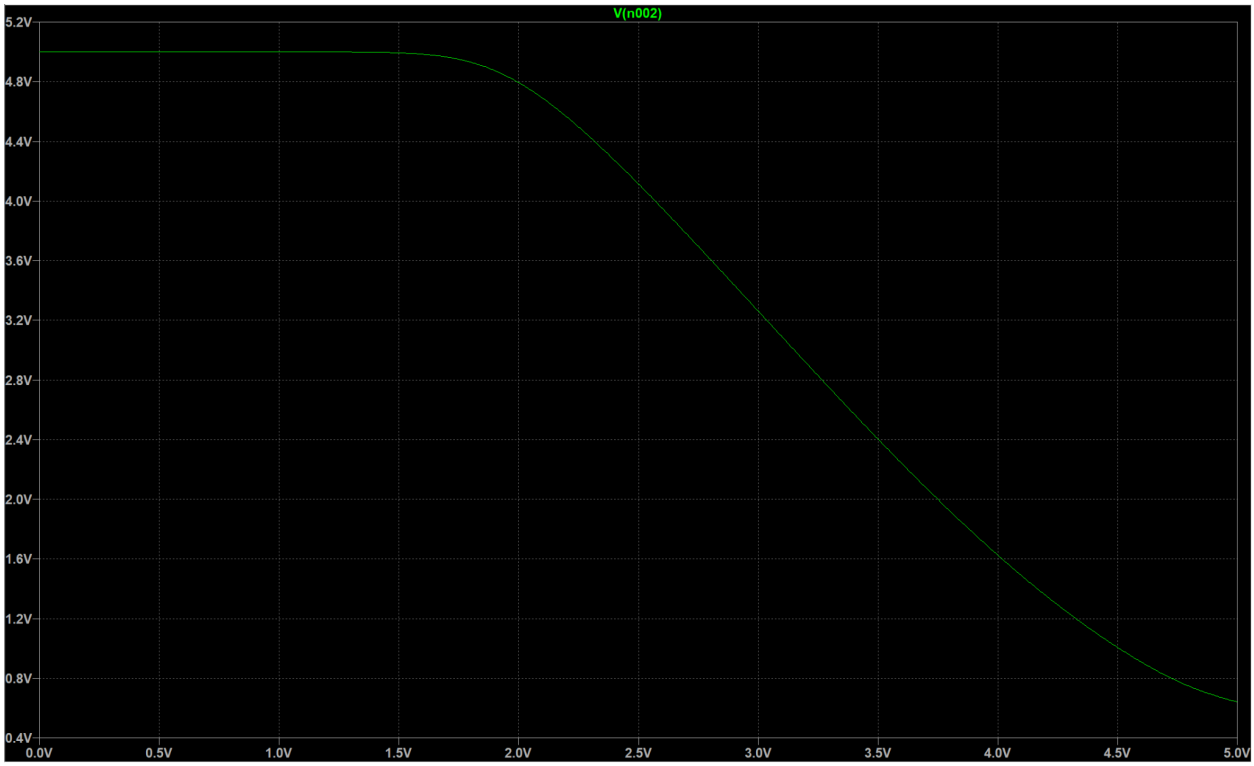

Fig. 2 plot for VTC with Rd = 1k ohm

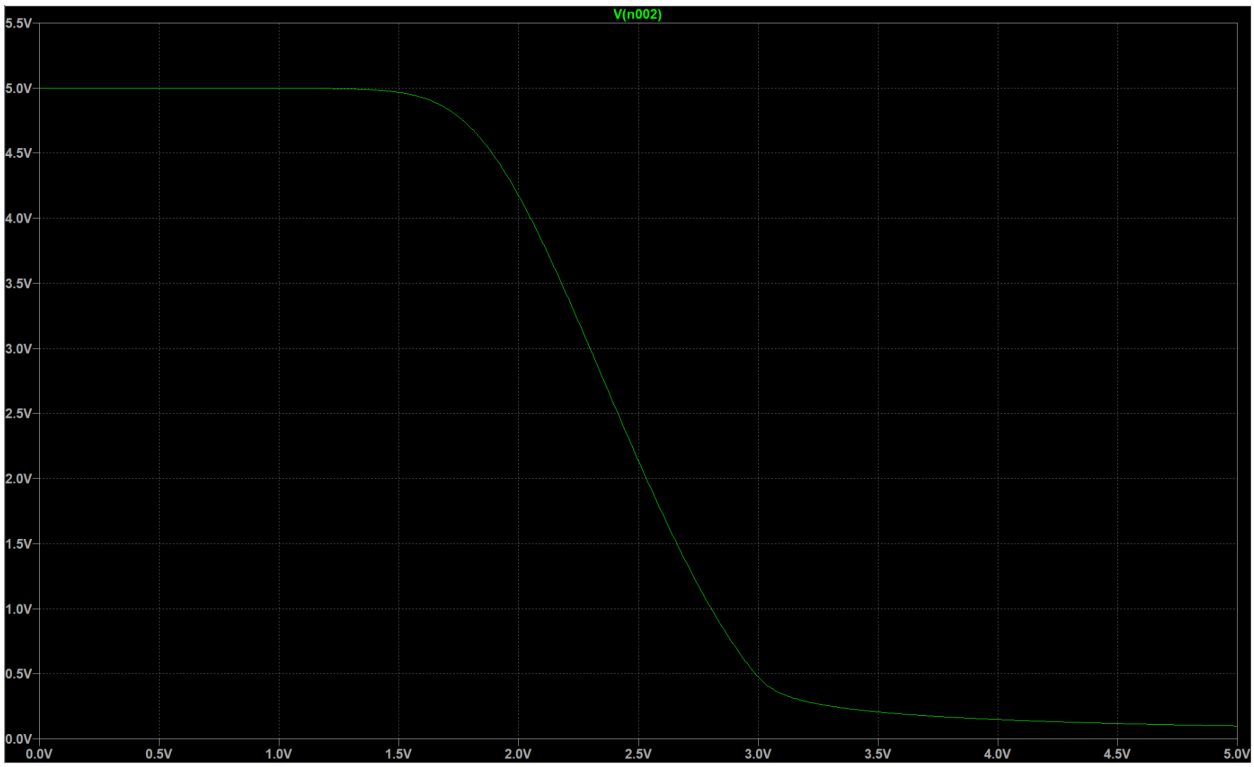

Fig. 3 plot for VTC with Rd = 4.7k ohm

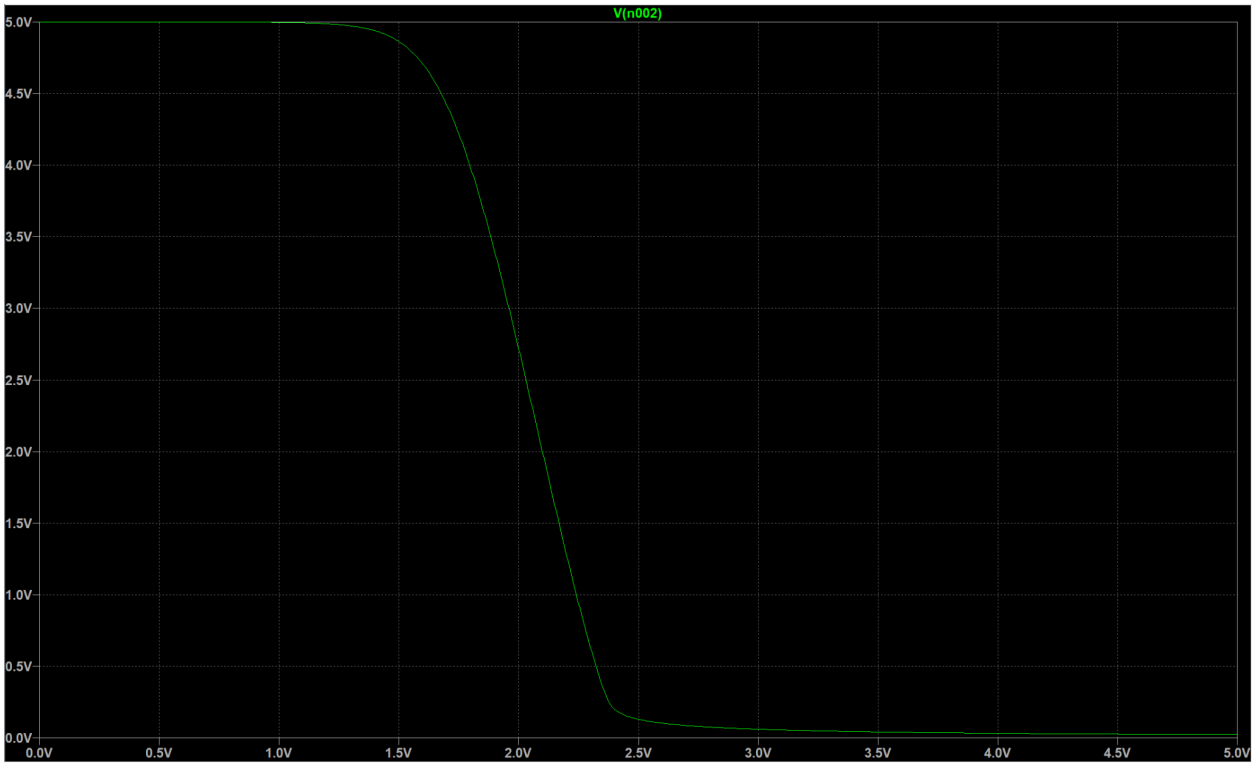

Fig. 4 plot for VTC with Rd = 20k ohm

2.2 E-mode MOSFET driver with D-mode load device (non-simulation)

In this procedure, we are given with the VTC for resistance of 1k Ohm and 10k Ohm in Fig. 5. Since V_IL = V_TN + 1/(K_n * R), V_IH = V_TN - 1/(K_n * R) + 1.63sqrt(Vdd/K_n * R), V_drop = V_IH - V_IL = 1.63sqrt(Vdd/K_n * R) - 2/ (K_n * R). While other parameters are the same, when R increases, the change under the square root will be less than that without the square root, indicating less increase but more decrease in V_drop when R is increasing. In other words, with R increasing, VTC goes through faster change , and results in a bigger gap. Therefore, we see that the lower curve has a faster and bigger voltage drop, indicating it requires a larger resistance to complete. Thus, the lower curve is R1 = 10k Ohm, the upper curve is R1 = 1k Ohm.

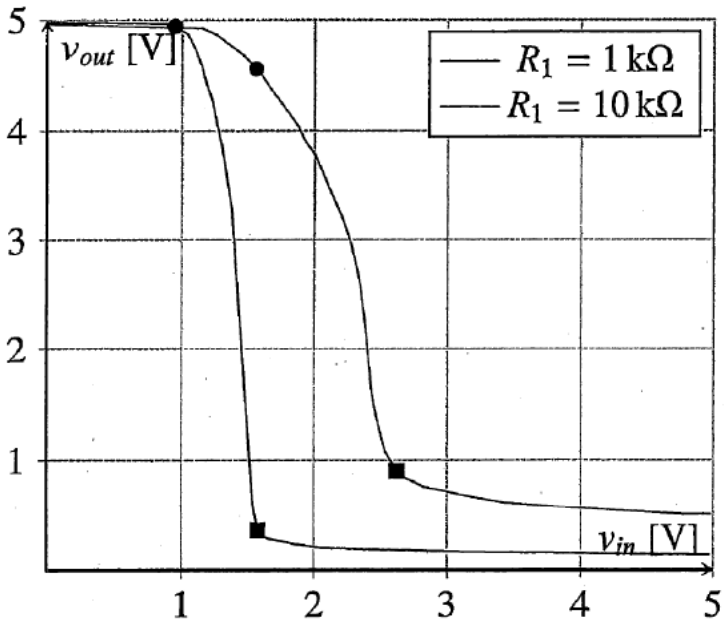

Fig. 5 VTC for the inverter gate with R1 = 1k ohm and R1= 10k ohm

2.3 CMOS inverter circuit

In procedure 3, we use a pair of PMOS and NMOS inside the CD4007 chip to create a CMOS and sweep the voltage Vin from 0V to 5V to observe the VTC of the circuit. Then, we need to analyze the behavior of CMOS in part 3.

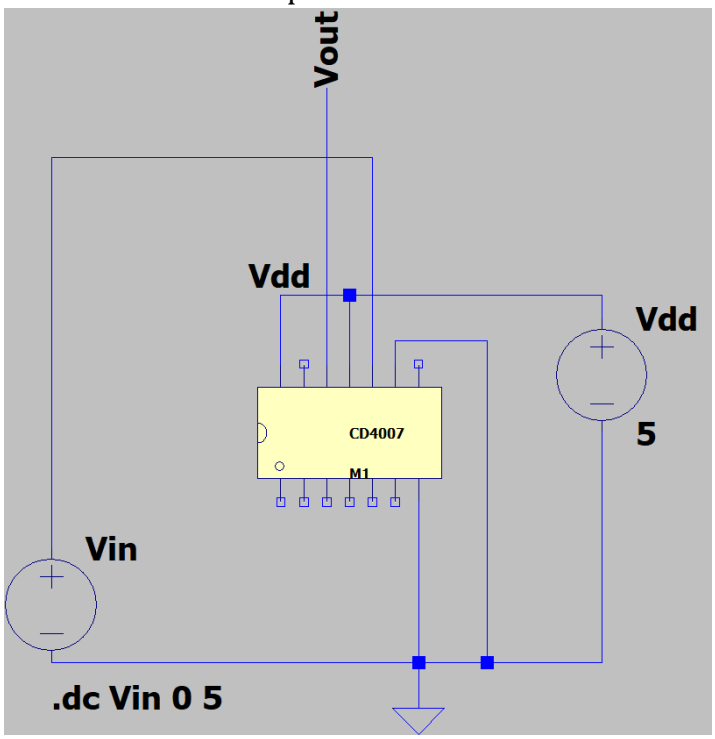

Fig. 6 Schematic of Procedure 3

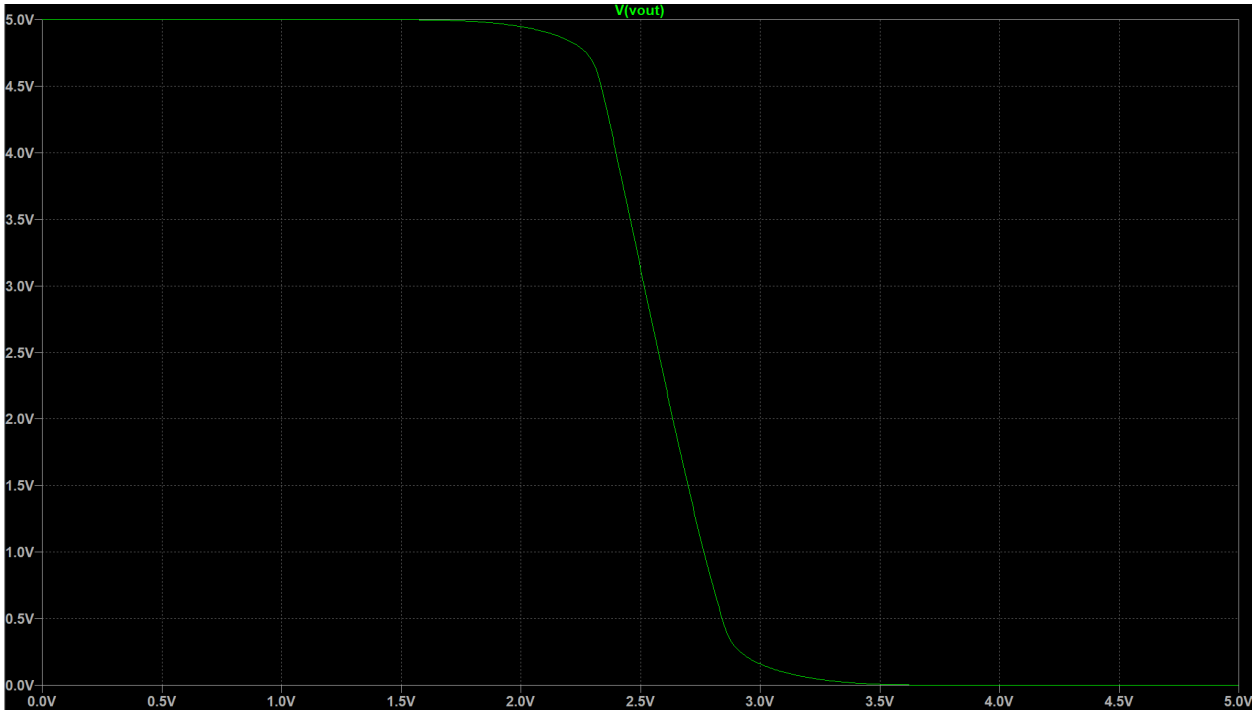

Fig. 7 plot of VTC of CMOS

3. Questions

3.1 E-mode MOSFET driver with resistor load

a) When the low voltage is applied to the gate, the inversion layer will not form and pn functions would block the current so the circuit acts as an open circuit. Thus, the output voltage is high. When the input voltage is high, the inversion layer forms and current would pass through the transistor. The transistor has inner resistance and the circuit as a voltage divider. The resistor divides much more voltage than the transistor so the output voltage is low.

b) For finding the output high voltage Voh and the output low voltage Vol. we need to locate the points where the slope is equal to -1.

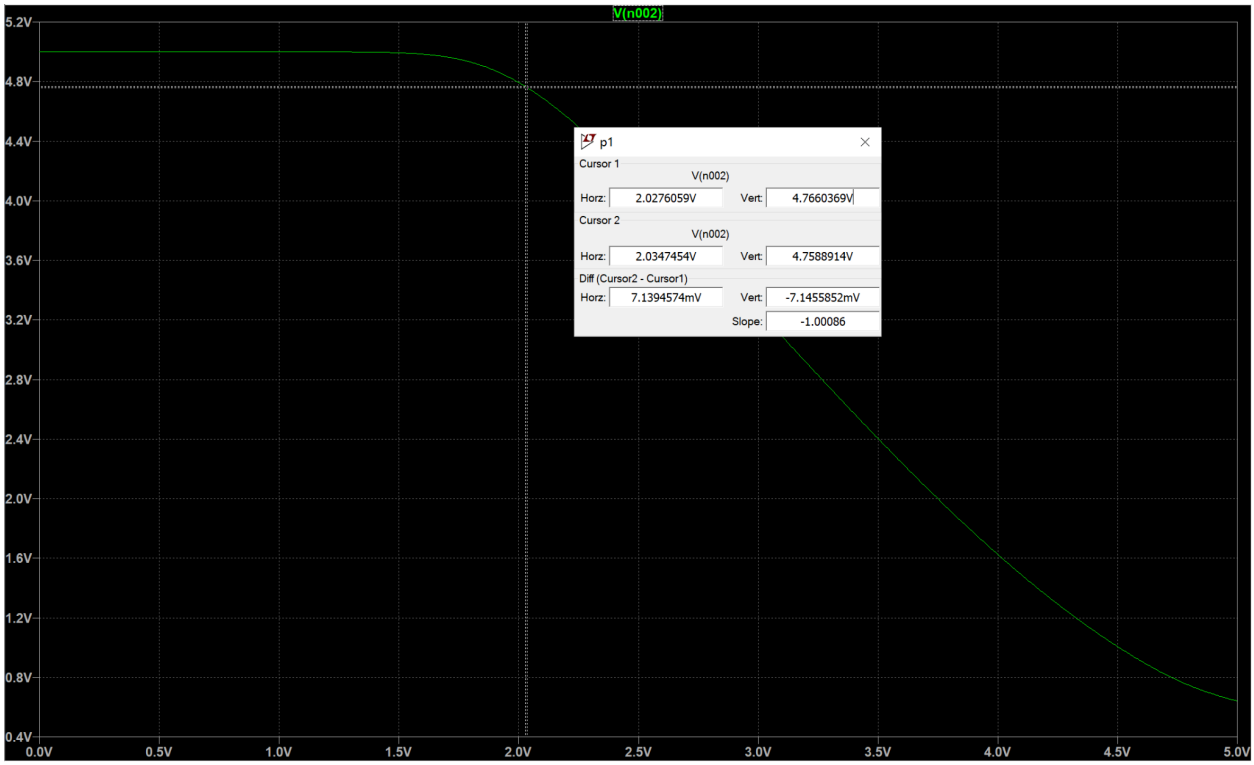

Fig. 8 Voh for Rd = 1k oh

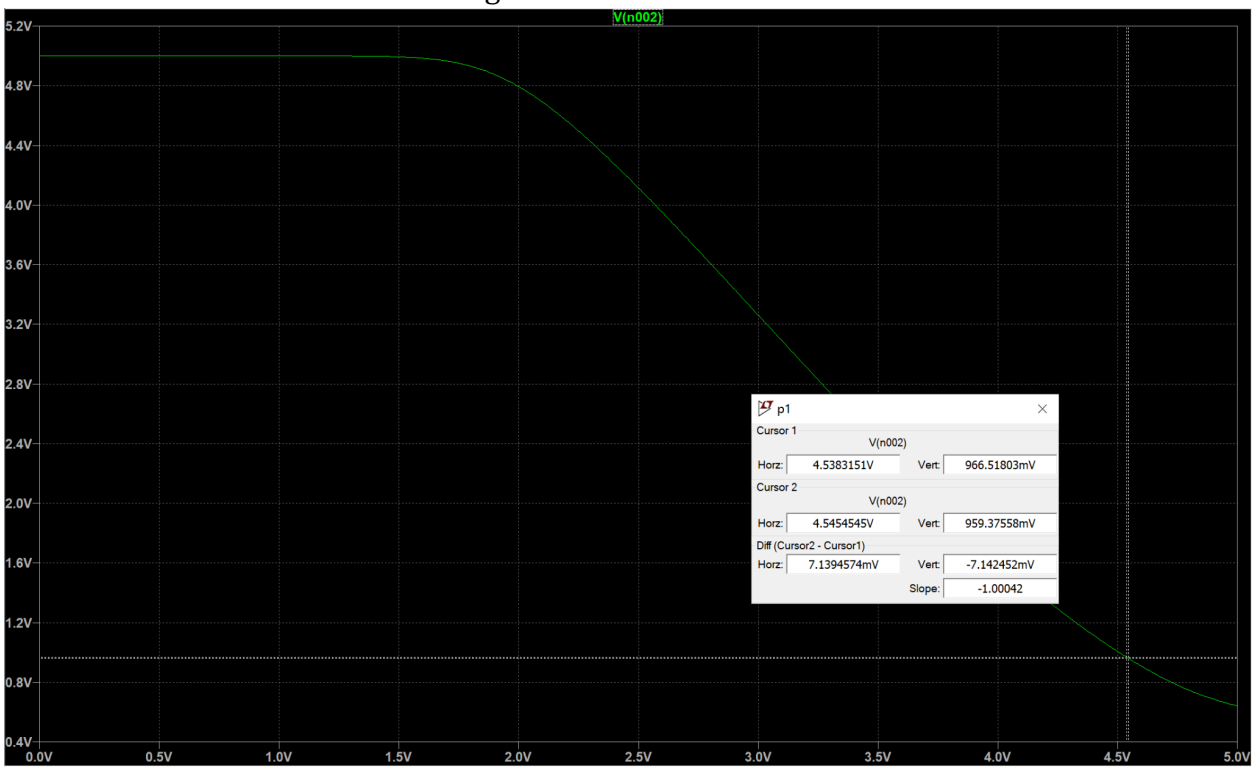

Fig. 9 Vol for Rd = 1k ohm

From Fig. 8 and Fig. 9, we can see that for Rd = 1k ohm, Voh = 4.76V, Vol = 0.96V

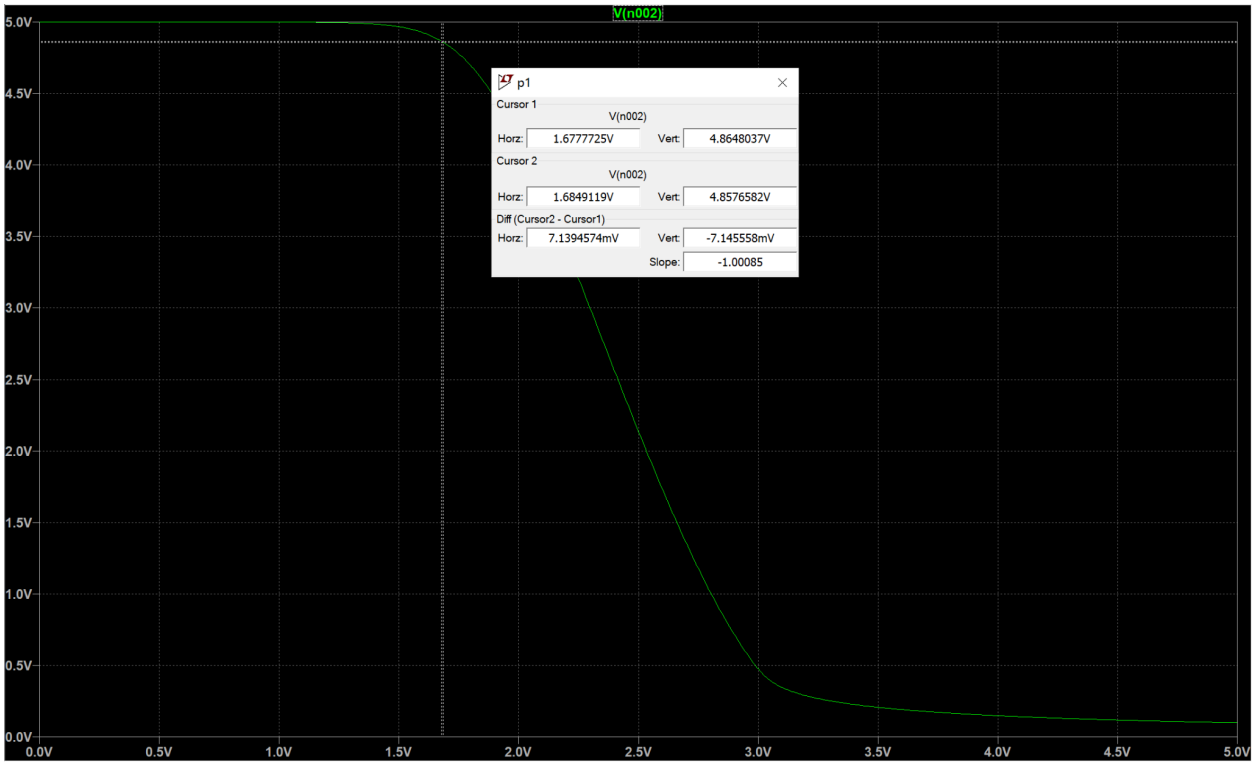

Fig. 10 Voh for Rd = 4.7k ohm

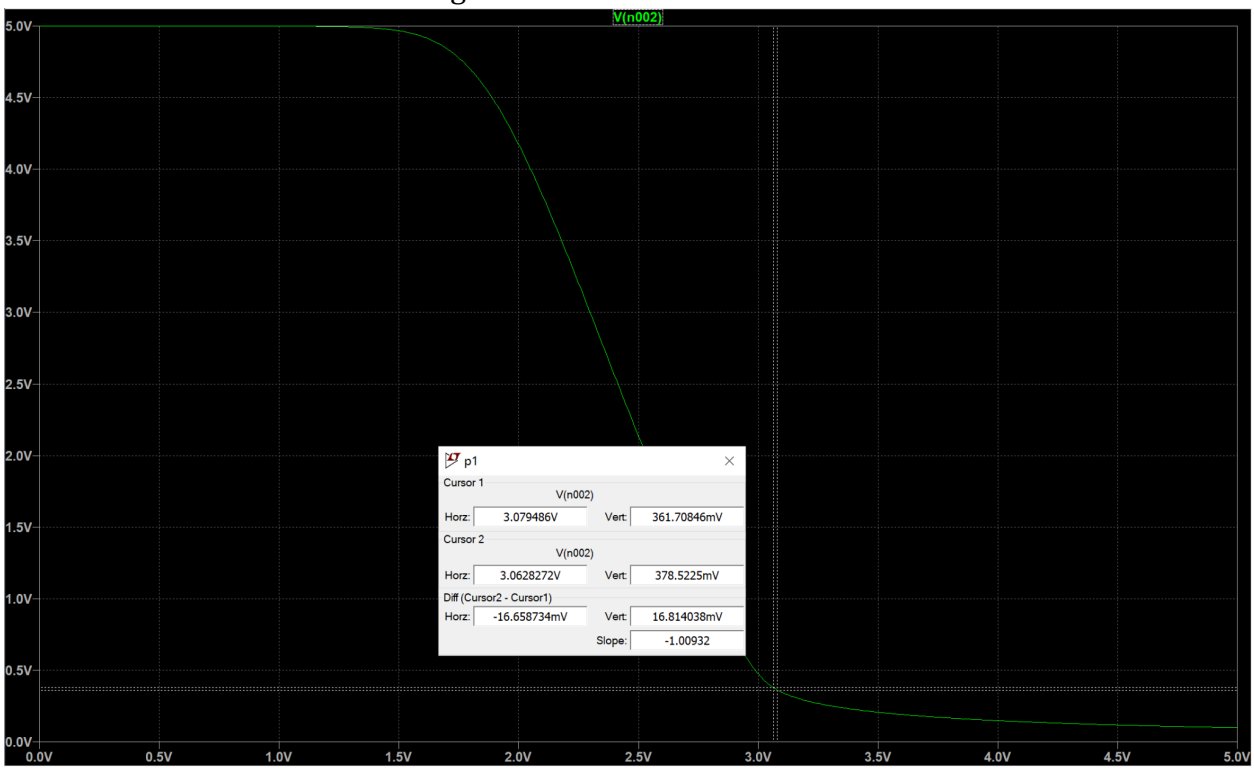

Fig. 11 Vol for Rd = 4.7k ohm

From Fig. 10 and Fig. 11, we can see that for Rd = 4.7k ohm, Voh = 4.86V, Vol = 0.37V

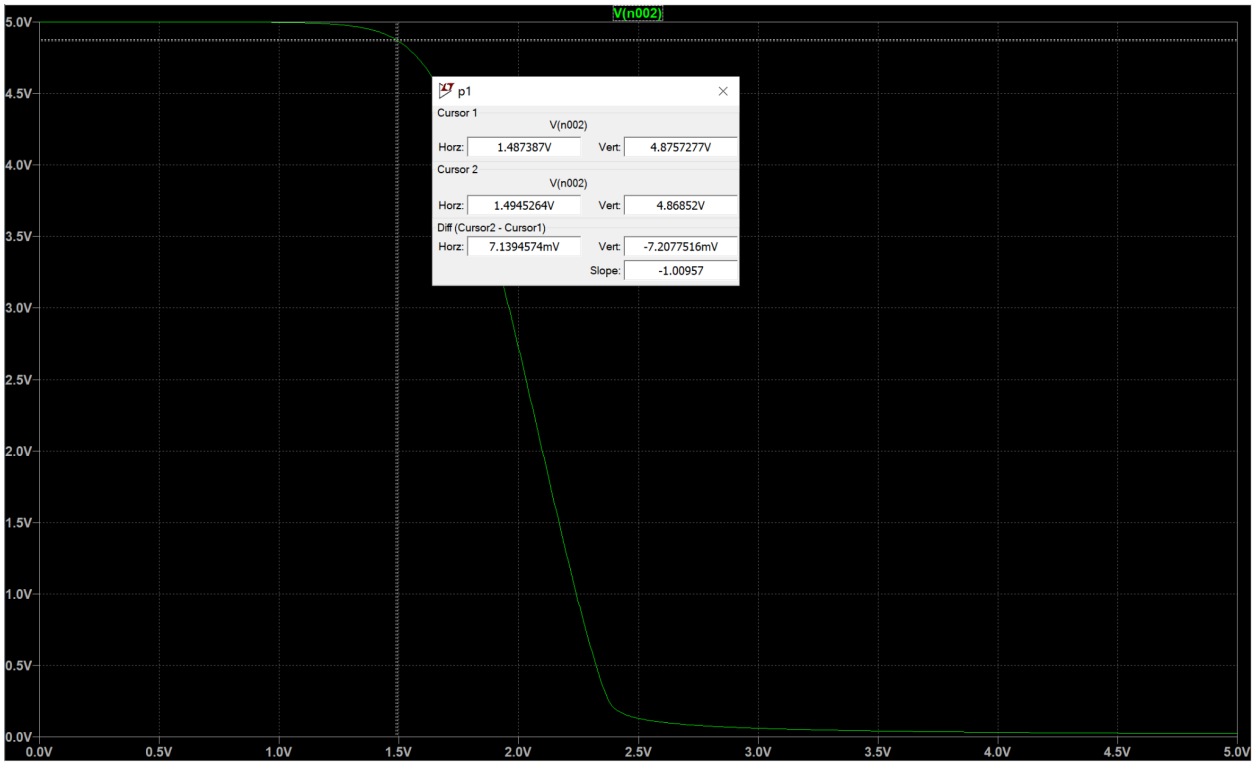

Fig. 12 Voh for Rd = 20k ohm

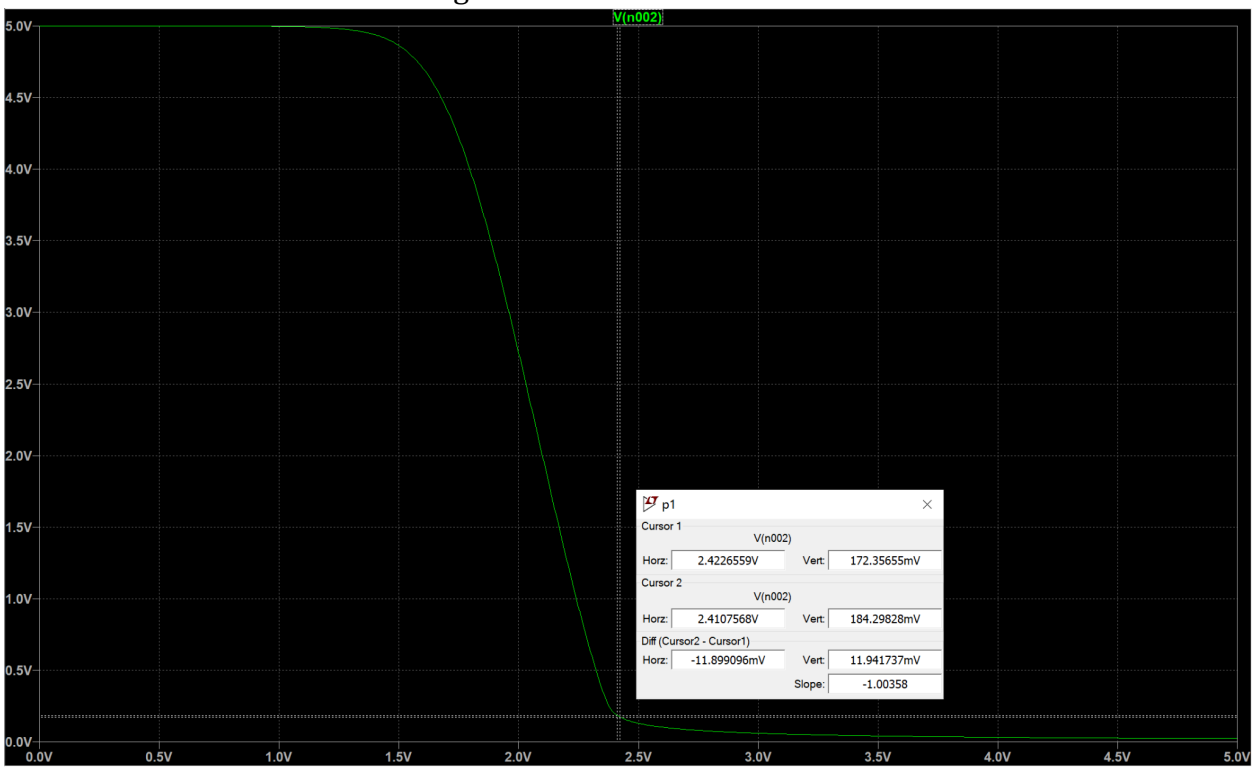

Fig. 13 Vol for Rd = 20k ohm

From Fig. 12 and Fig. 13, we can see that for Rd = 20k ohm, Voh = 4.87V, Vol = 0.18V

For different values of Rd, we can see that Voh changes slightly 4.8V (4.76V, 4.86V, 4.87V), while Vol changes more(0.96V, 0.37V, 0.18V). Both parameters depend upon the value of Rd, while Vol depends on Rd more than Voh does. When we analyze the circuit, we can see Vout = Vdd - Id*R. It also proves that these parameters depend upon the value of Rd .

c) For calculating noise margins, we use the equations NMh = Voh - Vih, NMl = Vil - Vol

From Fig. 8 and Fig. 9, we can see that for Rd = 1k ohm, Voh = 4.76V, Vol = 0.96V, Vil = 2.03V, Vih = 4.54V
From Fig. 10 and Fig. 11, we can see that for Rd = 4.7k ohm, Voh = 4.86V, Vol = 0.37V, Vil = 1.67V, Vih = 3.07V
From Fig. 12 and Fig. 13, we can see that for Rd = 20k ohm, Voh = 4.87V, Vol = 0.18V, Vil = 1.49V, Vih = 2.42V

1k ohm: NMh = 4.76V - 4.54V = 0.22V , NMl = 2.03 - 0.96 = 1.07V

4.7k ohm: NMh = 4.86V - 3.07V = 1.79V , NMl = 1.67V - 0.37V = 1.30V

20k ohm: NMh = 4.87V - 2.42V = 2.45V , NMl = 1.49V - 0.18V = 1.31V

To find the resistor that produces the best VTC for a logic family, we look for the resistor value that produces the biggest Noise Margin. Larger noise margin means better noise immunity. We can see that 20k ohm resistor produces both the biggest Noise Margin High and Noise Margin Low. So, 20k ohm is the best among these 3 three values for resistor R1.

3.2 E-mode MOSFET driver with D-mode load device (non-simulation)

a) There are two major differences between the two. First, the net difference between V_oL and V_oH is bigger for depletion mode devices than the resistor load device. Second, the change of voltage starts at a lower voltage and happens faster for the depletion mode device.

b) First, the depletion mode load design creates a bigger gap between V_oL and V_oH. Also, it has a fast change from low voltage to high voltage, which makes further optimization more convenient. In this case, the depletion mode device provides a clearer region that is closer to the ideal “1” and “0” region and has larger noise margins and better noise immunity, indicating it performs better than the resistor load device.

c) The depletion mode load has higher gain than the resistor load since two noise margin points are closer than resistor load.

d) JFET has some resistance, NMOS also has some resistance but is voltage controlled. Thus, based on the voltage dividing principles based on the resistance of NMOS, JFET and R1, the drop in V_o will happens faster and the final value of V_oL will be smaller for the greater R1, which results in a bigger and clearer gap between V_oL and V_oH, a better VTC.

3.3 CMOS inverter circuit

a) We observed that the VTC of CMOS is much more symmetrical than the resistive load inverter and depletion mode load inverter. Comparing two sides of the center point around Vin = 2.57V, the function is completely rotational symmetrical.

b) From the cursor in fig. 14 and fig. 15, we can calculate NMh = 4.84 - 2.95 = 1.89V and NMl = 2.20 - 0.21 = 1.99V. Comparing with the resistor load E-mode with 20K which NMh = 2.45V and NMl = 1.31V, CMOS has a more even noise margin and a wider total noise margin width while Vol and Voh (signal swing) are approximately the same. Thus, the CMOS inverter is a better VTC than the resistor load E-mode driver inverter.

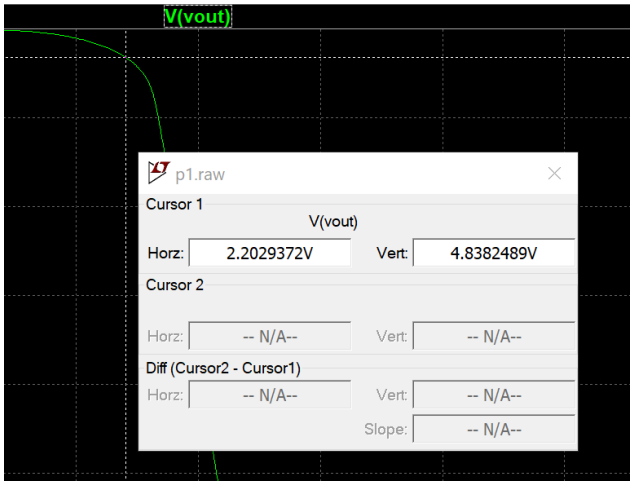

Fig. 14 Vil and Voh of CMOS

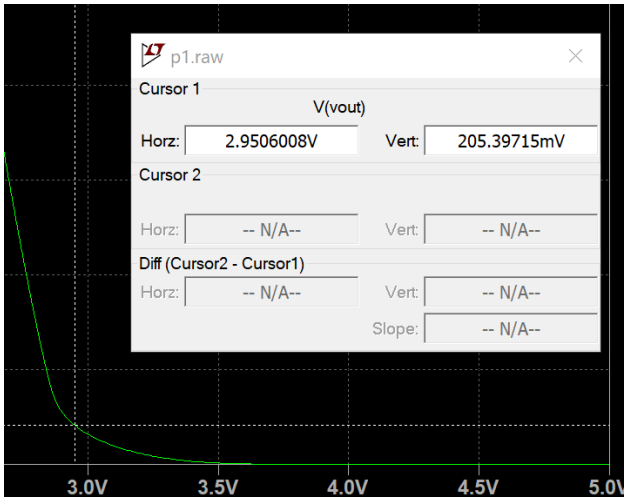

Fig. 15 Vih and Vol of CMOS

C) According to Fig. 7, the estimated threshold voltage of n-channel MOSFET is 1.57V since the Vout begins to decrease which means current begins to flow through the n-channel MOSFET. The estimated threshold voltage of the p-channel MOSFET is 3.62-5=-1.38V since the Vout drops to 0 which means the p-channel MOSFET becomes open circuit and the p-channel MOSFET is turned off when Vgs < Vtp.

4. Conclusion

In this lab, the team learned how to identify different logic levels and noise margins of the inverter circuit (ie: Vil, Vol, Vih, Voh) with different MOSFET inverter designs. It is shown that the inverter circuits can be designed in a variety of ways and each design has different characteristics. We eventually found out that CMOS inverter circuit has the best overall performance than other designs. In reality, CMOS dominates the computing chips because of its innate advantages of symmetrical VTC. In procedure 1, we build an E-mode MOSFET driver with resistor load inverter circuit and find out that the larger resistance results in better noise margin and higher gain (less delay) which is better for building logic gates. In procedure 2, we analyzed the VTC of D-mode load inverter circuits. The new circuit has a better noise margin and a higher gain than resistor load inverter circuit and larger resistance will also improve the performance. In procedure 3, we build a CMOS inverter circuit. We found that the VTC of a CMOS is very symmetrical which results in even NMh and NMl. We also observe the largest total noise margin width among three inverter designs which indicates CMOS is the best choice for logic gate designs. Overall, the most important concept we learned in this lab is to identify different logic levels and have an idea how different circuit designs affect the VTC.