STEP-MAX10
Software Manual

STEP FPGA

STEP-MAX10 Software Manual

CONCENTS

1. Introduction

The Altera® Quartus® Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA and CPLD design. Quartus Prime software delivers the highest productivity and performance for Altera FPGAs, CPLDs, and HardCopy® ASICs. Quartus Prime software delivers superior synthesis and placement and routing, resulting in compilation time advantages. Compilation time reduction features include:

· Multiprocessor support

· Rapid Recompile

· Incremental compilation

Incremental Compilation and Rapid Recompile Quartus Prime Analysis and Synthesis, together with the Quartus Prime Fitter, incrementally compiles only the parts of your design that change between compilations. By compiling only changed partitions, incremental compilation reduces compilation time by up to 70 percent. For small engineering change orders (ECOs), the Rapid Recompile feature maximizes your productivity by reducing your compilation time by 65 percent on average, and improves design timing preservation.

2.Installing Quartus Prime 16.1 Lite

2.1 Download Quartus Prime 16.1 Lite

This section provides detailed instructions for downloading and installing Intel FPGA software.

You download software from the Download Center on www.altera.com. You have several options for downloading software:

· Download a bundled set of software and device files, in .tar format

· Download individual executable files for customized download and installation

The method you choose depends on your download speed, design requirements, and method of installation. If you want the complete software package and device support for all supported families, use the .tar format. If you want to download select elements of the software, additional software, or additional device support, use the individual executable files.

Related Links

Download CenterRelated Links

· **Download Center**：https://www.altera.com/downloads/download-center.html

Select Quartus Prime 16.1 Lite and download it, The following options must be selected in order to use the STEP-MAX10.
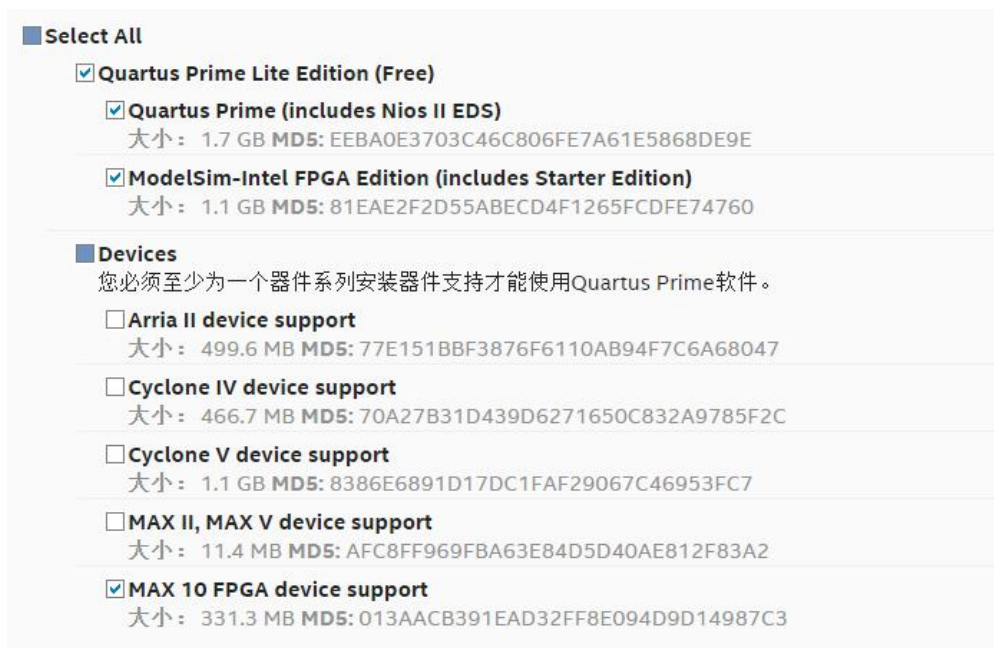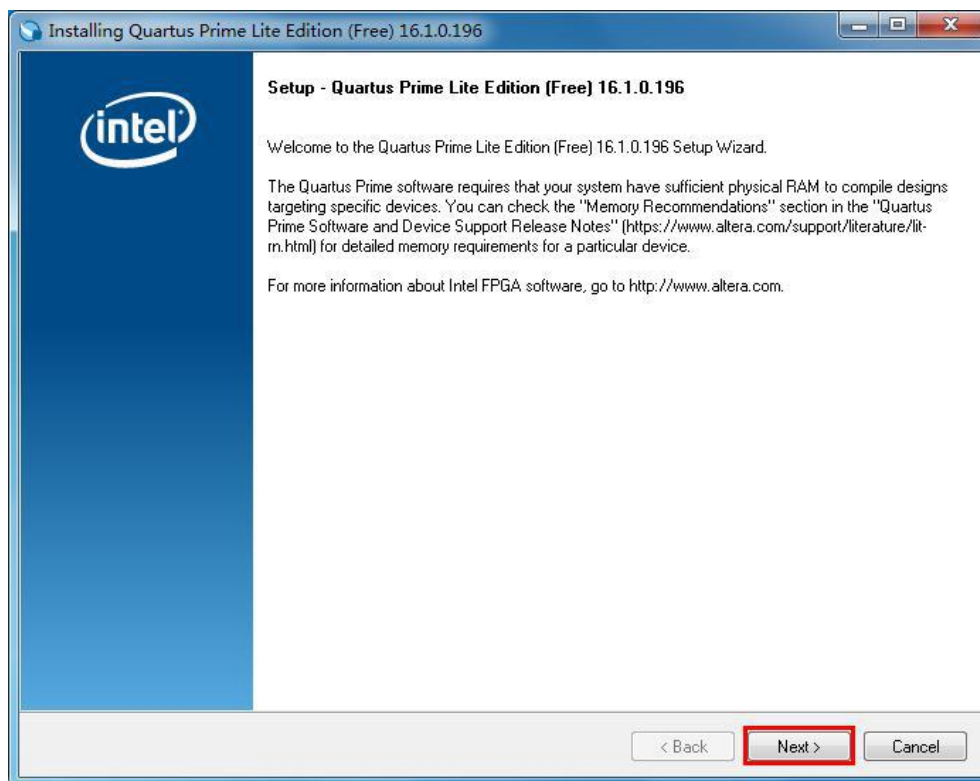
2.2 Installing Quartus Prime 16.1 Lite

Run **QuartusLiteSetup-16.1** to begin installation. The main Quartus® Prime software installer launches, automatically detects all other software and device support installation files in the same directory, and installs the software and device support.
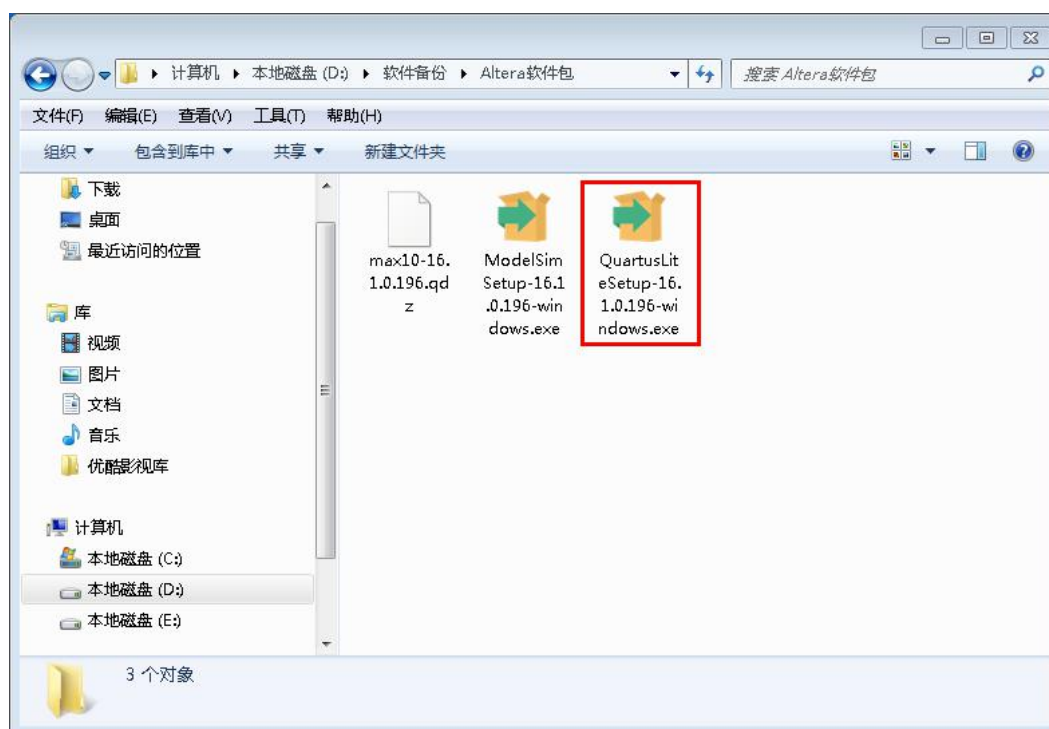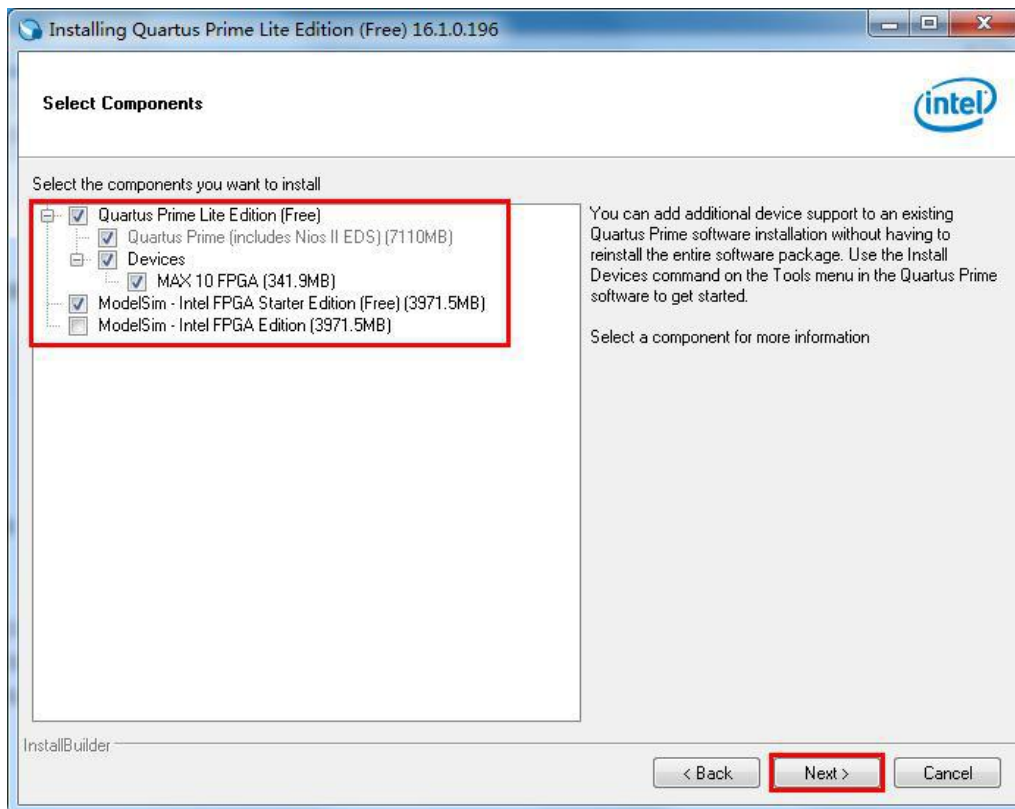
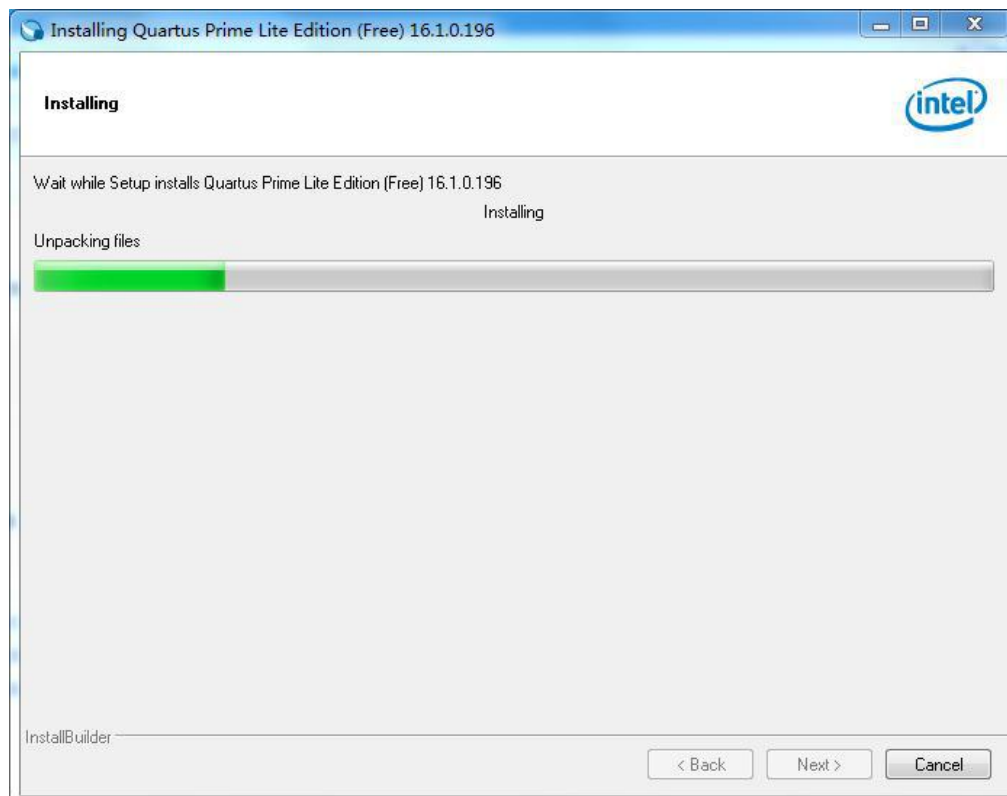The Welcome to the Quartus Prime Lite Setup Wizard opens, click 'Next'

Click Next to open the License Agreement dialog box. Read the license agreement. If you agree, click Yes, Next;
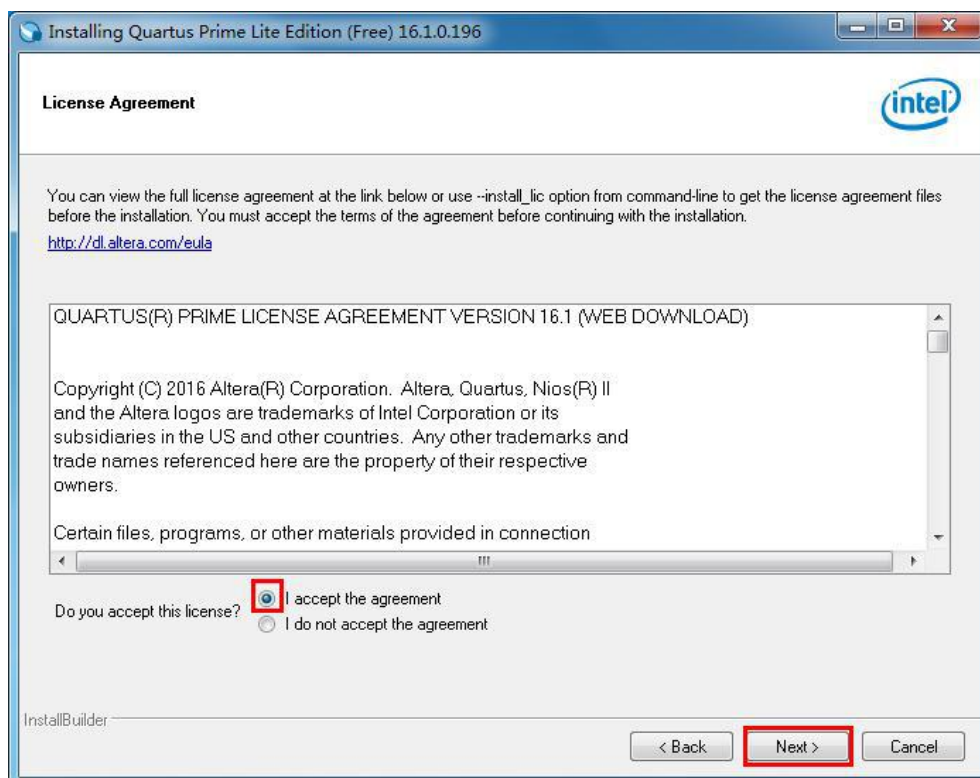
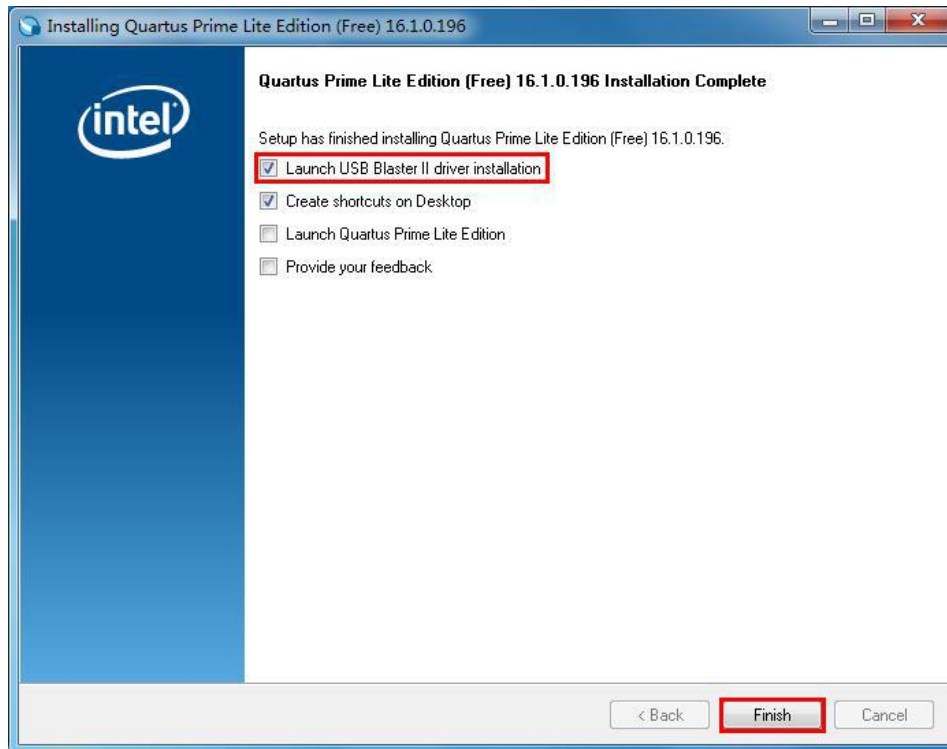Add additional device support to an existing Quartus Prime software installation, click Next.

The software will be installed.

Select 'Launch USB Blaster II driver installation' to launch USB Blaster II driver installation

and 'Create shortcuts on Desktop' , then click finish.

If the driver installation fails, you must install the appropriate programming cable drivers before you can use a download cable or programming unit to program devices with the Quartus Prime Software. The programming cable drivers are located in the following directories:

- Windows: <drive> :\<edition>\ <version number>\quartus\drivers
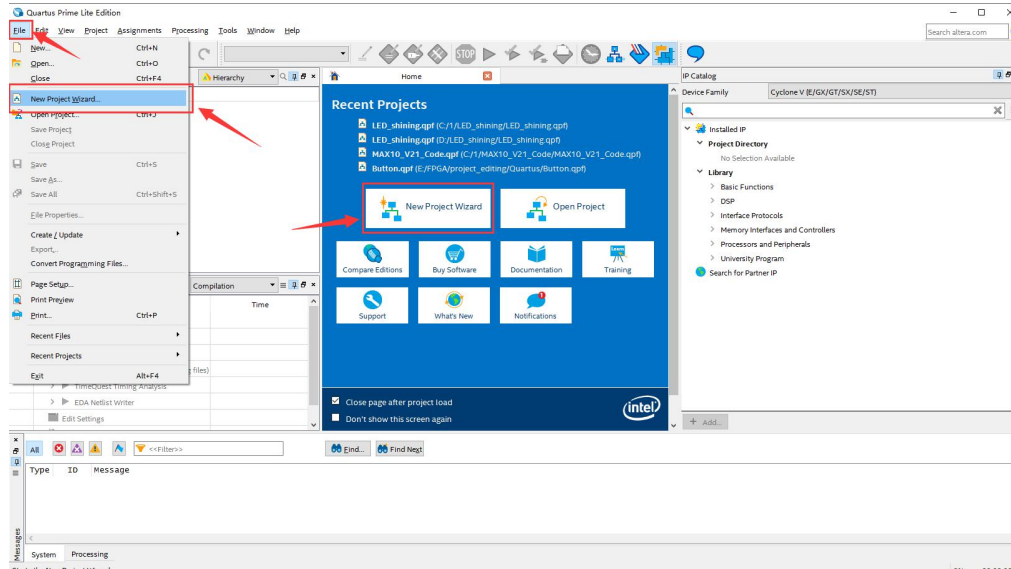
Cable and Adapter Drivers Information：

https://www.altera.com/support/support-resources/download/drivers/dri-index.html

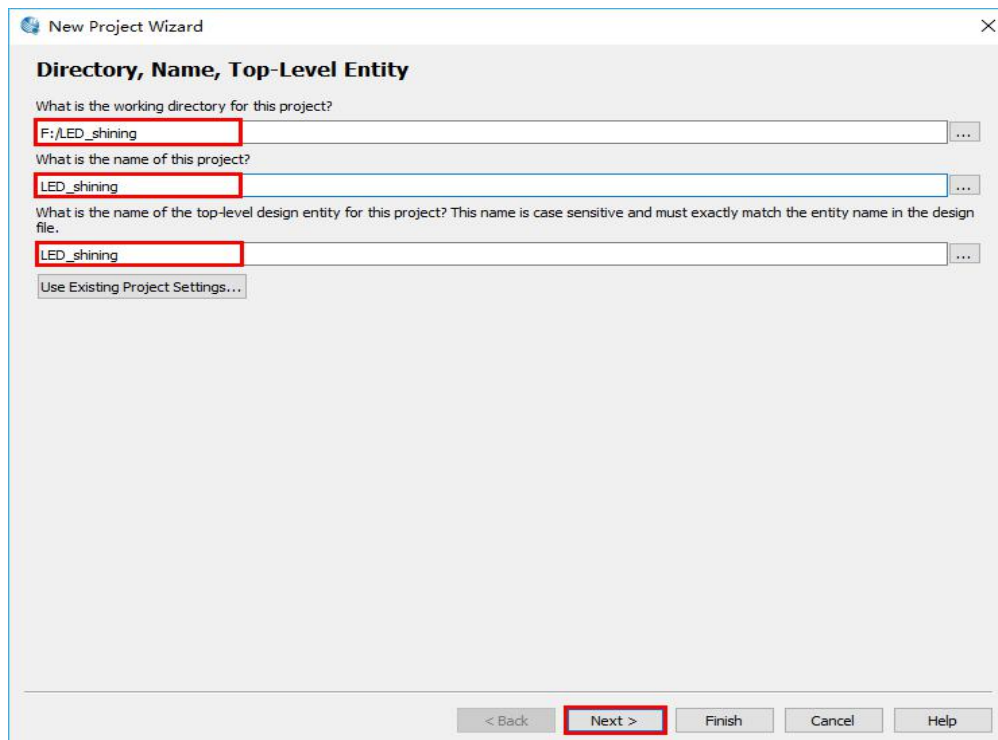Select 'Run the Quartus Prime software' , click 'OK' to launch the software.
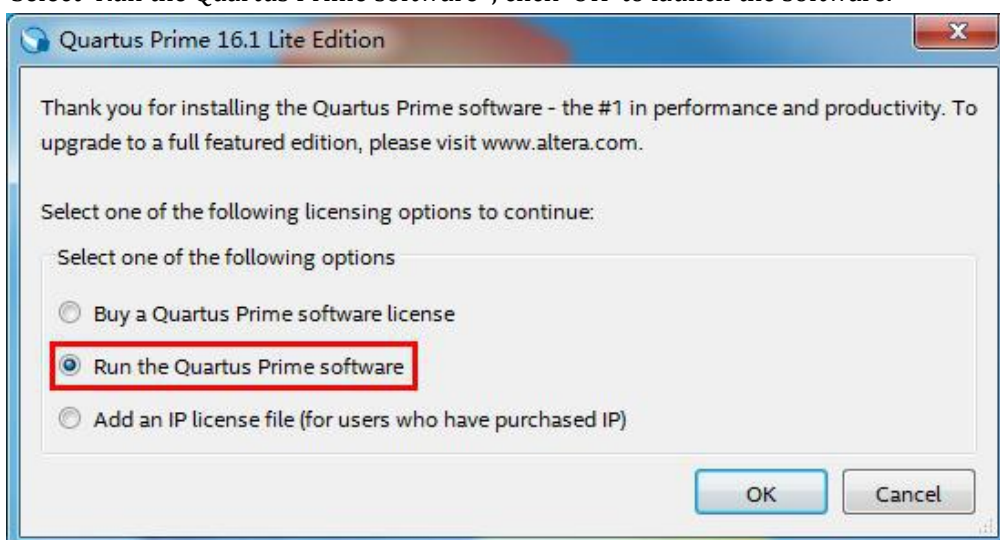
3.Quick Start

3.1 Create a new project

To quickly create a project and specify basic settings, click **File > New Project Wizard.**
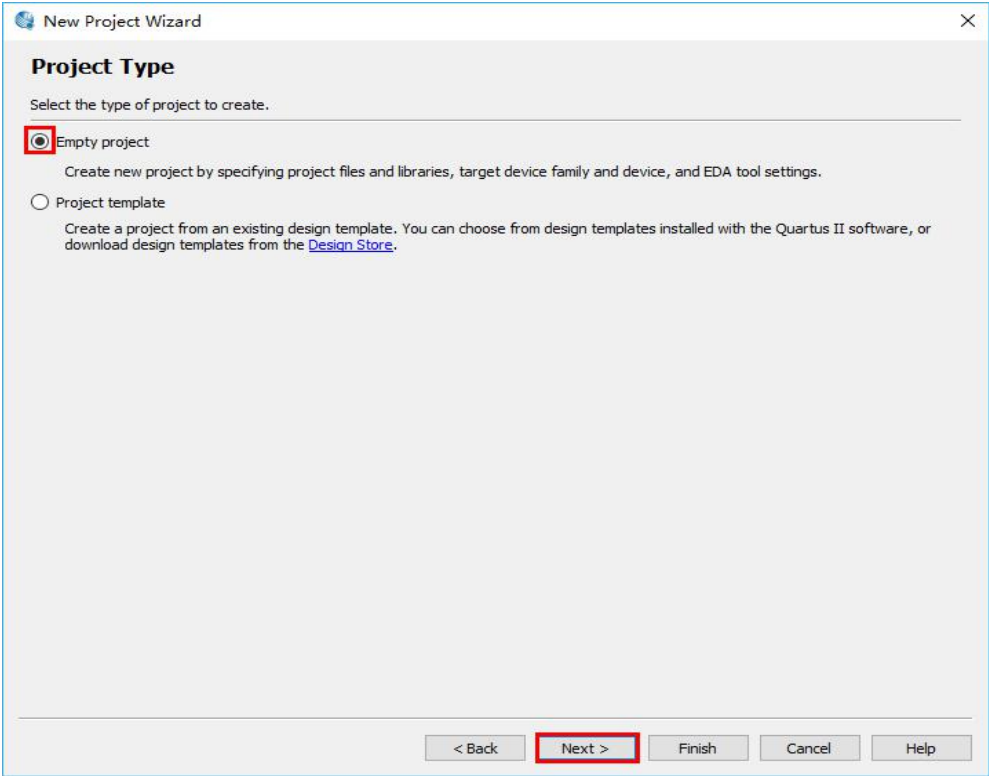

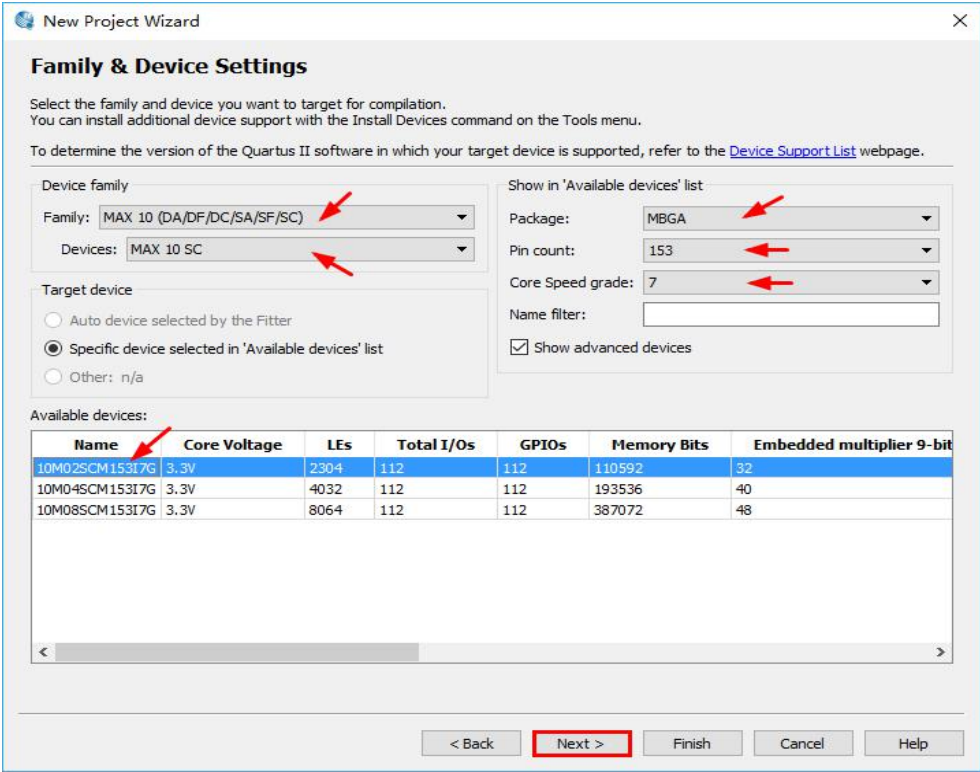Specify project directory, name, and top-level entily.

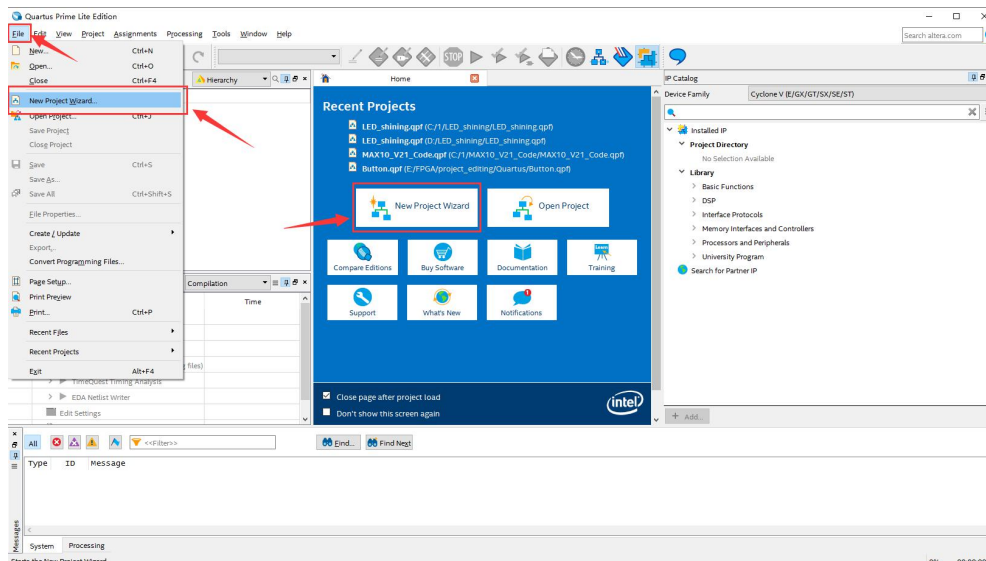Specify project design files, in this example, select empty project.

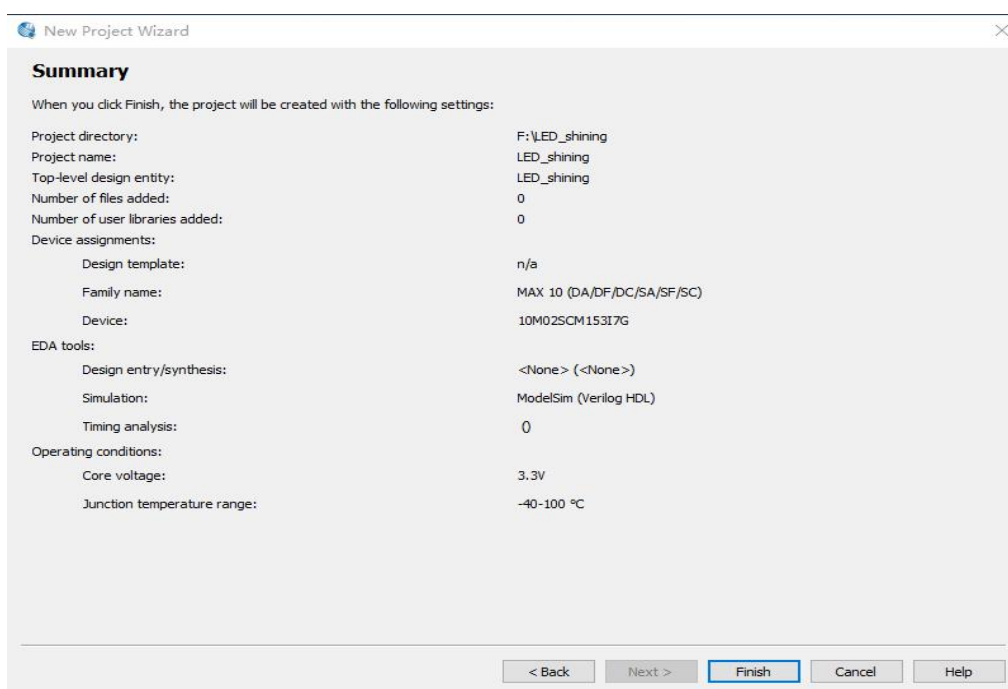Specify Altera device family for the design.

Family: MAX10(DA/DF/DC/SA/SF/SC)   Devices: MAX 10 SC

Package: MBGA   Pin Count: 153   Core Speed grade: 7
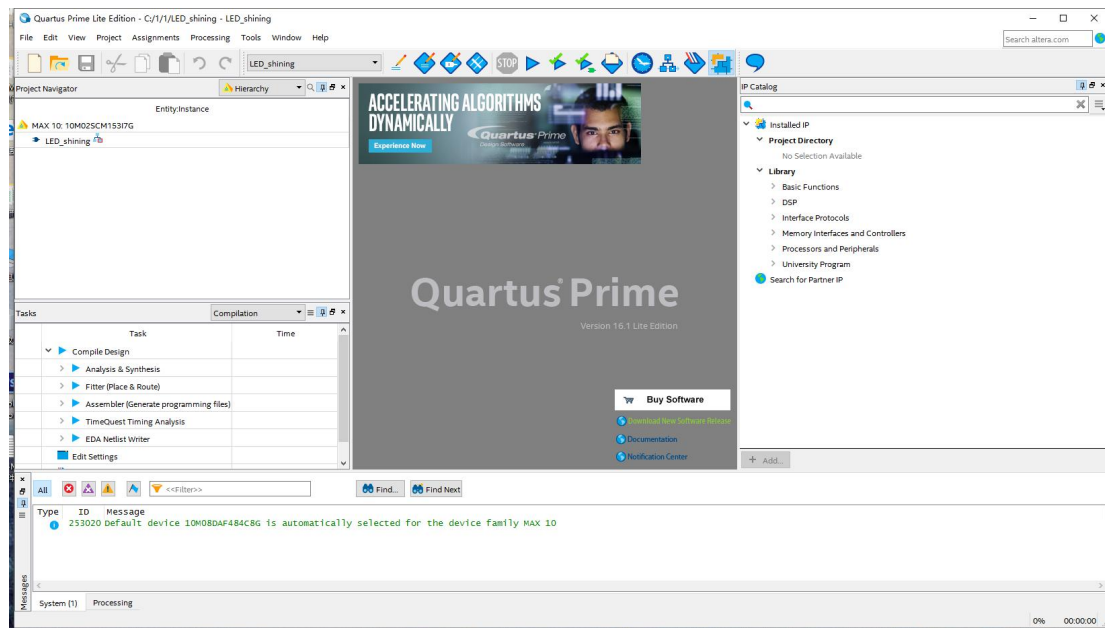
Device Name: 10M02SCM153I7G

Specify EDA tools to be used for this project.

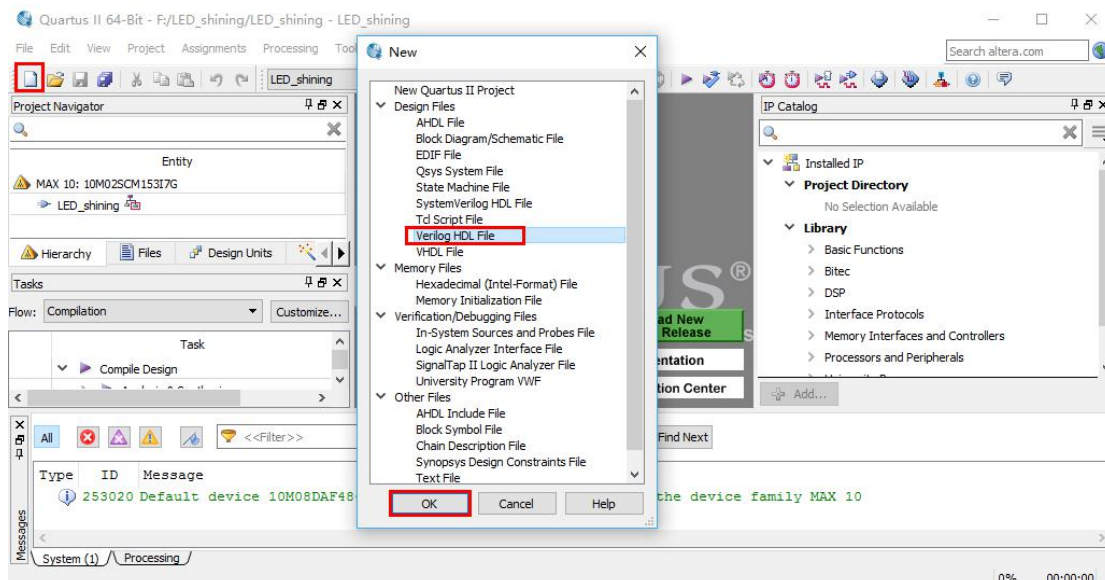Review project settings, if there is no problem, click Finish.
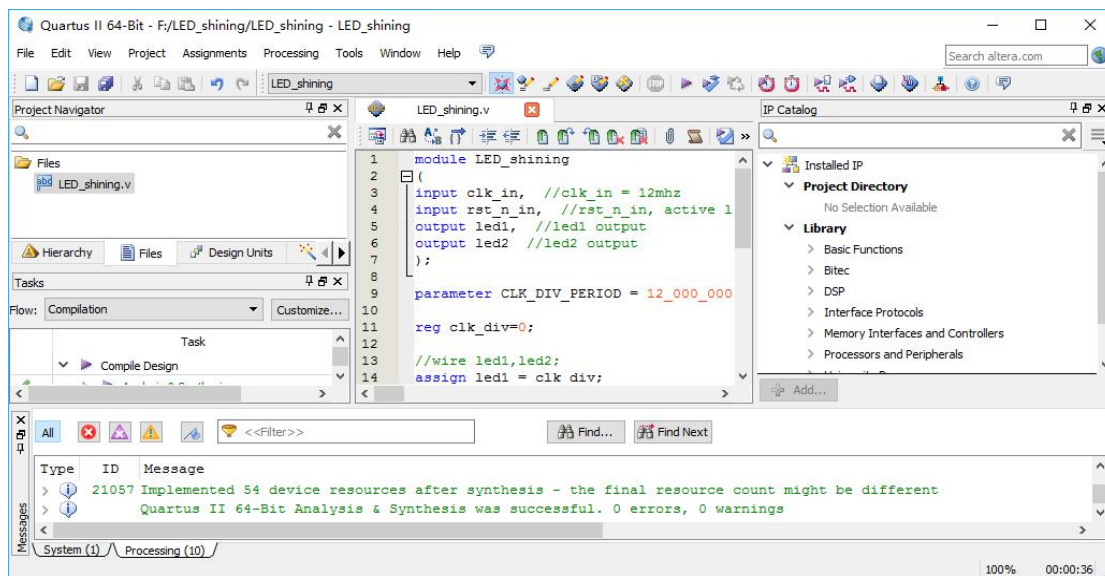
The new project has been created.

3.2 Add a Verilog HDL File

Select File→New or Click the 'New' button, select Verilog HDL File, click OK.

Write Verilog HDL in this file, press Crtl+s to save your files. The IDE will save the file to the file list. Enter the code shown below.

Verilog HDL code：

```verilog
module LED_shining
(
input clk_in,    //clk_in = 12mhz
input rst_n_in,    //rst_n_in, active low
output led1,    //led1 output
output led2    //led2 output
);

parameter CLK_DIV_PERIOD = 12_000_000;

reg clk_div=0;

//wire led1,led2;
assign led1 = clk_div;
assign led2 = ~clk_div;

//clk_div = clk_in/CLK_DIV_PERIOD
reg[24:0] cnt=0;
always@(posedge clk_in or negedge rst_n_in) begin
    if(!rst_n_in) begin
        cnt<=0;
        clk_div<=0;
    end else begin
        if(cnt==(CLK_DIV_PERIOD-1)) cnt <= 0;
        else cnt <= cnt + 1'b1;
        if(cnt<(CLK_DIV_PERIOD>>1)) clk_div <= 0;
        else clk_div <= 1'b1;
    end
end

endmodule
```
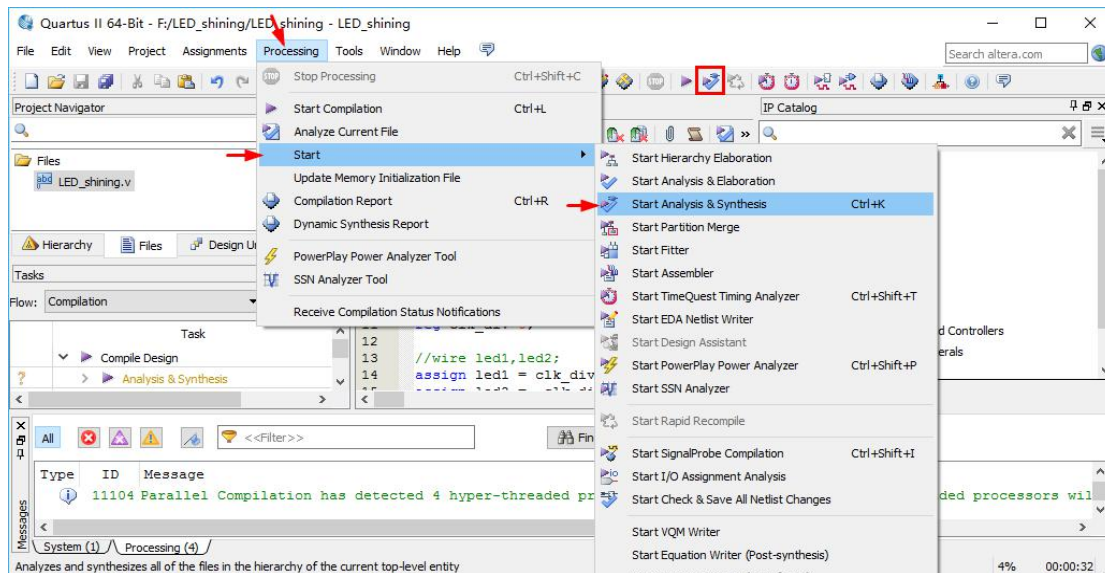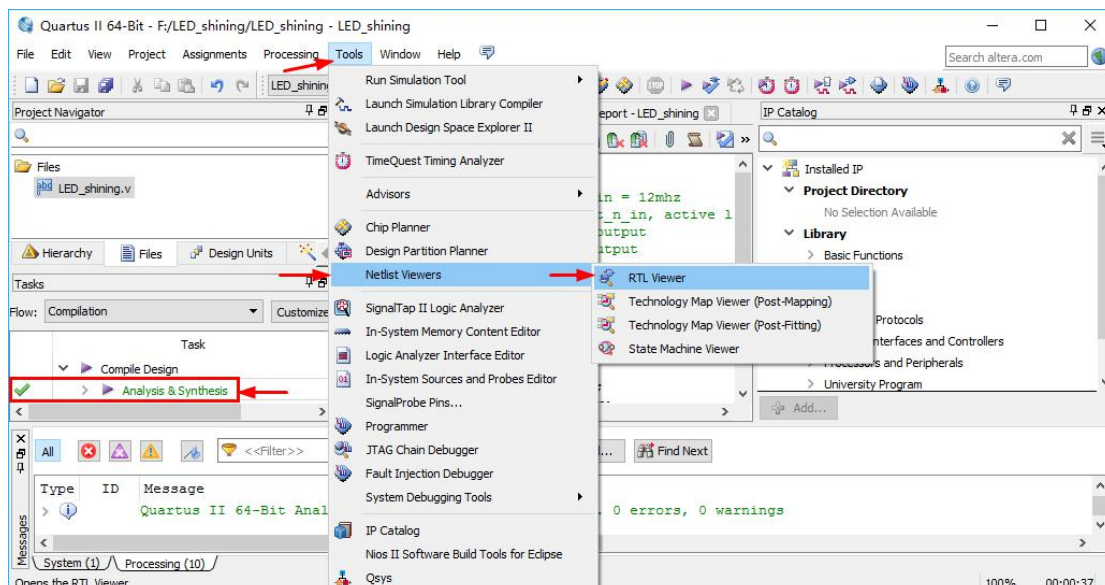
Select Processing → Start → Start Analysis & Synthesis or click Start Analysis & Synthesis button.

Quartus Prime will Analysis and Synthesis the files，if there is no error in the project，Analysis & Synthesis in the Synthesis Tasks column turns green and a green checkmark appears on the left. You can select Tools → Netlist Viewers → RTL Viewer to view the circuit.
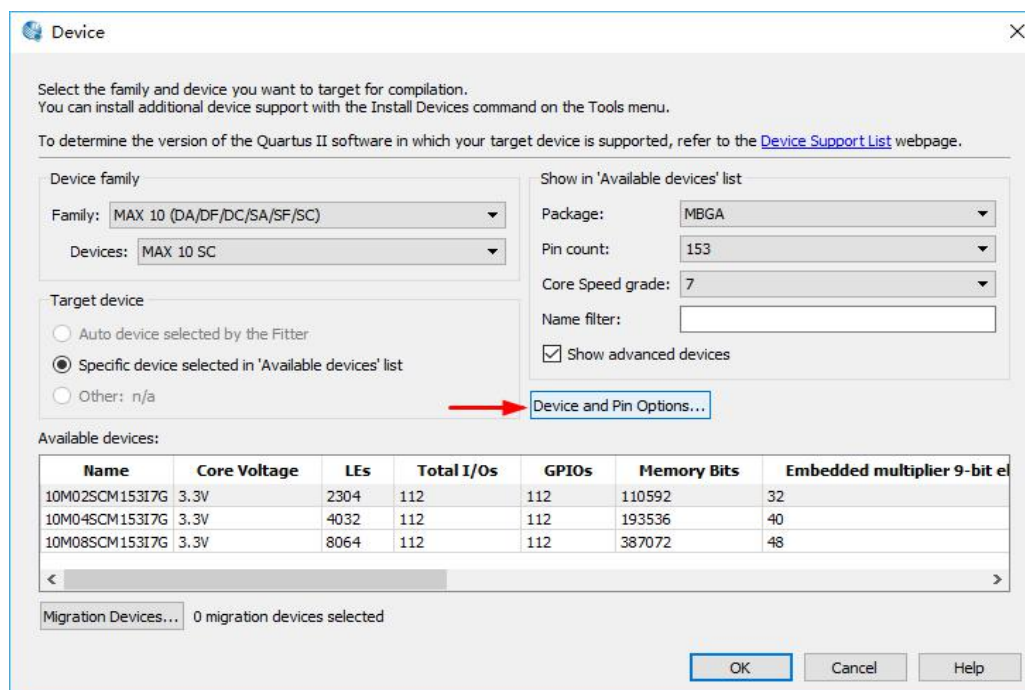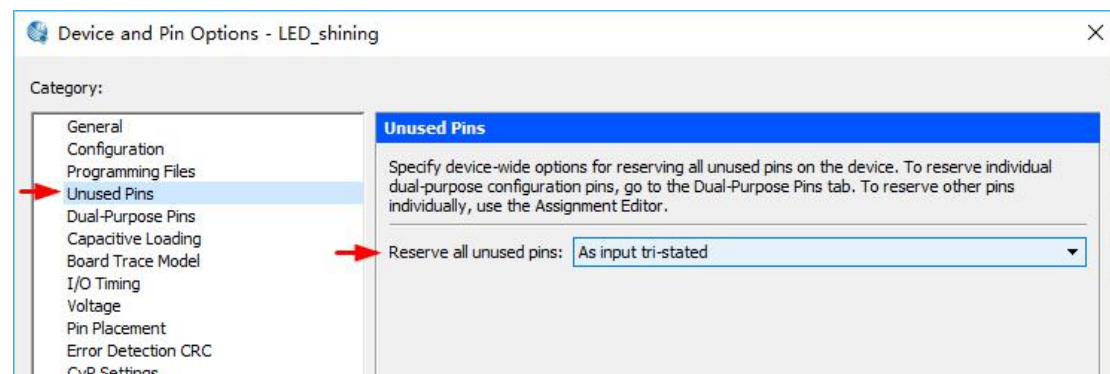

RTL circuit is as follows.
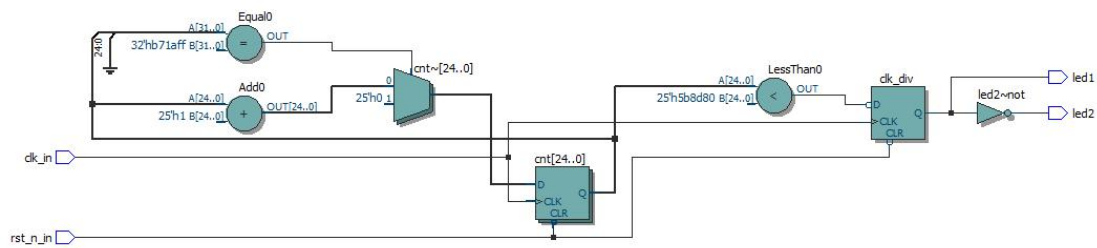
3.3 Pins Options

Select Assignments→Device to open the device configuration page, and then click the Device and Pin Options ... to open the device and pin options page.
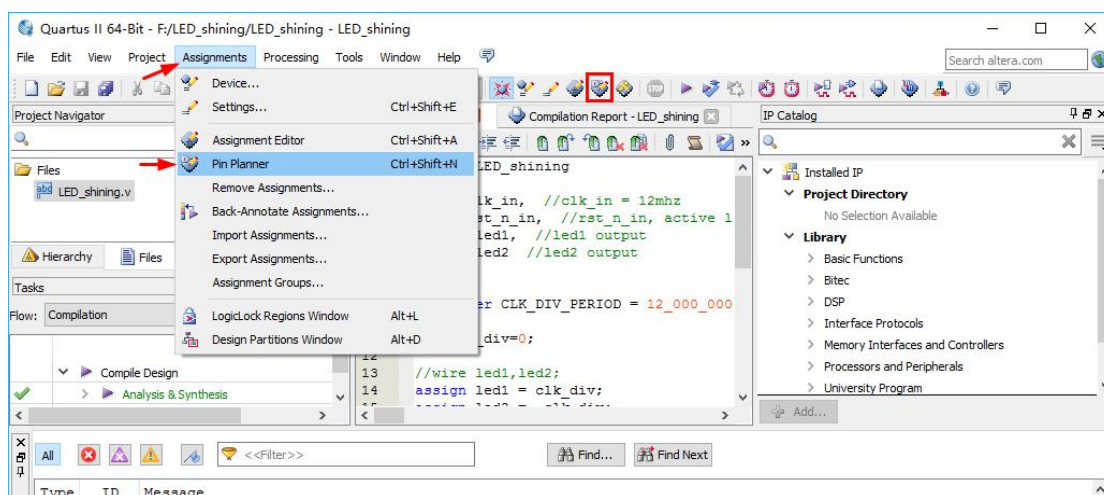

In the Unused Pins option to configure Reserve all unused pins to the As input tri-stated state.
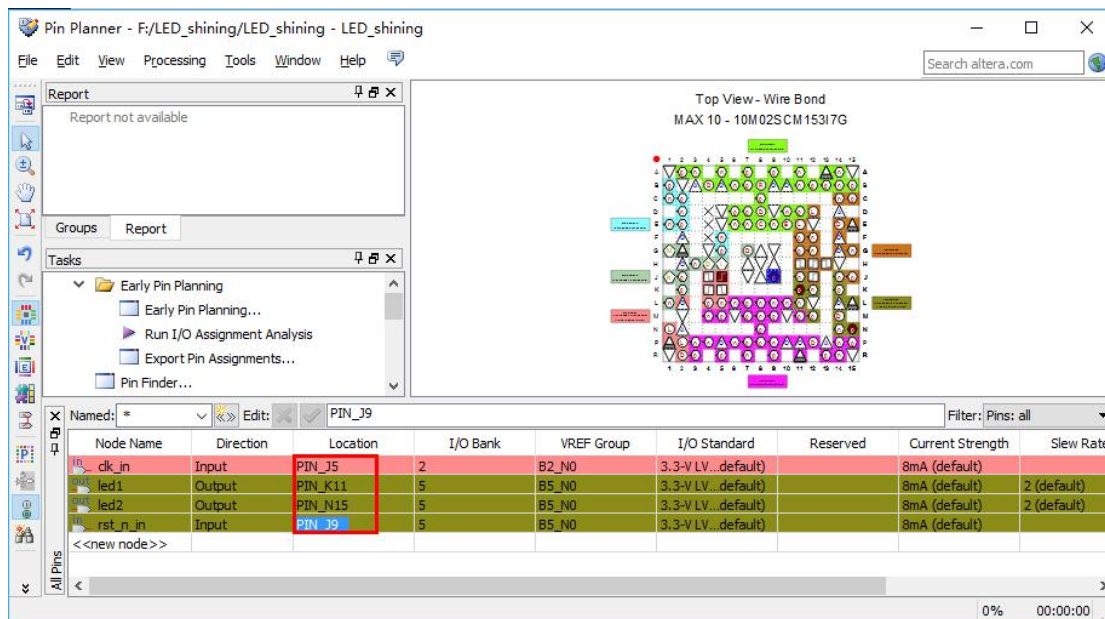
In the Voltage option to configure the Default I / O standard for the 3.3-V LVTTL state. Then click OK back to the design interface.
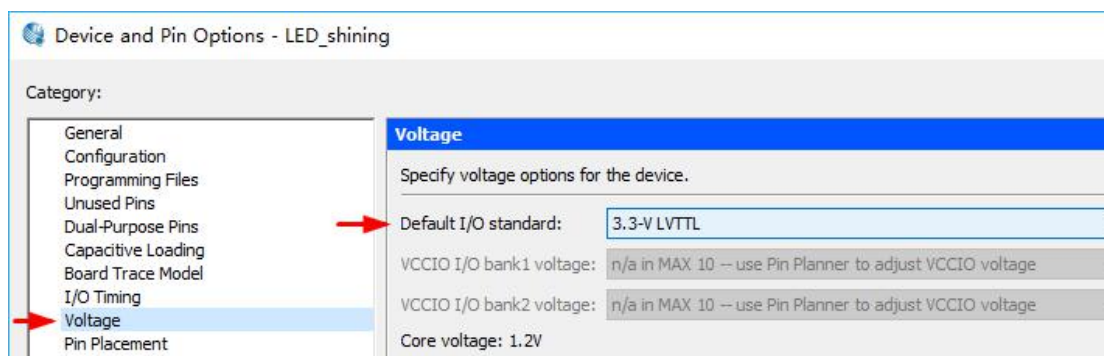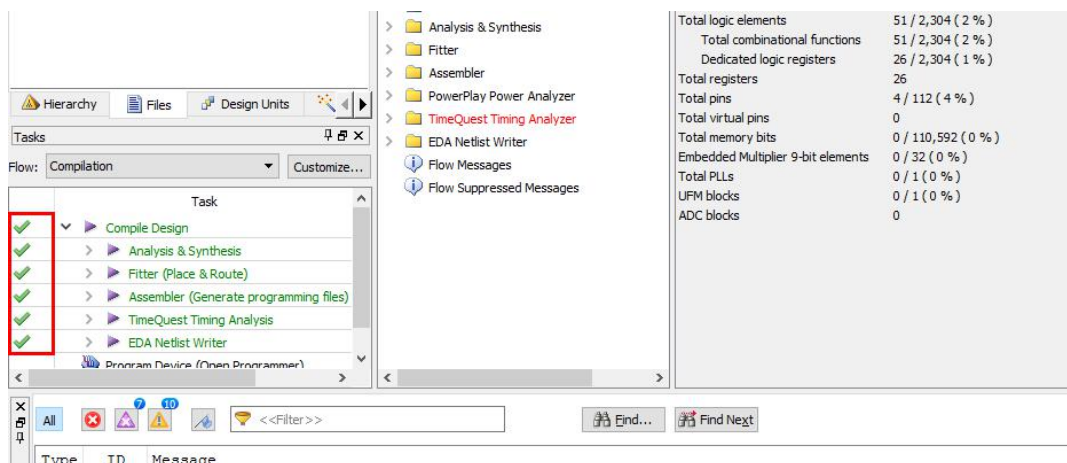

Select Assignments → Pin planner option or toolbar Pin planner button, enter the pin distribution interface.

In the Pin Planner page, all ports assigned to the corresponding FPGA pin, as shown below, then close (automatically saved).
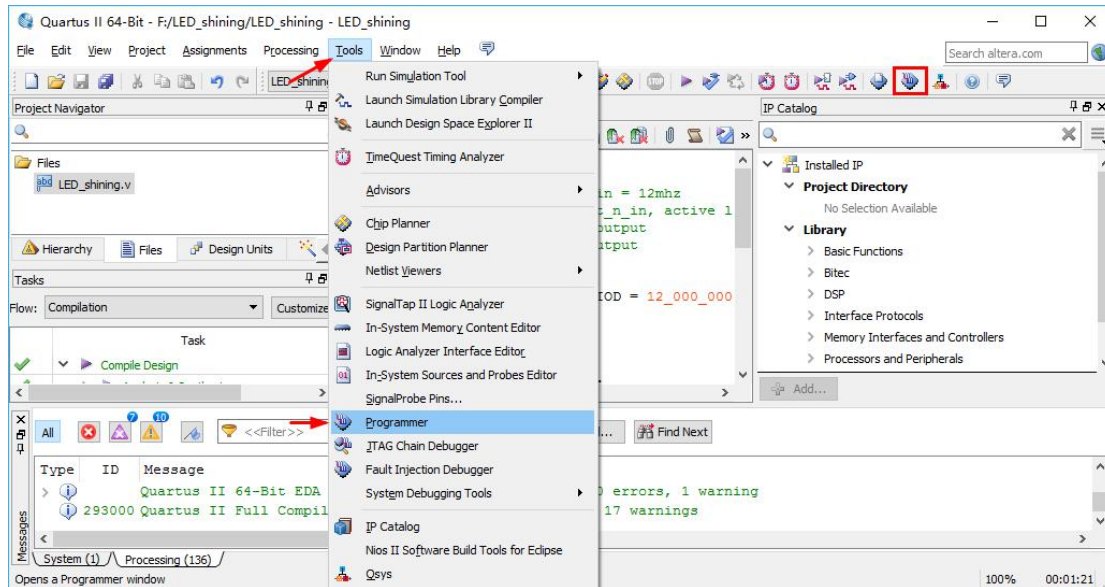
Select Processing→Start Compilation option, waiting for the Tasks list of all options to complete, as shown below.
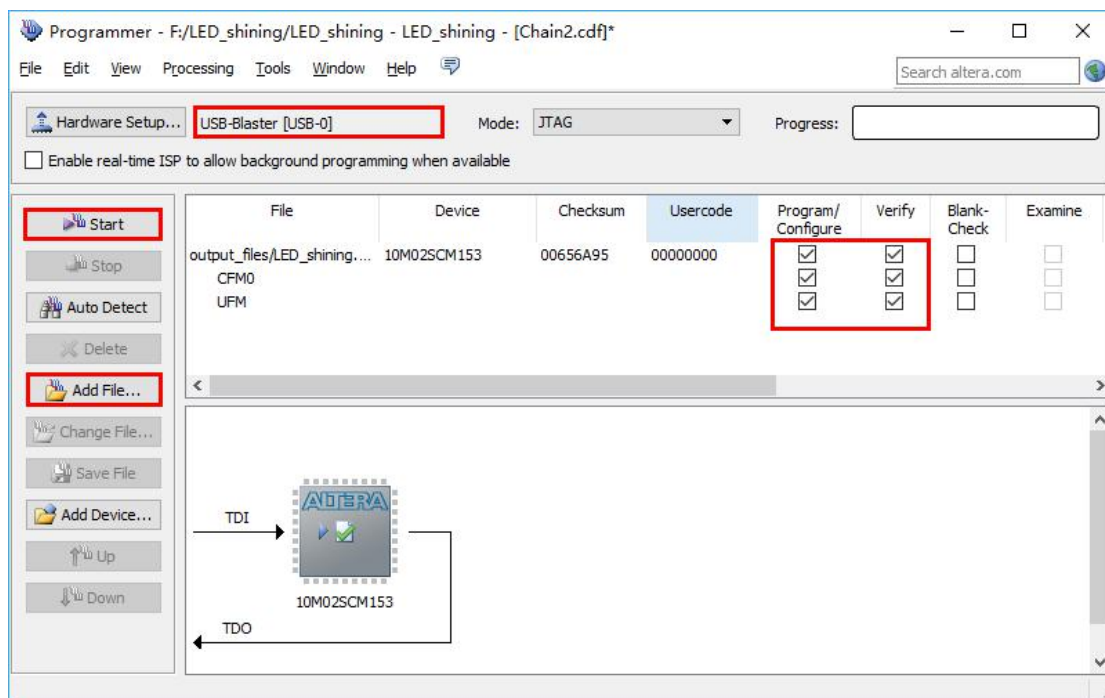

3.4 FPGA Programmer

Connect the the STEP-MAX10 to PC by micro-usb cable. Select Tools→Programmer or click Programmer button.

Programming interface as below，confirm the hardware driver is USB-Blaster[USB-0], select 'Add File' to add the project output file(.pof), select Program and Verify column, click the start button to programming for FPGA.

3、FPGA programming is complete, the progress shows 100%(successful). Observe the development board.
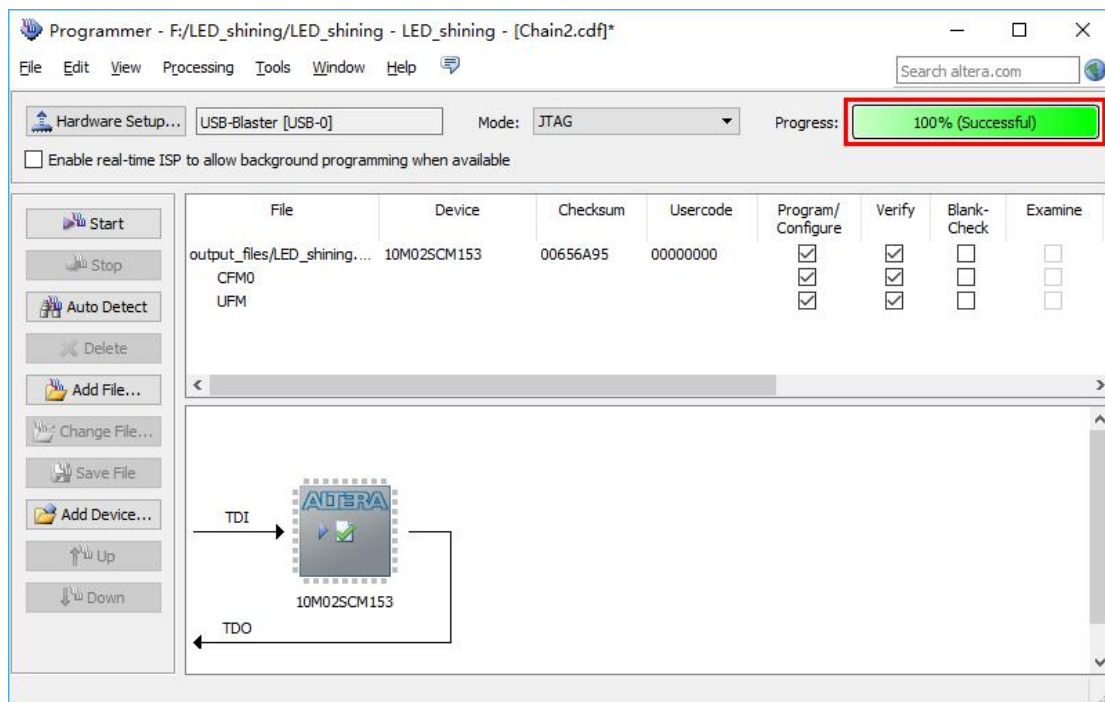
4.Modelsim-Intel quick start

The Quartus Prime software supports loose or tight integration with many industry standard EDA tools that may be used in a complete FPGA design flow. You can use the Mentor Graphics ModelSim-Intel FPGA Edition software, provided with the Quartus Prime software, to perform a functional simulation of a VHDL or Verilog HDL design that contains Intel-specific components with the ModelSim-Intel FPGA Edition interface, or with command-line commands.

1、First of all to prepare the testbench file：LED_shining_tb.v

```verilog
`timescale 1ns / 100ps
module LED_shining_tb;

parameter CLK_PERIOD = 40;

reg sys_clk;
initial
    sys_clk = 1'b0;
always
    sys_clk = #(CLK_PERIOD/2) ~sys_clk;

reg sys_rst_n;  //active low
initial
    begin
        sys_rst_n = 1'b0;
        #200;
        sys_rst_n = 1'b1;
    end
```
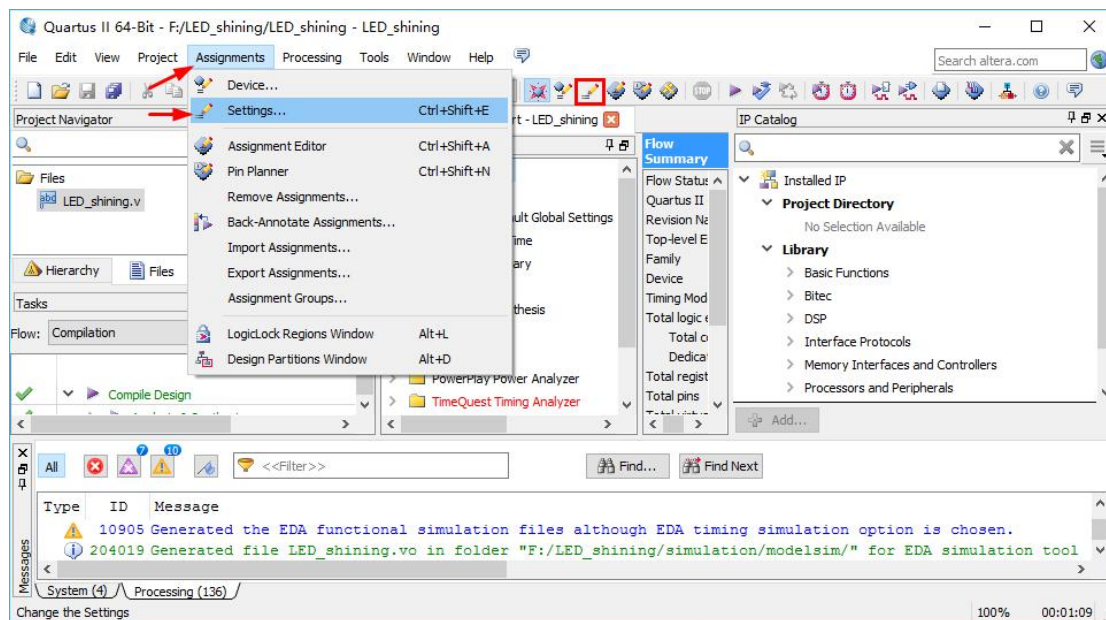
```
wire led1,led2;
LED_shining #
(
.CLK_DIV_PERIOD(4'd12)
)
LED_shining_uut
(
.clk_in(sys_clk),  //clk_in = 12mhz
.rst_n_in(sys_rst_n),  //rst_n_in, active low
.led1(led1),  //led1 output
.led2(led2)  //led2 output
);

endmodule
```
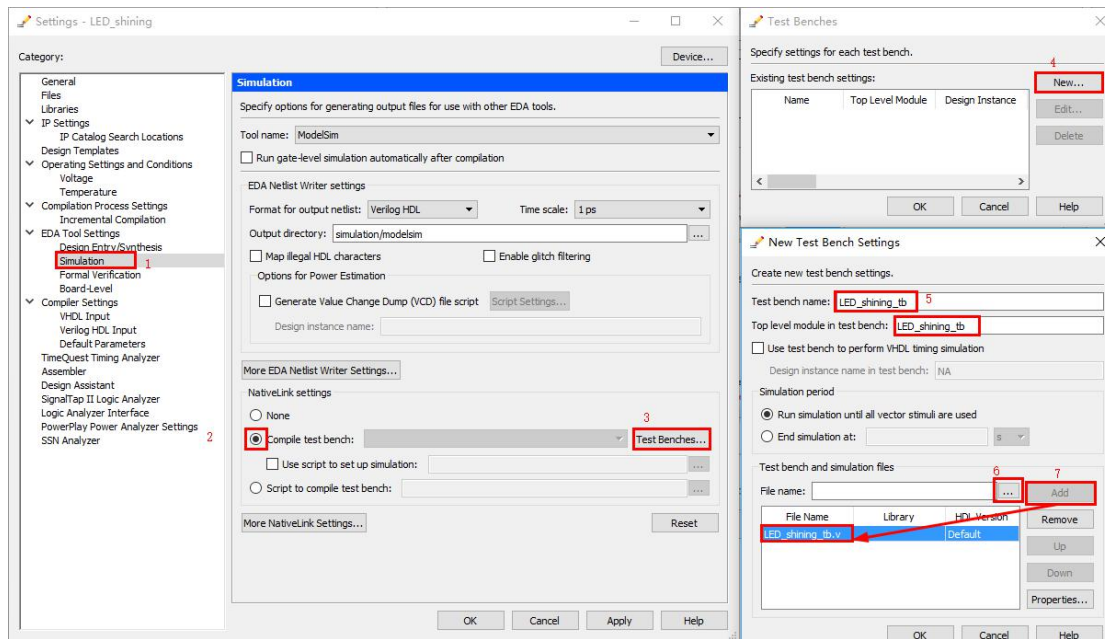
2、Choose the menu Assignments - > Settings or Settings button in the toolbar, set into the interface.


3、Choose the menu Setting, select Simulation options, then Compile test bench。Now you can click Test Benches to create a new testbench file. (Or you can add the prepared testbench file to your project directly).
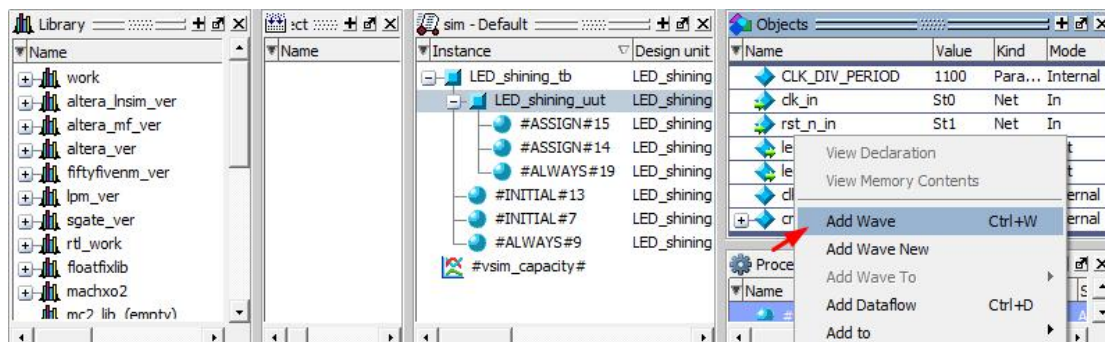
4、Choose the menu Tools -> Run Simulation Tool -> RTL Simulation or RTL Simulation button in the toolbar, start Modelsim-Intel software.
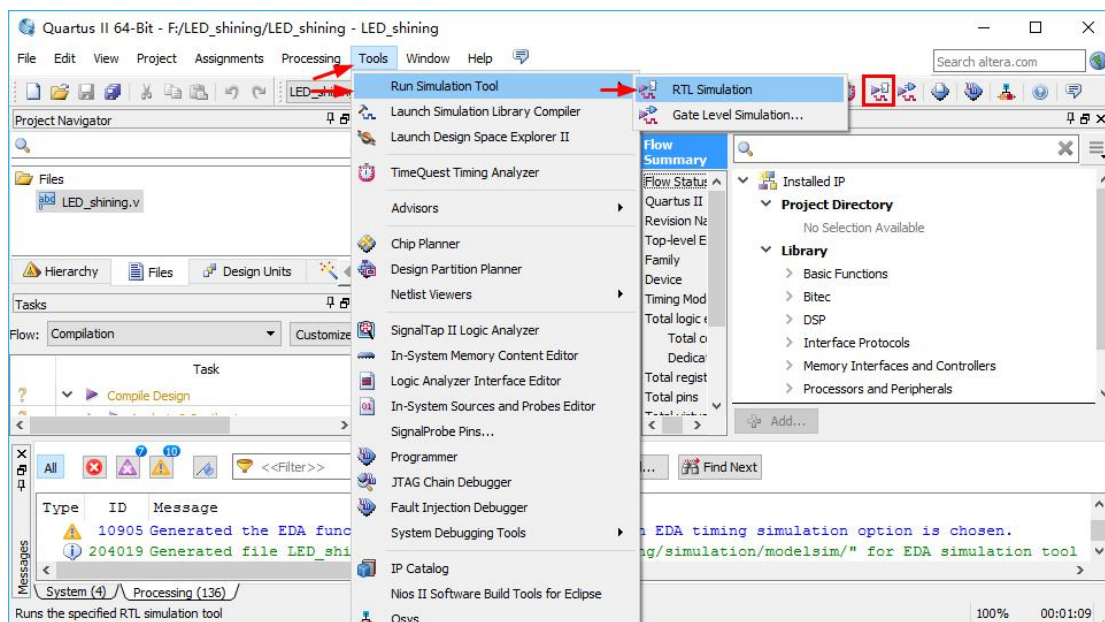
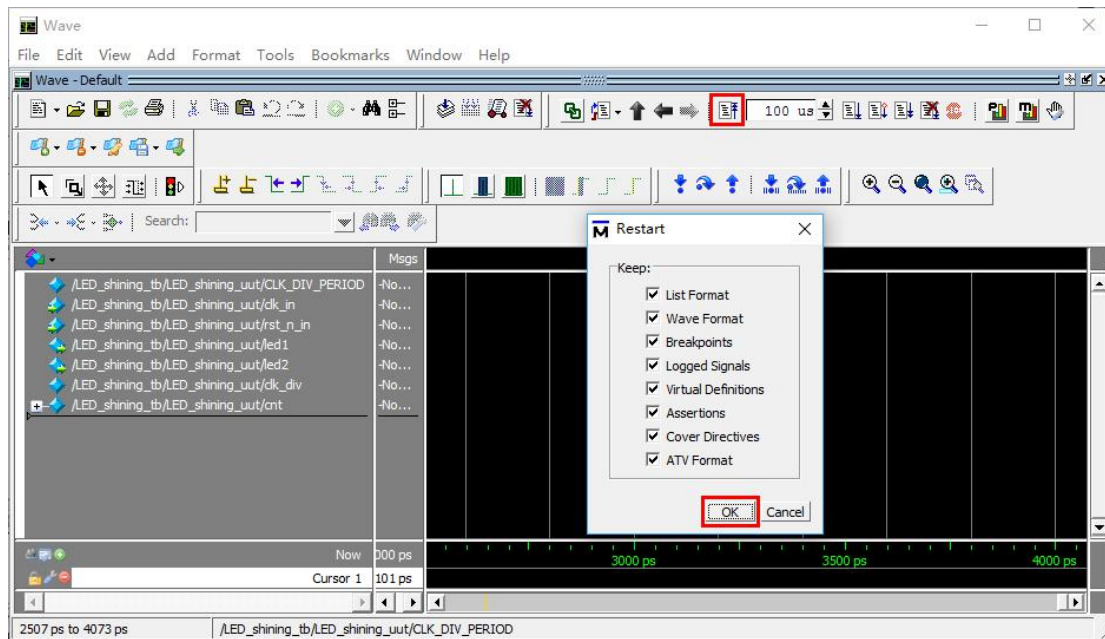5、Modelsim-Intel software start automatically after complete code compilation, as below.
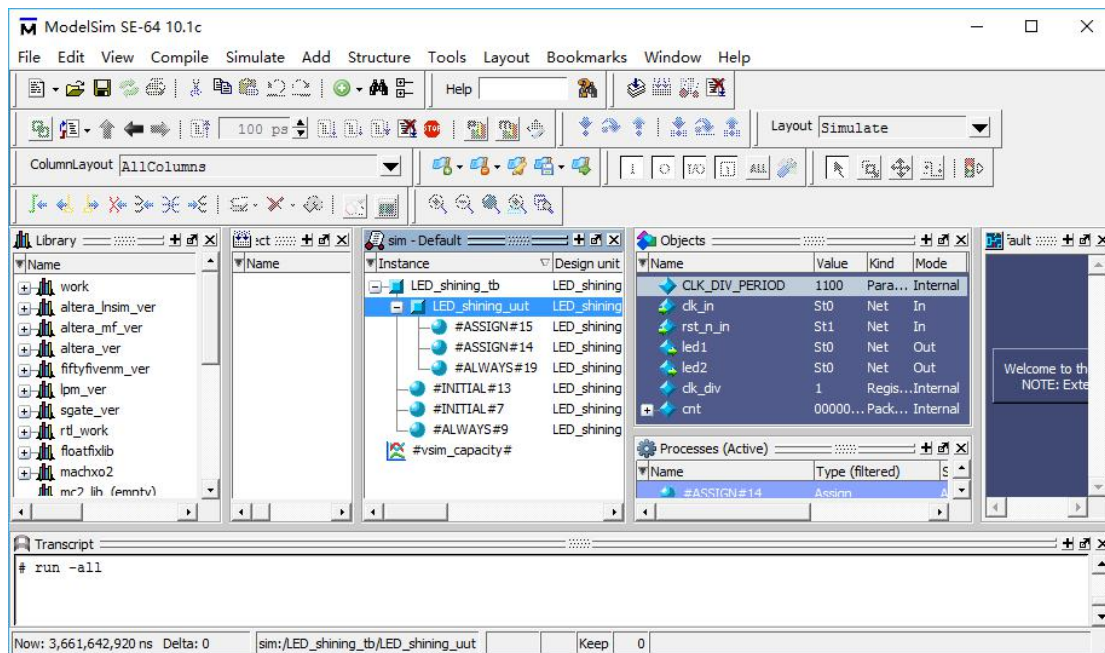
6、Right click Add Wave in the pop-up menu to add the selected signal that you want to oberve to the signal Wave window.
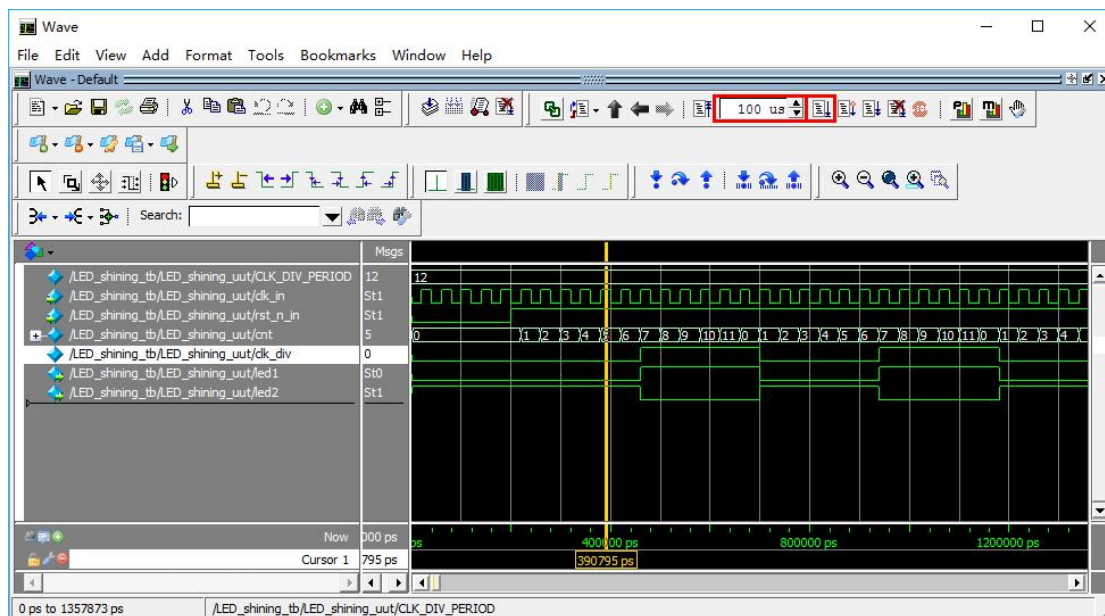

7、You can choose the menu Tools -> Restart or Restart button in the toolbar, to reset the simulation Wave window.

8、 You can modify the simulation time in the toolbar, then click the Run button. Now you can check the simulation wave or modify other parameters to generate the Wave as you want.

5.Version

Version number	Date	Comments
1.0	2017/2/14	Initial Version