

# Assignment5

Please complete the report and submit `report.pdf` through Blackboard

## 1. Q1 [50pts]

In a demand-paging memory management system, suppose the page table contents for a certain process are as follows (for a single-level page table, with H denoting hexadecimal values):

Virtual Page No.	Page Frame No.	Valid Bit
0		0
1	122H	1
2	233H	1

The page size is 4 KB, the access time for main memory is 100 ns, the access time for the TLB is 10 ns, and the average time to handle a page fault, including the time to update the TLB and page table, is  $10^8$  ns. Assuming:

1. The TLB is initially empty.
2. During address translation, the TLB is accessed first. If there is a miss in the TLB, the page table is accessed subsequently (ignoring the time taken to update the TLB after accessing the page table).
3. A valid bit set to 0 indicates that the page is not present in memory, causing a page fault interrupt. After the page fault interrupt handling is completed, the execution returns to the instruction that triggered the page fault to execute.

Given a virtual address access sequence of `1333H` , `0555H` , `2555H`:

(1) Assuming there are enough free pages available in OS. What is the time required to access each of the three virtual addresses mentioned above? Give the calculation process. The answer should include the time cost of the final access to the physical address.

(2) Suppose the operating system permits processes to use only two physical pages with frame numbers 122H and 233H, employing the Least Recently Used (LRU) replacement algorithm. Given the certain access sequence above, what is the physical address for the virtual address 0555H? Please explain the reasoning behind your answer.

## 2. Q2 [50pts]

Here is a computer with a **riscv64** architecture, employing the **Sv39** multi-level paging mechanism. The formats for physical and virtual addresses are as follows.

### Virtual Address (39bits)

38	12	11	0
Virtual Page Number			Page Offset

### Physical Address (56bits)

55	12	11	0
Physical Page Number			Page Offset

Assuming there are only three free physical pages in memory, with physical page numbers being 0x000\_0008\_6000 , 0x000\_0008\_6001 , and 0x000\_0008\_6002 . When a process requests a physical page, the operating system adopts an allocation strategy of assigning physical page numbers **from largest to smallest**. At a certain point, the value in the `satp` register is 0x8000\_0000\_0008\_4000 , with all PTEs in the root page table being zero. The current process attempts to access the valid virtual address 0x0000\_0021\_2345\_6789 .

Please simulate the computer's handling of the page fault interrupt, allocate the corresponding physical page, correctly fill in the corresponding page table entry, and find the corresponding physical address. Complete the following blanks (in hexadecimal, ignoring the actual setting of flag bits in each level of page table entries, all flags set to 0 is OK).

1. The physical address of the root page table is \_\_\_\_\_, and the value of the \_\_\_\_th page table entry is \_\_\_\_\_.
2. The physical address of second-level page table is \_\_\_\_\_, and the value of the \_\_\_\_th page table entry is \_\_\_\_\_.
3. The physical address of third-level page table is \_\_\_\_\_, and the value of the \_\_\_\_th page table entry is \_\_\_\_\_.
4. The physical address corresponding to the virtual address 0x0000\_0021\_2345\_6789 is \_\_\_\_\_.