Ramp and Pedestal triggering circuit:

The UJT is often used as a trigger device for SCRs and TRIACs. Ramp and pedestal triggering is an improved version of synchronized UJT-oscillator triggering. Fig. show the circuit of ramp and pedestal triggering of two SCRs connected in anti parallel for controlling power in ac load.

This trigger circuit can also be used for the Thyristors in a single-phase semi converter or a single-phase full converter. Zener diode voltage V_z is constant at its threshold voltage. R acts as a potential divider. Wiper of R_2 controls the value of pedestal voltage Vpd. Diode D allows C to be quickly charged to Vpd through the low resistance of the upper portion of R_2.

The setting of wiper on R is such that this value of Vpd is always less than the UJT firing point voltage ηVz. When wiper setting is such that Vpd is small, voltage Vz charges C through R. when this ramp voltage V_C reaches ηVz, UJT fires and voltage Vg, through the pulse transfer, is transmitted to the gate circuits of both SCRs T_1 and T_2. The forward biased SCR T_1 is turned on. After this, Vc reduces to Vpd and then to zero at wt = π. As V_C more than Vpd, during the charging of Capacitor C through charging resistor R, diode D is reverse biased and turned off.

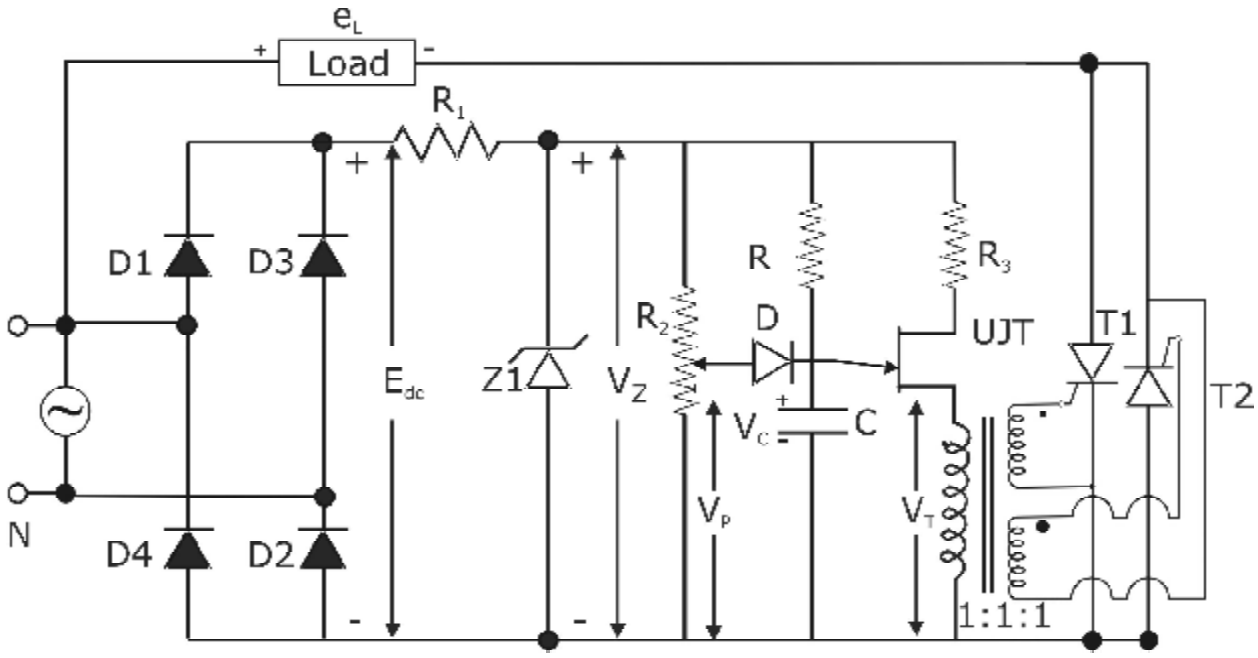
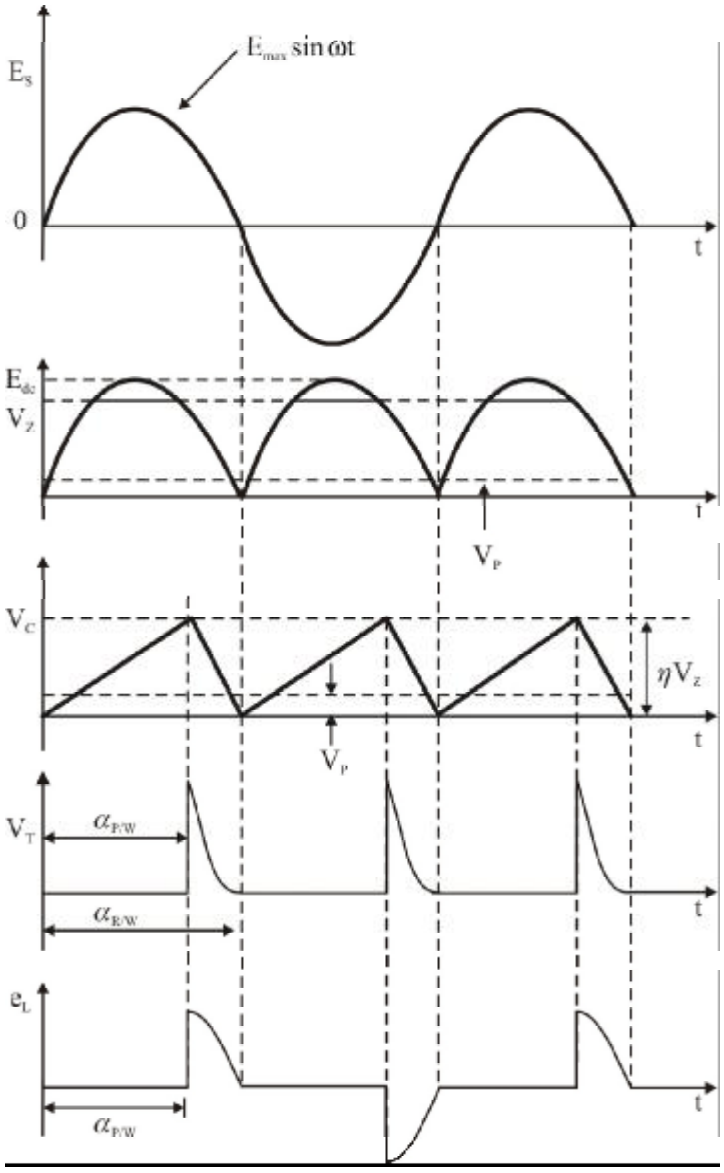


Fig. 1

Thus Vpd does not affect in any way the discharge of C through UJT emitter and primary of pulse transformer. From o to π, T_1 is forward biased and is turned on. From π to 2π, T_2 is forward biased and is turned on. In this manner, load is subjected to alternating voltage Vo.

With the setting of wiper on R_2, pedestal voltage Vpd on C can be adjusted. With low pedestal voltage across C, ramp charging of C to ηVz takes longer time .and firing angle delay is therefore more and output voltage is low. With high pedestal on C, voltage ramp charging of C through R reaches ηVz faster, firing angle delay is smaller, and output voltage is high. This shows that output voltage is proportional to the pedestal voltage.



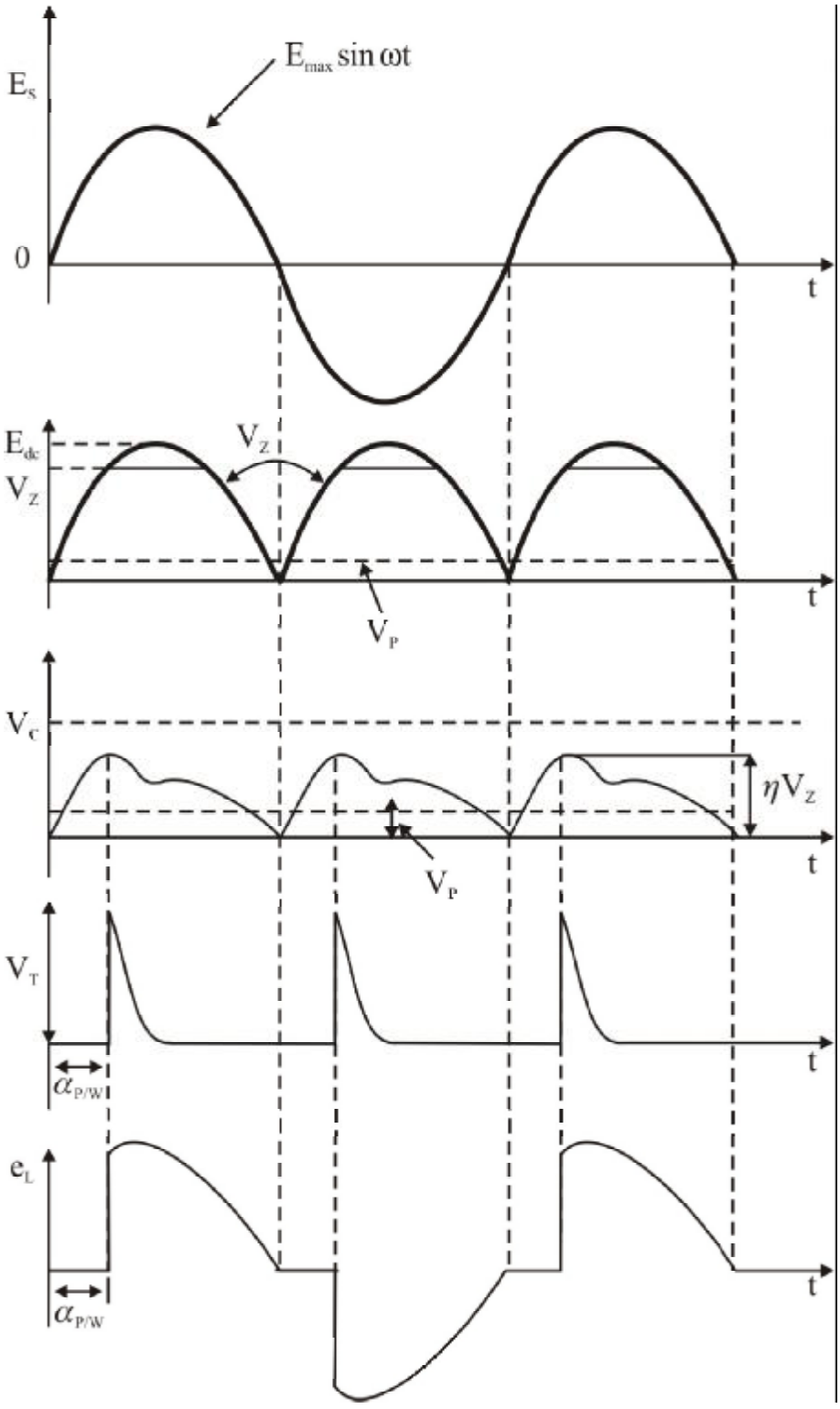


Fig. 2

The time T required for the capacitor to charge from pedestal voltage Vpd to ηVz can be obtained from the relation