Lattice Mapping Report File for Design Module 'dds_w_freq_select'

Design Information

```
Command line:   map -a MachXO3L -p LCMXO3L-6900C -t CABGA256 -s 5 -oc Commercial
     dds_improved_dds_improved.ngd -o dds_improved_dds_improved_map.ncd -pr
     dds_improved_dds_improved.prf -mp dds_improved_dds_improved.mrp
     C:/Users/userESD/Desktop/lab_11/lab_10/lattice/dds_improved.lpf -c 0 -gui
Target Vendor:  LATTICE
Target Device:  LCMXO3L-6900CCABGA256
Target Performance:   5
Mapper:  xo3c00a,  version:  Diamond (64-bit) 3.12.1.454
Mapped on:  05/03/23  15:59:50
```

Design Summary

```
   Number of registers:     49 out of  7485 (1%)
      PFU registers:           35 out of  6864 (1%)
      PIO registers:           14 out of   621 (2%)
   Number of SLICEs:       123 out of  3432 (4%)
      SLICEs as Logic/ROM:    123 out of  3432 (4%)
      SLICEs as RAM:            0 out of  2574 (0%)
      SLICEs as Carry:         41 out of  3432 (1%)
   Number of LUT4s:        239 out of  6864 (3%)
      Number used as logic LUTs:        157
      Number used as distributed RAM:     0
      Number used as ripple logic:       82
      Number used as shift registers:     0
   Number of PIO sites used: 27 + 4(JTAG) out of 207 (15%)
   Number of block RAMs:  0 out of 26 (0%)
   Number of GSRs:        1 out of 1 (100%)
   EFB used :        No
   JTAG used :       No
   Readback used :   No
   Oscillator used : No
   Startup used :    No
   POR :             On
   Bandgap :         On
   Number of Power Controller:  0 out of 1 (0%)
   Number of Dynamic Bank Controller (BCINRD):  0 out of 6 (0%)
   Number of Dynamic Bank Controller (BCLVDSO):  0 out of 1 (0%)
   Number of DCCA:  0 out of 8 (0%)
   Number of DCMA:  0 out of 2 (0%)
   Number of PLLs:  0 out of 2 (0%)
   Number of DQSDLLs:  0 out of 2 (0%)
   Number of CLKDIVC:  0 out of 4 (0%)
   Number of ECLKSYNCA:  0 out of 4 (0%)
   Number of ECLKBRIDGECS:  0 out of 2 (0%)
   Notes:-
      1. Total number of LUT4s = (Number of logic LUT4s) + 2*(Number of
     distributed RAMs) + 2*(Number of ripple logic)
      2. Number of logic LUT4s does not include count of distributed RAM and
     ripple logic.
   Number of clocks:  2
     Net clk_c: 36 loads, 36 rising, 0 falling (Driver: PIO clk )
     Net edge_det/un1_present_state_1_0_a3: 1 loads, 1 rising, 0 falling
     (Driver: edge_det/un1_present_state_1_0_a3 )
   Number of Clock Enables:  2

     Net N_16_i: 17 loads, 3 LSLICEs
     Net phase_accum/N_122_i: 1 loads, 1 LSLICEs
   Number of local set/reset loads for net reset_bar_c merged into GSR:  22
   Number of LSRs:  4
     Net phase_accum/up_down: 1 loads, 1 LSLICEs
     Net phase_accum/N_39: 1 loads, 1 LSLICEs
     Net edge_det/un1_present_state_1_0_a3: 1 loads, 1 LSLICEs
     Net edge_det/N_15_i: 2 loads, 2 LSLICEs
   Number of nets driven by tri-state buffers:  0
   Top 10 highest fanout non-clock nets:
     Net address[5]: 51 loads
     Net address[2]: 49 loads
     Net address[3]: 49 loads
     Net address[1]: 45 loads
     Net address[6]: 32 loads
     Net phase_accum/up_down: 30 loads
     Net phase_accum/un1_cnt_1_sqmuxa_1: 25 loads
     Net phase_accum/cnt_2_sqmuxa: 19 loads
     Net phase_accum/N_49: 18 loads
     Net address[4]: 17 loads




   Number of warnings:  1
   Number of errors:    0
```

Design Errors/Warnings

```
WARNING - map: Using local reset signal 'reset_bar_c' to infer global GSR net.
```

IO (PIO) Attributes

IO Name	Direction	Levelmode IO_TYPE	IO Register
dac_sine_value[0]	OUTPUT	LVCMOS25	
clk	INPUT	LVCMOS25	

pos	INPUT	LVCMOS25	
pos_sine	OUTPUT	LVCMOS25	
dac_sine_value[7]	OUTPUT	LVCMOS25	
dac_sine_value[6]	OUTPUT	LVCMOS25	
dac_sine_value[5]	OUTPUT	LVCMOS25	
dac_sine_value[4]	OUTPUT	LVCMOS25	
dac_sine_value[3]	OUTPUT	LVCMOS25	
dac_sine_value[2]	OUTPUT	LVCMOS25	
dac_sine_value[1]	OUTPUT	LVCMOS25	
load_frequency	INPUT	LVCMOS25	
freq_val[13]	INPUT	LVCMOS25	IN
freq_val[12]	INPUT	LVCMOS25	IN
freq_val[11]	INPUT	LVCMOS25	IN
freq_val[10]	INPUT	LVCMOS25	IN
freq_val[9]	INPUT	LVCMOS25	IN
freq_val[8]	INPUT	LVCMOS25	IN
freq_val[7]	INPUT	LVCMOS25	IN
freq_val[6]	INPUT	LVCMOS25	IN
freq_val[5]	INPUT	LVCMOS25	IN
freq_val[4]	INPUT	LVCMOS25	IN
freq_val[3]	INPUT	LVCMOS25	IN
freq_val[2]	INPUT	LVCMOS25	IN
freq_val[1]	INPUT	LVCMOS25	IN
freq_val[0]	INPUT	LVCMOS25	IN
reset_bar	INPUT	LVCMOS25	

Removed logic

Block VCC undriven or does not drive anything - clipped.
Block GND undriven or does not drive anything - clipped.
Block edge_det/GND undriven or does not drive anything - clipped.
Block frequency_reg/GND undriven or does not drive anything - clipped.
Block frequency_reg/VCC undriven or does not drive anything - clipped.
Block phase_accumulator_fsm/GND undriven or does not drive anything - clipped.
Block phase_accumulator_fsm/VCC undriven or does not drive anything - clipped.
Block sin_table/GND undriven or does not drive anything - clipped.
Block sin_table/VCC undriven or does not drive anything - clipped.
Block adder_subtractor/VCC undriven or does not drive anything - clipped.
Signal reset_bar_c_i was merged into signal reset_bar_c
Signal phase_accum/GND undriven or does not drive anything - clipped.
Signal adder_subtractor/GND undriven or does not drive anything - clipped.
Signal VCC undriven or does not drive anything - clipped.

Signal phase_accum/un6_cnt_compare_s_15_0_S1 undriven or does not drive anything
     - clipped.
Signal phase_accum/un6_cnt_compare_s_15_0_COUT undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_0_0_S1 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_0_0_S0 undriven or does not drive
     anything - clipped.
Signal phase_accum/N_3 undriven or does not drive anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_1_0_S1 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_1_0_S0 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_3_0_S1 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_3_0_S0 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_5_0_S1 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_5_0_S0 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_7_0_S1 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_7_0_S0 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_9_0_S1 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_9_0_S0 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_11_0_S1 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_11_0_S0 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_13_0_S1 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_cry_13_0_S0 undriven or does not drive
     anything - clipped.
Signal phase_accum/un17_cnt_compare_s_15_0_S1 undriven or does not drive
     anything - clipped.

Signal phase_accum/un17_cnt_compare_s_15_0_COUT undriven or does not drive
     anything - clipped.
Signal phase_accum/un10_leftover_cry_0_0_S1 undriven or does not drive anything
     - clipped.
Signal phase_accum/un10_leftover_cry_0_0_S0 undriven or does not drive anything
     - clipped.
Signal phase_accum/N_4 undriven or does not drive anything - clipped.
Signal phase_accum/un10_leftover_s_15_0_S1 undriven or does not drive anything -
     clipped.
Signal phase_accum/un10_leftover_s_15_0_COUT undriven or does not drive anything
     - clipped.
Signal phase_accum/un1_cnt_compare_inv_1_0_cry_0_0_S0 undriven or does not drive
     anything - clipped.
Signal phase_accum/N_5 undriven or does not drive anything - clipped.
Signal phase_accum/un1_cnt_compare_inv_1_0_s_15_0_S1 undriven or does not drive
     anything - clipped.
Signal phase_accum/un1_cnt_compare_inv_1_0_s_15_0_COUT undriven or does not

     drive anything - clipped.
Signal phase_accum/un6_cnt_compare_cry_0_0_S1 undriven or does not drive
     anything - clipped.
Signal phase_accum/un6_cnt_compare_cry_0_0_S0 undriven or does not drive
     anything - clipped.
Signal phase_accum/N_1 undriven or does not drive anything - clipped.
Signal adder_subtractor/outputVec_cry_0_0_S1 undriven or does not drive anything
     - clipped.
Signal adder_subtractor/outputVec_cry_0_0_S0 undriven or does not drive anything
     - clipped.
Signal adder_subtractor/N_1 undriven or does not drive anything - clipped.
Signal adder_subtractor/outputVec_s_7_0_S1 undriven or does not drive anything -
     clipped.
Signal adder_subtractor/outputVec_s_7_0_COUT undriven or does not drive anything
     - clipped.
Block reset_bar_pad_RNIBK19 was optimized away.
Block phase_accum/GND was optimized away.
Block adder_subtractor/GND was optimized away.

GSR Usage

GSR Component:
   The local reset signal 'reset_bar_c' of the design has been inferred as
        Global Set Reset (GSR). The reset signal used for GSR control is
        'reset_bar_c'.

     GSR Property:
   The design components with GSR property set to ENABLED will respond to global
        set reset while the components with GSR property set to DISABLED will
        not.

Run Time and Memory Usage

   Total CPU Time: 0 secs
   Total REAL Time: 0 secs
   Peak Memory Usage: 60 MB