
Module : 'full_adder'

Input files:

ABEL PLA file : full_adder_lb7.tt3
Device library : P22V10GC.dev

Output files:

Report file : full_adder_lb7.rpt
Programmer load file : full_adder_lb7.jed

P22V10GC Programmed Logic:

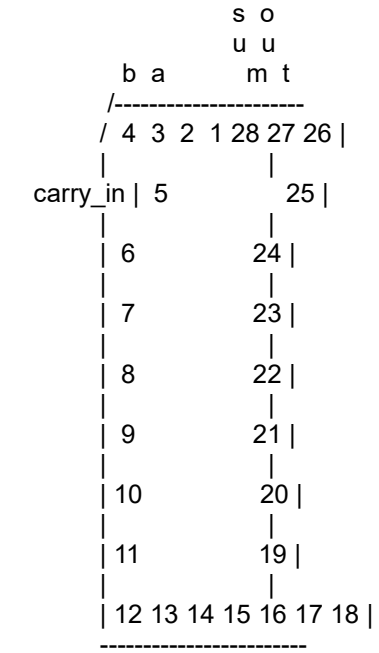
```
sum     = (  a & b & carry_in
         #   !a & !b & carry_in
         #   !a & b & !carry_in
         #   a & !b & !carry_in );

carry_out     = (  a & b
                #   a & carry_in
                #   b & carry_in );
```


P22V10GC Chip Diagram: (PLCC package)

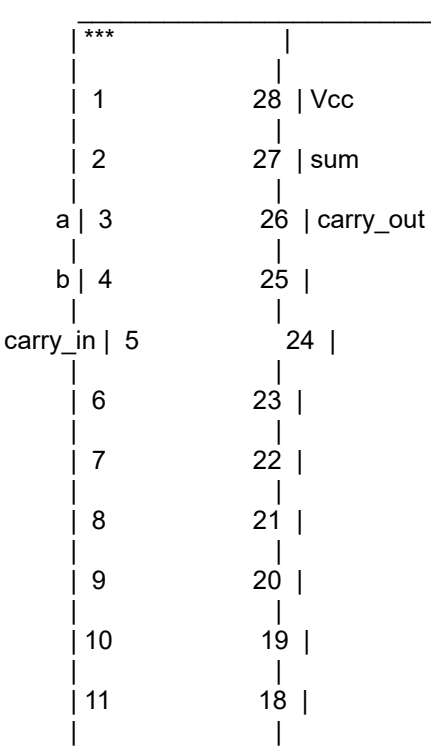
P22V10GC

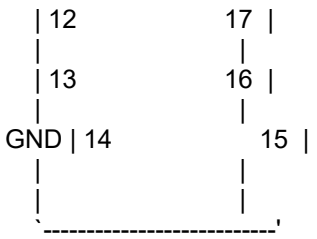
c
a
r
r
y
_



P22V10GC Chip Diagram: (SSOP package)

P22V10GC





SIGNATURE: N/A

P22V10GC Resource Allocations:

Device Resources	Resource Available	Design Requirement	Unused
Input Pins:			
Input:	12	3	9 (75 %)
Output Pins:			
In/Out:	10	2	8 (80 %)
Output:	-	-	-
Buried Nodes:			
Input Reg:	-	-	-
Pin Reg:	10	0	10 (100 %)
Buried Reg:	-	-	-

P22V10GC Product Terms Distribution:

Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
sum	27	4	8	4
carry_out	26	3	10	7

==== List of Inputs/Feedbacks ====

Signal Name	Pin	Pin Type
a	3	INPUT
b	4	INPUT
carry_in	5	INPUT

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P22V10GC Unused Resources:

Pin Number	Pin Type	Product Terms	Flip-flop Type
6	INPUT	-	-
7	INPUT	-	-
9	INPUT	-	-
10	INPUT	-	-
11	INPUT	-	-
12	INPUT	-	-
13	INPUT	-	-
16	INPUT	-	-
17	BIDIR	NORMAL 8	D
18	BIDIR	NORMAL 10	D
19	BIDIR	NORMAL 12	D
20	BIDIR	NORMAL 14	D
21	BIDIR	NORMAL 16	D
23	BIDIR	NORMAL 16	D
24	BIDIR	NORMAL 14	D
25	BIDIR	NORMAL 12	D