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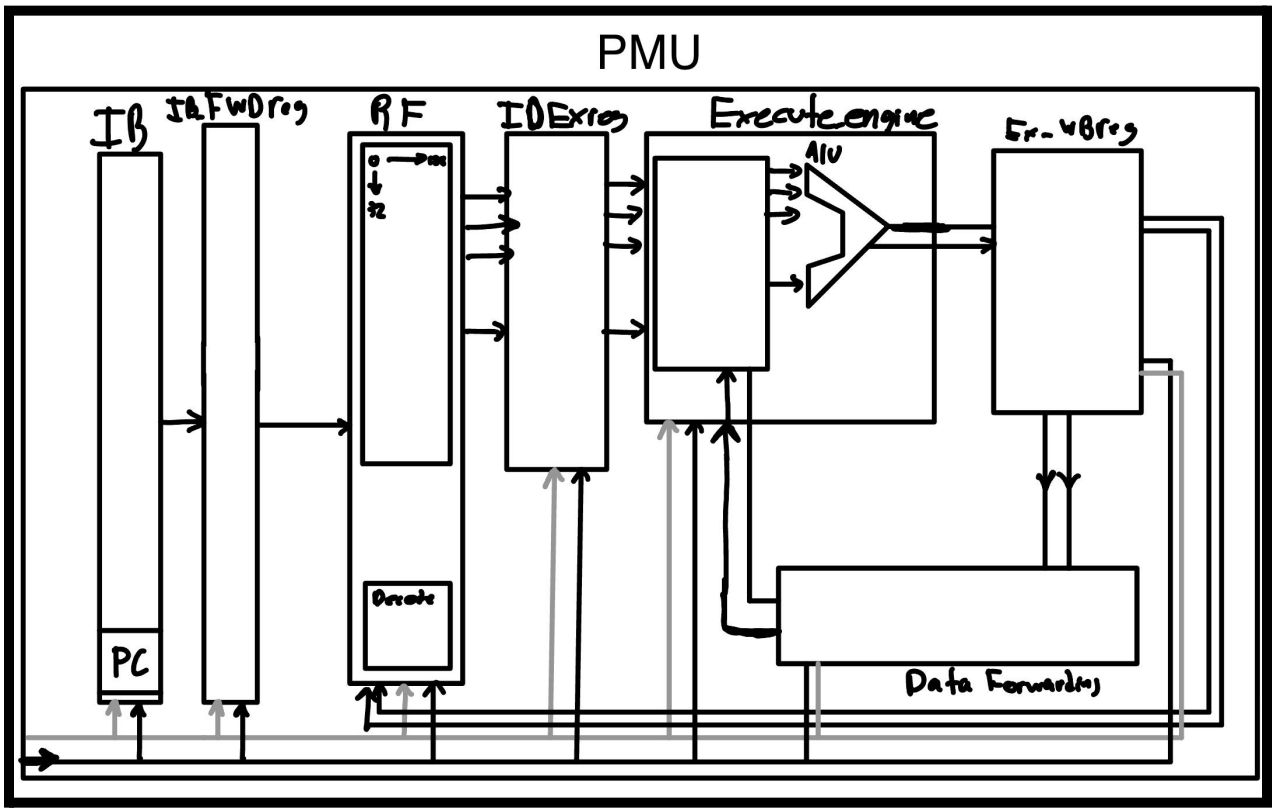

ESE 345 Design Procedure

The overall goal of this project was to implement a pipelined multimedia unit using VHDL. This included coding the different aspects of multimedia such as the register file, instruction buffer, assembler, and forwarding unit. We also created a results file within the testbench so that we can see what is happening at each stage of the pipeline for all of the instructions.

To approach this project, we first designed and built the entities. Afterward, we connected those entities, wrote the testbench, and debugged them as necessary. The main challenge we ran into was not realizing early on that creating debugging ports in the entities was useful for us to see what was happening in each pipeline state. This was, it would be reportable to the testbench. Another challenge was figuring out how to approach programming the instruction buffer and what kind of asynchronous process it would require. The third challenge of this project was understanding and figuring out how to solve the issue of the entities creating “phantom” instructions in the entities at earlier clock cycles. This would happen when the pipeline was empty and would create “U” data. To resolve this issue, we needed to implement a signal created by the instruction buffer that would propagate through with any instruction it sent out indicating a “Valid” Instruction.

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Through many tests of the system, our pipelined multimedia unit works. The registers at the end had all of the expected results after 64 instructions. Additionally, the instructions were forwarded when necessary and we were able to see the updates happening in each cycle for each instruction as expected.