```
#Build: Synplify Pro (R) S-2021.09-SP2, Build 244R, Jun  1 2022
#install: C:\Synopsys\fpga_S-2021.09-SP2
#OS: Windows 10 or later
#Hostname: DESKTOP-1LR5K5T

# Thu Nov 30 16:14:49 2023

#Implementation: rev_1


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Tool: Synplify Pro (R)
Build: S-2021.09-SP2
Install: C:\Synopsys\fpga_S-2021.09-SP2
OS: Windows 10 or later
Hostname: DESKTOP-1LR5K5T

Implementation : rev_1
Synopsys HDL Compiler, Version comp202109syn, Build 243R, Built Jun  1 2022 05:18:42, @

@N: :  | Running in 64-bit mode
############################################################[

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Hostname: DESKTOP-1LR5K5T

Implementation : rev_1
Synopsys VHDL Compiler, Version comp202109syn, Build 243R, Built Jun  1 2022 05:18:42, @

@N: :  | Running in 64-bit mode
@N: : RF.vhd(26) | Top entity is set to RF.
@N:CD140 :  | Using the VHDL 1993 Standard for file 'C:\Users\userESD\Desktop\345PROJECT-main\345PROJECT-chris-s-code\345Proj\ALU_Beta\src\ALU.vhd'
@N:CD140 :  | Using the VHDL 1993 Standard for file 'C:\Users\userESD\Desktop\345PROJECT-main\345PROJECT-chris-s-code\345Proj\ALU_Beta\src\EX_WBreg
@N:CD140 :  | Using the VHDL 1993 Standard for file 'C:\Users\userESD\Desktop\345PROJECT-main\345PROJECT-chris-s-code\345Proj\ALU_Beta\src\EXECUTE_
@N:CD140 :  | Using the VHDL 1993 Standard for file 'C:\Users\userESD\Desktop\345PROJECT-main\345PROJECT-chris-s-code\345Proj\ALU_Beta\src\IB.vhd'.
@N:CD140 :  | Using the VHDL 1993 Standard for file 'C:\Users\userESD\Desktop\345PROJECT-main\345PROJECT-chris-s-code\345Proj\ALU_Beta\src\IB_FWDre
@N:CD140 :  | Using the VHDL 1993 Standard for file 'C:\Users\userESD\Desktop\345PROJECT-main\345PROJECT-chris-s-code\345Proj\ALU_Beta\src\ID_EXreg
@N:CD140 :  | Using the VHDL 1993 Standard for file 'C:\Users\userESD\Desktop\345PROJECT-main\345PROJECT-chris-s-code\345Proj\ALU_Beta\src\RF.vhd'.
VHDL syntax check successful!
@N:CD630 : RF.vhd(26) | Synthesizing work.rf.behavioral.
@W:CD434 : RF.vhd(82) | Signal clk in the sensitivity list is not used in the process. Make sure all variables in the sensitivity list are referenc
@W:CG296 : RF.vhd(82) | Incomplete sensitivity list; assuming completeness. Make sure all referenced variables in message CG290 are included in the
@W:CG290 : RF.vhd(170) | Referenced variable valid_instruction_in_wb is not in sensitivity list.
@W:CG290 : RF.vhd(115) | Referenced variable valid_instruction_in is not in sensitivity list.
@W:CG290 : RF.vhd(170) | Referenced variable hold is not in sensitivity list.
@W:CG290 : RF.vhd(106) | Referenced variable ib_empty is not in sensitivity list.
Post processing for work.rf.behavioral
Running optimization stage 1 on RF .......
@A:CL109 : RF.vhd(170) | Too many clocks (> 8) for set/reset analysis of reg_B, try moving enabling expressions outside process
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_B(127 downto 0); possible missing assignment in an if or case statement.
@A:CL109 : RF.vhd(170) | Too many clocks (> 8) for set/reset analysis of reg_A, try moving enabling expressions outside process
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_A(127 downto 0); possible missing assignment in an if or case statement.
@A:CL109 : RF.vhd(170) | Too many clocks (> 8) for set/reset analysis of reg_C, try moving enabling expressions outside process
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_C(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_31(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_30(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_29(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_28(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_27(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_26(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_25(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_24(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_23(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_22(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_21(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_20(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_19(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_18(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_17(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_16(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_15(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_14(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_13(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_12(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_11(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_10(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_9(127 downto 0); possible missing assignment in an if or case statement.
```

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@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_8(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_7(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_6(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_5(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_4(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_3(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_2(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_1(127 downto 0); possible missing assignment in an if or case statement.
@W:CL117 : RF.vhd(170) | Latch generated from process for signal reg_0(127 downto 0); possible missing assignment in an if or case statement.
Finished optimization stage 1 on RF (CPU Time 0h:00m:00s, Memory Used current: 140MB peak: 141MB)
Running optimization stage 2 on RF .......
@W:CL246 : RF.vhd(37) | Input port bits 24 to 5 of wb_opcodedata(24 downto 0) are unused. Assign logic for all port bits or change the input port s
@N:CL159 : RF.vhd(35) | Input clk is unused.
Finished optimization stage 2 on RF (CPU Time 0h:00m:02s, Memory Used current: 169MB peak: 170MB)

For a summary of runtime and memory usage per design unit, please see file:
============================================================
Linked File:  layer0.rt.csv


At c_vhdl Exit (Real Time elapsed 0h:00m:03s; CPU Time elapsed 0h:00m:03s; Memory used current: 170MB peak: 170MB)

Process took 0h:00m:03s realtime, 0h:00m:03s cputime

Process completed successfully.
# Thu Nov 30 16:14:52 2023

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Tool: Synplify Pro (R)
Build: S-2021.09-SP2
Install: C:\Synopsys\fpga_S-2021.09-SP2
OS: Windows 10 or later
Hostname: DESKTOP-1LR5K5T

Implementation : rev_1
Synopsys Synopsys Netlist Linker, Version comp202109syn, Build 243R, Built Jun  1 2022 05:18:42, @

@N: :  | Running in 64-bit mode
@N:NF107 : rf.vhd(26) | Selected library: work cell: RF view behavioral as top level
@N:NF107 : rf.vhd(26) | Selected library: work cell: RF view behavioral as top level

At syn_nfilter Exit (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 95MB peak: 96MB)

Process took 0h:00m:01s realtime, 0h:00m:01s cputime

Process completed successfully.
# Thu Nov 30 16:14:52 2023

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For a summary of runtime and memory usage for all design units, please see file:
============================================================
Linked File:  PMU_comp.rt.csv

@END

At c_hdl Exit (Real Time elapsed 0h:00m:03s; CPU Time elapsed 0h:00m:03s; Memory used current: 23MB peak: 23MB)

Process took 0h:00m:03s realtime, 0h:00m:03s cputime

Process completed successfully.
# Thu Nov 30 16:14:53 2023

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Tool: Synplify Pro (R)
Build: S-2021.09-SP2
Install: C:\Synopsys\fpga_S-2021.09-SP2
OS: Windows 10 or later
Hostname: DESKTOP-1LR5K5T

Implementation : rev_1
Synopsys Synopsys Netlist Linker, Version comp202109syn, Build 243R, Built Jun  1 2022 05:18:42, @

@N: :  | Running in 64-bit mode
@N:NF107 : rf.vhd(26) | Selected library: work cell: RF view behavioral as top level
@N:NF107 : rf.vhd(26) | Selected library: work cell: RF view behavioral as top level
```

```
At syn_nfilter Exit (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 97MB peak: 98MB)

Process took 0h:00m:01s realtime, 0h:00m:01s cputime

Process completed successfully.
# Thu Nov 30 16:14:54 2023

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Premap Report

# Thu Nov 30 16:14:54 2023


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Tool: Synplify Pro (R)
Build: S-2021.09-SP2
Install: C:\Synopsys\fpga_S-2021.09-SP2
OS: Windows 10 or later
Hostname: DESKTOP-1LR5K5T

Implementation : rev_1
Synopsys Lattice Technology Pre-mapping, Version map202109syn, Build 243R, Built Jun  1 2022 05:17:33, @


Mapper Startup Complete (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 118MB peak: 118MB)


Done reading skeleton netlist (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 125MB peak: 131MB)

@A:MF827 :  | No constraint file specified.
Linked File:  PMU_scck.rpt
See clock summary report "C:\Users\userESD\Desktop\345PROJECT-main\345PROJECT-chris-s-code\345Proj\ALU_Beta\Synplify\rev_1\PMU_scck.rpt"
@N:MF916 :  | Option synthesis_strategy=base is enabled.
@N:MF248 :  | Running in 64-bit mode.
@N:MF666 :  | Clock conversion enabled. (Command "set_option -fix_gated_and_generated_clocks 1" in the project file.)

Design Input Complete (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 135MB peak: 135MB)


Mapper Initialization Complete (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 135MB peak: 136MB)


Start loading timing files (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 148MB peak: 148MB)


Finished loading timing files (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 149MB peak: 151MB)


Starting HSTDM IP insertion (Real Time elapsed 0h:00m:07s; CPU Time elapsed 0h:00m:07s; Memory used current: 205MB peak: 205MB)


Finished HSTDM IP insertion (Real Time elapsed 0h:00m:07s; CPU Time elapsed 0h:00m:07s; Memory used current: 205MB peak: 205MB)


Starting clock optimization phase (Real Time elapsed 0h:00m:08s; CPU Time elapsed 0h:00m:08s; Memory used current: 221MB peak: 221MB)


 mixed edge conversion for GCC is OFF
Finished clock optimization phase (Real Time elapsed 0h:00m:08s; CPU Time elapsed 0h:00m:08s; Memory used current: 228MB peak: 228MB)

@N:BZ111 :  | Number of ICGs considered for optimization : 0
@N:MT611 :  | Automatically generated clock RF|reg_0_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_1_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_2_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_3_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_4_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_5_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_6_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_7_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_8_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_9_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_10_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_11_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_12_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_13_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_14_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_15_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_16_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_17_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_18_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_19_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_20_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_21_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_22_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_23_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_24_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_25_1_sqmuxa_inferred_clock is not used and is being removed
```

```
@N:MT611 :  | Automatically generated clock RF|reg_26_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_27_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_28_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_29_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_30_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_31_1_sqmuxa_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_C_1_sqmuxa_1_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_B_1_sqmuxa_3_inferred_clock is not used and is being removed
@N:MT611 :  | Automatically generated clock RF|reg_A_1_sqmuxa_inferred_clock is not used and is being removed

Starting clock optimization report phase (Real Time elapsed 0h:00m:08s; CPU Time elapsed 0h:00m:08s; Memory used current: 225MB peak: 228MB)


 mixed edge conversion for GCC is OFF
 mixed edge conversion for GCC is OFF
 mixed edge conversion for GCC is OFF
 mixed edge conversion for GCC is OFF
Finished clock optimization report phase (Real Time elapsed 0h:00m:08s; CPU Time elapsed 0h:00m:08s; Memory used current: 225MB peak: 228MB)

@N:FX1184 :  | Applying syn_allowed_resources blockrams=240 on top level netlist RF

Finished netlist restructuring (Real Time elapsed 0h:00m:08s; CPU Time elapsed 0h:00m:08s; Memory used current: 225MB peak: 228MB)



Clock Summary
******************

          Start     Requested     Requested     Clock     Clock     Clock
Level     Clock     Frequency     Period        Type      Group     Load
------------------------------------------------------------------------
========================================================================



Clock Load Summary
***********************

          Clock     Source     Clock Pin       Non-clock Pin     Non-clock Pin
Clock     Load      Pin        Seq Example     Seq Example       Comb Example
---------------------------------------------------------------------------------
=================================================================================

@W:MT531 : rf.vhd(170) | Found signal identified as System clock which controls 4480 sequential elements including reg_0_out[127].  Using this cloc

ICG Latch Removal Summary:
Number of ICG latches removed: 0
Number of ICG latches not removed:      0
For details review file gcc_ICG_report.rpt


@S |Clock Optimization Summary



#### START OF PREMAP CLOCK OPTIMIZATION REPORT #####[

0 non-gated/non-generated clock tree(s) driving 0 clock pin(s) of sequential element(s)
35 gated/generated clock tree(s) driving 4480 clock pin(s) of sequential element(s)
0 instances converted, 4480 sequential instances remain driven by gated/generated clocks

============================================================ Gated/Generated Clocks ============================================================
Clock Tree ID     Driving Element           Drive Element Type     Unconverted Fanout     Sample Instance     Explanation
--------------------------------------------------------------------------------------------------------------------------------------------
ClockId_0_0       uclk_reg_0_outor.OUT      or                     128                    reg_0_out[127]      Derived clock on input (not legal for
ClockId_0_1       uclk_reg_1_outor.OUT      or                     128                    reg_1_out[127]      Derived clock on input (not legal for
ClockId_0_2       uclk_reg_2_outor.OUT      or                     128                    reg_2_out[127]      Derived clock on input (not legal for
ClockId_0_3       uclk_reg_3_outor.OUT      or                     128                    reg_3_out[127]      Derived clock on input (not legal for
ClockId_0_4       uclk_reg_4_outor.OUT      or                     128                    reg_4_out[127]      Derived clock on input (not legal for
ClockId_0_5       uclk_reg_5_outor.OUT      or                     128                    reg_5_out[127]      Derived clock on input (not legal for
ClockId_0_6       uclk_reg_6_outor.OUT      or                     128                    reg_6_out[127]      Derived clock on input (not legal for
ClockId_0_7       uclk_reg_7_outor.OUT      or                     128                    reg_7_out[127]      Derived clock on input (not legal for
ClockId_0_8       uclk_reg_8_outor.OUT      or                     128                    reg_8_out[127]      Derived clock on input (not legal for
ClockId_0_9       uclk_reg_9_outor.OUT      or                     128                    reg_9_out[127]      Derived clock on input (not legal for
ClockId_0_10      uclk_reg_10_outor.OUT     or                     128                    reg_10_out[127]     Derived clock on input (not legal for
ClockId_0_11      uclk_reg_11_outor.OUT     or                     128                    reg_11_out[127]     Derived clock on input (not legal for
ClockId_0_12      uclk_reg_12_outor.OUT     or                     128                    reg_12_out[127]     Derived clock on input (not legal for
ClockId_0_13      uclk_reg_13_outor.OUT     or                     128                    reg_13_out[127]     Derived clock on input (not legal for
ClockId_0_14      uclk_reg_14_outor.OUT     or                     128                    reg_14_out[127]     Derived clock on input (not legal for
ClockId_0_15      uclk_reg_15_outor.OUT     or                     128                    reg_15_out[127]     Derived clock on input (not legal for
ClockId_0_16      uclk_reg_16_outor.OUT     or                     128                    reg_16_out[127]     Derived clock on input (not legal for
ClockId_0_17      uclk_reg_17_outor.OUT     or                     128                    reg_17_out[127]     Derived clock on input (not legal for
ClockId_0_18      uclk_reg_18_outor.OUT     or                     128                    reg_18_out[127]     Derived clock on input (not legal for
ClockId_0_19      uclk_reg_19_outor.OUT     or                     128                    reg_19_out[127]     Derived clock on input (not legal for
ClockId_0_20      uclk_reg_20_outor.OUT     or                     128                    reg_20_out[127]     Derived clock on input (not legal for
ClockId_0_21      uclk_reg_21_outor.OUT     or                     128                    reg_21_out[127]     Derived clock on input (not legal for
ClockId_0_22      uclk_reg_22_outor.OUT     or                     128                    reg_22_out[127]     Derived clock on input (not legal for
ClockId_0_23      uclk_reg_23_outor.OUT     or                     128                    reg_23_out[127]     Derived clock on input (not legal for
ClockId_0_24      uclk_reg_24_outor.OUT     or                     128                    reg_24_out[127]     Derived clock on input (not legal for
ClockId_0_25      uclk_reg_25_outor.OUT     or                     128                    reg_25_out[127]     Derived clock on input (not legal for
ClockId_0_26      uclk_reg_26_outor.OUT     or                     128                    reg_26_out[127]     Derived clock on input (not legal for
```

ClockId_0_27	uclk_reg_27_outor.OUT	or	128	reg_27_out[127]	Derived clock on input (not legal for
ClockId_0_28	uclk_reg_28_outor.OUT	or	128	reg_28_out[127]	Derived clock on input (not legal for
ClockId_0_29	uclk_reg_29_outor.OUT	or	128	reg_29_out[127]	Derived clock on input (not legal for
ClockId_0_30	uclk_reg_30_outor.OUT	or	128	reg_30_out[127]	Derived clock on input (not legal for
ClockId_0_31	uclk_reg_31_outor.OUT	or	128	reg_31_out[127]	Derived clock on input (not legal for
ClockId_0_32	reg_C_1_sqmuxa_1.OUT	and	128	reg_C[127]	Derived clock on input (not legal for
ClockId_0_33	reg_B_1_sqmuxa_3.OUT	and	128	reg_B[127]	Derived clock on input (not legal for
ClockId_0_34	reg_A_1_sqmuxa.OUT	and	128	reg_A[127]	Derived clock on input (not legal for

```
##### END OF CLOCK OPTIMIZATION REPORT ######

@N:FX1143 :  | Skipping assigning INTERNAL_VREF to iobanks, because the table of mapping from pin to iobank is not initialized.
Finished Pre Mapping Phase.

Starting constraint checker (Real Time elapsed 0h:00m:10s; CPU Time elapsed 0h:00m:10s; Memory used current: 223MB peak: 228MB)


Finished constraint checker preprocessing (Real Time elapsed 0h:00m:10s; CPU Time elapsed 0h:00m:10s; Memory used current: 223MB peak: 228MB)


Finished constraint checker (Real Time elapsed 0h:00m:10s; CPU Time elapsed 0h:00m:10s; Memory used current: 231MB peak: 231MB)

Pre-mapping successful!

At Mapper Exit (Real Time elapsed 0h:00m:10s; CPU Time elapsed 0h:00m:10s; Memory used current: 139MB peak: 231MB)

Process took 0h:00m:10s realtime, 0h:00m:10s cputime
# Thu Nov 30 16:15:05 2023

##########################################################]
Map & Optimize Report

# Thu Nov 30 16:15:05 2023


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and may only be used pursuant to the terms and conditions of a written license agreement
with Synopsys, Inc. All other use, reproduction, modification, or distribution of the
Synopsys software or the associated documentation is strictly prohibited.
Tool: Synplify Pro (R)
Build: S-2021.09-SP2
Install: C:\Synopsys\fpga_S-2021.09-SP2
OS: Windows 10 or later
Hostname: DESKTOP-1LR5K5T

Implementation : rev_1
Synopsys Lattice Technology Mapper, Version map202109syn, Build 243R, Built Jun  1 2022 05:17:33, @


Mapper Startup Complete (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 118MB peak: 118MB)

@N:MF916 :  | Option synthesis_strategy=base is enabled.
@N:MF248 :  | Running in 64-bit mode.
@N:MF666 :  | Clock conversion enabled. (Command "set_option -fix_gated_and_generated_clocks 1" in the project file.)

Design Input Complete (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 120MB peak: 130MB)


Mapper Initialization Complete (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 120MB peak: 130MB)


Start loading timing files (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 133MB peak: 133MB)


Finished loading timing files (Real Time elapsed 0h:00m:00s; CPU Time elapsed 0h:00m:00s; Memory used current: 135MB peak: 137MB)



Starting Optimization and Mapping (Real Time elapsed 0h:00m:01s; CPU Time elapsed 0h:00m:01s; Memory used current: 208MB peak: 208MB)

@N:MT206 :  | Auto Constrain mode is enabled

Finished RTL optimizations (Real Time elapsed 0h:00m:04s; CPU Time elapsed 0h:00m:04s; Memory used current: 218MB peak: 219MB)

@N:MF179 : rf.vhd(178) | Found 5 by 5 bit equality operator ('==') un8_register_write (in view: work.RF(behavioral))
@N:MF179 : rf.vhd(181) | Found 5 by 5 bit equality operator ('==') un11_register_write (in view: work.RF(behavioral))
@N:MF179 : rf.vhd(184) | Found 5 by 5 bit equality operator ('==') un14_register_write (in view: work.RF(behavioral))

Starting factoring (Real Time elapsed 0h:00m:13s; CPU Time elapsed 0h:00m:13s; Memory used current: 241MB peak: 260MB)


Finished factoring (Real Time elapsed 0h:00m:17s; CPU Time elapsed 0h:00m:17s; Memory used current: 267MB peak: 267MB)


Available hyper_sources - for debug and ip models
        None Found
```

```
Finished generic timing optimizations - Pass 1 (Real Time elapsed 0h:00m:22s; CPU Time elapsed 0h:00m:22s; Memory used current: 284MB peak: 300MB)

Starting Early Timing Optimization (Real Time elapsed 0h:00m:25s; CPU Time elapsed 0h:00m:25s; Memory used current: 288MB peak: 300MB)

Finished Early Timing Optimization (Real Time elapsed 0h:00m:38s; CPU Time elapsed 0h:00m:38s; Memory used current: 294MB peak: 300MB)

Finished generic timing optimizations - Pass 2 (Real Time elapsed 0h:00m:39s; CPU Time elapsed 0h:00m:39s; Memory used current: 295MB peak: 300MB)

Finished preparing to map (Real Time elapsed 0h:00m:42s; CPU Time elapsed 0h:00m:42s; Memory used current: 285MB peak: 300MB)

Finished technology mapping (Real Time elapsed 0h:00m:45s; CPU Time elapsed 0h:00m:45s; Memory used current: 301MB peak: 301MB)

Pass             CPU time               Worst Slack             Luts / Registers
------------------------------------------------------------
   1            0h:00m:46s                  -0.73ns             10736 /         0
   2            0h:00m:47s                  -0.73ns             10736 /         0

   3            0h:00m:48s                  -0.73ns             10736 /         0


   4            0h:00m:54s                  -0.73ns             10736 /         0
@N:FX104 : rf.vhd(36) | Inserting 4 buffers on net opcode_c[19] (with fanout of 2052) because of a soft fanout limit of 1000.
@N:FX104 : rf.vhd(36) | Inserting 3 buffers on net opcode_c[18] (with fanout of 1031) because of a soft fanout limit of 1000.
@N:FX104 : rf.vhd(36) | Inserting 4 buffers on net opcode_c[14] (with fanout of 2050) because of a soft fanout limit of 1000.
@N:FX104 : rf.vhd(36) | Inserting 3 buffers on net opcode_c[13] (with fanout of 1026) because of a soft fanout limit of 1000.
@N:FX104 : rf.vhd(36) | Inserting 4 buffers on net opcode_c[9] (with fanout of 2050) because of a soft fanout limit of 1000.
@N:FX104 : rf.vhd(36) | Inserting 3 buffers on net opcode_c[8] (with fanout of 1026) because of a soft fanout limit of 1000.
Net buffering Report for view:work.RF(behavioral):
Added 15 Buffers
Added 0 Registers via replication
Added 0 LUTs via replication

Finished technology timing optimizations and critical path resynthesis (Real Time elapsed 0h:01m:00s; CPU Time elapsed 0h:01m:00s; Memory used curr

@N:FX164 :  | The option to pack registers in the IOB has not been specified. Please set syn_useioff attribute.

Finished restoring hierarchy (Real Time elapsed 0h:01m:10s; CPU Time elapsed 0h:01m:10s; Memory used current: 293MB peak: 306MB)

Start Writing Netlists (Real Time elapsed 0h:01m:11s; CPU Time elapsed 0h:01m:10s; Memory used current: 205MB peak: 306MB)

Writing Analyst data base C:\Users\userESD\Desktop\345PROJECT-main\345PROJECT-chris-s-code\345Proj\ALU_Beta\Synplify\rev_1\synwork\PMU_m.srm

Finished Writing Netlist Databases (Real Time elapsed 0h:01m:13s; CPU Time elapsed 0h:01m:12s; Memory used current: 280MB peak: 306MB)

Writing EDIF Netlist and constraint files
@N:FX1056 :  | Writing EDF file: C:\Users\userESD\Desktop\345PROJECT-main\345PROJECT-chris-s-code\345Proj\ALU_Beta\Synplify\rev_1\PMU.edn
@N:BW106 :  | Synplicity Constraint File capacitance units using default value of 1pF
@W:BW150 :  | Clock RF|reg_0_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_1_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_2_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_3_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_4_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_5_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_6_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_7_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_8_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_9_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_10_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_11_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_12_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_13_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_14_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_15_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_16_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_17_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_18_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_19_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_20_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_21_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_22_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_23_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_24_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_25_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_26_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_27_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_28_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_29_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_30_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_31_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_C_1_sqmuxa_1_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_B_1_sqmuxa_3_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated
@W:BW150 :  | Clock RF|reg_A_1_sqmuxa_inferred_clock in set_clock_groups command cannot be found and will not be forward annotated

Finished Writing EDIF Netlist and constraint files (Real Time elapsed 0h:01m:15s; CPU Time elapsed 0h:01m:15s; Memory used current: 297MB peak: 306
```

Finished Writing Netlists (Real Time elapsed 0h:01m:15s; CPU Time elapsed 0h:01m:15s; Memory used current: 297MB peak: 306MB)

Start final timing analysis (Real Time elapsed 0h:01m:16s; CPU Time elapsed 0h:01m:15s; Memory used current: 292MB peak: 306MB)

START OF TIMING REPORT #####[
Timing report written on Thu Nov 30 16:16:22 2023
#

Top view: RF
Requested Frequency: 302.8 MHz
Wire load mode: top
Paths requested: 5
Constraint File(s):
@N:MT320 : | This timing report is an estimate of place and route data. For final timing results, use the FPGA vendor place and route report.

@N:MT322 : | Clock constraints include only register-to-register paths associated with each individual clock.

Performance Summary
****

Worst slack in design: -0.583

Starting Clock	Requested Frequency	Estimated Frequency	Requested Period	Estimated Period	Slack	Clock Type	Clock Group
System	302.8 MHz	257.4 MHz	3.303	3.885	-0.583	system	system_clkgroup

Clock Relationships
****

Clocks		rise to rise		fall to fall		rise to fall		fall to rise	
Starting	Ending	constraint	slack	constraint	slack	constraint	slack	constraint	slack
System	System	3.303	-0.583	No paths	-	No paths	-	No paths	-

Note: 'No paths' indicates there are no paths in the design for that pair of clock edges.
'Diff grp' indicates that paths exist but the starting clock and ending clock are in different clock groups.

Interface Information
****

No IO constraint found

==========
Detailed Report for Clock: System
==========

Starting Points with Worst Slack
****

Instance	Starting Reference Clock	Type	Pin	Net	Arrival Time	Slack
reg_0_out[0]	System	FD1S1AY	Q	reg_0_out_c[0]	1.180	-0.583
reg_0_out[1]	System	FD1S1AY	Q	reg_0_out_c[1]	1.180	-0.583
reg_0_out[2]	System	FD1S1AY	Q	reg_0_out_c[2]	1.180	-0.583
reg_0_out[3]	System	FD1S1AY	Q	reg_0_out_c[3]	1.180	-0.583
reg_0_out[4]	System	FD1S1AY	Q	reg_0_out_c[4]	1.180	-0.583
reg_0_out[5]	System	FD1S1AY	Q	reg_0_out_c[5]	1.180	-0.583
reg_0_out[6]	System	FD1S1AY	Q	reg_0_out_c[6]	1.180	-0.583
reg_0_out[7]	System	FD1S1AY	Q	reg_0_out_c[7]	1.180	-0.583
reg_0_out[8]	System	FD1S1AY	Q	reg_0_out_c[8]	1.180	-0.583
reg_0_out[9]	System	FD1S1AY	Q	reg_0_out_c[9]	1.180	-0.583

Ending Points with Worst Slack
****

Instance	Starting Reference Clock	Type	Pin	Net	Required Time	Slack
reg_A[0]	System	FD1S1AY	D	N_55730_i	3.391	-0.583
reg_A[1]	System	FD1S1AY	D	N_57325_i	3.391	-0.583
reg_A[2]	System	FD1S1AY	D	N_54314_i	3.391	-0.583
reg_A[3]	System	FD1S1AY	D	N_54313_i	3.391	-0.583
reg_A[4]	System	FD1S1AY	D	N_55105_i	3.391	-0.583
reg_A[5]	System	FD1S1AY	D	N_54312_i	3.391	-0.583
reg_A[6]	System	FD1S1AY	D	N_56782_i	3.391	-0.583
reg_A[7]	System	FD1S1AY	D	N_54311_i	3.391	-0.583
reg_A[8]	System	FD1S1AY	D	N_56781_i	3.391	-0.583
reg_A[9]	System	FD1S1AY	D	N_54310_i	3.391	-0.583

Worst Path Information
View Worst Path in Analyst
****

Path information for path number 1:

Requested Period:	3.303
- Setup time:	-0.089
+ Clock delay at ending point:	0.000 (ideal)
+ Estimated clock delay at ending point:	0.000
= Required time:	3.391
- Propagation time:	3.974
- Clock delay at starting point:	0.000 (ideal)
- Estimated clock delay at start point:	-0.000
= Slack (critical) :	-0.583
Number of logic level(s):	6
Starting point:	reg_0_out[0] / Q
Ending point:	reg_A[0] / D
The start point is clocked by	System [rising] on pin CK
The end point is clocked by	System [rising] on pin CK

Instance / Net Name	Type	Pin Name	Pin Dir	Delay	Arrival Time	No. of Fan Out(s)
reg_0_out[0]	FD1S1AY	Q	Out	1.180	1.180 r	-
reg_0_out_c[0]	Net	-	-	-	-	5
reg_A_3_3_am[0]	ORCALUT4	C	In	0.000	1.180 r	-
reg_A_3_3_am[0]	ORCALUT4	Z	Out	1.017	2.197 r	-
reg_A_3_3_am[0]	Net	-	-	-	-	1
reg_A_3_3[0]	PFUMX	BLUT	In	0.000	2.197 r	-
reg_A_3_3[0]	PFUMX	Z	Out	-0.033	2.164 r	-
reg_A_3_3[0]	Net	-	-	-	-	1
reg_A_3_7[0]	L6MUX21	D0	In	0.000	2.164 r	-
reg_A_3_7[0]	L6MUX21	Z	Out	0.265	2.428 r	-
reg_A_3_7[0]	Net	-	-	-	-	1
reg_A_3_15[0]	L6MUX21	D0	In	0.000	2.428 r	-
reg_A_3_15[0]	L6MUX21	Z	Out	0.265	2.693 r	-
reg_A_3_15[0]	Net	-	-	-	-	1
reg_A_3_31[0]	L6MUX21	D0	In	0.000	2.693 r	-
reg_A_3_31[0]	L6MUX21	Z	Out	0.265	2.957 r	-
reg_A_3[0]	Net	-	-	-	-	1
reg_A_RNO[0]	ORCALUT4	C	In	0.000	2.957 r	-
reg_A_RNO[0]	ORCALUT4	Z	Out	1.017	3.974 r	-
N_55730_i	Net	-	-	-	-	1
reg_A[0]	FD1S1AY	D	In	0.000	3.974 r	-

Path information for path number 2:

Requested Period:	3.303
- Setup time:	-0.089
+ Clock delay at ending point:	0.000 (ideal)
+ Estimated clock delay at ending point:	0.000
= Required time:	3.391
- Propagation time:	3.974
- Clock delay at starting point:	0.000 (ideal)
- Estimated clock delay at start point:	-0.000
= Slack (critical) :	-0.583
Number of logic level(s):	6
Starting point:	reg_0_out[1] / Q
Ending point:	reg_A[1] / D
The start point is clocked by	System [rising] on pin CK
The end point is clocked by	System [rising] on pin CK

Instance / Net Name	Type	Pin Name	Pin Dir	Delay	Arrival Time	No. of Fan Out(s)
reg_0_out[1]	FD1S1AY	Q	Out	1.180	1.180 r	-
reg_0_out_c[1]	Net	-	-	-	-	5

```
reg_A_3_3_am[1]     ORCALUT4     C        In      0.000      1.180 r     -
reg_A_3_3_am[1]     ORCALUT4     Z        Out     1.017      2.197 r     -
reg_A_3_3_am[1]     Net          -        -       -          -           1
reg_A_3_3[1]        PFUMX        BLUT     In      0.000      2.197 r     -
reg_A_3_3[1]        PFUMX        Z        Out     -0.033     2.164 r     -
reg_A_3_3[1]        Net          -        -       -          -           1
reg_A_3_7[1]        L6MUX21      D0       In      0.000      2.164 r     -
reg_A_3_7[1]        L6MUX21      Z        Out     0.265      2.428 r     -
reg_A_3_7[1]        Net          -        -       -          -           1
reg_A_3_15[1]       L6MUX21      D0       In      0.000      2.428 r     -
reg_A_3_15[1]       L6MUX21      Z        Out     0.265      2.693 r     -
reg_A_3_15[1]       Net          -        -       -          -           1
reg_A_3_31[1]       L6MUX21      D0       In      0.000      2.693 r     -
reg_A_3_31[1]       L6MUX21      Z        Out     0.265      2.957 r     -
reg_A_3[1]          Net          -        -       -          -           1
reg_A_RNO[1]        ORCALUT4     C        In      0.000      2.957 r     -
reg_A_RNO[1]        ORCALUT4     Z        Out     1.017      3.974 r     -
N_57325_i           Net          -        -       -          -           1
reg_A[1]            FD1S1AY      D        In      0.000      3.974 r     -
================================================================================


Path information for path number 3:
      Requested Period:                      3.303
    - Setup time:                            -0.089
    + Clock delay at ending point:           0.000 (ideal)
    + Estimated clock delay at ending point: 0.000
    = Required time:                         3.391

    - Propagation time:                      3.974
    - Clock delay at starting point:         0.000 (ideal)
    - Estimated clock delay at start point:  -0.000
    = Slack (critical) :                     -0.583

    Number of logic level(s):                6
    Starting point:                          reg_0_out[2] / Q
    Ending point:                            reg_A[2] / D
    The start point is clocked by            System [rising] on pin CK
    The end   point is clocked by            System [rising] on pin CK

Instance / Net                  Pin      Pin               Arrival     No. of
Name                Type        Name     Dir     Delay     Time        Fan Out(s)
--------------------------------------------------------------------------------
reg_0_out[2]        FD1S1AY     Q        Out     1.180     1.180 r     -
reg_0_out_c[2]      Net         -        -       -         -           5
reg_A_3_3_am[2]     ORCALUT4    C        In      0.000     1.180 r     -
reg_A_3_3_am[2]     ORCALUT4    Z        Out     1.017     2.197 r     -
reg_A_3_3_am[2]     Net         -        -       -         -           1
reg_A_3_3[2]        PFUMX       BLUT     In      0.000     2.197 r     -
reg_A_3_3[2]        PFUMX       Z        Out     -0.033    2.164 r     -
reg_A_3_3[2]        Net         -        -       -         -           1
reg_A_3_7[2]        L6MUX21     D0       In      0.000     2.164 r     -
reg_A_3_7[2]        L6MUX21     Z        Out     0.265     2.428 r     -
reg_A_3_7[2]        Net         -        -       -         -           1
reg_A_3_15[2]       L6MUX21     D0       In      0.000     2.428 r     -
reg_A_3_15[2]       L6MUX21     Z        Out     0.265     2.693 r     -
reg_A_3_15[2]       Net         -        -       -         -           1
reg_A_3_31[2]       L6MUX21     D0       In      0.000     2.693 r     -
reg_A_3_31[2]       L6MUX21     Z        Out     0.265     2.957 r     -
reg_A_3[2]          Net         -        -       -         -           1
reg_A_RNO[2]        ORCALUT4    C        In      0.000     2.957 r     -
reg_A_RNO[2]        ORCALUT4    Z        Out     1.017     3.974 r     -
N_54314_i           Net         -        -       -         -           1
reg_A[2]            FD1S1AY     D        In      0.000     3.974 r     -
================================================================================


Path information for path number 4:
      Requested Period:                      3.303
    - Setup time:                            -0.089
    + Clock delay at ending point:           0.000 (ideal)
    + Estimated clock delay at ending point: 0.000
    = Required time:                         3.391

    - Propagation time:                      3.974
    - Clock delay at starting point:         0.000 (ideal)
    - Estimated clock delay at start point:  -0.000
    = Slack (critical) :                     -0.583

    Number of logic level(s):                6
    Starting point:                          reg_0_out[3] / Q
    Ending point:                            reg_A[3] / D
    The start point is clocked by            System [rising] on pin CK
    The end   point is clocked by            System [rising] on pin CK

Instance / Net                  Pin      Pin               Arrival     No. of
Name                Type        Name     Dir     Delay     Time        Fan Out(s)
--------------------------------------------------------------------------------
reg_0_out[3]        FD1S1AY     Q        Out     1.180     1.180 r     -
reg_0_out_c[3]      Net         -        -       -         -           5
reg_A_3_3_am[3]     ORCALUT4    C        In      0.000     1.180 r     -
```

```
reg_A_3_3_am[3]     ORCALUT4     Z        Out     1.017      2.197 r     -
reg_A_3_3_am[3]     Net          -        -       -          -           1
reg_A_3_3[3]        PFUMX        BLUT     In      0.000      2.197 r     -
reg_A_3_3[3]        PFUMX        Z        Out     -0.033     2.164 r     -
reg_A_3_3[3]        Net          -        -       -          -           1
reg_A_3_7[3]        L6MUX21      D0       In      0.000      2.164 r     -
reg_A_3_7[3]        L6MUX21      Z        Out     0.265      2.428 r     -
reg_A_3_7[3]        Net          -        -       -          -           1
reg_A_3_15[3]       L6MUX21      D0       In      0.000      2.428 r     -
reg_A_3_15[3]       L6MUX21      Z        Out     0.265      2.693 r     -
reg_A_3_15[3]       Net          -        -       -          -           1
reg_A_3_31[3]       L6MUX21      D0       In      0.000      2.693 r     -
reg_A_3_31[3]       L6MUX21      Z        Out     0.265      2.957 r     -
reg_A_3[3]          Net          -        -       -          -           1
reg_A_RNO[3]        ORCALUT4     C        In      0.000      2.957 r     -
reg_A_RNO[3]        ORCALUT4     Z        Out     1.017      3.974 r     -
N_54313_i           Net          -        -       -          -           1
reg_A[3]            FD1S1AY      D        In      0.000      3.974 r     -
==============================================================================


Path information for path number 5:
      Requested Period:                       3.303
    - Setup time:                             -0.089
    + Clock delay at ending point:            0.000 (ideal)
    + Estimated clock delay at ending point:  0.000
    = Required time:                          3.391

    - Propagation time:                       3.974
    - Clock delay at starting point:          0.000 (ideal)
    - Estimated clock delay at start point:   -0.000
    = Slack (critical) :                      -0.583

    Number of logic level(s):                 6
    Starting point:                           reg_0_out[4] / Q
    Ending point:                             reg_A[4] / D
    The start point is clocked by             System [rising] on pin CK
    The end   point is clocked by             System [rising] on pin CK

Instance / Net                  Pin      Pin               Arrival     No. of
Name                Type        Name     Dir     Delay     Time        Fan Out(s)
------------------------------------------------------------------------------
reg_0_out[4]        FD1S1AY     Q        Out     1.180     1.180 r     -
reg_0_out_c[4]      Net         -        -       -         -           5
reg_A_3_3_am[4]     ORCALUT4    C        In      0.000     1.180 r     -
reg_A_3_3_am[4]     ORCALUT4    Z        Out     1.017     2.197 r     -
reg_A_3_3_am[4]     Net         -        -       -         -           1
reg_A_3_3[4]        PFUMX       BLUT     In      0.000     2.197 r     -
reg_A_3_3[4]        PFUMX       Z        Out     -0.033    2.164 r     -
reg_A_3_3[4]        Net         -        -       -         -           1
reg_A_3_7[4]        L6MUX21     D0       In      0.000     2.164 r     -
reg_A_3_7[4]        L6MUX21     Z        Out     0.265     2.428 r     -
reg_A_3_7[4]        Net         -        -       -         -           1
reg_A_3_15[4]       L6MUX21     D0       In      0.000     2.428 r     -
reg_A_3_15[4]       L6MUX21     Z        Out     0.265     2.693 r     -
reg_A_3_15[4]       Net         -        -       -         -           1
reg_A_3_31[4]       L6MUX21     D0       In      0.000     2.693 r     -
reg_A_3_31[4]       L6MUX21     Z        Out     0.265     2.957 r     -
reg_A_3[4]          Net         -        -       -         -           1
reg_A_RNO[4]        ORCALUT4    C        In      0.000     2.957 r     -
reg_A_RNO[4]        ORCALUT4    Z        Out     1.017     3.974 r     -
N_55105_i           Net         -        -       -         -           1
reg_A[4]            FD1S1AY     D        In      0.000     3.974 r     -
==============================================================================



##### END OF TIMING REPORT #####]

Timing exceptions that could not be applied

Finished final timing analysis (Real Time elapsed 0h:01m:17s; CPU Time elapsed 0h:01m:16s; Memory used current: 298MB peak: 306MB)


Finished timing report (Real Time elapsed 0h:01m:17s; CPU Time elapsed 0h:01m:16s; Memory used current: 298MB peak: 306MB)

----------------------------------------
Resource Usage Report
Part: lcmxo3l_6900c-5

Register bits: 0 of 54912 (0%)
Latch bits:      4480
PIC Latch:       0
I/O cells:       8766


Details:
FD1S1AY:        4480
GSR:            1
IB:             164
L6MUX21:        2688
```

```
OB:             8602
ORCALUT4:       10734
PFUMX:          3072
PUR:            1
VHI:            1
VLO:            1
Mapper successful!

At Mapper Exit (Real Time elapsed 0h:01m:17s; CPU Time elapsed 0h:01m:16s; Memory used current: 122MB peak: 306MB)

Process took 0h:01m:17s realtime, 0h:01m:16s cputime
# Thu Nov 30 16:16:22 2023

############################################################]
```