Laboratory 03: Clock Control Module CLKCTRL and Software Delays

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Questions 1. Explain why you got the waveform you did at CLKOUT when you compiled and ran the program clk_per_to_clkout with the optimization level at -O0.

The waveform stayed low the whole time because at -O0 there are too many assembly instructions created after the unlocking of the protected registers, this means that the protected registers relock before the code gets a chance to change them, so the clock is never properly set

2. Explain your strategy for determining whether changing CLK_OUT (or CLK_PER) using the Main Clock Prescaler also changes CLK_CPU. What was your determination as to the independence or dependence of these two clocks?

Our strategy was to measure both CLK_OUT and CLK_CPU before and after changing the prescaler, this way we could see if only one of them or if both of them would change indicating if they are connected or not

3. Can you tell from the data you took in Task 3 whether either the percent error or the absolute error stay the same as you change the argument of the delay function for the different toggle times. Please explain your answer.

The percent error stayed the same, as each of the periods were exactly double each other, this means that the error will scale with the delay

4. In Design Task 1 you had to configure the CLKCTRL module to generate a 1 MHz output at CLKOUT. Briefly describe two different ways that you could do this.

You could do this by prescaling the CLK_OUT to divide by 4, as the true frequency of the cpu is 4Mhz, or you could change the frequency of the oscillator to be 2^0 MHz (1MHz)

5. Briefly explain how you could, in software, improve the accuracy of the output in Laboratory Task 4. Would this solution work in production when you are going to manufacture 1,000,000 copies of the system? Explain

You could measure the error of the system and toggle the delays to be more accurate, however this would not be scalable to 1,000,000 copies as this would have to be customized for every chip