DEPARTMENT OF COMPUTER ENGINEERING
SECOND SEMESTER IA 2023/2024
CPEN 202 DIGITAL SYSTEMS DESIGN

INSTRUCTION: Answer All Questions
TIME ALLOWED: Two and Half (2½) Hours.

Q1. (a) Draw a flow chart for a basic digital hardware design unit. ---- [3 marks]

(b) Briefly explain the development cycle using the flow chart ---------- [2 marks]

(c) A company has four directors A, B, C, D. The percentage of shares held by them are 35%, 30%, 25% and 10% respectively. Their voting power is proportional to shares they hold. Any major decision taken must have a support of 60% or above the stock.

(i) Design a suitable logic circuit to implement the voting system ---------- [8marks]

(ii) List all the steps or procedures used to design the logic circuit ---------- [2marks]

(d) Write VHDS code to realize the logic circuit ---------- [5marks]

Q2. (a) Draw a graphical ~~diagram~~ symbol (block diagram) and a truth table of 3-to-8 line decoder ---------- [3 marks]

(b) Use the truth table to explain the function of the decoder ---------- [6 marks]

(c) With a aid of a logic diagram and truth table of an ~~two~~ input comparator write the Boolean expression. [6 marks]

(d) Briefly explain how it works - [3 marks]

(e) Give two applications of a three state logic device ---------- [2 marks]

Q3 (a) With the aid of a circuit diagram, briefly explain how binary parallel addition of an output of two shift register A and B ~~fed~~ with data 0111 and 1001 respectively, fed into could four (4) full adders which are connected in parallel, be added ---------- [10 marks]

(b) Give one advantage of binary parallel addition over serial mode of addition - [2 marks]

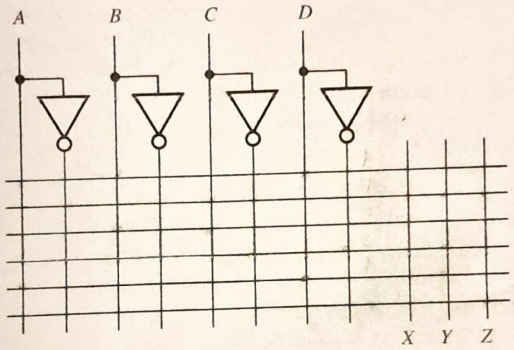
(c) Give the binary data that will appear at the output of the third register connected to the output of the parallel full adders ---- [8 marks]

Q4 (a) Give two advantages of Programmable logic device (PLD) over the conventional IC's with fixed parts - - - - - - - - - - [5 marks]

(b) State the main structural difference between Programmable logic array (PLA) and programmable array logic (PAL) device - - - - - - - - - - [5 marks]

(c) The PLA below will be used to implement the following equations:

$$X = ABD + A'C' + BC + C'D'$$
$$Y = A'C' + AD + C'D'$$
$$Z = CD + A'C' + AB\,D$$



(a) Indicate the connections that will be made to program the PLA to imple- - [10 marks]

Q5 (a) Draw a block diagram of a digital controlled Multiplex and briefly explain how it works [5 marks]

(b) If the input signals to Multiplexer are labelled A, B, C, D the input control signal E, F and the desired output line as Y

(i) Draw the truth table of the Multiplexer and use it to explain the conditions under which the input B will be selected and place in the output [8 marks]

(ii) Write the logic equation for the 1-to-4 multiplexer - - - - - - - - - - [5 marks]

(c) Give one practical areas where the multiplexer could be used - - - - - [2 marks]