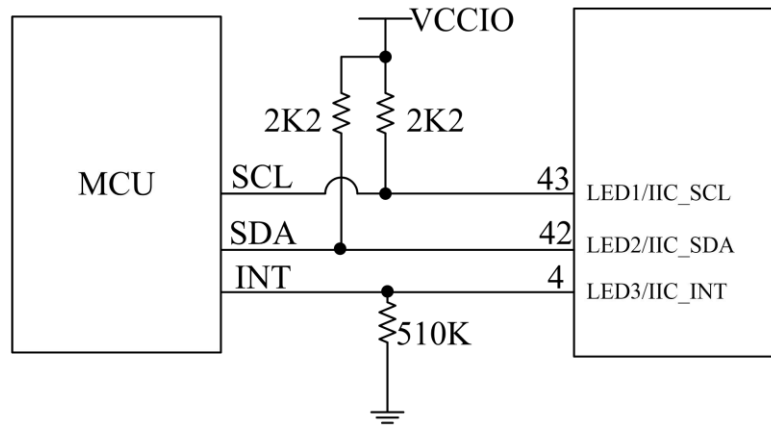# 1   Typical application description
1.1   I2C connection method

IP2368 can be used as a slave device. The MCU can read or set the voltage, current, power and other information of IP2368 through the I2C interface. The connection method of IP2368I2C is as follows:

VCCIO

MCU

2K2   2K2

SCL   43   LED1/IIC_SCL
SDA   42   LED2/IIC_SDA
INT   4   LED3/IIC_INT

510K

1.2   I2C Precautions

- IP2368 I2C device address: written as 0xEA, read as 0xEB. If you need to set it to another address, you can customize it;
- The I2C communication voltage of IP2368 is 3.3V. If the MCU terminal is 5V voltage, you need to add a level conversion chip to 3.3V;
- IP2368 INT application description: IP2368 will wake up when it detects that INT is high during sleep. After waking up, IP2368 actively pulls up INT. After 100ms, the MCU can perform I2C communication and register read and write operations; Before IP2368 enters sleep, it will switch to the input high resistance to detect the INT state. If it is high, it is considered that the MCU does not allow IP2368 to enter sleep, if it is low, then IP2368 enters sleep; after the MCU detects that INT is low, 16ms to stop accessing the IC;
- The I2C of IP2368 supports a maximum communication frequency of 250k. Considering the clock deviation, it is recommended that the MCU's I2C communication clock use 100k-200k;
- If you want to modify the value of a register in IP2368, you need to read out the value of the corresponding register first, and then after the bit that needs to be modified is summed or calculated, the calculated value is written to the register. Other unopened registers cannot be modified at will. The default value of the register is subject to the read value. The default value of different ICS may be different;
- IP2368 I2C communication is real-time data. After receiving the request, it needs to be interrupted for data preparation. The preparation time is long, so when the MCU communicates with I2C, it needs to determine whether the ACK is received after sending the address and increase the delay by 50us (refer to the I2C application example); it is recommended to read a single byte, 100k I2C communication frequency, and increase the delay by 1ms between each byte;
- At the end of the I2C read data, after the last byte is read, a NACK signal must be given, otherwise IP2368 will think that the data is still being read, and the next clock will continue to output the next data, resulting in the STOP signal cannot be received, and the last read error;
- Reserved registers cannot write data at will, and the original value cannot be changed, otherwise unexpected results will occur. The operation of the register must be carried out in accordance with read-modify-write, only the bits to be used are modified, and the values of other unused bits cannot be modified;
- This document is only for IP2368_I2C_COUT/IP2368_I2C_NACT models, other models are invalid;

1.3   I2C application example

After the IP2368 INT pin continues to be high for 100ms, the MCU can perform I2C communication. You can initialize the register first (only modify the register when you need to modify special functions, if you don't need to modify, you cannot write the register); then read the internal information of IP2368 (power, charge and discharge status, button status); and finally perform special operations (such as special indicators, charge and discharge management, fast charge request management); after the MCU detects that the INT is low, it needs to stop accessing I2C within 16ms.
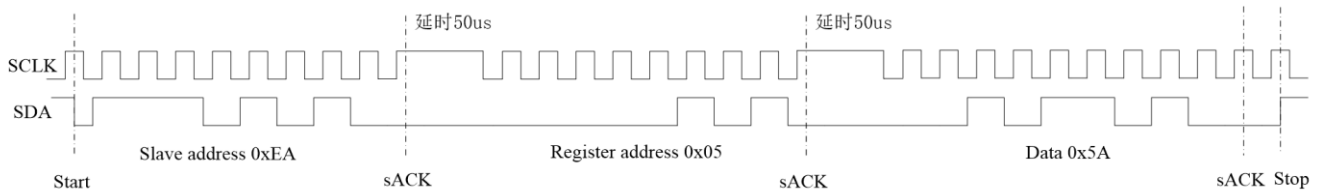For example:

Write data 0x5A to 0x05 register

Figure 1: I2C Write 0x05

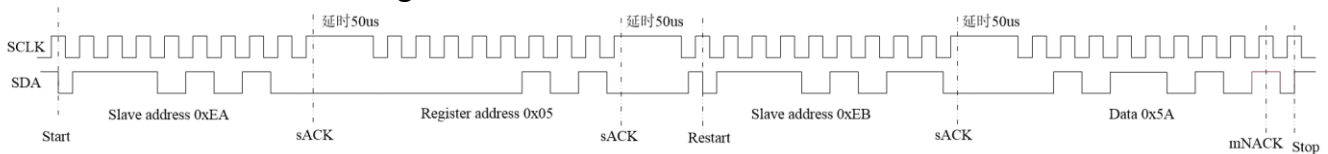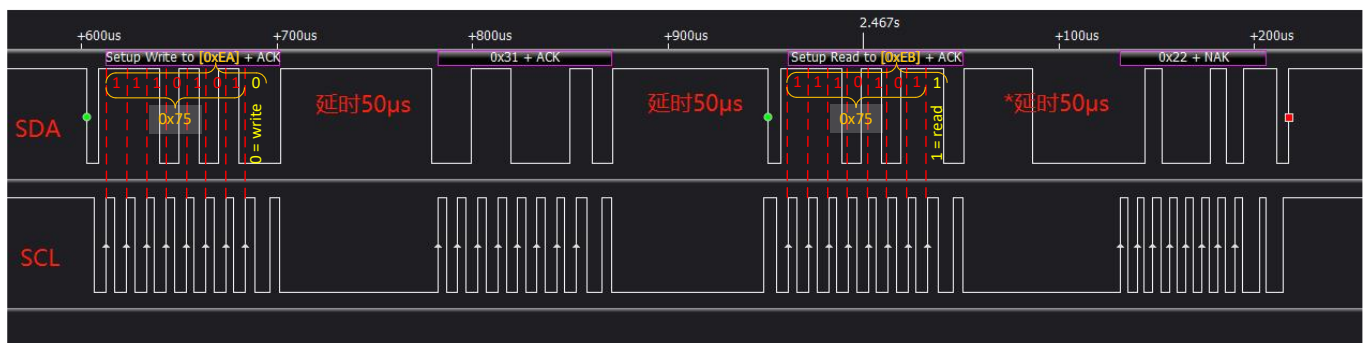**Read data from 0x05 register**

Figure 2: I2C Read 0x05

Actually, read back data from the 0x31 register:

Figure 3: I2C Read 0x31

2   Register list:

2.1   Read/write operation register

[0x00] SYS_CTL0 (charge enable register)

Bit(s)	Name	Description	R/w	rst
7	En_LOADOTP	Enable reset the register value after boot or wake up: 0: Do not reset the register value 1: Reset the register value again It is not recommended to modify this bit to 0. If it needs to be modified, the software needs to reset the default value of the register regularly, such as after the VINOk VBUOk signal is triggered.	R/W	1
6	En_RESETMCU	MCU reset register Write 1: Reset the register to the default value, after reset, the bit will automatically return to 0	R/W	0
5	En_INT_low	When there is an exception, the INT is pulled down by 2MS, indicating that the MCU has an exception. 1: Enable 0: disable	R/W	0
4	En_Vbus_SinkDPdM	Type-C port input DM DP fast charge is enabled 1: Enable 0: disable	R/W	1
3	En_Vbus_SinkPd	Type-C port input PD fast charge is enabled 1: Enable 0: disable	R/W	1
2	En_Vbus_SinkSCP	Type-C port input SCP fast charge is enabled 1: Enable 0: disable	R/W	1
1	En_Vbus_Sinkctrl	Type-C port MOS input is enabled 1: Enable, open C port MOS 0: disable, close C port MOS	R/W	1
0	En_Charger	Charger Charging is enabled (not configurable after shutdown) 1: Enable 0: disable	R/W	1

[0x01] SYS_CTL1 (series number setting, battery type, current setting mode)

Bit(s)	Name	Description	R/w	rst
7:4	*Reserved*			
3	En_BATmode_set	Set the battery type to enable (the battery type is set by register 0x01[2]) 1: Enable, it is allowed to set the battery type 0: disable, it is not allowed to set the battery type	R/W	0
2	Set_BATmode	Battery type setting 0: Lithium iron phosphate battery, single battery trickle to constant current voltage 2.5V, full voltage is about 3.6V 1: Ordinary lithium battery, single battery trickle to constant current voltage of 3.0V, full voltage of about 4.2V	R/W	1
1	En_Isetmode_set	select current setting mode enable 1: Enable, allow current selection Setting mode 0: disable, it is not allowed to select the current setting mode	R/W	0
0	Set_Isetmode	select the current setting mode (current and power register 0x03 [6:0]) 0: Iset sets the battery terminal current 1: Iset sets the input terminal power	R/W	1

[0x02] SYS_CTL2 (Vset full charge voltage setting)

Bit(s)	Name	Description	R/w	rst
7	En_Vset_set	Set the full voltage to enable 1: Enable, it is allowed to set 0: Disable, it is not allowed to set the full voltage to the full voltage	R/W	0
6:0	Vset	Full voltage setting	R/W	0x0A

| | | In lithium iron phosphate battery mode (0x01[2]=0), the full voltage of a single battery Vset=N*10+3500mV (up to 3.7V)
In normal lithium battery mode (0x01[2]=1), the full voltage of a single battery Vset=N*10+4000mV (up to 4.4V) | | |

[0x03] SYS_CTL3 (Iset charging power or current setting)

Bit(s)	Name	description	R/w	rst
7	En_Iset_set	Set the charging power or current to enable 1: Enable, allow the charging power or current to be set 0: disable, do not allow the charging power or current to be set	R/W	0
6:0	Iset	Battery terminal current or power setting. When set to battery terminal current (0x01[0]=0), battery terminal current Iset=N*100mA (maximum 5A) When set to the charging input power mode (0x01[0]=1), the set charging power Pmax=N*1W (maximum charging is 100W)	R/W	0x3C

[0x04] SYS_CTL4 (battery capacity setting)

Bit(s)	Name	Description	R/w	rst
7	En_FCAP_set	Setting the battery capacity function enables 1: Enable, allowing setting the battery capacity 0: disable, not allowing setting the battery capacity	R/W	0
6:0	Fcap	Battery capacity FCAP=N*200mAh	R/W	0x28

[0x06] SYS_CTL6 (current battery power)

Bit(s)	Name	Description	R/w	rst
7:0	Cap_Now	Current power (read and write) Cap_Now=N	R/W	x

[0x07] SYS_CTL7 (trickle charging current, threshold, and charging timeout settings)

Bit(s)	Name	Description	R/w	rst
7:4	Itk	trickle charging current setting *(maximum trickle charging current 400ma)* Itk=N*50mA	R/W	0x04
3:2	Vtk	single battery trickle to constant current charging voltage threshold when set to lithium iron phosphate mode (0x01[2]=0) 00:2.3V 01:2.4V 10:2.5V 11:2.6V When set to normal lithium battery mode(0x01[2]=1) 00:2.8V 01:2.9 V 10:3.0 V 11:3.1V	R/W	10
1:0	Charge_OT	Charging timeout setting 00: disable, there is no charging timeout function 01:24h 10:36h 11:48h	R/W	0x02

[0x08] SYS_CTL8 (stop charging current and recharge threshold setting)

Bit(s)	Name	Description	R/w	rst
7:4	Istop	stop charging Charging current setting Istop=N*50mA	R/W	0x02
3:2	Vrch	recharging threshold 00: There is no recharging function after full charge 01: VTRGT-N*0.05 10: VTRGT-N*0.1 11: VTRGT-N*0.2 VTRGT–full charge voltage N–Number of battery cells in series	R/W	0x02
1:0	*Reserved*			

[0x09] SYS_CTL9 (standby enable and low voltage setting)

Bit(s)	Name	Description	R/w	rst
7	En_Standby	standby enable 1: Enable 0: Do not enable	R/W	1
6	En_BATlow_Set	Battery low voltage setting enable (battery voltage setting register 0x0A) 0: disable 1: Enable	R/W	0
5	En_BAT_Low	Turn off the battery. Low voltage Shutdown function 0: disable 1: Enable	R/W	0
4:0	*Reserved*			

[0x0A] SYS_CTL10 (battery low voltage setting)

Bit(s)	Name	Description	R/w	rst
7:5	Set_BATlow	Battery low voltage setting 000: Lithium battery 2.80 V*N /Lithium iron battery 2.3 V*N 001: Lithium battery 2.90 V*N /Lithium iron battery 2.4 V*N 010: Lithium battery 3.00 V*N /Lithium iron battery 2.5 V*N 011: Lithium battery 3.10V*N/Lithium iron battery 2.6 V*N 100: Lithium battery 3.20 V*N/Lithium iron battery 2.7 V*N N: Number of battery cells in series	R/W	0x02
4:0	*Reserved*			

[0x0B] SYS_CTL11 (output enable register)

Bit(s)	Name	Description	R/w	rst
7	En_Dc_Dc_Output	Discharge output is enabled (not output after shutdown) 1: Enable 0: Do not enable	R/W	1
6	En_Vbus_Src_DP_dM	C port output DP/DM fast charge is enabled 1: Enable 0: Disable	R/W	1
5	En_Vbus_SrcPd	C Port output PD fast charge is enabled 1: Enable 0: disable	R/W	1
4	En_Vbus_SrcSCP	C port output SCP fast charge is enabled 1: Enable 0: disable	R/W	1
3:0	*Reserved*			

[0x0C] SYS_CTL12 (output maximum power selection register)

Bit(s)	Name	Description	R/w	rst
7:5	Vbus_Src_Power	Vbus1 Output power selection: 000:20W 001:25W 010:30WW 011:45W 100:60W 101:100W	R/W	0x05
4:0	*Reserved*			

100W requires an Emark recognition circuit.

[0x22] TypeC_CTL8 (TYPE-C mode control register)

Bit(s)	Name	Description	R/w	rst
7:6	Vbus_Mode_Set	Vbus CC mode selection 00: UFP: Upstream Facing Port (device connected as a consumer) 01: DFP: Downstream Facing Port (device connected as a power source) 11: DRP: Dual Role Port (device can act as both a source and a consumer)	R/W	0
5:0	*Reserved*			

[0x23] TypeC_CTL9 (output Pdo current setting register)

Bit(s)	Name	Description	R/W	rst
7	En_5VPdo_3A/2.4 A	5VPdo current setting 1: 3A 0: 2.4 A	R/W	1
6	En_Pps2Pdo_Iset	Pps2 Pdo current set enable 1: Enable 0: disable * After enabling, the output power and overcurrent are subject to the set Pdo current, and the overcurrent is 1.1 times the set Pdo current.	R/W	0
5	En_Pps1Pdo_Iset	Pps1 Pdo current set enable 1: Enable 0: disable * After enabling, the output power and overcurrent are subject to the set Pdo current, and the overcurrent is 1.1 times the set Pdo current.	R/W	0
4	En_20VPdo_Iset	20VPdo current set enable 1: Enable 0: disable * After enabling, the output power and overcurrent are subject to the set Pdo current, and the overcurrent is 1.1 times the set Pdo current.	R/W	0
3	En_15VPdo_Iset	15VPdo current set enable 1: Enable 0: disable * After enabling, the output power and overcurrent are subject to the set Pdo current, and the overcurrent is 1.1 times the set Pdo current.	R/W	0
2	En_12VPdo_Iset	12VPdo current set enable 1: Enable 0: disable * After enabling, the output power and overcurrent are subject to the set Pdo current, and the overcurrent is 1.1 times the set Pdo current.	R/W	0
1	En_9VPdo_Iset	9VPdo current set enable 1: Enable 0: disable * After enabling, the output power and overcurrent are subject to the set Pdo current, and the overcurrent is 1.1 times the set Pdo current.	R/W	0
0	En_5VPdo_Iset	5VPdo current set enable 1: Enable 0: disable	R/W	0

[0x24] TypeC_CTL10 (5VPdo current setting register)

Bit(s)	Name	Description	R/W	rst
7:0	5VPdo_Iset	5VPdo current setting 5VPdo=20mA*N (default 3A,Max=3A)	R/W	0x96

[0x25] TypeC_CTL11 (9VPdo current setting register)

Bit(s)	Name	Description	R/W	rst
7:0	9VPdo_Iset	9VPdo current setting 9VPdo=20mA*N (default 3A,Max=3A)	R/W	0x96

[0x26] TypeC_CTL12 (12VPdo current setting register)

Bit(s)	Name	Description	R/W	rst
7:0	12VPdo_Iset	12VPdo current setting 12VPdo=20mA*N (default 3A,Max=3A)	R/W	0x96

[0x27] TypeC_CTL13 (15VPdo current setting register)

Bit(s)	Name	Description	R/W	rst
7:0	15VPdo_Iset	15VPdo current setting 15VPdo=20mA*N (default 3A,Max=3A)	R/W	0x96

[0x28] TypeC_CTL14 (20VPdo current setting register)

Bit(s)	Name	Description	R/W	rst
7:0	20VPdo_Iset	20VPdo current setting 20VPdo=20mA*N (Default is 5A, emark needs to be recognized, Max=5A) if emark is not recognized, 3A	R/W	0xFA

[0x29] TypeC_CTL23 (Pps1 Pdo current setting register)

Bit(s)	Name	Description	R/W	rst
7:0	Pps1Pdo_Iset	Pps1 Pdo current setting Pps1 Pdo=50mA*N (Default is 5A, emark needs to be recognized, Max=5A) if emark is not recognized, 3A	R/W	0x3C

[0x2A] TypeC_CTL24 (Pps2 Pdo current setting register)

Bit(s)	Name	Description		rst
7:0	Pps2Pdo_Iset	Pps2 Pdo current setting Pps2 Pdo=50mA*N (Default is 5A, emark needs to be recognized, Max=5A) if emark is not recognized, 3A	R/W	0x3C

[0x2B] TypeC_CTL17 (output Pdo setting register)

Bit(s)	Name	Description	R/w	rst
7	Reserved		R	R
6	En_Src_Pps2Pdo	Pps2 Pdo is enabled 1: Enable 0: disable * There is no Pps Pdo after disable	R/W	1
5	En_Src_Pps1Pdo En_Src_Pps1Pdo	Pps1 Pdo is enabled 1: Enable 0: disable * There is no Pps1 Pdo after disable	R/W	1
4	En_Src_20VPdo	20VPdo enable 1: Enable 0: disable * There is no 20V Pdo after disable	R/W	1
3	En_Src_15VPdo	15VPdo enable 1: Enable 0: disable * There is no 15V Pdo after disable	R/W	1
2	En_Src_12VPdo	12VPdo enable 1: Enable 0: disable * There is no 12V Pdo after disable	R/	WW 1
1	En_Src_9VPdo	9VPdo is enabled 1: Enable 0: disable * There is no 9V Pdo after disable	R/W	1
0	Reserved		R	R

2.2 Read-only status indication register

[0x30] SOC_CAP_DATA (battery level data register)

Bit(s)	Name	Description	R/W	rst
7:0	Soc_Cap	cell percentage power Data (%) Soc Cap=N	R	X

[0x31] STATE_CTL0 (state of charge control register)

Bit(s)	Name	Description	R/W	rst
7: 6	*Reserved*		*R*	*X*
5	CHG_En	charging flag 1: Charging state (VbusOk means charging state) 0: Non-charging state	R	X
4	CHG_End	full state flag 1: fully charged 0: charged not fully	R	X
3	Output_En	discharge state Flag 1: Discharge state and the output port has been opened, there is no abnormality 0: Discharge state, the output is not turned on or there is an abnormal discharge	R	X
2:0	Chg_state	Chg state 000: Standby 001: Trickle 010: Constant current charging 011: Constant voltage charging 100: Charging is waiting (including when charging is not turned on, etc.) 101: Full state 110: Charging timeout	R	X

[0x32] STATE_CTL1 (state of charge control register)

Bit(s)	Name	Description	R/w	rst
7:6	Chg_State	Chg state 00: 5V input charging 01: High voltage input fast charging	R	X
5:0	*Reserved*		*R*	*X*

[0x33] STATE_CTL2 (input Pd status control register)

Bit(s)	Name	Description	R/w	rst
7	Vbus_Ok	Vbus Ok 1: Vbus has power 0: Vbus has no power	R	X
6	Vbus_Ov	Vbus Ov 1: Vbus input overvoltage 0: Vbus input without overvoltage	R	X
5:3	*Reserved*			*X*
2:0	Chg_Vbus	charging voltage 111: 20V Charging 110: 15V charging 101: 12V charging 100: 9V charging 011: 7V charging 010: 5V charging	R	X

[0x34] TypeC_STATE (system status indication register)

Bit(s)	Name	Description	R/w	rst
7	Sink_Ok	Type-C Sink Input connection flag 1: Valid 0: Invalid	R	X
6	Src_Ok	Type-C Src output connection flag 1: Valid 0: Invalid	R	X

5	Src_Pd_Ok Src_Pd_Ok	Src_Pd_Ok Output connection flag 1: Valid 0: Invalid	R	X
4	Sink_Pd_Ok	Sink Pd Ok input connection flag 1: Valid 0: Invalid	R	X
3	Vbus_Sink_Qc_Ok	input fast charge valid flag Qc5Vand Pd5V are not counted as fast charge Ok 1: Valid 0: Invalid	R	X
2	Vbus_Src_Qc_Ok	output fast charge valid flag Qc5V and Pd5V are not counted as fast charge Ok 1: Valid 0: Invalid	R	X
1:0	Reserved			

[0x35] MOS_STATE (input MOS status indication register)

Bit(s)	Name	Description	R/w	rst
7	7Reserved		R	X
6	Vbus_Mos_State	Vbus port input MOS state 0: Closed state 1: Open state	R	X
5:0	Reserved		R	X

[0x38] STATE_CTL3 (system overcurrent indication register)

Bit(s)	Name	Description	R/w	rst
7:6	Reserved		R	X
5	Vsys_Oc	Vsys outputs the overcurrent flag, you need to write 1 to clear 0 1: Vsys output has a trigger overcurrent signal 0: Vsys output does not trigger overcurrent signal The system continuously detects more than two overcurrent states within 600mS and considers the overcurrent to be valid, and positions this flag at 1. The external master can read this flag to determine whether there is an abnormal overcurrent; from the occurrence of the overcurrent state to the system sleep, the time is about 1.5s, and this flag will remain at 1 after sleep, so the external master needs to read the flag within this time and make corresponding processing, and then write 1 to clear the flag to 0; if you need to judge that the overcurrent state is revoked, you need to reopen the output port (register 0x22[7] First write 0 Write 1 again), and then read the status flag.	R	X
4		Vsys output short circuit flag, need to write 1 to clear 0 1: Vsys output has a trigger short circuit signal 0: Vsys output does not trigger a short circuit signal The system continuously detects more than two short-circuit states within 600mS and considers the short-circuit to be valid, and positions this flag at 1. The external master can read this flag to determine whether there is an abnormal short-circuit; from the short-circuit state to the system sleep, the time is about 1.5s, after sleep, this flag will be maintained at 1, so the external master needs to read the flag within this time and make corresponding processing, and then write 1 to clear the flag to 0; if you need to judge that the short-circuit state is revoked, you need to reopen the output port (register 0x22[7] first write 0 and then write 1), Then read the status flag.	R	X
3:0	Reserved		R	

[0x50] BATVADC_DAT0 (VBAT voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	BATVADC[7:0]	Low 8bit of BATVADC data Voltage of VBATPIN	R	X

[0x51] BATVADC_DAT1 (VBAT voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	BATVADC[15:8]	High 8bit of BATVADC data Voltage of VBATPIN VBAT=BATVADC (mV)	R	X

[0x52] VsysVADC_DAT0 (Vsys voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VsysVADC[7:0]	Low 8bit Vsys voltage data Voltage of VsysPIN	R	X

[0x53] VsysVADC_DAT1 (Vsys voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VsysVADC[15:8]	Vsys voltage data high 8bit VsysPIN voltage Vsys=VsysVADC (mV)	R	X

[0x54] IVbus_Sink_IADC_DAT0 (input current register)

Bit(s)	Name	Description	R/w	rst
7:0	IVbus_ADCADC[7:0]	The current of the low 8bit Vbus input of the charging input current data	R	X

[0x55] IVbus_Sink_IADC_DAT1 (input current register)

Bit(s)	Name	Description	R/W	rst
7:0	IVbusADC[15:8]	The current of the high 8-bit Vbus input of the charging input current data Iin=IVbusADC(mA)	R	X

When charging, the current is stored in 0X54 and 0x55．0x31 register bit5 is the charging flag.

[0x56] IVbus_Src_IADC_DAT_Src_IADC_DAT0 (output current register)

Bit(s)	Name	Description	R/w	rst
7:0	IVbus_ADCADC[7:0]	Discharge output current data of the low 8bit Vbus output current	R	X

[0x57] IVbus_Src_IADC_DAT1 (output current register)

Bit(s)	Name	Description	R/W	rst
7:0	IVbusADC[15:8]	Discharge output current data of the high 8-bit Vbus output current Iout=IVbusADC (mA)	R	X

When discharging, the current is stored in 0X56 and 0x57．0x31 register bit3 is the discharge flag.

[0x6E] IBATIADC_DAT0 (BAT terminal current register)

Bit(s)	Name	Description	R/W	rst
7:0	IBATIADC[7: 0]	Battery terminal current Low 8bit	R	

[0x6F] IBATIADC_DAT1 (BAT terminal current register)

Bit(s)	Name	Description	R/W	rst
7:0	IBATIADC[15:8]	Cell terminal current high 8bits of BATIADC data IBAT=IBATIADC(mA)	R	X

[0x70] ISYS_IADC_DAT0 (IVsys terminal current register)

Bit(s)	Name	Description	R/W	rst
7:0	ISYSIADC[7:0]	IVsys terminal current VsysIADCV data low 8bit	R	X

[0x71] IVsys_IADC_DAT1 (IVsys terminal current register)

Bit(s)	Name	Description	R/W	rst
7:0	IVsysIADC[15:8]	IVsys terminal current High 8bits of VsysIADCV data IVsys= IVsysIADC (mA)	R	X

[0x74] Vsys_POW_DAT0 (Vsys terminal power register)

Bit(s)	Name	Description	R/W	rst
7:0	Vsys_POW_ADC[7:0]	Vsys terminal power ADC data low 8bit	R	X

[0x75] Vsys_POW_DAT1 (Vsys terminal power register)

Bit(s)	Name	Description	R/W	rst
7:0	Vsys_POW_ADC[15:8]	Vsys terminal power ADC data in 8bits	R	X

[0x76] Vsys_POW_DAT2 (Vsys terminal power register)

Bit(s)	Name	Description	R/W	rst
7:0	Vsys_POW_ADC[7: 0]	Vsys terminal power ADC data high 8bit Vsys_POW = Vsys_POW_ADC(mW)	R	X

[0x77] INTC_IADC_DAT0 (NTC output current register)

Bit(s)	Name	Description	R/w	rst
7	NTC_IADC_DAT	0: Output 20uA 1: output 80uA	R	X
6:0	Reserved			X

[0x78] VGPIO0_NTC_DAT0 (VGPIO0_NTC_ADC voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VGPIO0_DAT0[7:0]	VGPIO0 ADC data low 8bit	R	X

[0x79] VGPIO0_NTC_DAT1 (VGPIO0_NTC_ADC voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VGPIO0_DAT1 [15:8]	High0 ADC8High 8bits of VGPIO 0 ADC data0 VGPIO0 DAT=VGPIO0 ADC (mV)(0~3.3V)	R	X

[0x7A] VGPIO1_Iset_DAT0 (VGPIO1_Iset_ADC voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VGPIO1_DAT0[7:0]	VGPIO1 ADC data low 8bit	R	X

[0x7B] VGPIO1_Iset_DAT1 (VGPIO1_Iset_ADC voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VGPIO1_DAT1[15:8]	High1_ADC High 8bits of VGPIO 1_ADC data VGPIO1 VGPIO1 DAT=VGPIO11 ADC (mV)(0~3.3V)	R	X

[0x7C] VGPIO2_Vset_DAT0 (VGPIO2_Vset_ADC voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VGPIO2_DAT0[7: 0]	Low 8bit of VGPIO2 ADC data	R	X

[0x7D] VGPIO2_Vset_DAT1 (VGPIO2_Vset_ADC voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VGPIO2_DAT1[15:8]	High2 ADC8High 8bits of VGPIO 2 ADC data2 VGPIO2 DAT=VGPIO2 ADC (mV)(0~3.3V)	R	X

[0x7E] VGPIO3_FCAP_DAT0 (VGPIO3_FCAP_ADC voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VGPIO3_DAT0[7: 0]	Low 8bit of VGPIO3 ADC data	R	X

[0x7F] VGPIO3_FCAP_DAT1 (VGPIO3_FCAP_ADC voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VGPIO3_DAT1[15:8]	High3 High8bits of VGPIO 3 ADC 8data dataVGPIO3_DATDAT=VGPIOVGPIO3_ADCADC (mV)(0~3.3V)	R	X

[0x80] VGPIO4_BATNUM_DAT0 (VGPIO4_BATNUM_ADC voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VGPIO4_DAT0[7:0]	Low 8bit of VGPIO4_ADC data	R	X

[0x81] VGPIO4_BATNUM_DAT1 (VGPIO4_BATNUM_ADC voltage register)

Bit(s)	Name	Description	R/W	rst
7:0	VGPIO4_DAT0[15:8]	High4_ADC High 8bits of VGPIO 4_ADC data VGPIO3_DATDAT =VGPIO3_ADCADC (mV)(0~3.3V)	R	X

3   Version/revision history:

Version	date	Revision content	Draftsman/revision person
V1.00	2021-10-25	First version release	IT360
V1.60	2022-05-16	Modify the layout and description	IT360
V1.61	2022-07-13	Increase the VSYS power register to a high of 8 bits	IT360
V1.62	2022-09-13	Modify the system overcurrent indication register description	IT555
V1.63	2023-11-27	Modify the I2C application example, no delay is required to read data back	IT555