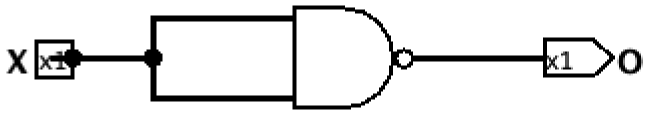
Assignment 1

Mission 1: Creating gates using NAND gates.

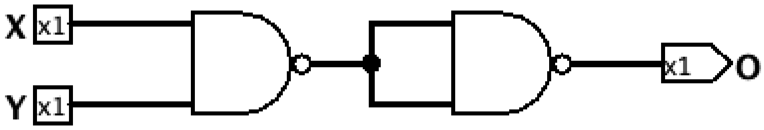
a) NOT gate Boolean Expression: $O = \overline{X.X} = \overline{X}$



NOT gate

X	O
0	1
1	0

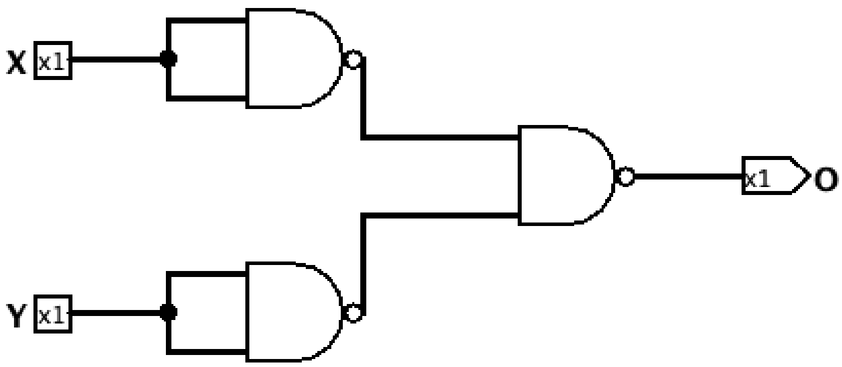
b) AND gate Boolean Expression: $O = \sim(\sim(X{\cdot}Y){\cdot}\sim(X{\cdot}Y)) = X.Y$



And gate

X	Y	O
0	0	0
0	1	0
1	0	0
1	1	1

c) OR gate Boolean Expression: $O = \sim(\sim(X \cdot X) \cdot \sim(Y \cdot Y)) = X + Y$



OR gate

X	Y	O
0	0	0
0	1	1
1	0	1
1	1	1

Mission 2 Making two-bit Half Adder:

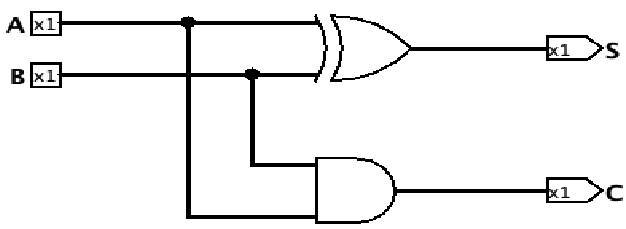
a) Truth Table:

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

b) Boolean Expression: $S = A \oplus B$

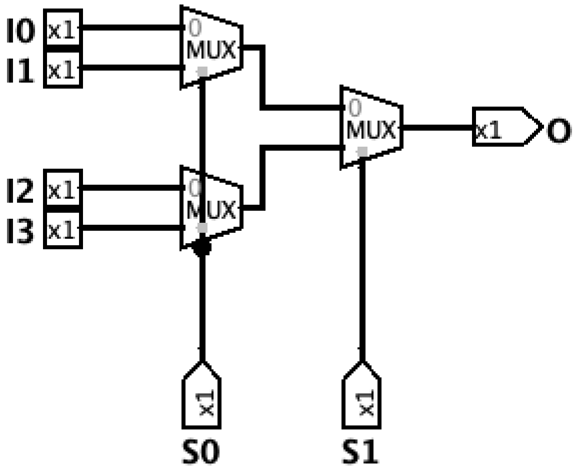
$C = A.B$

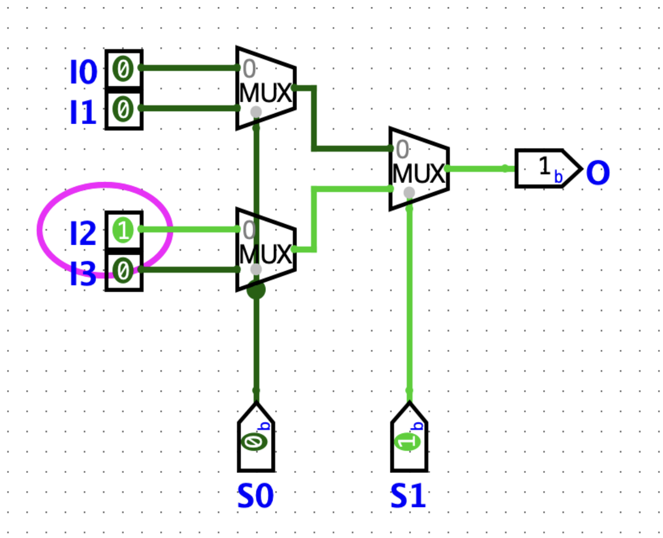
c) Circuit:



Mission 3 Building a Smart Selector:

Boolean Expression: $O = I3{\cdot}S0{\cdot}S1 + I2{\cdot}{\sim}S0{\cdot}S1 + I1{\cdot}S0{\cdot}{\sim}S1 + I0{\cdot}{\sim}S0{\cdot}{\sim}S1$





Mission 4: Pattern Detector

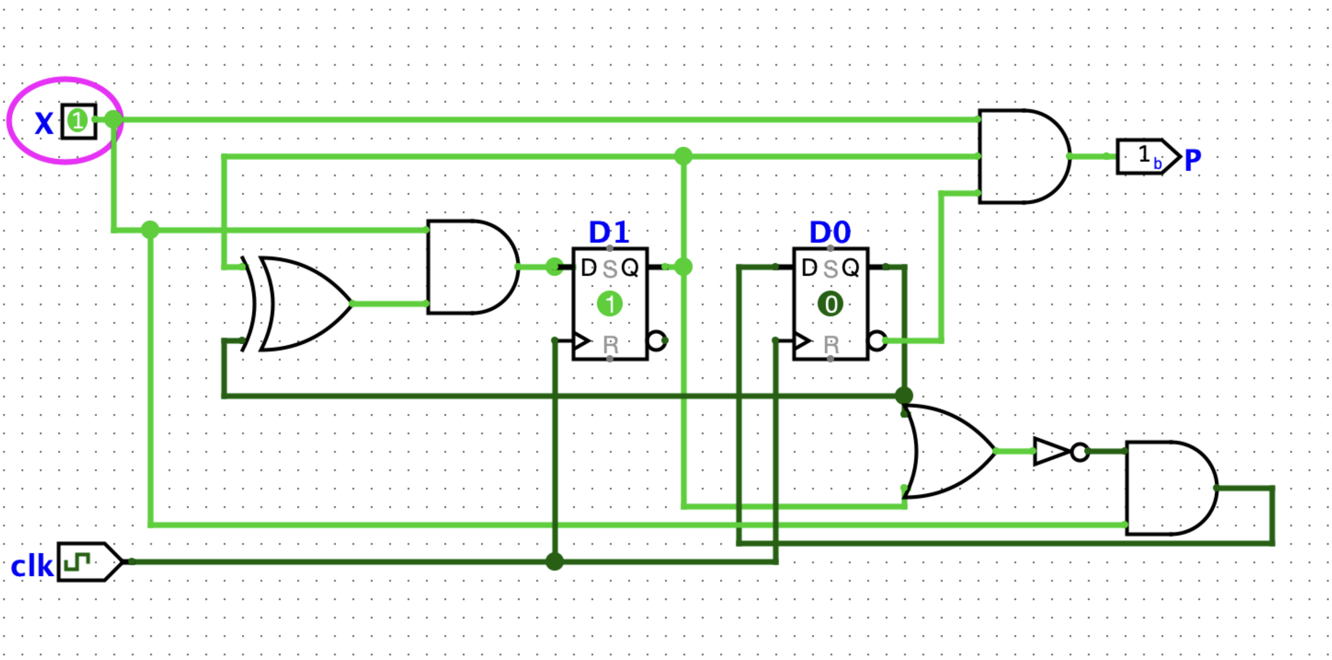
a) We will need 2 D flip-flops. Because in the state diagram(mealy/moore) of pattern recognition '111' , it will need 3 states (00,01,10). So to represent three different states, we will need 2 bits , thus 2 flip-flops.

Current State (Q_1Q_0)	**Input (X)**	**Next State (D_1D_0)**	**Output (P)**
S0 (00)	0	**S0** (00)	**0**
S0 (00)	1	**S1** (01)	**0**
S1 (01)	0	**S0** (00)	**0**
S1 (01)	1	**S2** (10)	**0**
S2 (10)	0	**S0** (00)	**0**
S2 (10)	1	**S2** (10)	**1**

b) If Q_1 is output of D_1 and Q_0 is output of D_0 , and P is our Output then:

$$D_1 = X.(Q_1 \oplus Q_0)$$
$$D_2 = X.(\overline{Q_1 + Q_0})$$
$$P = X.Q_1.\overline{Q_0}$$

Therefore circuit will look be:



Mission 5: Designing 2-bit counter for sequence 00->01->10->11->00 using D flip-flops.

As it is a two bit counter ,it will use 2 D flip flops. Lets say our two flips-flops are D_1 and D_0, and Q_1 ,Q_0 are their outputs respectively with Q_0 being the LSB.

a) State transition table will nothing but our desired sequence which will be:

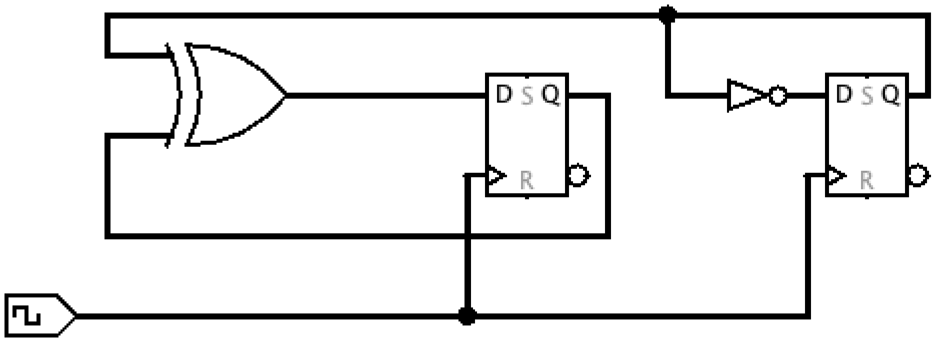
Q_1	Q_0	D_1	D_0
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

Here, Q_1 = Present state/ current output of D_1 flip flop.
Q_0 = Present state/ current output of D_0 flip flop.
D_1 = Next state / current input of D_1 flip flop.
D_0 = Next state / current input of D_0 flip flop.

b) Boolean expression derived from the above transition table would be:

$$D_1 = Q_1 \oplus Q_0$$
$$D_0 = \overline{Q_0}$$

c)



Link of video simulating counter: Counter_using_DFlipflop.mov

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