

# **ICS122 Computer Organization**

## **Assignment – II**

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**Course Instructor: Dr. Goutam Mali**

**Department of Computer Science and Engineering**  
**Indian Institute of Information Technology Kottayam**

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1. Given an instruction sequence, draw the data path execution for the following MIPS instructions:

add \$t0, \$t1, \$t2

lw \$t3, 8(\$t4)

sw \$t5, 12(\$t6)

Identify the critical path for each instruction.

2. If an ALU operation takes 2 ns, memory access takes 10 ns, and register read/write takes 1 ns, estimate the execution time for a load instruction in a single-cycle processor.
3. A processor has a 2-level cache hierarchy. Level-1 cache has a hit rate of 90%, and Level-2 cache has a hit rate of 95%. The main memory access time is 100 ns. If Level-1 cache access time is 2 ns and Level-2 cache access time is 10 ns, compute the average memory access time (AMAT).
4. Suppose a virtual memory system has a page size of 4 KB and a physical memory of 16 MB. How many page table entries are required for a process with an address space of 64 MB? Assume a single-level page table.
5. Consider a CPU with a clock rate of 3 GHz. If a program consists of 30% load/store instructions (taking 5 cycles each), 50% ALU operations (taking 4 cycles each), and 20% branch instructions (taking 3 cycles

each), calculate the average CPI and execution time for a program with 1 million instructions.

6. A 5-stage pipeline (IF, ID, EX, MEM, WB) is used to execute a program. Given the following sequence:

lw \$t1, 0(\$t2)

add \$t3, \$t1, \$t4

sw \$t3, 4(\$t5)

Identify any hazards and suggest solutions to minimize stalls.

7. A processor with a cache system has a miss penalty of 50 cycles and a cache miss rate of 3%. If the processor runs at 2 GHz, calculate the average memory stall time per instruction.
8. A direct-mapped cache has 64 blocks, and each block can store 16 words. The memory address is 32 bits. Determine the number of bits used for the block offset, index, and tag.