CA Lab: Homework 9

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Task Description

Immediate Extension Unit

Solution

The module:

```
module ALU (
    input i,
    input [31:0] SrcA, SrcB,
    input [3:0] af,
    output reg [31:0] Alures,
    output Zero, Neg, ovfalu
);
    always @(af or i or SrcA or SrcB) begin
        case (af)
            4'b0000 : Alures = SrcA + SrcB ;
            4'b0001 : Alures = SrcA + SrcB ;
            4'b0010 : Alures = SrcA - SrcB ;
            4'b0011 : Alures = SrcA - SrcB ;
            4'b0100 : Alures = SrcA & SrcB ;
            4'b0101 : Alures = SrcA | SrcB ;
            4'b0110 : Alures = SrcA ^ SrcB ;
            4'b0111 : Alures = i ? SrcB << 16 : SrcA ~| SrcB;
            4'b1010 : Alures = SrcA < SrcB ;
            4'b1011 : Alures = SrcA < SrcB ;
        endcase
    end
    assign Zero = Alures == 0;
    assign Neg = (af < 4) & Alures[31];
    assign ovfalu = (af == 0 | af == 2) & (Alures[31] ? (SrcA[31] &
    SrcB[31]) : (SrcA[31] | SrcB[31]));
endmodule
```

The testbench:

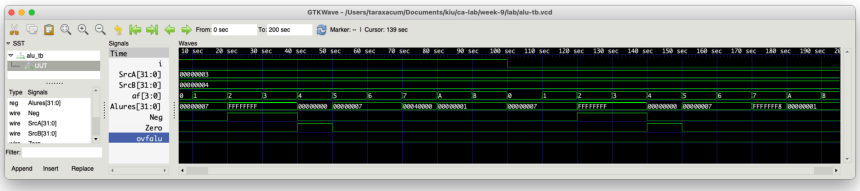
```
module alu_tb();

  reg i;
  reg [31:0] SrcA;
  reg [31:0] SrcB;
```

```
  reg [3:0] af;
  wire [31:0] Alures;
  wire Zero;
  wire Neg;
  wire ovfalu;

  ALU UUT (
    .i(i),
    .SrcA(SrcA),
    .SrcB(SrcB),
    .af(af),
    .Alures(Alures),
    .Zero(Zero),
    .Neg(Neg),
    .ovfalu(ovfalu)
  );

  initial begin
    $dumpfile("alu-tb.vcd");
    $dumpvars(0, alu_tb);
    SrcA = 32'd3;
    SrcB = 32'd4;
    i = 1;
    af = 4'b0000;
    #10;
    af = 4'b0001;
    #10;
    af = 4'b0010;
    #10;
    af = 4'b0011;
    #10;
    af = 4'b0100;
    #10;
    af = 4'b0101;
    #10;
    af = 4'b0110;
    #10;
    af = 4'b0111;
    #10;
    af = 4'b1010;
    #10;
    af = 4'b1011;
    #10;
    i = 0;
    af = 4'b0000;
    #10;
    af = 4'b0001;
    #10;
    af = 4'b0010;
    #10;
    af = 4'b0011;
    #10;
    af = 4'b0100;
    #10;
    af = 4'b0101;
    #10;
    af = 4'b0110;
```

```
63      #10;
64      af = 4'b0111;
65      #10;
66      af = 4'b1010;
67      #10;
68      af = 4'b1011;
69      #10;
70    end
71  endmodule
```

Simulation and Testing

The timing diagrams:



Reference

- me