CA Lab: Homework 3

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March 25, 2023

Task Description

Full adder has 3 inputs and 2 outputs.

a) Write the equations for the output.

b) Create truth table for the inputs A, B, C. Fill out the columns of the outputs.

c) Write Verilog HDL code of this logic diagram.

Solution

a)

$$X = \overline{(A \wedge B)} \vee C$$

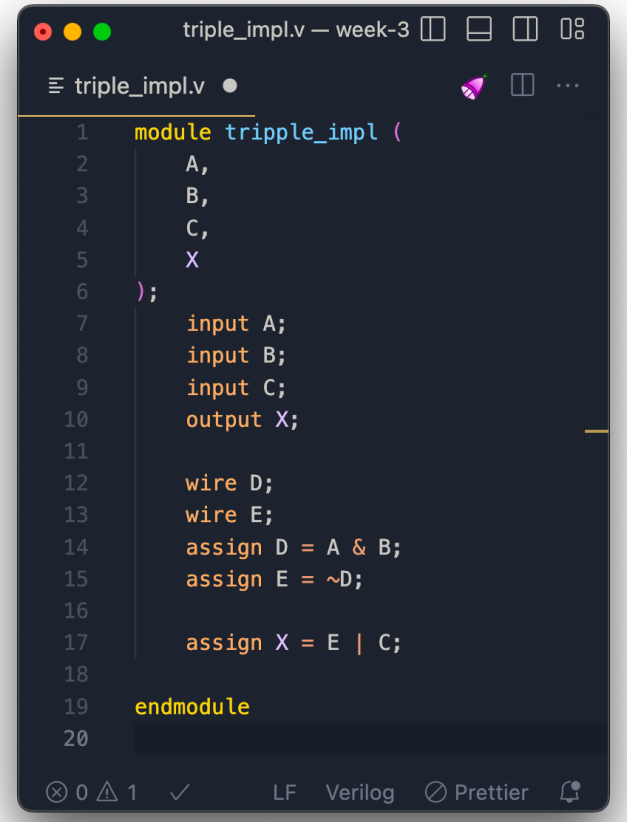
b)

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

c) The Verilog HDL code of the given logic diagram:

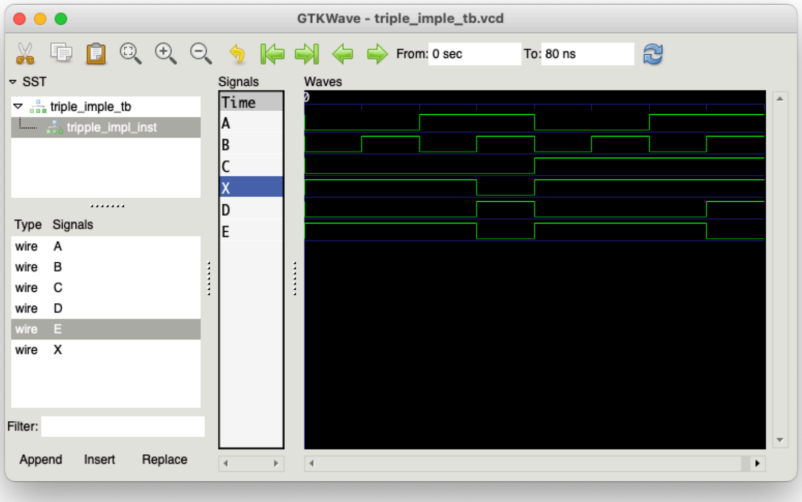
```
module tripple_impl (
    A,
    B,
    C,
    X
);
    input A;
```

```
    input B;
    input C;
    output X;

    wire D;
    wire E;
    assign D = A & B;
    assign E = ~D;

    assign X = E | C;

endmodule
```



Simulation & Verification

here's the results of the simulation I ran.



Conclusion

I had to do write verilog in VSCode, I hope it's written the way it was supposed to be.

Reference

I used GTKWave for graphing the simulation results.