CA Lab: Lab 4

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Task Description

a) Write the equations for the outputs. (15 points)

b) Create truth table for the inputs X, Y, Z. Fill out the columns of the outputs. (10 points)

c) Please, write what does this logic circuit represents? (15 points)

d) Write Verilog HDL code of this logic diagram. (50 points)

Solution

a)

$$D = Z \oplus X \oplus Y$$

$$B = (\overline{(X \oplus Y)} \wedge Z) \vee (\overline{X} \wedge Y)$$

b)

Z	X	Y	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

c) This is a full subtractor

d)
```
module mux (
    input Z,
    input X,
    input Y,
    output D,
```

```
    output B);

assign D = Z ^ X ^ Y;
assign B = (~(X ^ Y) & Z) | (~X & Y);

endmodule
```

Conclusion

the homework has concluded here.

Reference

there is nothing to reference.