CA Lab: Lab 6

student: Dimitri Tabatadze

April 11, 2024

Task Description

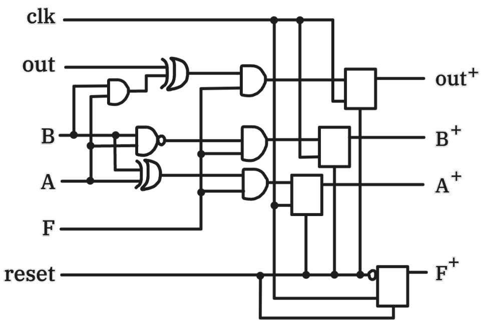
Design of Clock divider, where the input clock is divided by an odd integer.

1. Draw the circuits. *10 points*
2. Write the equation. *10 points*
3. Write and test the code. *70 points* (main file *40 points*, run to the board-*30 points*)

Please, solve the problems (write the comments) *5 points*, take the clear screenshots and combine all your solutions in one pdf file, then upload in teams. *5 points*

Solution

1. The circuit diagram:



2. The equations

$$
\begin{aligned}
A^+ &= F \land (A \oplus B) \\
B^+ &= F \land \overline{(A \land B)} \\
\mathrm{out}^+ &= F \land (\mathrm{out} \oplus (A \land B)) \\
F^+ &= \overline{reset}
\end{aligned}
$$

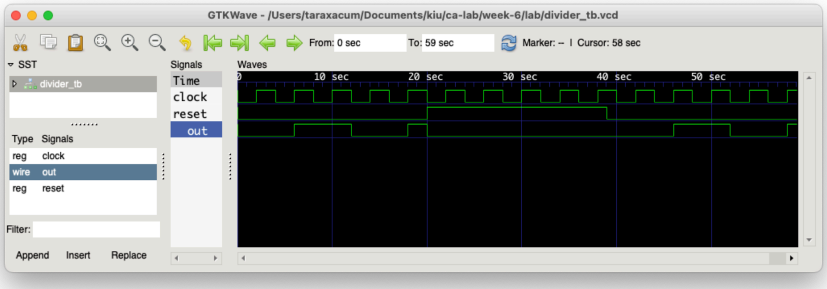
3. The Verilog code:

```
module divider (
    input clock,
    input reset,
    output reg out = 0
);

reg A = 0;
reg B = 0;
reg F = 0;

always @(clock, posedge reset) begin
    if (~reset) begin
        A <= F & (A ^ B);
        B <= F & ~(A & B);
        out <= F & (out ^ (A & B));
        F <= ~reset;
    end else begin
        A <= 0;
        B <= 0;
        F <= 0;
        out <= 0;
    end
end

endmodule
```

Conclusion

This task took me more time than I would have prefered it to. I can assure you, this code works, here's the timing diagram along with a testbench:

```
module divider_tb();

reg clock;
reg reset;
wire out;

divider UUT(.clock(clock), .reset(reset), .out(out));

always #2 clock = ~clock;

initial begin
    clock = 0;
    reset = 0;
    #20;
    reset = 1;
    #19;
    reset = 0;
    #20;
    $finish;
end

endmodule
```



GTKWave - /Users/taraxacum/Documents/kiu/ca-lab/week-6/lab/divider_tb.vcd

From: 0 sec To: 59 sec Marker: -- | Cursor: 58 sec

Type	Signals
reg	clock
wire	out
reg	reset

Reference

- My whiteboard