Exercises for week 10

1. Timer specification. Define a hardware device with the following properties:

   (a) I/O-ports: i) $counter \in \mathbb{B}^{64}$, ii) command and status register $cmsr \in \mathbb{B}^{32}$.

   (b) two bits of $cmsr$ are meaningful: i) $cmsr[0]$: ticking and ii) $cmrs[1]$: interrupt.

   While the timer is ticking, the counter is decreased in every hardware cycle. Interrupt is activated when the counter reaches zero, at which time the timer stops ticking, and can only be cleared by a write to $cmsr$.
   (30 points)

   Hint: this is similar to the specification of a hardware disk.

2. Processor + timer.

   (a) Specify an ISA model for processor + timer. (15 points)
   Attention: the number of cycles for the execution of instructions varies. Just formulate liveness: at some instruction the timer stops ticking.

   (b) Suppose you start the timer (by writing to $cmsr$) with value $T = \langle counter \rangle$. Give upper and lower bounds for the number of instructions that can be executed before the timer stops ticking. (5 points)

   (c) Assume the hardware is clocked at 1 GHz. How much time passes until the interrupt? (5 points)

3. (a) In C+A+disk+interrupts we have two sources of nondeterminism. What are they? (15 points)

   (b) State the reorder theorem for MIPS + disc. (15 points)

   (c) In the semantics of C+A+disk+interrupts we did not treat the case that a disk access ends while translated C-code is running. How could we justify this? (15 points)