

CA Lab: Homework 3

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Task Description

Full adder has 3 inputs and 2 outputs.

- a) Write the equations for the output.
- b) Create truth table for the inputs A, B, C. Fill out the columns of the outputs.
- c) Write Verilog HDL code of this logic diagram.

Solution

a)

$$X = \overline{(A \wedge B)} \vee C$$

b)

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

c) The Verilog HDL code of the given logic diagram:

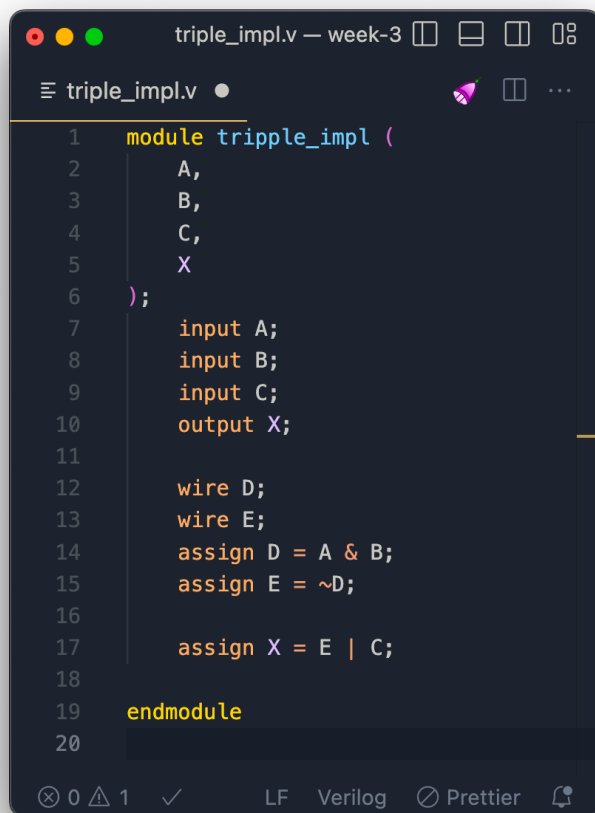
```
module tripple_impl (  
    A,  
    B,  
    C,  
    X  
);  
    input A;
```

```
    input B;
    input C;
    output X;

    wire D;
    wire E;
    assign D = A & B;
    assign E = ~D;

    assign X = E | C;

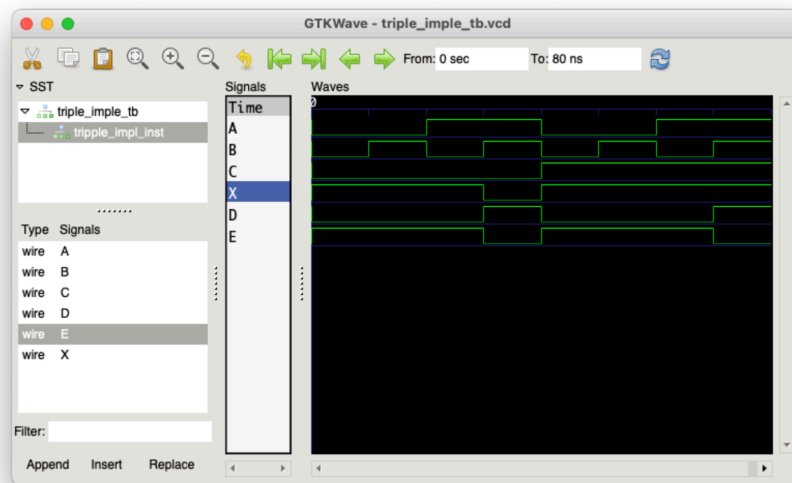
endmodule
```



```
triple_impl.v — week-3
triple_impl.v
1  module tripple_impl (
2      A,
3      B,
4      C,
5      X
6  );
7      input A;
8      input B;
9      input C;
10     output X;
11
12     wire D;
13     wire E;
14     assign D = A & B;
15     assign E = ~D;
16
17     assign X = E | C;
18
19 endmodule
20
```

Simulation & Verification

here's the results of the simulation I ran.



Conclusion

I had to do write verilog in VSCode, I hope it's written the way it was supposed to be.

Reference

I used GTKWave for graphing the simulation results.