

CA Lab: Lab 3

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Task Description

Full adder has 3 inputs and 2 outputs.

- a Create truth table of full adder. (10 points)
- b Write Boolean expressions for the outputs. (15 points)
- c Draw the circuit diagram for full adder. (10 points)
- d Write the code of adder in Verilog. (50 points)

Solution

a)

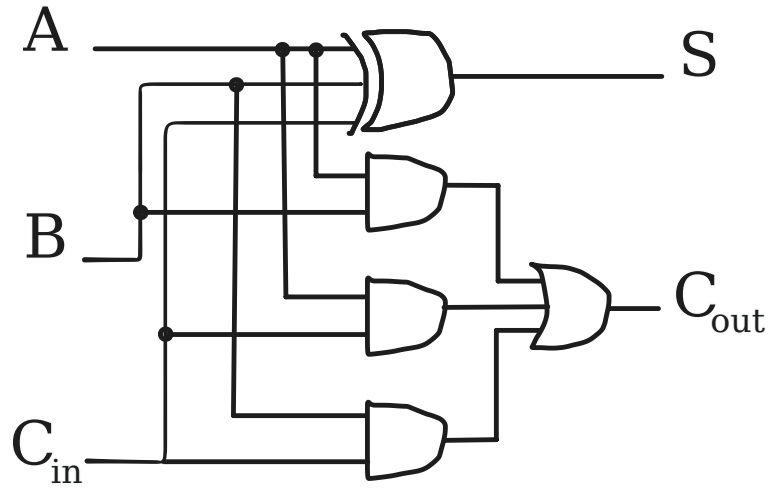
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

b)

$$\begin{aligned} S &= (\overline{A} \wedge \overline{B} \wedge C_{in}) \vee (\overline{A} \wedge B \wedge \overline{C_{in}}) \vee (A \wedge \overline{B} \wedge \overline{C_{in}}) \vee (A \wedge B \wedge C_{in}) \\ &= (\overline{A} \wedge (\overline{B} \wedge C_{in} \vee B \wedge \overline{C_{in}})) \vee (A \wedge (\overline{B} \wedge \overline{C_{in}} \vee B \wedge C_{in})) \\ &= (\overline{A} \wedge (B \oplus C_{in})) \vee (A \wedge \overline{(B \oplus C_{in})}) \\ &= A \oplus (B \oplus C_{in}) \\ &= A \oplus B \oplus C_{in} \end{aligned}$$

$$\begin{aligned}
C_{out} &= (\overline{A} \wedge B \wedge C_{in}) \vee (A \wedge \overline{B} \wedge C_{in}) \vee (A \wedge B \wedge \overline{C_{in}}) \vee (A \wedge B \wedge C_{in}) \\
&= (A \wedge (\overline{B} \wedge C_{in} \vee B \wedge \overline{C_{in}} \vee B \wedge C_{in})) \vee (\overline{A} \wedge B \wedge C_{in}) \\
&= (A \wedge (B \vee C_{in})) \vee (\overline{A} \wedge (B \wedge C_{in})) \\
&= (B \wedge C_{in}) \vee (A \wedge (B \vee C_{in})) \\
&= (B \wedge C_{in}) \vee (A \wedge B) \vee (A \wedge C_{in})
\end{aligned}$$

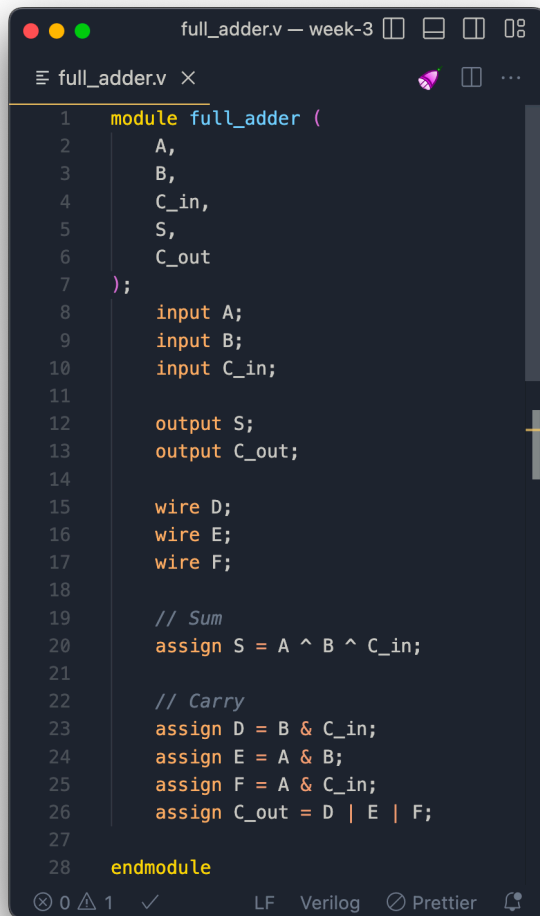
c) The circuit diagram:



d) The code in Verilog:

```
module full_adder (  
    A,  
    B,  
    C_in,  
    S,  
    C_out  
);  
    input A;  
    input B;  
    input C_in;  
  
    output S;  
    output C_out;  
  
    wire D;  
    wire E;  
    wire F;  
  
    // Sum  
    assign S = A ^ B ^ C_in;  
  
    // Carry  
    assign D = B & C_in;  
    assign E = A & B;  
    assign F = A & C_in;  
    assign C_out = D | E | F;  
  
endmodule
```

and a screenshot of highlighted code:



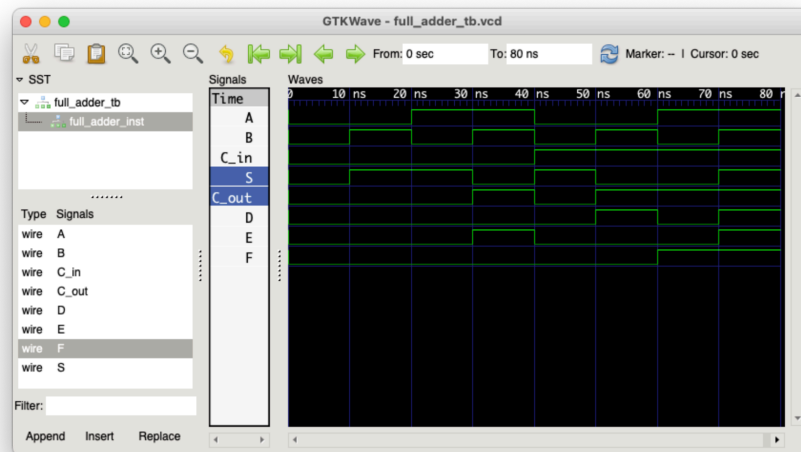
The image shows a screenshot of a code editor window titled "full_adder.v — week-3". The editor contains Verilog code for a full adder module. The code is as follows:

```
1  module full_adder (  
2      A,  
3      B,  
4      C_in,  
5      S,  
6      C_out  
7  );  
8      input A;  
9      input B;  
10     input C_in;  
11  
12     output S;  
13     output C_out;  
14  
15     wire D;  
16     wire E;  
17     wire F;  
18  
19     // Sum  
20     assign S = A ^ B ^ C_in;  
21  
22     // Carry  
23     assign D = B & C_in;  
24     assign E = A & B;  
25     assign F = A & C_in;  
26     assign C_out = D | E | F;  
27  
28 endmodule
```

The editor interface includes a tab labeled "full_adder.v", a search icon, and a settings menu. The bottom status bar shows "0 1 ✓", "LF Verilog", "Prettier", and a bell icon.

Simulation & Verification

here's the results of the simulation I ran.



Conclusion

I had to do write verilog in VSCode, I hope it's written the way it was supposed to be.

Reference

I used <https://tldraw.com> for drawing the diagram.