CA Lab: Homework 4

student: Dimitri Tabatadze

March 31, 2023

Task Description

a Write the code of 4×1 MUX in Verilog. (50 points)

b Show the timing diagram of MUX in Quartus. (40 points)

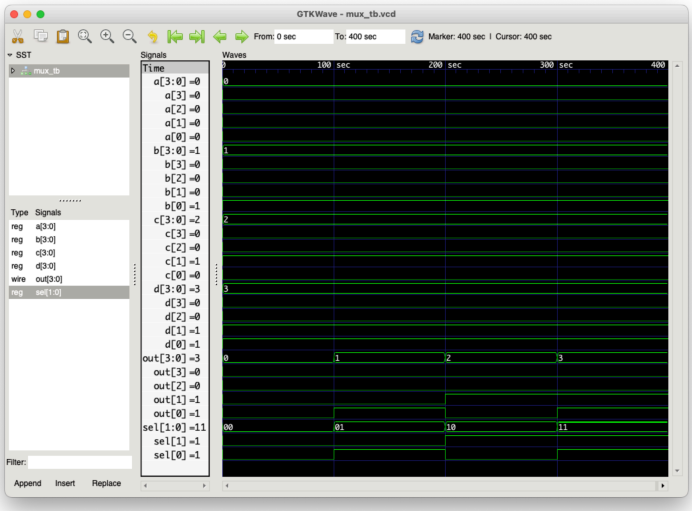
Solution

a)
```
module mux (
    input [3:0] a,
    input [3:0] b,
    input [3:0] c,
    input [3:0] d,
    input [1:0] sel,
    output reg [3:0] out);

always @ (a or b or c or d or sel)
begin
    if (sel == 0) out = a;
    else if (sel == 1) out = b;
    else if (sel == 2) out = c;
    else if (sel == 3) out = d;
end

out = (a & ~sel[0] & ~sel[0]) ^ (b & ~sel[0] & sel[0]) ^ (c & sel[0] & ~sel[

endmodule
```



b)

Conclusion

the homework has concluded here.

Reference

there is nothing to reference.