Performance Analysis of Synchronous DRAM

The modern DRAM and recent development can be attributed in mainly two categories: device data rate and row cycle time. The different rates at which each of this is scaled with every new development influences the overall development of synchronous DRAM.

The idea behind development is introducing new features but not increasing the size. the crucial role of evaluating design and considering trade-off points between cost of various features and potential performance benefits of those features.

Peak burst bandwidth : Currently, CPUs are incapable of ingesting burst data at a rate faster than one CPU bus clock. SDRAM already satisfies this requirement.

Higher bandwidth: Sometimes, the CPU must contend with master mode peripherals over DRAM. If a peripheral is busy accessing DRAM at the precise moment that the CPU stalls on a cache miss, higher bandwidth DRAM can resolve the conflict a little faster. But fast latency DRAM can achieve the same result or better depending on burst length.

Latency: When the CPU experiences a cache miss, part or all of the CPU stalls for a surprisingly long period of time. Faster latency DRAM allows the CPU to resume operation quicker. The CPU realizes this benefit each time it accesses DRAM.

What's more important, faster latency or faster burst bandwidth?

**Why we chose this topic?**

Ever-growing application data footprints demand faster main memory with larger capacity. DRAM has been the technology choice for main memory due to its low latency and high density.

As a rule of thumb for today's desktop PC, faster latency will almost always deliver a performance benefit. Increasing peak burst bandwidth sometimes offers a performance benefit, but not in every case, and not usually as much. CPU needs latency, caches want bandwidth. We want to find out what amount of latency and burst bandwidth is optimal for a DRAM.

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