INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR

HARDWARE DESCRIPTION LANGUAGE

PROJECT REPORT

DIGITALLY OPERATED WATER PUMP

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INTRODUCTION

Electricity and water are the most valuable properties for any country. In our country, the want of electricity and water are the burning question. Load shedding has become a very common problem in our daily life. Water also plays a vital role in our life. To perform any sort of family task water is must. Nowadays most probably every house, office, industry and etc. use water pump for needed water. But switching on and off the water pump is a boring task. And most of the times we forget to start water pump in appropriate time or even we start may forget to switch off the water pump, for that reason there is a huge wastage of water as well as the electricity. To solve these sorts of problem we've made an automatic switch for water pump. This will start the water pump when the water level fall a certain predetermine level and will automatically shut off the pump when the water rise in the over low level

OBJECTIVE

1. To save Electricity as well as Electric bill.

2. Appropriate running of water pump.

3. To eliminate the concern about water pump switch on and off.

4. To ensure the availability of water in water tank.

EQUIPMENTS

The required number of *EQUIPMENTS* are as follows.

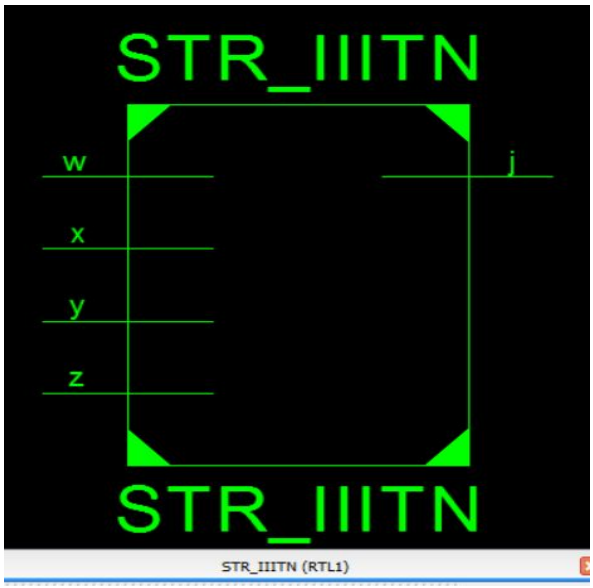
1. AND Gate(3 and 4 inputs)
2. NOT Gate
3. OR Gate (3 inputs)
4. Xilinx ISE Simulator
5. Bread Board
6. Wires and power supply

Target Customer

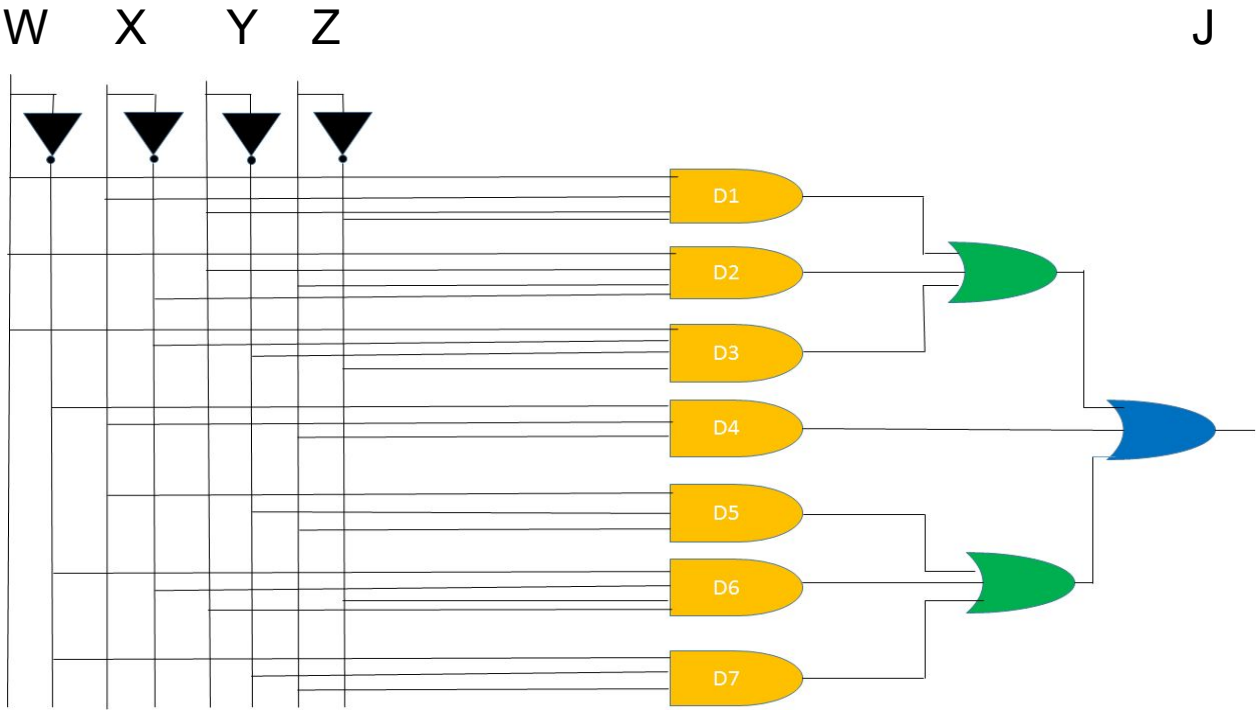
The target customers of our product are,

1. House/Restaurant owner with water pump
2. Industrial section
3. Any customer with having water pump for their water Tank
4. Hostels (IIITN hostel)

LOGIC DIAGRAM



Logic Circuits:-Input : w,x,y,z Outputs : j



TRUTH TABLE

Boolean Equation:-

$$ABC\overline{D} + A\overline{B}CD + A\overline{BC}D + \overline{AB}C\overline{D} + \overline{A}BD + B\overline{C}D + \overline{A}D\overline{C}$$

INPUTS				OUTPUT
A	B	C	D	J
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

HDL CODE

This project use a Structural Style of modelling

STR_IIITN.vhd

```
use IEEE.STD_LOGIC_1164.ALL;
entity STR_IIITN is          -----Entity declaration input and output
   Port ( w : in  bit;
          x : in  bit;
          y : in  bit;
          z : in  bit;
          j: out  bit);
end STR_IIITN;
architecture Behavioral of STR_IIITN is    -------- architecture declaration
component AND_4                                    structural style
        port(a: in bit;
                 b: in bit;              ---------component four input and gate
                 c: in bit;                                  declaration
                 d: in bit;
                 e: out bit);
end component;
component AND_3                 ---------component three input and gate
        port(f:in bit;                        declaration
                 g: in bit;
                 h: in bit;
                 i: out bit);
end component;
component OR2_IIIT          ---------component 3 input or gate
        port(a1,b1,c1: in bit;
                       d1: out bit);
end component;
```

```
component OR_2          ---------component 2 input or gate
   Port ( a2 : in  bit;
          b2 : in  bit;
          k : out  bit);
end component;
signal s1,s2,s3,s4,s5,s6,s7,M,N: bit;  ---Signal  declaration
begin
A1:AND_4  port map(d=>not(z),c=>y,b=>x,a=>w,e=>s1);
A2:AND_4 port map(d=>z,c=>y,b=>not(x),a=>w,e=>s2);
A3:AND_4 port map(d=>not(z),c=>not(y),b=>not(x),a=>w,e=>s3);
A4:AND_4 port map(d=>not(z),c=>y,b=>not(x),a=>not(w),e=>s4);
A5:AND_3 port map(h=>z,g=>x,f=>not(w),i=>s5);
A6:AND_3  port map(h=>z,g=>not(y),f=>not(w),i=>s6);
A7:AND_3  port map(h=>z,g=>not(y),f=>x,i=>s7);
o1:OR2_IIIT port map(a1=>s1,b1=>s2,c1=>s3,d1=>M);
o2:OR2_IIIT port map(a1=>M,b1=>s5,c1=>s6,d1=>N);
o3:OR_2 port map(a2=>s7,b2=>N,k=>j);
end Behavioral ;

AND_4.vhd      ------------AND_4 file use in structural style of modelling
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity AND_4 is
   Port ( a : in  bit;     -----Entity declaration input and output
          b : in  bit;
          c : in  bit;     ----------four input AND gate declaration
          d : in  bit;
          e : out  bit);
end AND_4;
architecture Behavioral of AND_4 is    ------architecture declaration in
begin                                          concurrent style of modelling
e<= a and b and c and d;
end Behavioral ;
```

```
AND_3.vhd          ------------AND_3 file use in structural style of modelling
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity AND_3 is        -----Entity declaration input and output
   Port ( f : in  bit;
          g : in  bit;       ----------three input AND gate declaration
          h : in  bit;
          i : out  bit);
end AND_3;
architecture Behavioral of AND_3 is   ------architecture declaration in
begin                                                  concurrent style of modelling
i<=f and g and h ;
end Behavioral;

OR_2.vhd    ------------OR_2 file use in structural style of modelling
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity OR_2 is          -----Entity declaration input and output
   Port ( a2 : in  bit;       ----------three input OR gate declaration
          b2 : in  bit;
          k : out  bit);
end OR_2;
architecture Behavioral of OR_2 is    ------architecture declaration in
begin                                          concurrent style of modelling
k<=a2 or b2;
end Behavioral;

OR_IIIT.vhd        ------------OR_IIIT file use in structural style of modelling
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity OR2_IIIT is      -----Entity declaration input and output
   Port ( a1 : in  bit;
          b1 : in  bit;       ---------- 2 input OR gate declaration
```

```
            c1 : in  bit;
                    d1: out bit);
end OR2_IIIT;
architecture Behavioral of OR2_IIIT is     ------architecture declaration in
begin                                                concurrent style of modelling
d1<=a1 or b1 or c1 ;
end Behavioral;
```

Problem Statements:-

A Water pump is digitally operated (ON/OFF) in order to fill the water tank for 4 storey IIITN hostel building (Ground,first,second and third).For the same, a two way switch is installed on each floor. When a switch is pressed from either of a floors,the motor would turn OFF if the motor is ON.Note:Assume that the motor is initially in OFF position for each combination of switch position.

Problem Analysis:-

1) On above problem we should analyse a problem first that the switch is located on a floor(1,2,and 3) include ground floor is consider as 4 independent operation .

2) Consider a ground ,1st ,2nd and 3rd floor take it is a variable A, B, C, D and J is a output which is operated on motor.

3) Because of all 4 floor take it as boolean combination of 16 possible combination of ON and OFF switch.

4) For a given assumption initially motor is OFF ,so after analisis 1st condition we know that for odd value of input the output is high(1) and for other is low(0).

5)From a truth table we should have draw a corresponding boolean equation and write a HDL code using structural style

ADVANTAGES

1. Corrosion Free.
2. Sturdy and durable, need not maintain.
3. No current / voltage is passed through water, therefore no electrolysis.
4. Long life.
5. Rust proof (The switch is made with stillness steel and covered with water tight pack)
6. Can be used in hard water -fuel-such as diesel, kerosene, oil etc.
7. Save of electricity due to perfect timing of water pump operation.
8. Elimination of concern about the water pump switching ON/OFF.
9. Elimination of embracing situation due to water scarcity.
10. The cost is amazingly low compared to other existing market product. (Only 296 Tk!!! Where the existing product is about 1500 Tk)
11. Compact size.
12. Ease of use.
13. Two motor can be control at the same time with two different inputs.
14. Reservoir check condition, for the first time in Bangladesh.
15. Completely home technology, so some foreign currency can be saved

APPLICATION

1. Bungalows

2. Hospitals

3. Factories

4. Hotels and restaurants

5. Commercial centers

6. All places with water tanks

DESIGN LIMITATION

As all designs have their own limitations depending upon the nature and the need of their design

application and implementation, this project has also some of its limitations in design. Some of them

come from the components incapability. The design limitation for the device is:

1. For automatic switch we needed some customized switch but as we didn't find those so we used

poly-bag to make the input switch watertight. However in mass production the switch can be

developed

Conclusion and Results

1)The design of project required knowledge of Very high speed hardware description language(VHDL). Language offers a very good interface between Integrated circuit and digital circuit.

2) Due to increasing no of floor requirements of switch in each floor is increases due to this require no of gates in a circuit is increases this increase a delay of circuit .

3) Structural style of modelling is based way to implements a hardware of a (circuit) of boolean expression

4)In the course of the project, different kinds of ICs are analyzed and implemented them practically in the circuit design. Finally, with the appropriate circuit design and its hardware implementation, the automated switch is successfully built.

Refrences

1. 1st year , Semester 2, sessional 2 ,Digital Electronics paper.
2.https://www.researchgate.net/publication/274893722_Automatic_switch_for_water_pump.