Light Gun - FPGA VGA

PCS 3335 - Lab Digital A Proposta 12
Jogo “Light Gun” em FPGA

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Princípio de funcionamento e HARDWARE

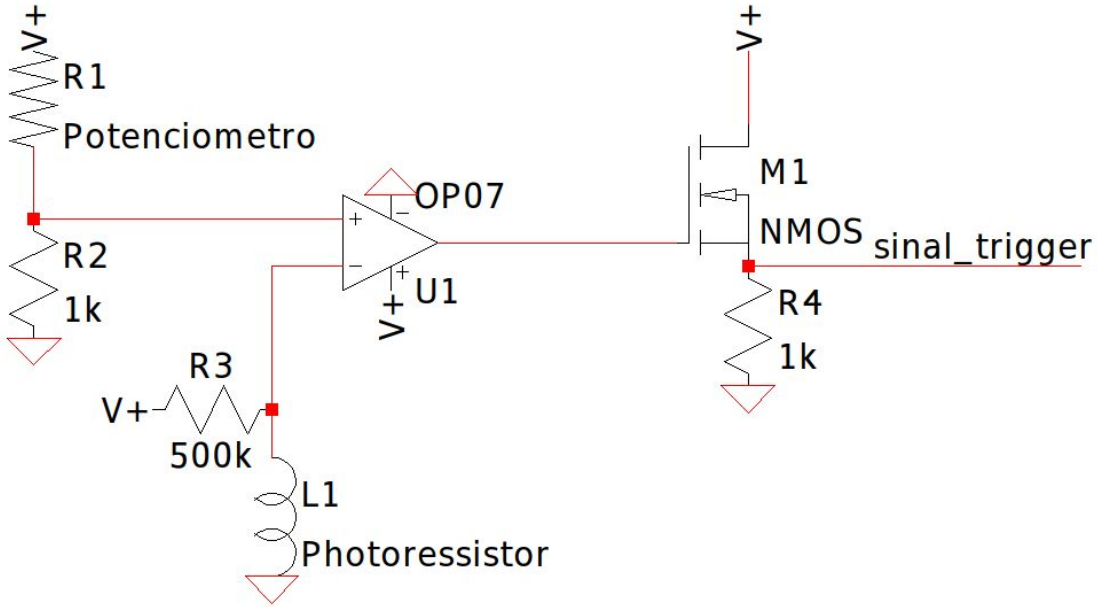
-> Ao se clicar no gatilho, o jogo faz com que apenas os alvos sejam iluminados , de forma com que se a mira estiver correta, o circuito sensor de luz deve enviar um sinal lógico high para a FPGA, indicando assim um tiro certeiro.

-> Ao se detectar um tiro certeiro a Unidade de Controle, deve eliminar a aparição do objeto que recebeu o tiro.

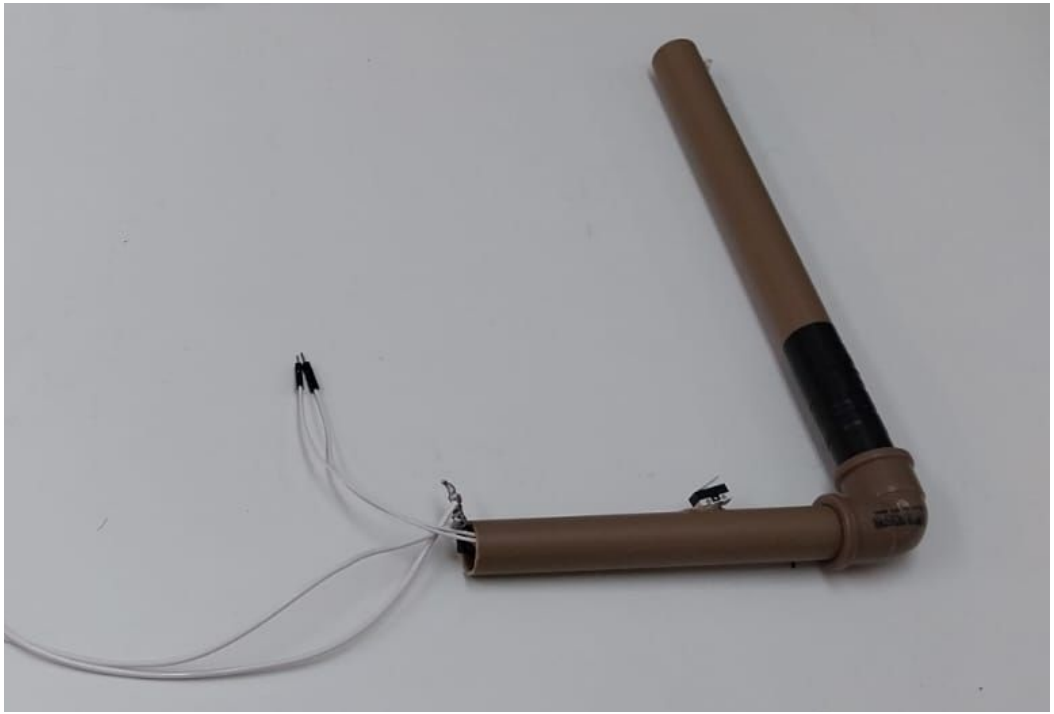
Princípio de funcionamento e HARDWARE

Duck Hunt NES on a CRT TV - YouTube

circuito de detecção de luz



Construção física da light gun



Protocolo VGA

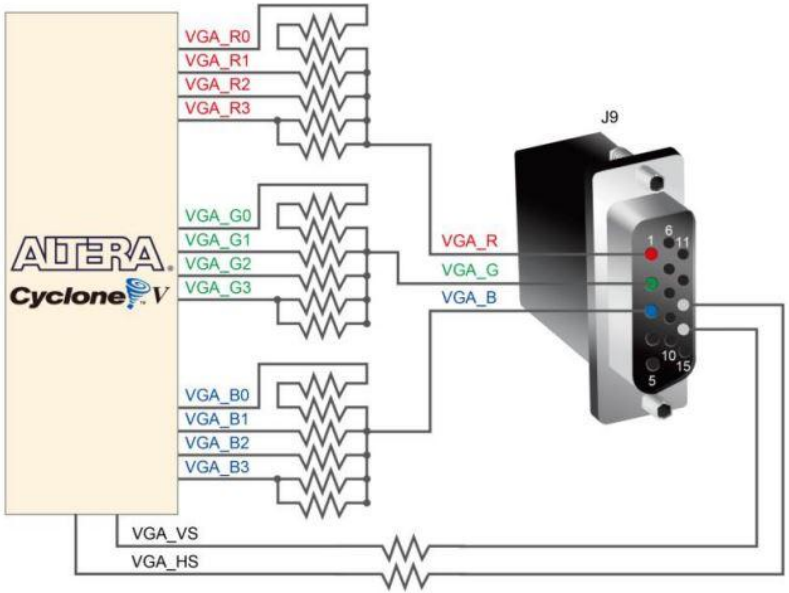


Figure 3-13 Connections between the FPGA and VGA

Protocolo VGA

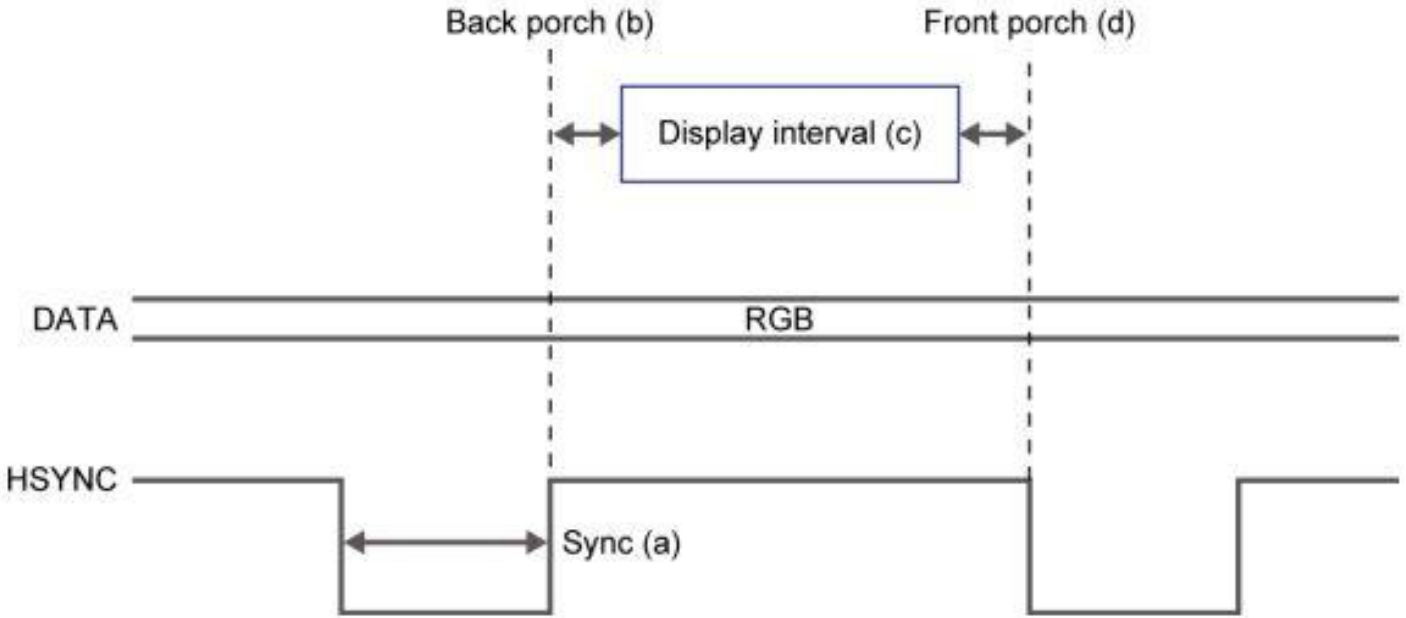


Figure 3-14 VGA horizontal timing specification

Protocolo VGA

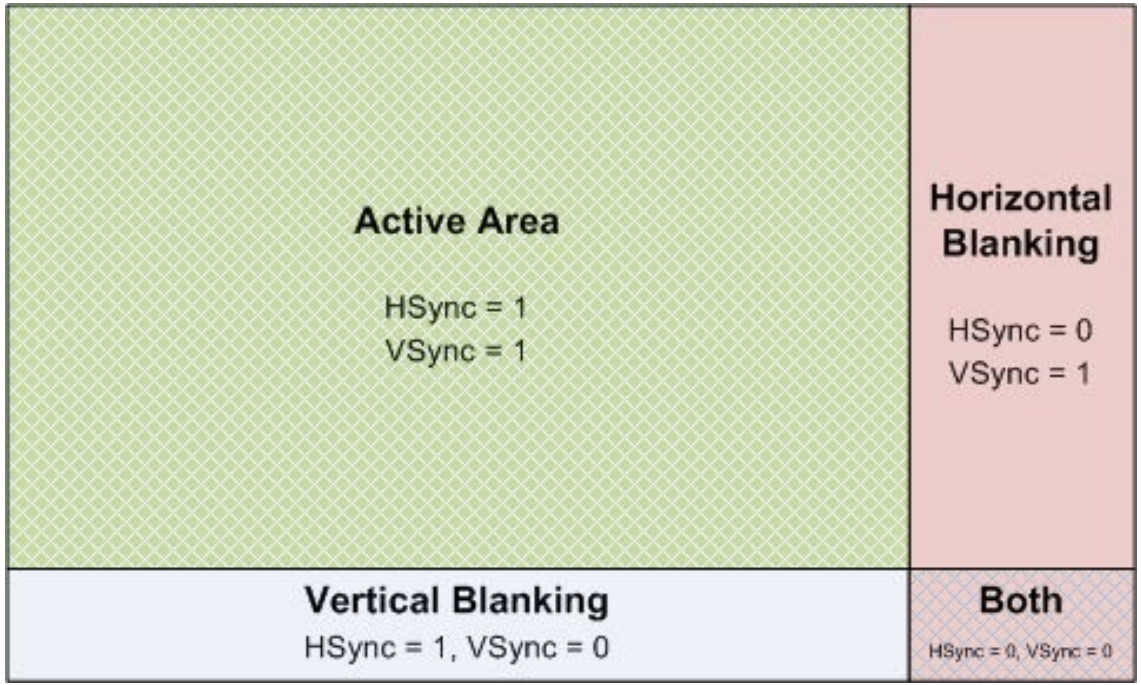
Table 3-8 VGA Horizontal Timing Specification

VGA mode		Horizontal Timing Spec				
Configuration	Resolution(HxV)	a(pixel clock cycle)	b(pixel clock cycle)	c(pixel clock cycle)	d(pixel clock cycle)	Pixel clock(MHz)
VGA(60Hz)	640x480	96	48	640	16	25

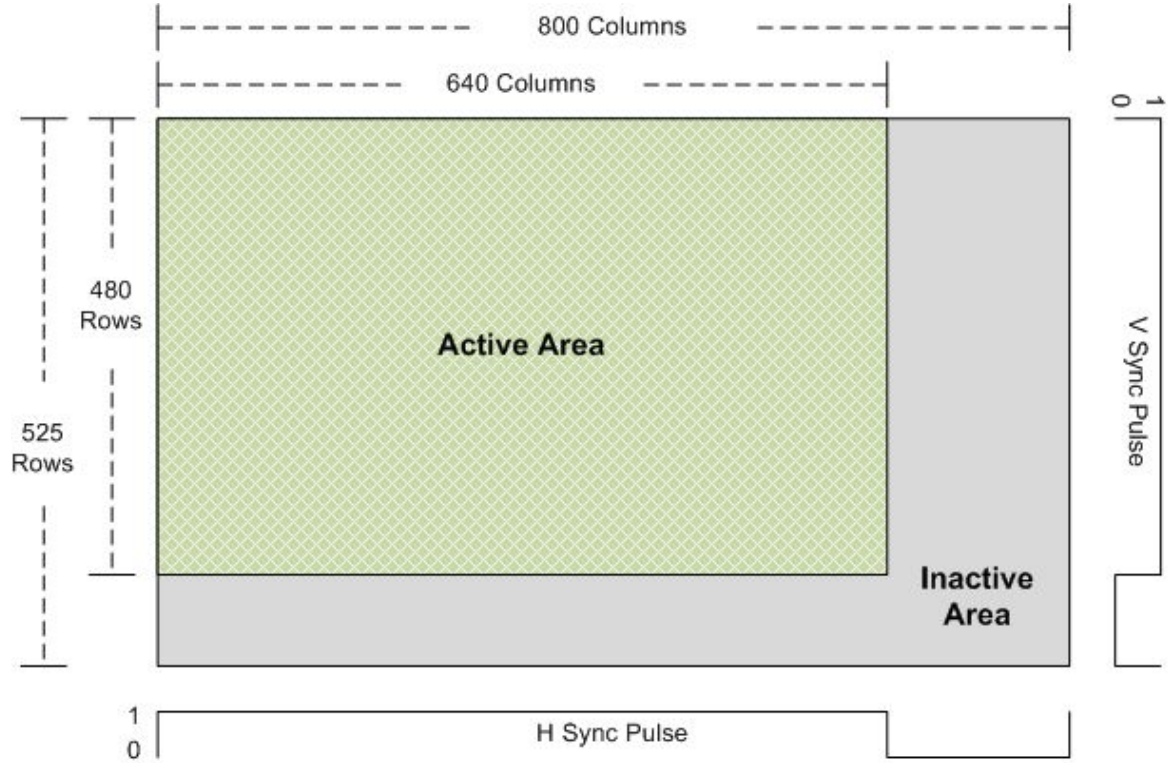
Table 3-9 VGA Vertical Timing Specification

VGA mode		Vertical Timing Spec				
Configuration	Resolution(HxV)	a(lines)	b(lines)	c(lines)	d(lines)	Pixel clock(MHz)
VGA(60Hz)	640x480	2	33	480	10	25

Protocolo VGA



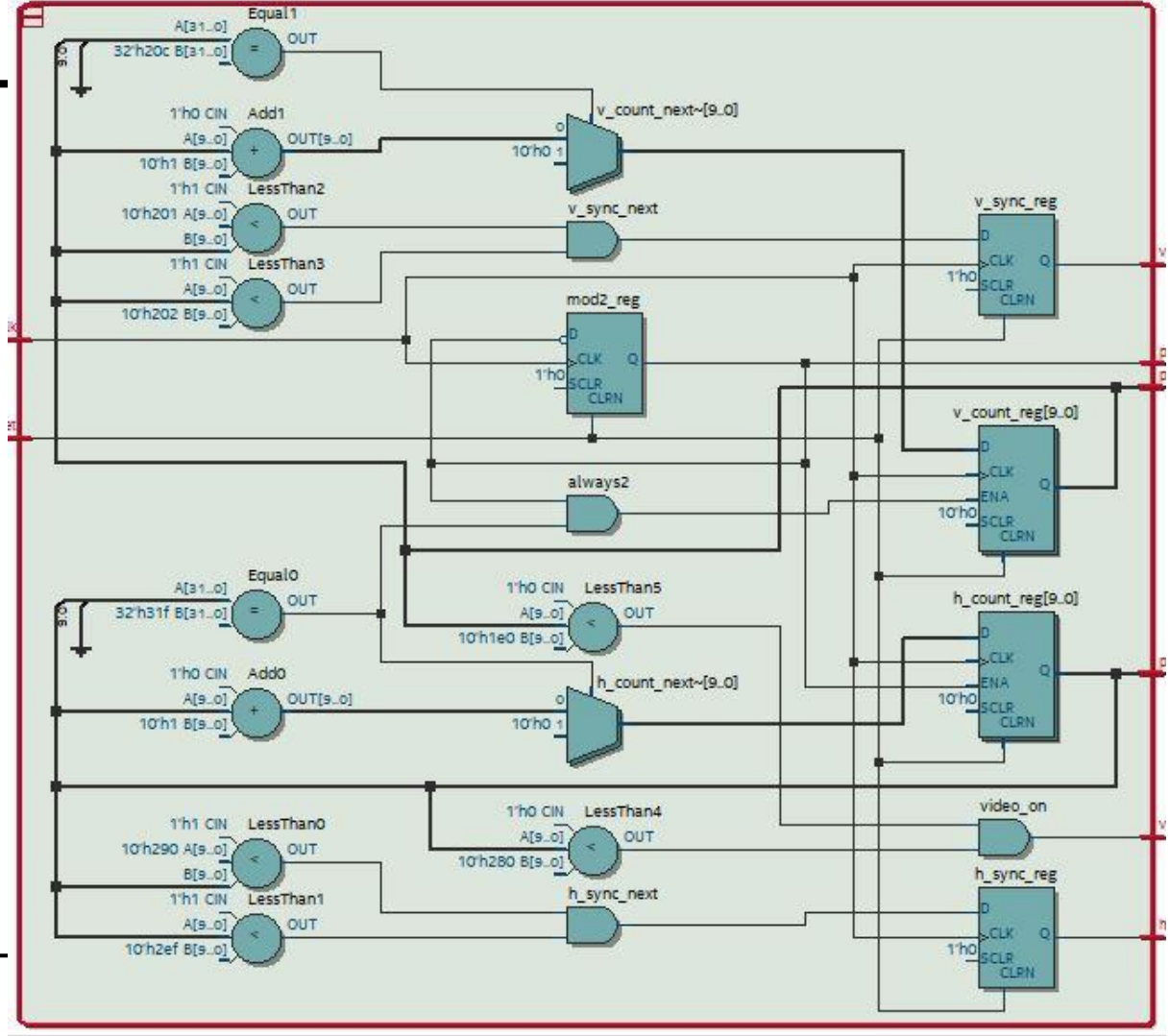
Protocolo VGA



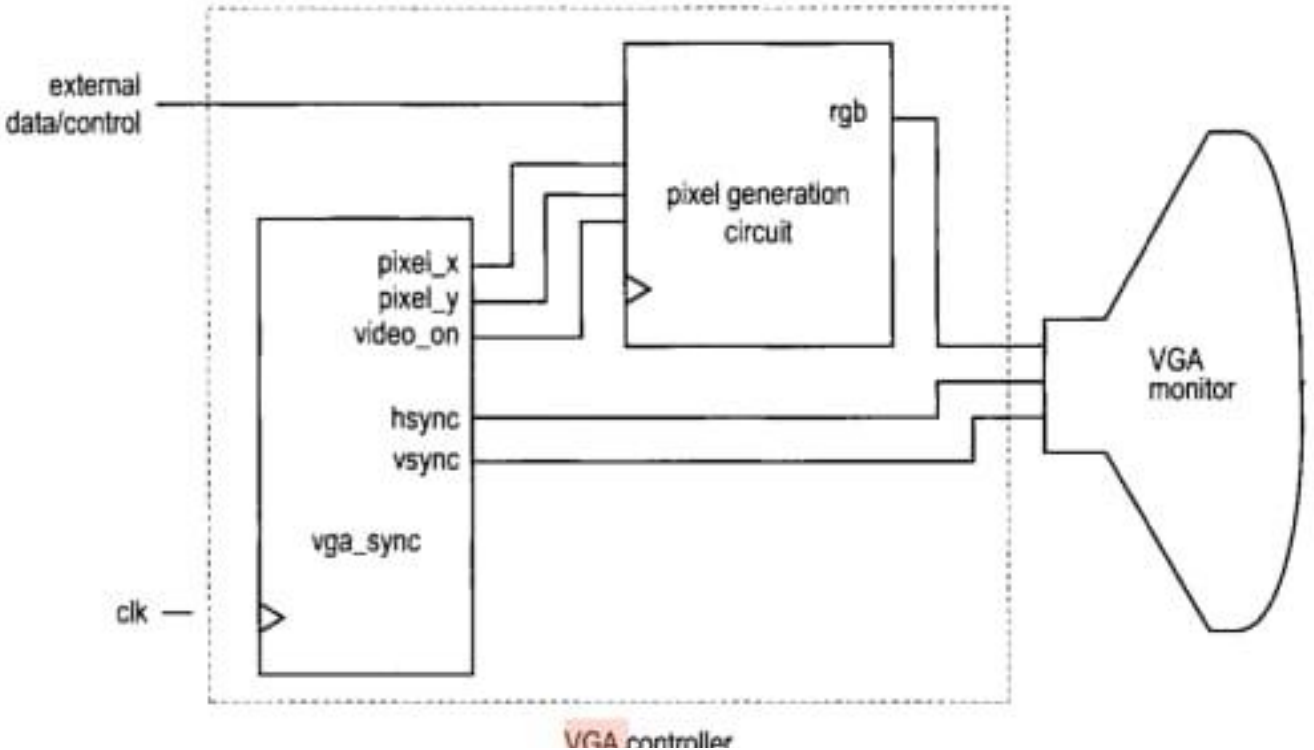
Protocolo VGA

VGA Timings using 25 MHz Clock		
Line/Frame Part	Horizontal Pixels	Vertical Lines
Whole Area	800	525
Visible Area	640	480
Front Porch	18	10
Sync Pulse	92	2
Back Porch	50	33

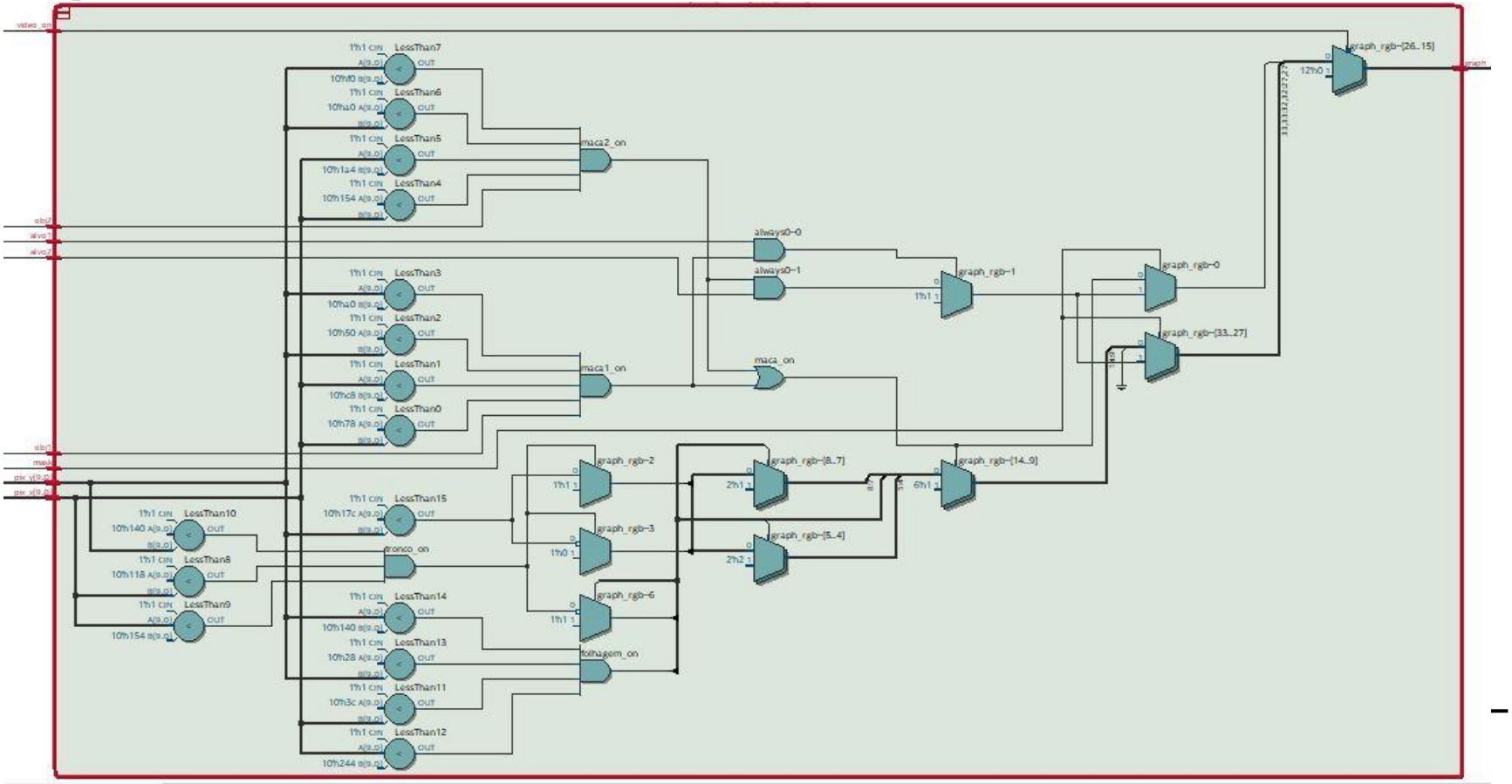
vga_sync.v


Equal1
A[31..0]
32'h20c B[31..0]
OUT
9:0
1'h0 CIN
Add1
A[9..0]
10'h1 B[9..0]
OUT[9..0]
v_count_next~[9..0]
10'h0
1'h1 CIN
LessThan2
10'h201 A[9..0]
B[9..0]
OUT
v_sync_next
v_sync_reg
1'h1 CIN
LessThan3
A[9..0]
10'h202 B[9..0]
OUT
mod2_reg
D
CLK
Q
SCLR
CLRN
1'h0
v_count_reg[9..0]
ENA
always2
Equal0
32'h31f B[31..0]
1'h0 CIN
LessThan5
10'h1e0 B[9..0]
h_count_next~[9..0]
h_count_reg[9..0]
1'h1 CIN
LessThan0
10'h290 A[9..0]
LessThan1
10'h2ef B[9..0]
1'h0 CIN
LessThan4
10'h280 B[9..0]
video_on
h_sync_next
h_sync_reg

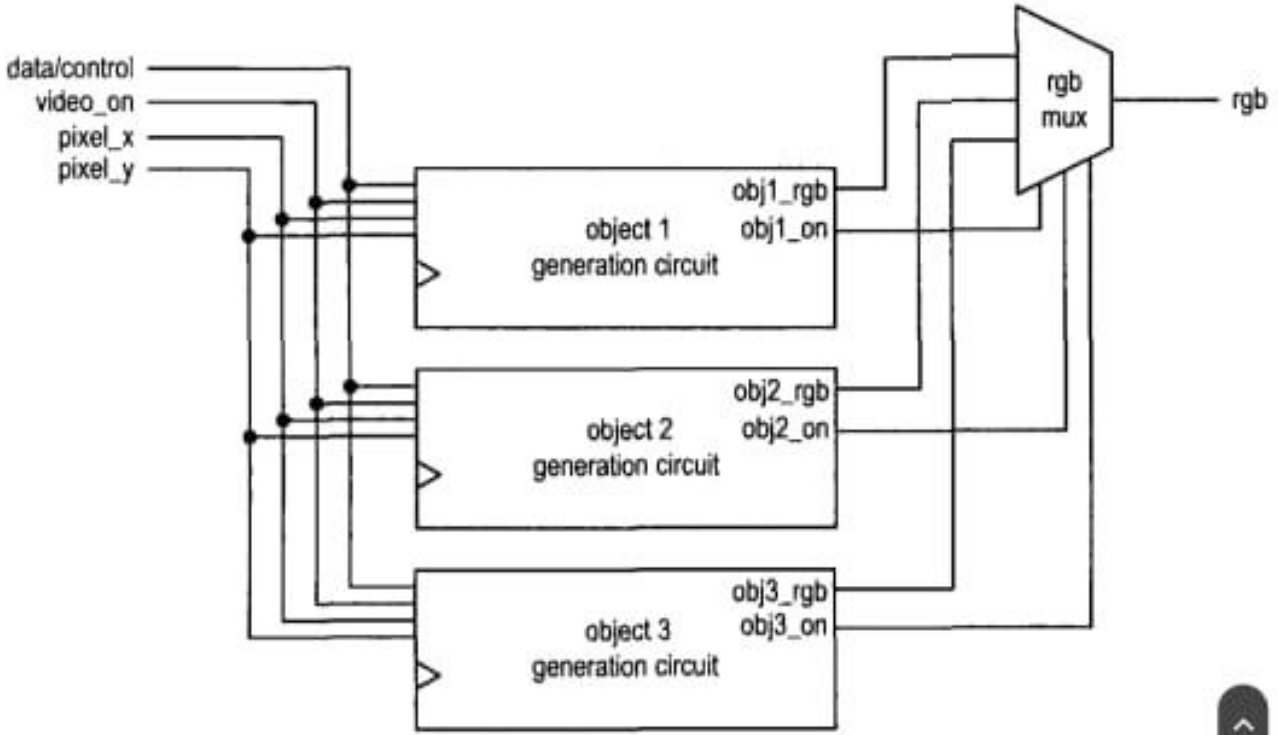
vga_sync.v


external
data/control
rgb
pixel generation
circuit
pixel_x
pixel_y
video_on
hsync
vsync
vga_sync
clk
VGA
monitor
VGA controller

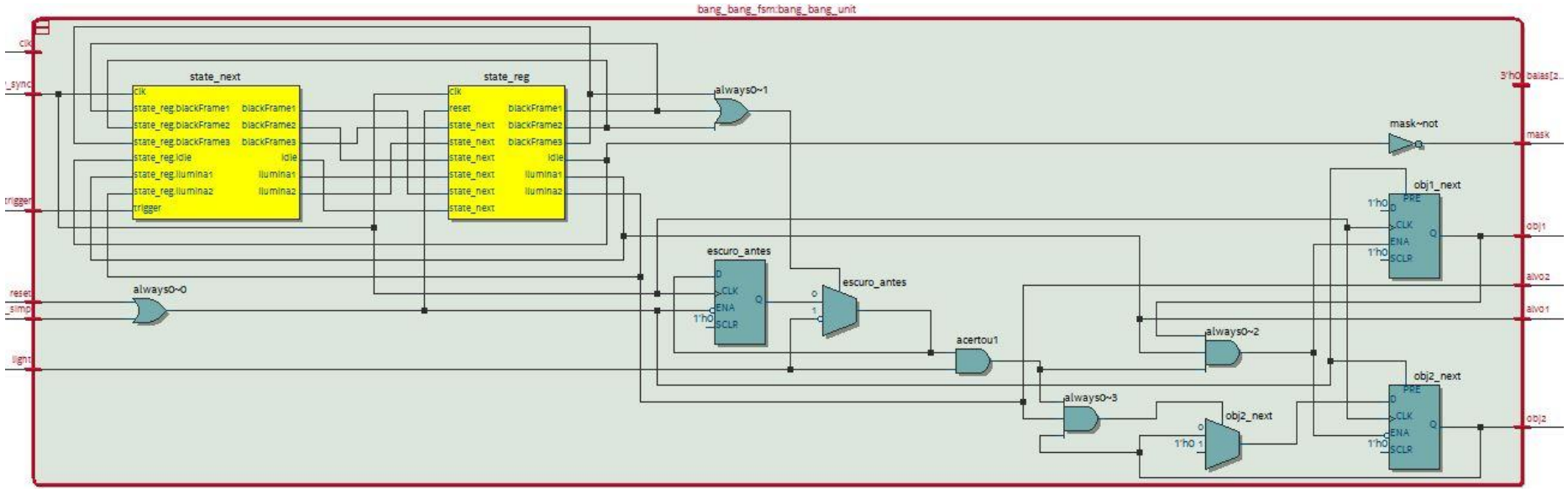
graph_circuit.v



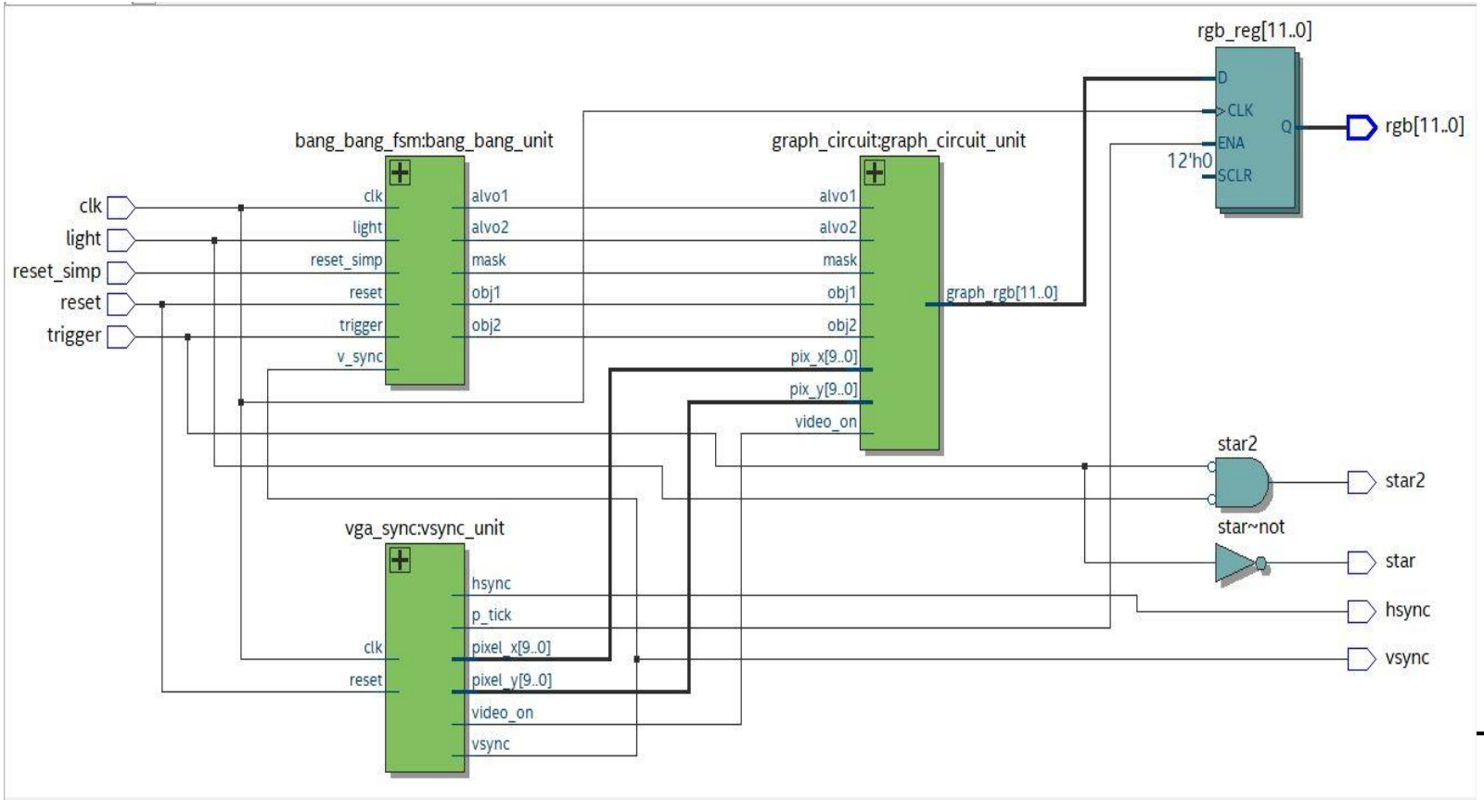
graph_circuit.v



bang_bang_fsm.v / RTL



graficos_top.v / RTL



Link GITHUB

https://github.com/PCS-Poli-USP/projeto-final-projeto-12