

CSD18510KCS 40-V N-Channel NexFET™ Power MOSFET

1 Features

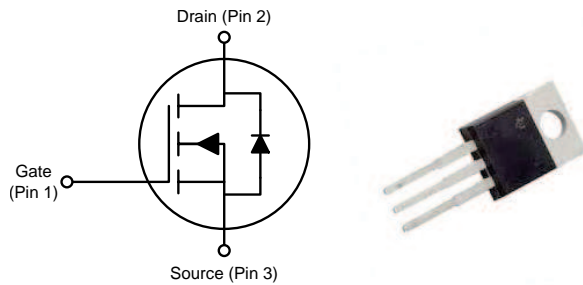
- Low Q_g and Q_{gd}
- Low $R_{DS(on)}$
- Low-Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 40-V, 1.4-m Ω , TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	40		V
Q_g	Gate Charge Total (10 V)	118		nC
Q_{gd}	Gate Charge Gate-to-Drain	21		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	2.0	m Ω
		$V_{GS} = 10\text{ V}$	1.4	
$V_{GS(th)}$	Threshold Voltage	1.7		V

Device Information⁽¹⁾

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD18510KCS	Tube	50	TO-220 Plastic Package	Tube

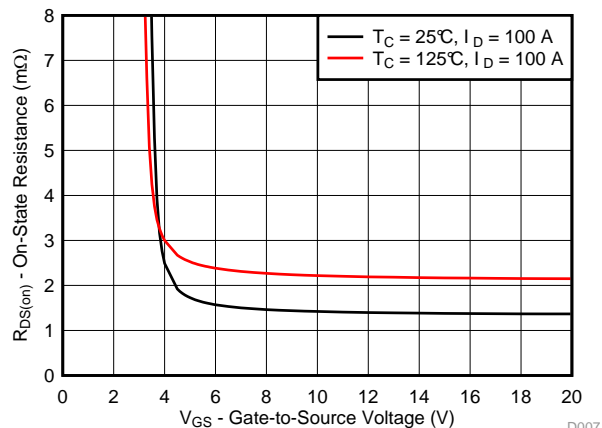
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current (Package Limited)	200	A
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	288	
	Continuous Drain Current (Silicon Limited), $T_C = 100^\circ\text{C}$	204	
I_{DM}	Pulsed Drain Current ⁽¹⁾	400	A
P_D	Power Dissipation	250	W
T_J, T_{stg}	Operating Junction, Storage Temperature	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche Energy, Single Pulse $I_D = 81\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\text{ }\Omega$	328	mJ

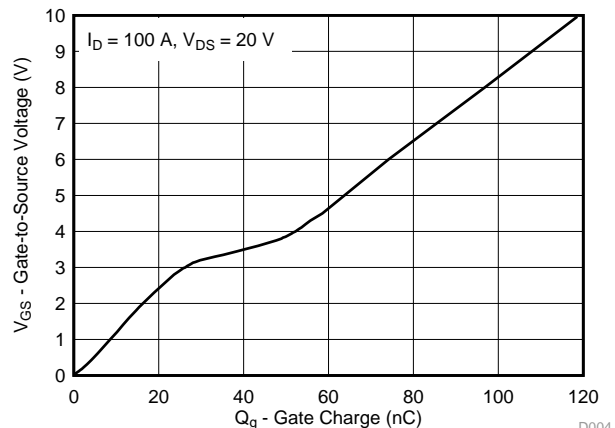
(1) Max $R_{\theta JC} = 0.6^\circ\text{C/W}$, pulse duration $\leq 100\text{ }\mu\text{s}$, duty cycle $\leq 1\%$.

$R_{DS(on)}$ vs V_{GS}



D007

Gate Charge



D004



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4 Revision History

Changes from Original (March 2017) to Revision A	Page
• Corrected package type in Features section	1

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	40			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 32 V	1			μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 20 V	100			nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.4	1.7	2.3	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 4.5 V, I _D = 100 A	2.0			mΩ
		V _{GS} = 10 V, I _D = 100 A	1.4			
g _{fs}	Transconductance	V _{DS} = 4 V, I _D = 100 A	330			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	8770	11400	pF	
C _{oss}	Output capacitance		832	1080	pF	
C _{rss}	Reverse transfer capacitance		424	551	pF	
R _G	Series gate resistance		0.9	1.8	Ω	
Q _g	Gate charge total (4.5 V)	V _{DS} = 20 V, I _D = 100 A	58	75	nC	
Q _g	Gate charge total (10 V)		118	153	nC	
Q _{gd}	Gate charge gate-to-drain		21	nC		
Q _{gs}	Gate charge gate-to-source		28	nC		
Q _{g(th)}	Gate charge at V _{th}		15	nC		
Q _{oss}	Output charge	V _{DS} = 20 V, V _{GS} = 0 V	35	nC		
t _{d(on)}	Turnon delay time	V _{DS} = 20 V, V _{GS} = 10 V, I _{DS} = 100 A, R _G = 0 Ω	10	ns		
t _r	Rise time		8	ns		
t _{d(off)}	Turnoff delay time		29	ns		
t _f	Fall time		8	ns		
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 100 A, V _{GS} = 0 V	0.85	1.0	V	
Q _{rr}	Reverse recovery charge	V _{DS} = 20 V, I _F = 100 A, di/dt = 300 A/μs	70	nC		
t _{rr}	Reverse recovery time		41	ns		

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C}/\text{W}$

5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

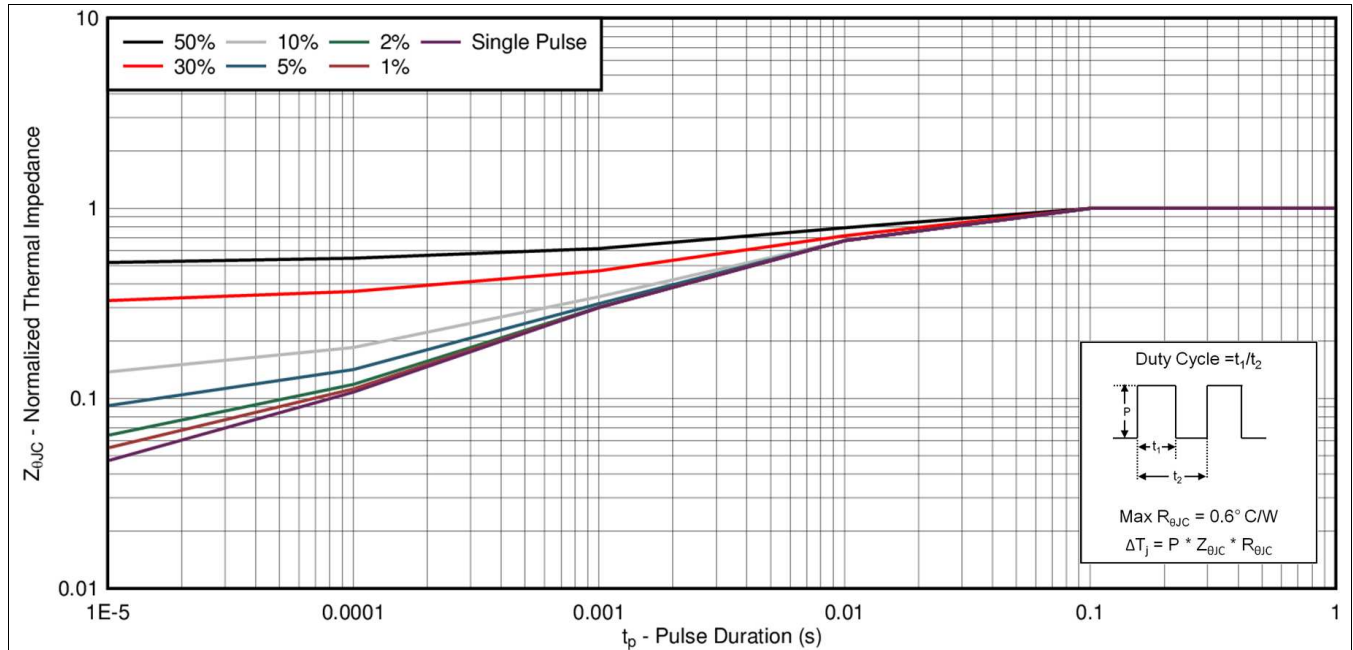


Figure 1. Transient Thermal Impedance

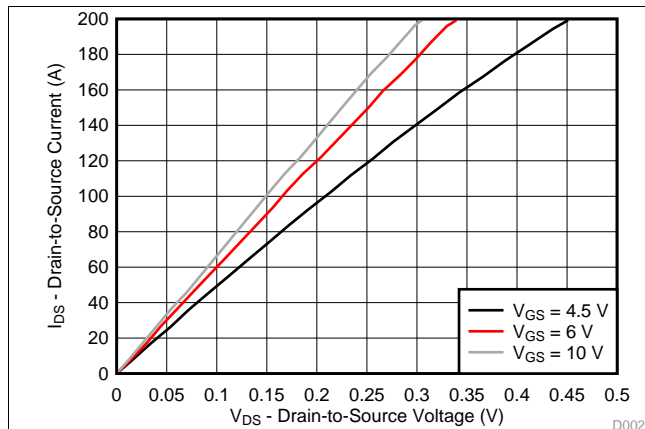


Figure 2. Saturation Characteristics

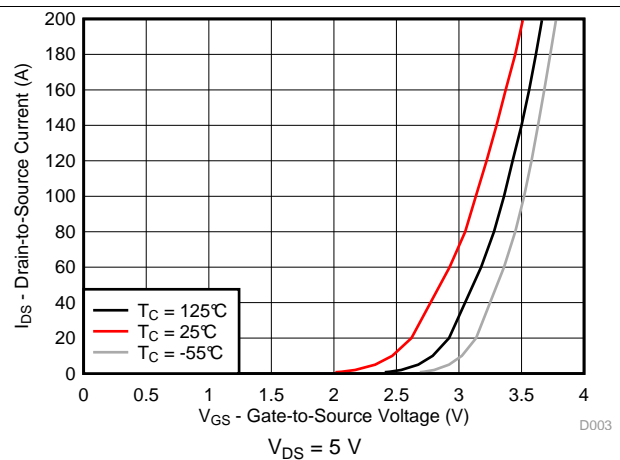


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

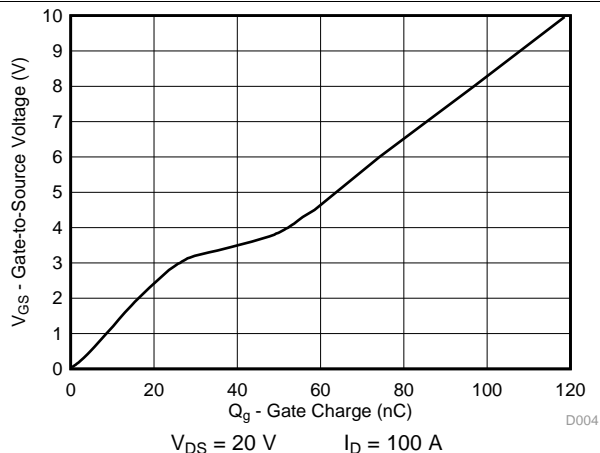


Figure 4. Gate Charge

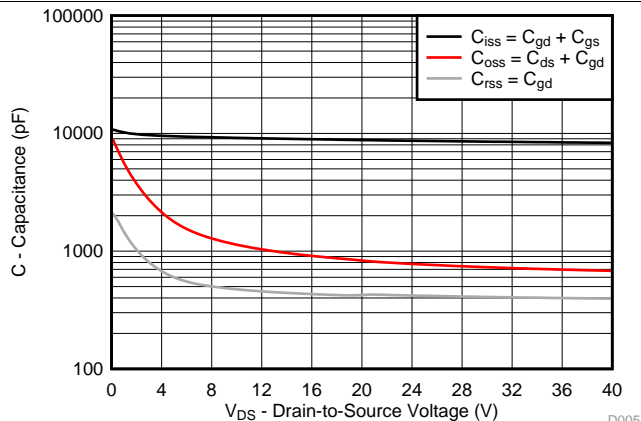


Figure 5. Capacitance

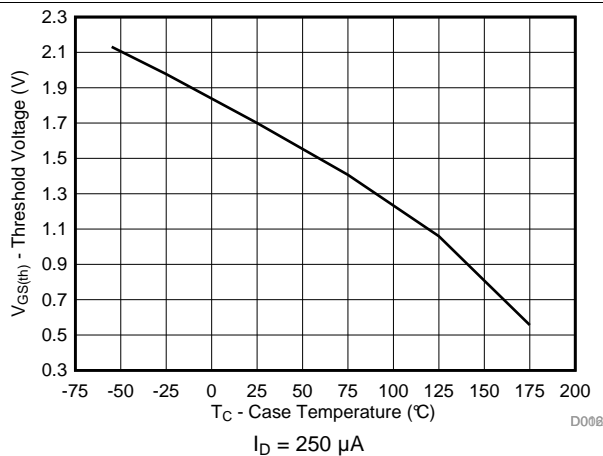


Figure 6. Threshold Voltage vs Temperature

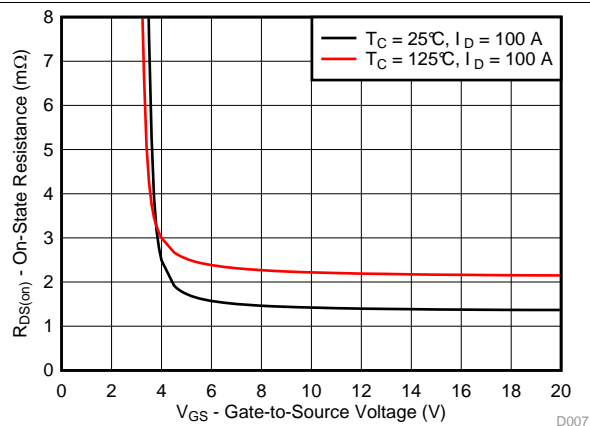


Figure 7. On-State Resistance vs Gate-to-Source Voltage

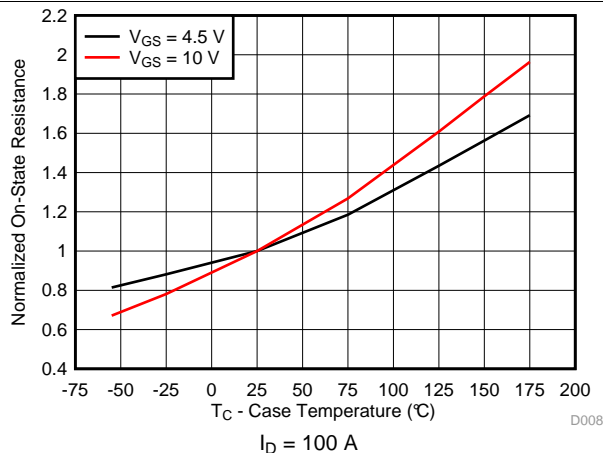


Figure 8. Normalized On-State Resistance vs Temperature

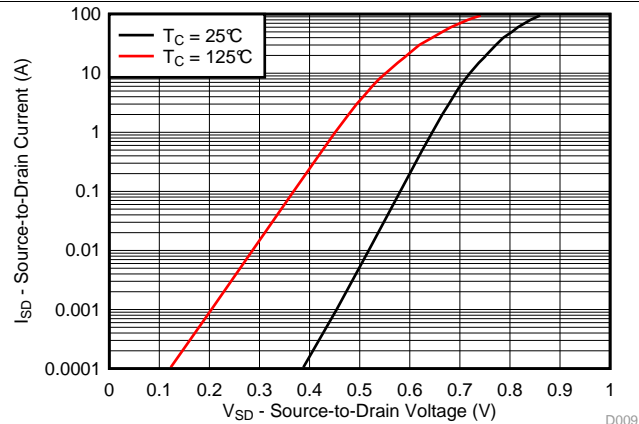


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

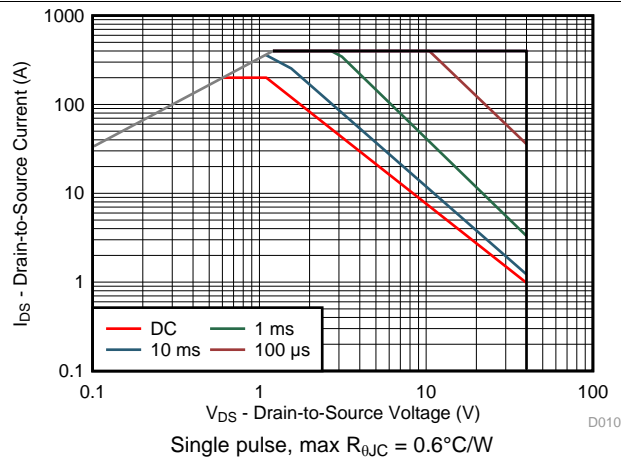


Figure 10. Maximum Safe Operating Area

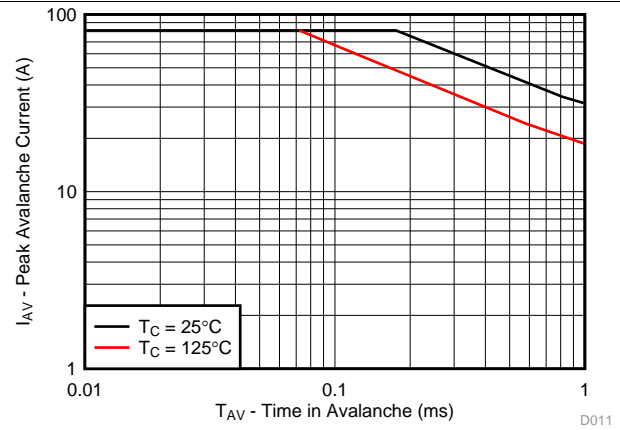


Figure 11. Single Pulse Unclamped Inductive Switching

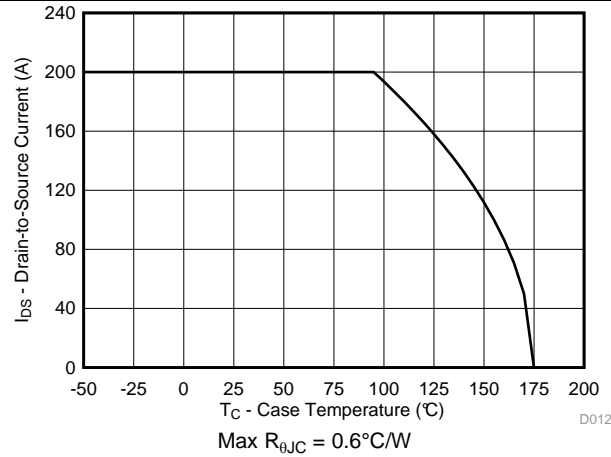


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
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6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

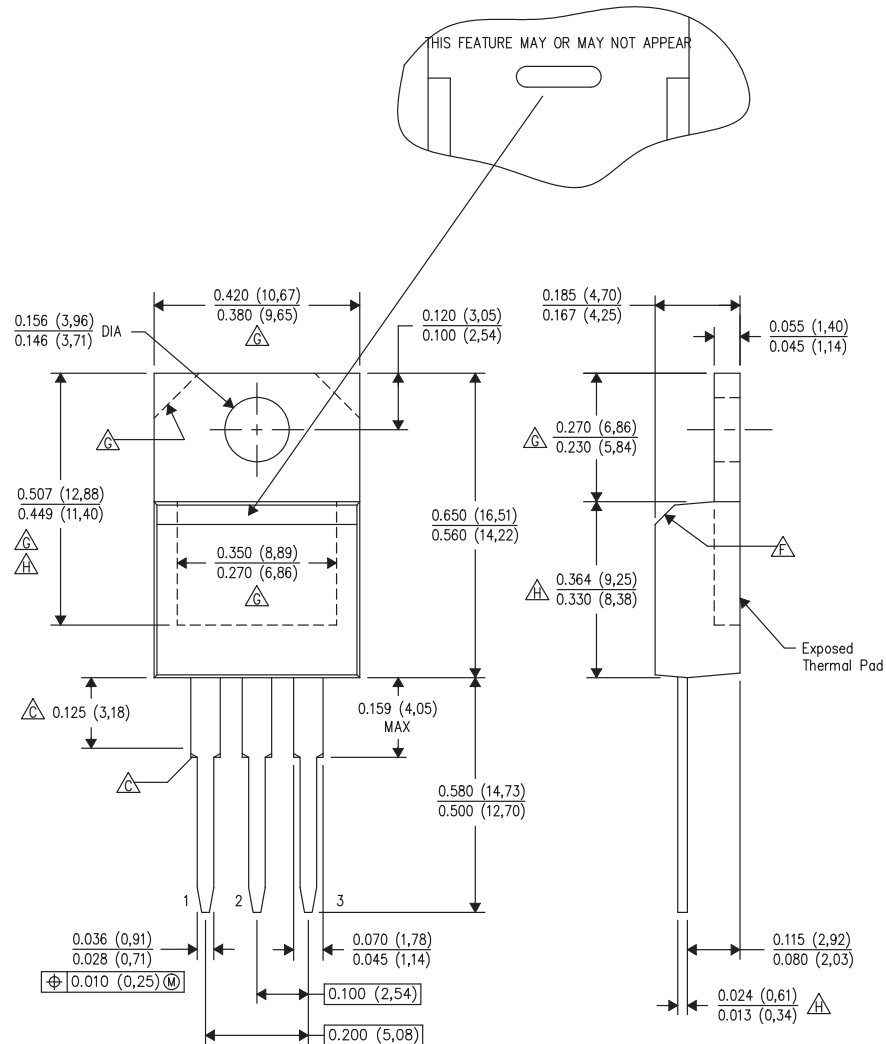
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KCS Package Dimensions



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Lead dimensions are not controlled within this area. Chamfer may or may not appear
 - D. All lead dimensions apply before solder dip.
 - E. The center lead is in electrical contact with the mounting tab.
 - F. The chamfer is optional.
 - G. Thermal pad contour optional within these dimensions.
 - H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

Table 1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18510KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS Exempt)	CU SN	N / A for Pkg Type	-55 to 175	CSD18510KCS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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