MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL
(Formerly West Bengal University of Technology) Syllabus
of BCA
(Effective from 2023-24 Academic Sessions)

SEMESTER: II

DEFINITION OF CREDIT

1 HR LECTURE PER WEEK	1 CREDIT
1 HR TUTORIAL PER WEEK	1CREDIT
2 HR PRACTICAL PER WEEK	1 CREDIT

SUBJECT NUMBERING SCHEME:

CODE FOR THE DEPT. OFFERING SUBJECT	SUBJECT TYPE	SEM	SUBJECT CODE

C	CORE MAJOR

SUBJECT NAME: Computer Architecture **Credit: 3L + 2P**
SUBJECT CODE: BCAC201

COURSE OBJECTIVE:

The objective of the course "Computer Architecture" is to provide students with a comprehensive understanding of the fundamental principles, components, and design principles that govern modern computer systems. Throughout the course, students will delve into the intricate workings of computer hardware, its organization, and how it interacts with software. The main goals are to enable students to grasp the inner workings of computers, analyze their performance, and make informed design decisions for efficient and reliable computing systems.

COURSE OUTCOME	
CO1	To enable the students to understand the functionality and implementation of computer system.
CO2	To familiarize with the various instruction codes and formats of different CPUs.

CO3	To introduce the students to I/O and memory organization of computer system
CO4	To deliver an overview of Control Unit of a computer system
CO5	To learn the usage of parallel and vector processing.

DETAILED SYLLABUS:

Module No:	NAME OF THE TOPIC	HOURS	MARKS
M1	Data Representation: Number Systems – decimal, binary, octal, hexadecimal, alphanumeric representation, 2. Complements – 1's complement, 2' complement, 9's complement, 10' complement, [r-1]'s complement, r's complement, 3. Fixed point representation – Integer representation, arithmetic addition, arithmetic subtraction, overflow, decimal fixed point representation, 4. Floating point representation, 5. IEEE 754 floating point representation	**4**	**5**
M2	Computer arithmetic: Addition algorithm of sign magnitude numbers, Subtraction algorithm of sign magnitude numbers, Addition algorithm of signed 2's complement data, Subtraction algorithm of signed 2's complement data, Multiplication algorithm, Booth's algorithm, Division algorithm	**4**	**5**
M3	Register transfer and micro-operations: Register transfer language, Register transfer, Bus system for registers, Memory transfers – memory read, memory write, Micro operations – register transfer micro operations, arithmetic micro operations, logic micro operations, shift micro operations, Binary adder, binary adder subtractor, binary incrementer, arithmetic circuit for arithmetic micro operations, One stage logic circuit, Selective set, Selective complement, Selective clear, ask, Insert, Clear	**5**	**5**
M4	Basic Computer organization and design: Instruction codes, Direct address, Indirect address & Effective address, List of basic computer registers, Computer instructions: memory reference, register reference & input – output instructions, Block diagram & brief idea of control unit of basic computer, Instruction cycle	**4**	**5**
M5	Micro programmed control: Control memory, Address sequencing, Micro program examples	**4**	**5**

M6	Central processing unit: General register organization, Stack organization, Register stack, Memory stack, Stack operations – push & pop, Evaluation of arithmetic expression using stack, Instruction format, Types of CPU organization [single accumulator, general register & stack organization] & example of their instructions, Three, two, one & zero address instruction, Definition and example of data transfer, data manipulation & program control instructions, Basic idea of different types of interrupts [external, internal & software interrupts], Difference between RISC & CISC	**6**	**5**
M7	Pipeline and vector processing: Parallel processing, Flynn's classification, Pipelining, Example of pipeline, space time diagram, speedup, Basic idea of arithmetic pipeline, example of floating point addition/ subtraction using pipeline	**6**	**10**
M8	Input – output organization: Peripheral devices, Input – output interface, Isolated I/O, Memory mapped I/O, Asynchronous data transfer: strobe & handshaking, Programmed I/O, Interrupt initiated I/O, Basic idea of DMA & DMAC Input – output processor	**6**	**10**
M9	Memory organization: Memory hierarchy, Main memory definition, types of main memory, types of RAM, ROM, difference between SRAM & DRAM, Cache memory, Cache memory mapping – Direct, Associative, Set Associative, CAM, hardware organization of CAM, Virtual memory, mapping using pages, page fault, mapping using segments, TLB, Auxiliary memory, diagrammatic representation of magnetic disk & hard disk drive, Definitions of seek time, rotational delay, access time, transfer time, latency	**6**	**20**
	INTERNAL EXAMINATION	**3**	**30**
	TOTAL	**48**	**100**

Practical:

SUBJECT NAME: Computer Architecture Lab **Credit: 2**
SUBJECT CODE: BCAC291

List of Practical:

1. Basic gates and Universal gates. Implementation of Half & full adder. Half & full subtractor,
2. 4 bit logical unit, 4 bit arithmetic unit, BCD adder, 4 bit adder/ subtractor, Carry look ahead adder, Design of ALU for multi bit operation, comparators.
3. 8:1 MUX IC verification, 16:1 MUX using IC 74151, dual 2 to 4 Decoder/ Demultiplexer IC evaluation. Priority encoder.
4. Read/ write operation using RAM IC, Cascading RAM ICs

SUGGESTED READING:

1. V. Carl, G. Zvonko and S. G. Zaky, "Computer organization", McGraw Hill, 1978.

2. B. Brey and C. R. Sarma, "The Intel microprocessors", Pearson Education, 2000.

3. J. L. Hennessy and D. A. Patterson, "Computer Architecture A Quantitative Approach", Morgan Kauffman, 2011.

4. W. Stallings, "Computer organization", PHI, 1987.

5. M. Morris Mano "Computer System Architecture " PEARSON

6. Rajaraman – "Computer Organization & Architecture", PHI

7. B.Ram – "Computer Organization & Architecture", Newage Publications

8. J.P. Hayes " Computer Architecture & Organisation", TATA MCGRAW HILL