CHAPTER 5 Transistors Bias Circuits

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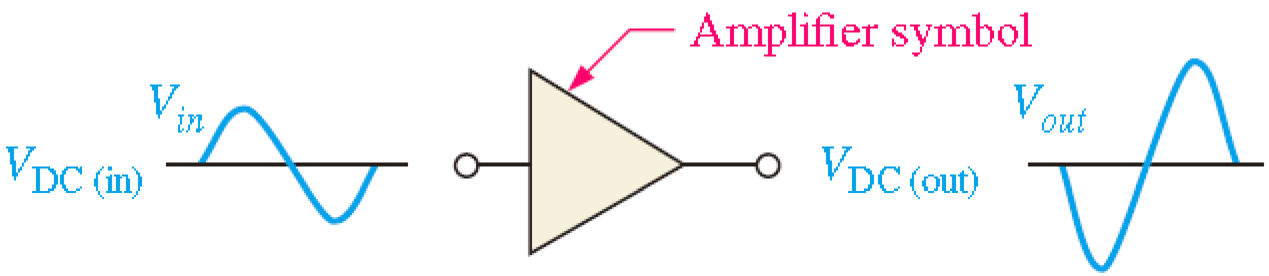
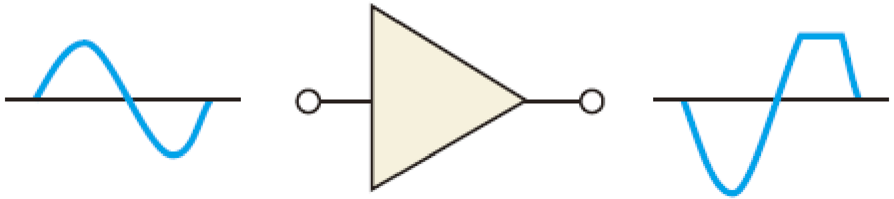
5.1 The DC Operation Point   DC Bias

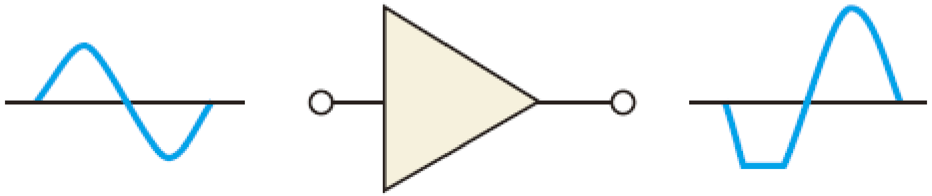
- Bias establishes the dc operating point (Q-point) for proper linear operation of an amplifier. If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied. Figure 5–1 shows the effects of proper and improper dc biasing of an inverting



(a) Linear operation: larger output has same shape as input except that it is inverted



(b) Nonlinear operation: output voltage limited (clipped) by cutoff

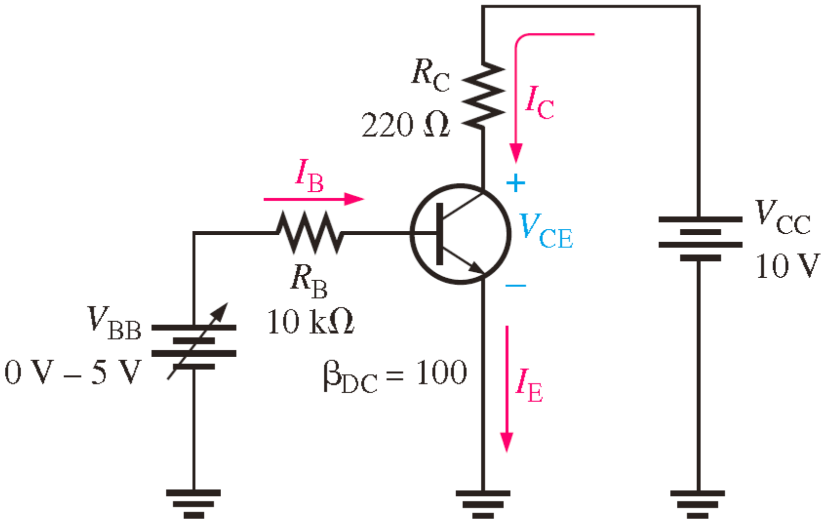


(c) Nonlinear operation: output voltage limited (clipped) by saturation

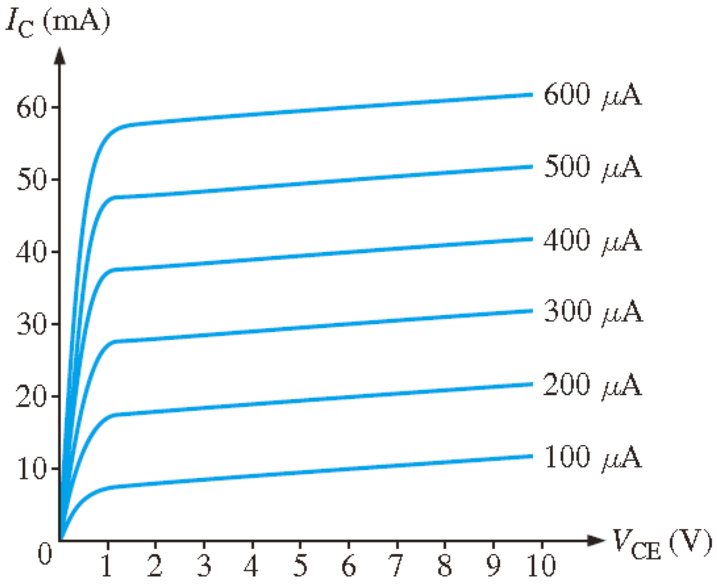
FIGURE 5-1
Examples of linear and nonlinear operation of an inverting amplifier (the triangle symbol).

Graphical Analysis

- The transistor in Figure 5–2(a) is biased with V_{CC} and V_{BB} to obtain certain values of I_B, I_C, IE, and V_{CE}. The collector characteristic curves for this particular transistor are shown in Figure 5–2(b); we will use these curves to graphically illustrate the effects of dc bias.



(a) DC biased circuit



(b) Collector characteristic curves

FIGURE 5-2

A dc-biased transistor circuit with variable bias voltage (V_{BB}) for generating the collector characteristic curves shown in part (b).

Graphical Analysis

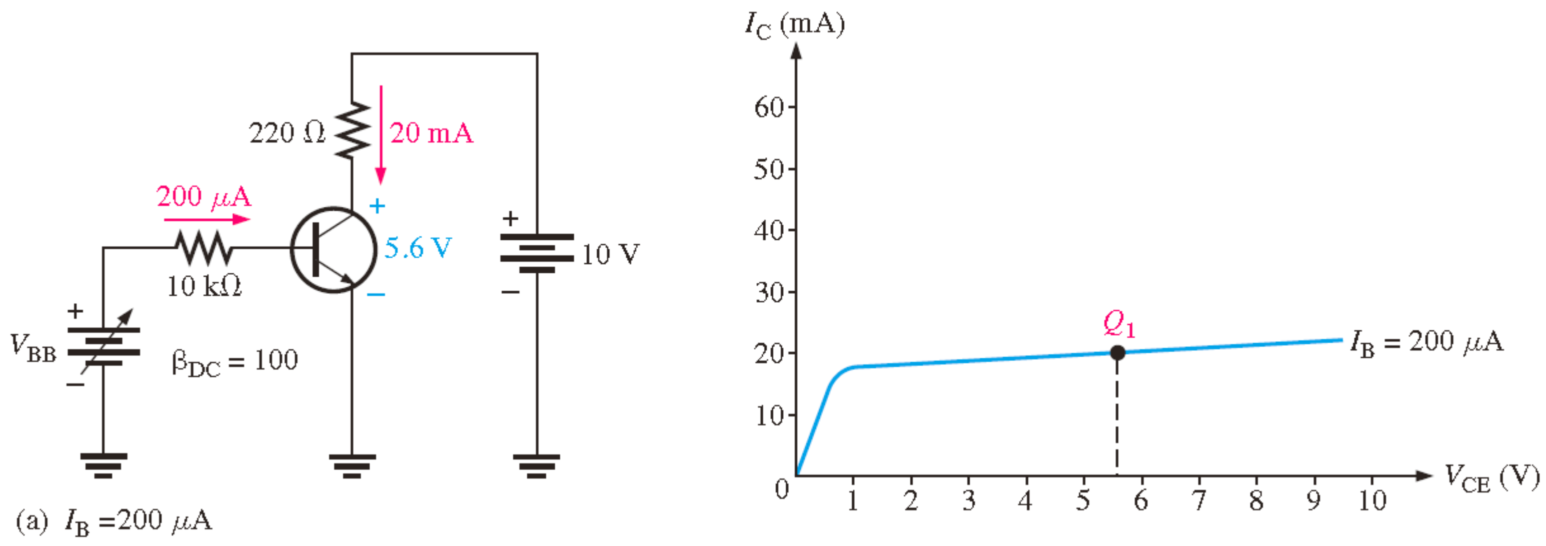


FIGURE 5-3 Illustration of Q-point adjustment.

In Figure 5–3, we assign three values to I_B and observe what happens to I_C and V_{CE}. First, V_{BB} is adjusted to produce an I_B of 200 μA, as shown in Figure 5–3(a). Since $I_C = \beta_{DC} I_B$, the collector current is 20 mA, as indicated, and

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (20\text{ mA})(220\ \Omega) = 10\text{ V} - 4.4\text{ V} = 5.6\text{ V}$$

Graphical Analysis

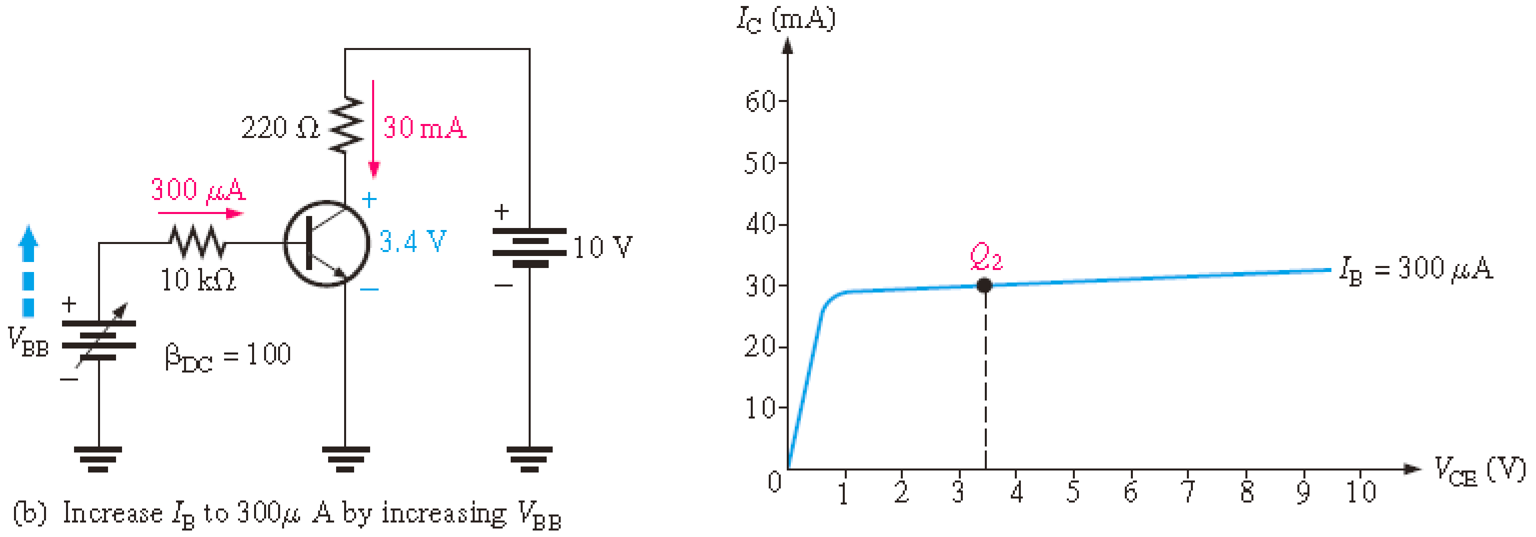


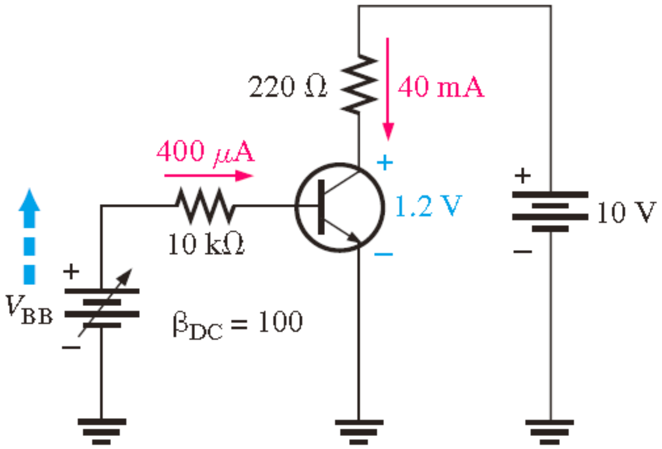
FIGURE 5-3 Illustration of Q-point adjustment.

Next, as shown in Figure 5–3(b), V_{BB} is increased to produce an I_B of 300 μA and an I_C of 30 mA.

$$V_{CE} = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 10\text{ V} - 6.6\text{ V} = 3.4\text{ V}$$

The Q-point for this condition is indicated by Q_2 on the graph.

Graphical Analysis



(c) Increase I_B to 400μ A by increasing V_{BB}

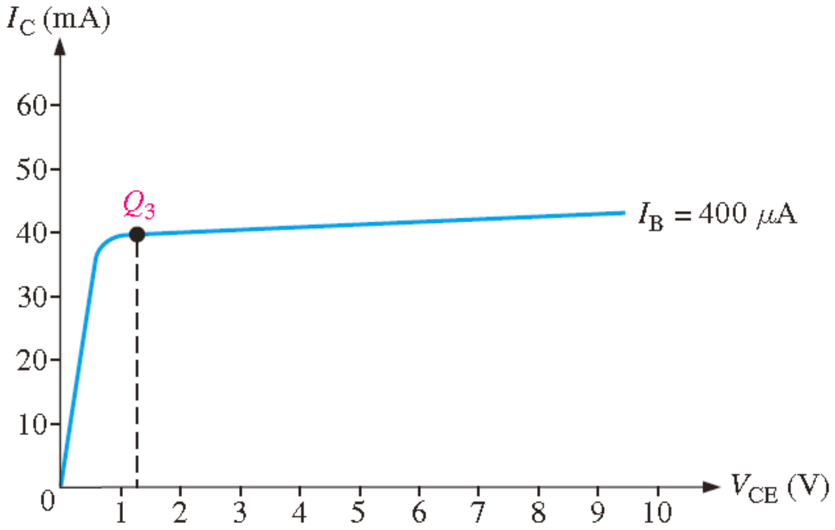


FIGURE 5-3 Illustration of Q-point adjustment.

Finally, as in Figure 5–3(c), V_{BB} is increased to give an I_B of 400 μA and an I_C of 40 mA.

$$V_{CE} = 10\text{ V} - (40\text{ mA})(220\ \Omega) = 10\text{ V} - 8.8\text{ V} = 1.2\text{ V}$$

Q_3 is the corresponding Q-point on the graph.

DC Load Line

- The dc operation of a transistor circuit can be described graphically using a dc load line. This is a straight line drawn on the characteristic curves from the saturation value where $I_C = I_{C(sat)}$ on the y-axis to the cutoff value where $V_{CE} = V_{CC}$ on the x-axis, as shown in Figure 5–4(a).

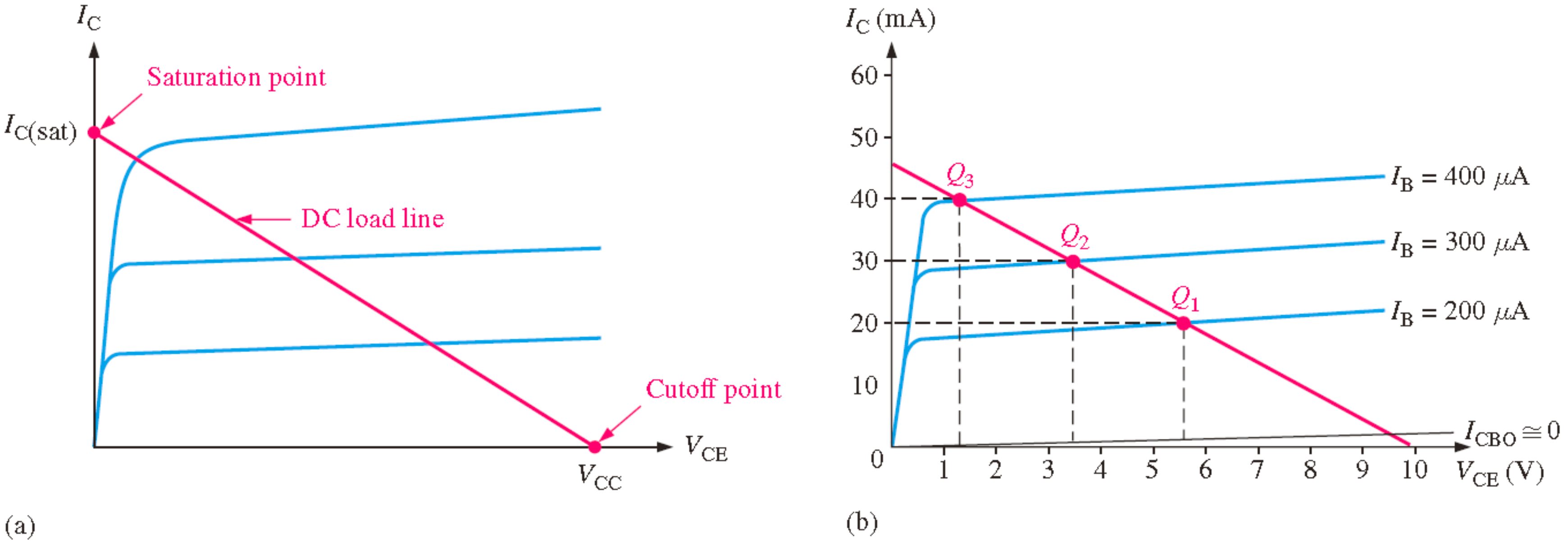


FIGURE 5-4 The dc load line.

DC Load Line

- The equation for I_C is $I_C = \dfrac{V_{CC} - V_{CE}}{R_C} = \dfrac{V_{CC}}{R_C} - \dfrac{V_{CE}}{R_C} = -\dfrac{V_{CE}}{R_C} + \dfrac{V_{CC}}{R_C} = -\left(\dfrac{1}{R_C}\right)V_{CE} + \dfrac{V_{CC}}{R_C}$

This is the equation of a straight line with a slope of $-1/R_C$, an x intercept of $V_{CE} = V_{CC}$, and a y intercept of V_{CC}/R_C, which is $I_{C(sat)}$.

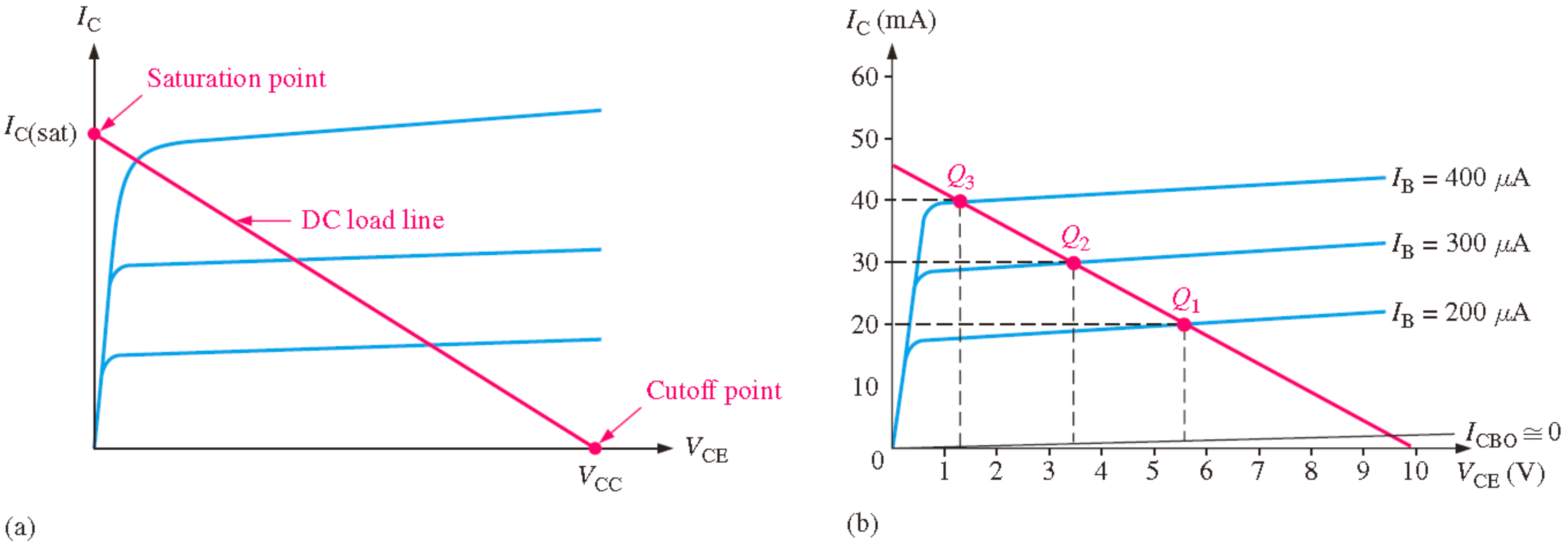
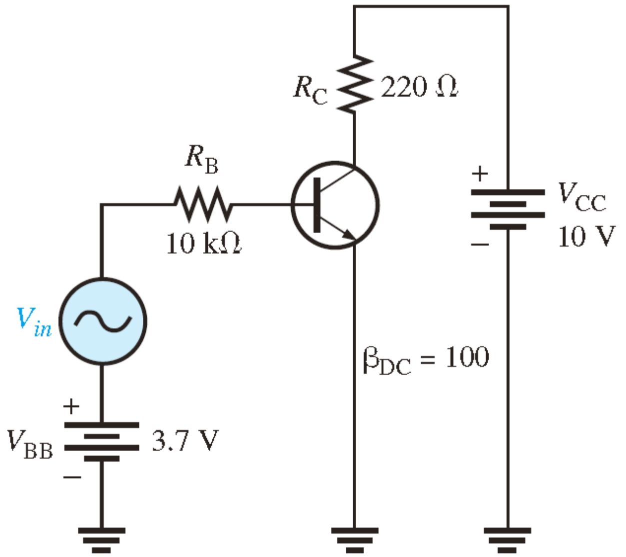


FIGURE 5-4 The dc load line.

Linear Operation

- The region along the load line including all points between saturation and cutoff is generally known as the linear region of the transistor's operation. As long as the transistor is operated in this region, the output voltage is a linear reproduction of the input.



$$I_{BQ} = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{3.7\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 300\ \mu\text{A}$$

$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\ \mu\text{A}) = 30\text{ mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 3.4\text{ V}$$

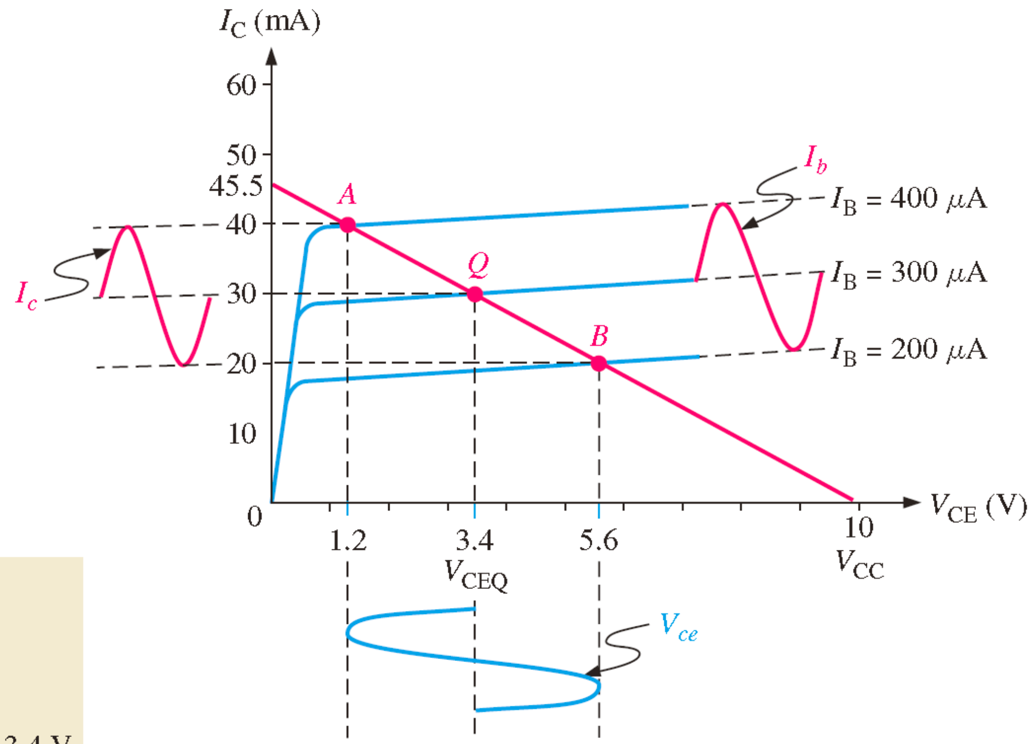
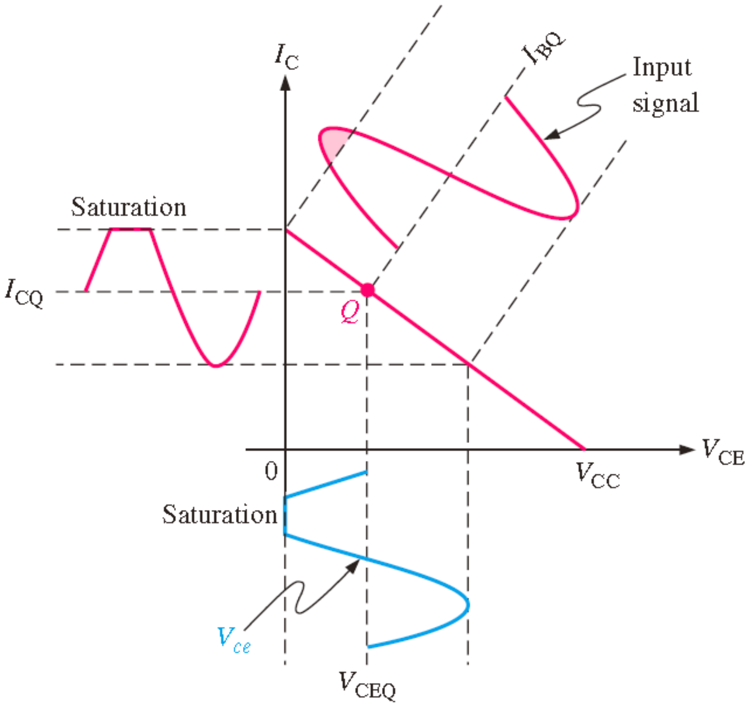


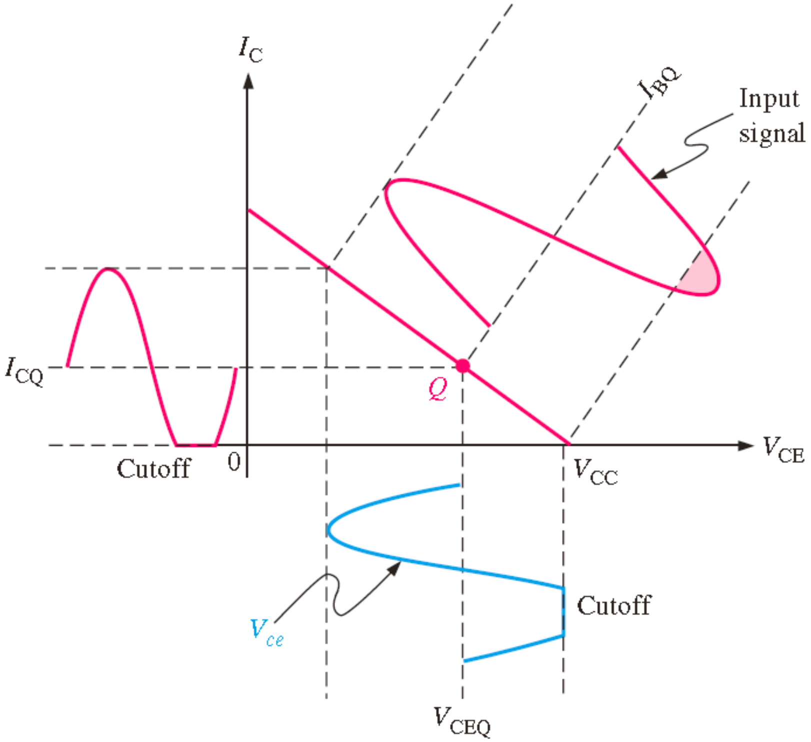
FIGURE 5-5 Variations in collector current and collector-to-emitter voltage as a result of a variation in base current.

Waveform Distortion

- As previously mentioned, under certain input signal conditions the location of the Q-point on the load line can cause one peak of the V_{ce} waveform to be limited or clipped, as shown in parts (a) and (b) of Figure 5–6.



(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.



(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.

FIGURE 5-6 Graphical load line illustration of a transistor being driven into saturation and/or cutoff.

5-2 Voltage-divider Bias

- A more practical bias method is to use V_{CC} as the single bias source, as shown in Figure 5–9. To simplify the schematic, the battery symbol is omitted and replaced by a line termination circle with a voltage indicator (V_{CC}) as shown.

- <u>A dc bias voltage at the base of the transistor can be developed by a resistive voltage divider that consists of R_1 and R_2</u>, as shown in Figure 5–9. V_{CC} is the dc collector supply voltage. Two current paths are between point A and ground: one through R_2 and the other through the base-emitter junction of the transistor and R_E.

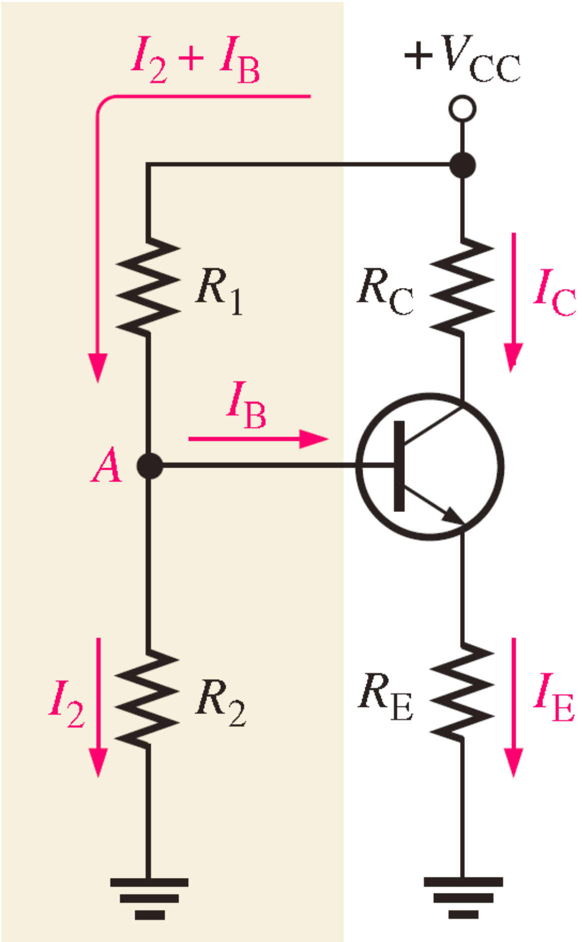


FIGURE 5-9 Voltage-divider bias.

Voltage-divider Bias

- A voltage divider in which the base current is small compared to the current in R_2 is said to be a stiff voltage divider because the base voltage is relatively independent of different transistors and temperature effects.

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

$$V_E = V_B - V_{BE}$$

$$I_C \cong I_E = \frac{V_E}{R_E}$$

$$V_C = V_{CC} - I_C R_C$$

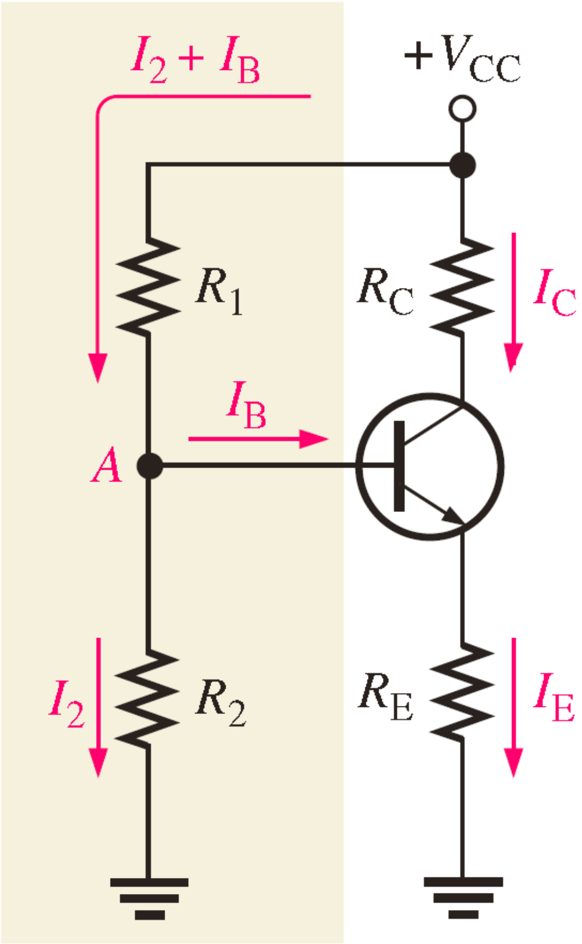


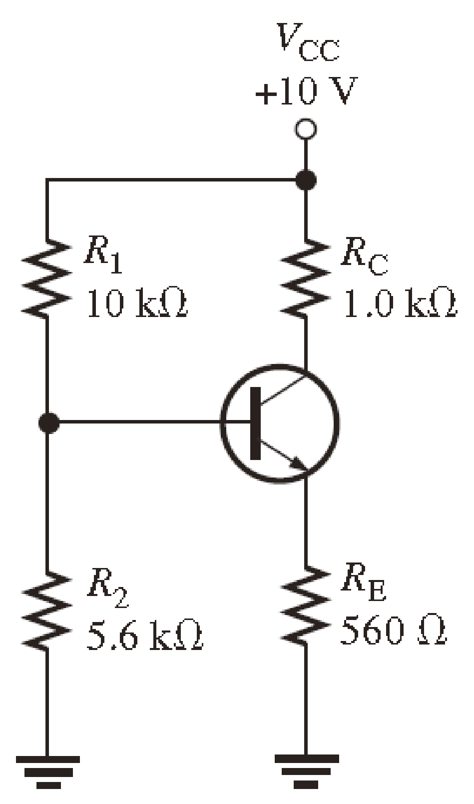
FIGURE 5-9 **Voltage-divider bias.**

Example

EXAMPLE 5–2

Determine V_{CE} and I_C in the stiff voltage-divider biased transistor circuit of Figure 5–10 if $\beta_{DC} = 100$.

▶ FIGURE 5–10



Example

Solution The base voltage is

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{5.6\ \text{k}\Omega}{15.6\ \text{k}\Omega}\right)10\ \text{V} = 3.59\ \text{V}$$

So,

$$V_E = V_B - V_{BE} = 3.59\ \text{V} - 0.7\ \text{V} = 2.89\ \text{V}$$

and

$$I_E = \frac{V_E}{R_E} = \frac{2.89\ \text{V}}{560\ \Omega} = 5.16\ \text{mA}$$

Therefore,

$$I_C \cong I_E = \mathbf{5.16\ mA}$$

and

$$V_C = V_{CC} - I_C R_C = 10\ \text{V} - (5.16\ \text{mA})(1.0\ \text{k}\Omega) = 4.84\ \text{V}$$
$$V_{CE} = V_C - V_E = 4.84\ \text{V} - 2.89\ \text{V} = \mathbf{1.95\ V}$$

5-3 Other Bias Methods   Emitter Bias

- Emitter bias provides excellent bias stability in spite of changes in β or temperature. It uses both a positive and a negative supply voltage.

$$V_{EE} + V_{R_B} + V_{BE} + V_{R_E} = 0$$

Substituting, using Ohm's law,

$$V_{EE} + I_B R_B + V_{BE} + I_E R_E = 0$$

Substituting for $I_B \cong I_E/\beta_{DC}$ and transposing V_{EE},

$$\left(\frac{I_E}{\beta_{DC}}\right)R_B + I_E R_E + V_{BE} = -V_{EE}$$

Factoring out I_E and solving for I_E,

$$I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}}$$

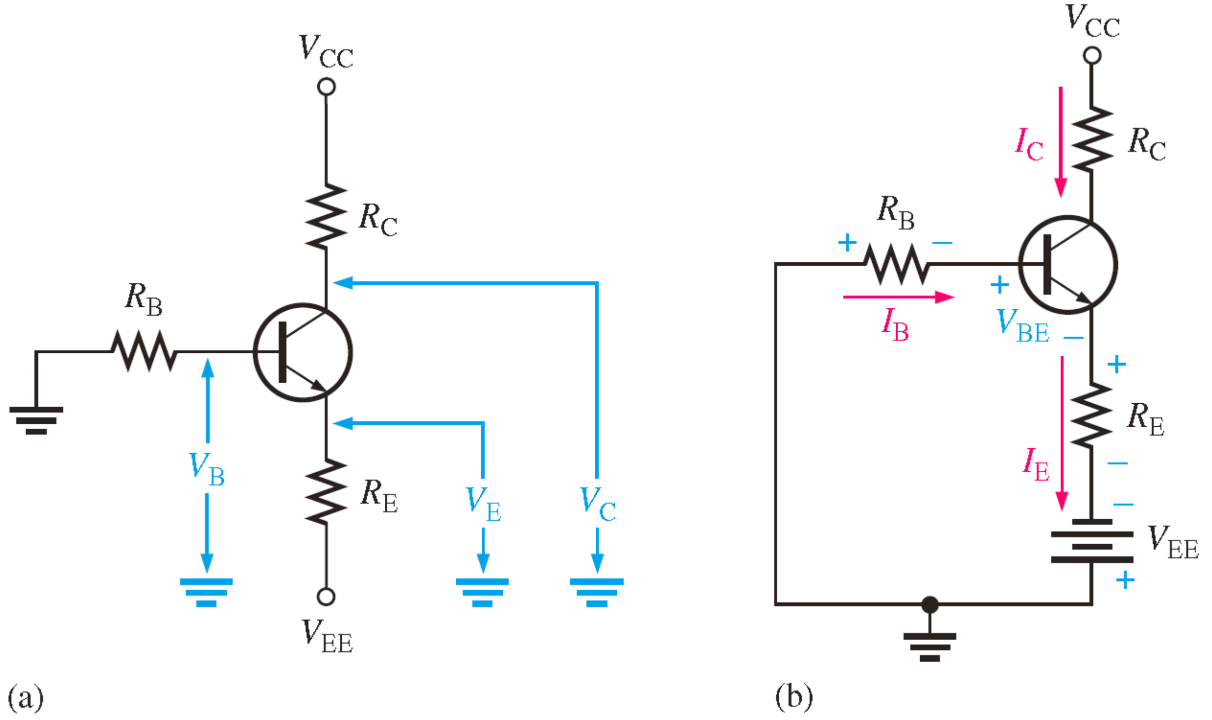


FIGURE 5-11
An npn transistor with emitter bias. Voltages with respect to ground are indicated with a single subscript.

Emitter Bias

Voltages with respect to ground are indicated by a single subscript. The emitter voltage with respect to ground is

$$V_E = V_{EE} + I_E R_E$$

The base voltage with respect to ground is

$$V_B = V_E + V_{BE}$$

The collector voltage with respect to ground is

$$V_C = V_{CC} - I_C R_C$$

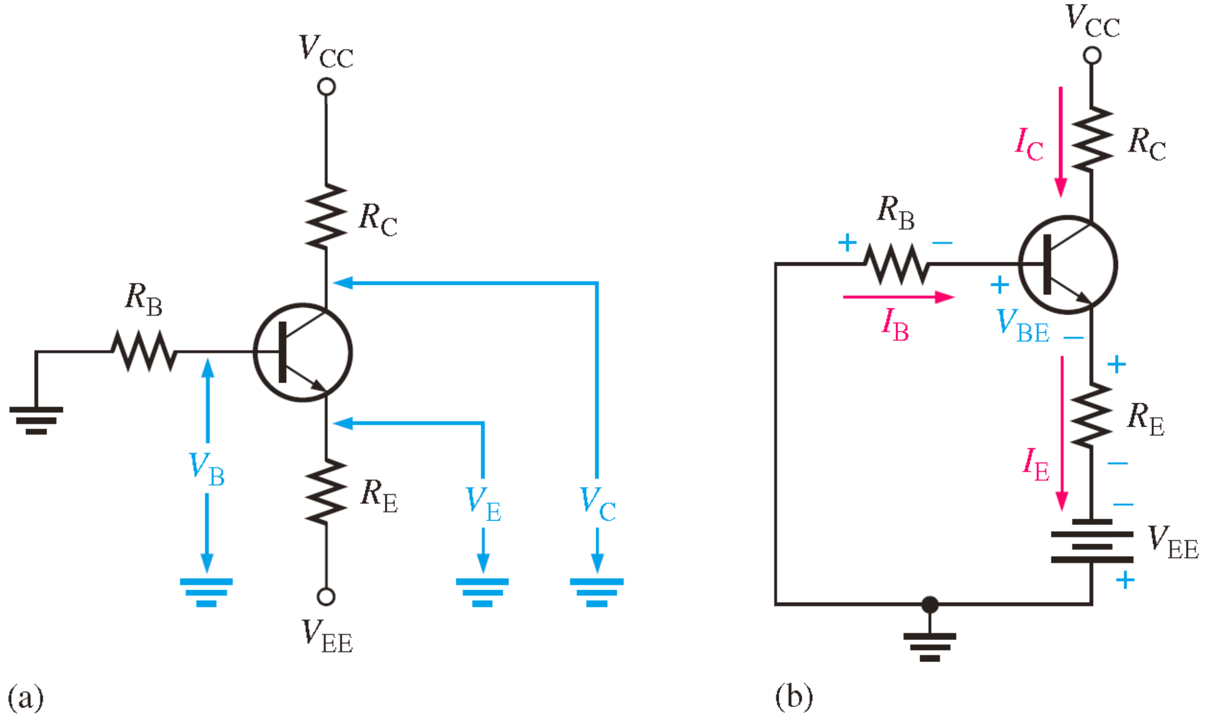


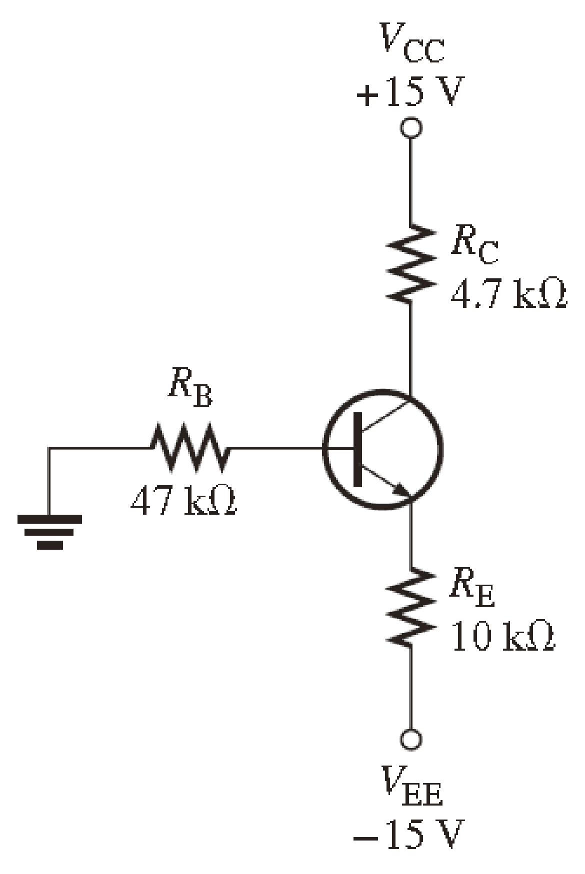
FIGURE 5-11
An npn transistor with emitter bias. Voltages with respect to ground are indicated with a single subscript.

Example

EXAMPLE 5–7

Determine how much the Q-point (I_C, V_{CE}) for the circuit in Figure 5–18 will change if β_{DC} increases from 100 to 200 when one transistor is replaced by another.

▶ FIGURE 5–18



Example

Solution For $\beta_{DC} = 100$,

$$I_{C(1)} \cong I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{-(-15\text{ V}) - 0.7\text{ V}}{10\text{ k}\Omega + 47\text{ k}\Omega/100} = 1.37\text{ mA}$$

$$V_C = V_{CC} - I_{C(1)}R_C = 15\text{ V} - (1.37\text{ mA})(4.7\text{ k}\Omega) = 8.56\text{ V}$$

$$V_E = V_{EE} + I_E R_E = -15\text{ V} + (1.37\text{ mA})(10\text{ k}\Omega) = -1.3\text{ V}$$

Therefore,

$$V_{CE(1)} = V_C - V_E = 8.56\text{ V} - (-1.3\text{ V}) = 9.83\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} \cong I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{-(-15\text{ V}) - 0.7\text{ V}}{10\text{ k}\Omega + 47\text{ k}\Omega/200} = 1.38\text{ mA}$$

$$V_C = V_{CC} - I_{C(2)}R_C = 15\text{ V} - (1.38\text{ mA})(4.7\text{ k}\Omega) = 8.51\text{ V}$$

$$V_E = V_{EE} + I_E R_E = -15\text{ V} + (1.38\text{ mA})(10\text{ k}\Omega) = -1.2\text{ V}$$

Therefore,

$$V_{CE(2)} = V_C - V_E = 8.51\text{ V} - (-1.2\text{ V}) = 9.71\text{ V}$$

Base Bias

- Base bias is common in switching circuits, and it has the advantage of simplicity because it uses only one resistor to obtain bias.

$$V_{CC} - V_{R_B} - V_{BE} = 0$$

Substituting $I_B R_B$ for V_{R_B}, you get

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Then solving for I_B,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

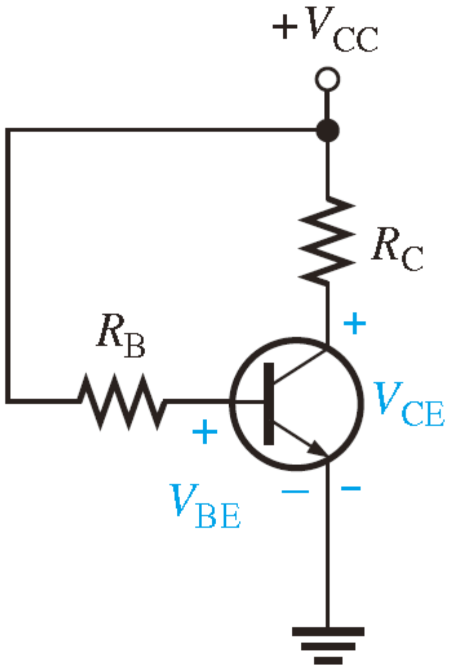


FIGURE 5-12
Base bias.

Base Bias

Kirchhoff's voltage law applied around the collector circuit in Figure 5–19 gives the following equation:

$$V_{CC} - I_C R_C - V_{CE} = 0$$

Solving for V_{CE},

$$\mathbf{V_{CE} = V_{CC} - I_C R_C}$$

Substituting the expression for I_B into the formula $I_C = \beta_{DC} I_B$ yields

$$\mathbf{I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right)}$$

Q-Point Stability of Base Bias Notice the above Equation shows that I_C is dependent on β_{DC}. The disadvantage of this is that a variation in β_{DC} causes I_C and, as a result, V_{CE} to change, thus changing the Q-point of the transistor. This makes the base-bias circuit extremely β-dependent and unpredictable.

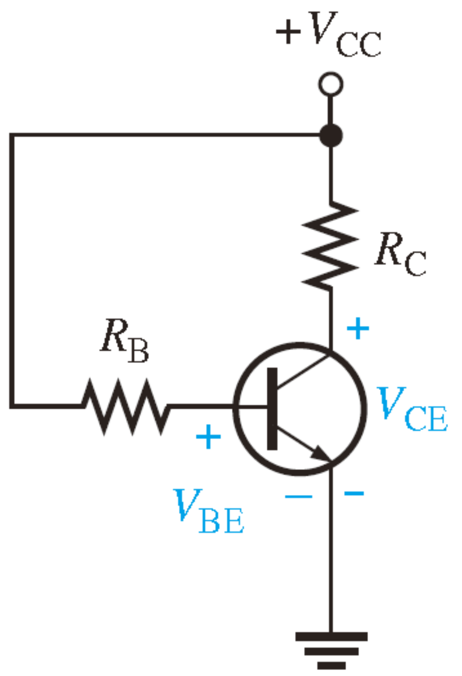


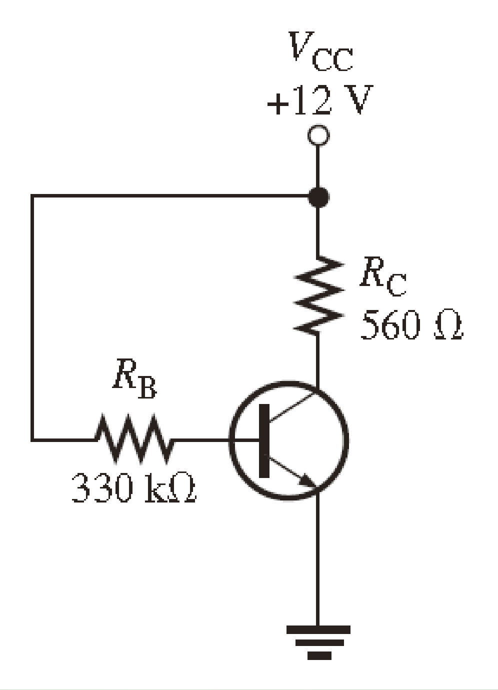
FIGURE 5-12
Base bias.

Example

EXAMPLE 5–8

Determine how much the Q-point (I_C, V_{CE}) for the circuit in Figure 5–20 will change over a temperature range where β_{DC} increases from 100 to 200.

► FIGURE 5–20



Example

Solution For $\beta_{DC} = 100$,

$$I_{C(1)} = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 100\left(\frac{12\text{ V} - 0.7\text{ V}}{330\text{ k}\Omega}\right) = 3.42\text{ mA}$$

$$V_{CE(1)} = V_{CC} - I_{C(1)}R_C = 12\text{ V} - (3.42\text{ mA})(560\ \Omega) = 10.1\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 200\left(\frac{12\text{ V} - 0.7\text{ V}}{330\text{ k}\Omega}\right) = 6.84\text{ mA}$$

$$V_{CE(2)} = V_{CC} - I_{C(2)}R_C = 12\text{ V} - (6.84\text{ mA})(560\ \Omega) = 8.17\text{ V}$$

The percent change in I_C as β_{DC} changes from 100 to 200 is

$$\%\Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right)100\%$$

$$= \left(\frac{6.84\text{ mA} - 3.42\text{ mA}}{3.42\text{ mA}}\right)100\% = \mathbf{100\%}\ \text{(an increase)}$$

The percent change in V_{CE} is

$$\%\Delta V_{CE} = \left(\frac{V_{CE(2)} - V_{CE(1)}}{V_{CE(1)}}\right)100\%$$

$$= \left(\frac{8.17\text{ V} - 10.1\text{ V}}{10.1\text{ V}}\right)100\% = \mathbf{-19.1\%}\ \text{(a decrease)}$$