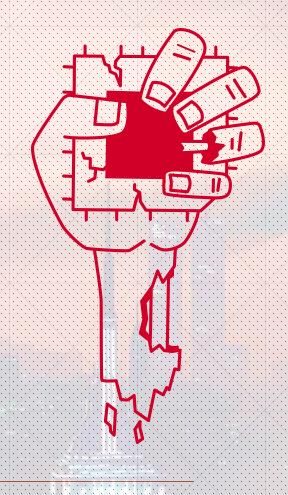


ZombieLoad

Cross-Privilege-Boundary Data Sampling

Michael Schwarz, Moritz Lipp, **Daniel Moghimi**, Jo Van Bulck, Julian Stecklina, Thomas Prescher, Daniel Gruss





whoami

- Daniel Moghimi (@danielmgmi)
- Computer Security Enthusiast since 2010
 - Reverse Engineering
 - Application Security
- PhD Student since 2017
 - Microarchitectural Security
 - Side Channels
 - Breaking Cryptographic Implementations





```
char secret = *(char *) 0xfffffff81a0123;
printf("%c\n", secret);
```

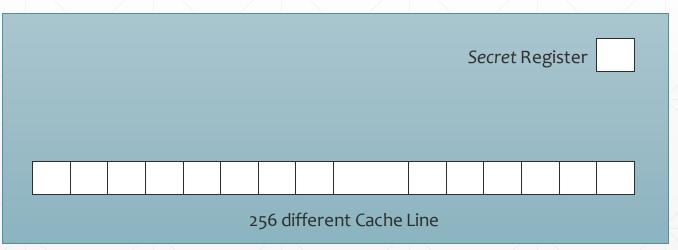
Segmentation Fault! Inaccessible Address.



```
char oracle[4096 * 256];
char secret = *(char *) 0xfffffff81a0123;
char x = \text{oracle[secret } * 4096];
for(char secret = 0; i < 256; i++){</pre>
   if(flush reload(oracle[i * 4096]) < threshold)</pre>
      printf("%c\n", i);
                                 CPU Microarchitecture
```

Virtual Address Space

User Space Oracle Kernel Space oxf...81a0123 P A S S W O R D





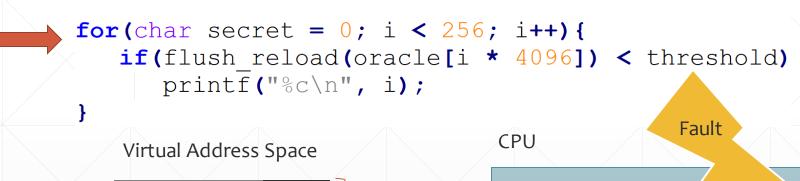
```
char oracle[4096 * 256];
        char secret = *(char *) 0xfffffff81a0123;
        char x = \text{oracle[secret } * 4096];
        for(char secret = 0; i < 256; i++){</pre>
            if(flush reload(oracle[i * 4096]) < threshold)</pre>
               printf("%c\n", i);
                                                             Fault
                                             CPU
            Virtual Address Space
                                 User Space
               Oracle
                                                                                      Secret Register
                                 Kernel Space
oxf...81a0123
           P A S S W O R D
                                                                   256 different Cache Line
```



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char oracle[4096 * 256];
        char secret = *(char *) 0xfffffff81a0123;
        char x = \text{oracle[secret } * 4096];
        for(char secret = 0; i < 256; i++){</pre>
           if(flush reload(oracle[i * 4096]) < threshold)</pre>
               printf("%c\n", i);
                                                            Fault
                                             CPU
            Virtual Address Space
               Oracle
                                                                                     Secret Register
                                 Space
                                 Kernel Space
oxf...81a0123
           P A S S W O R D
                                                                  256 different Cache Line
```



```
char oracle[4096 * 256];
char secret = *(char *) 0xffffffff81a0123;
char x = oracle[secret * 4096];
```

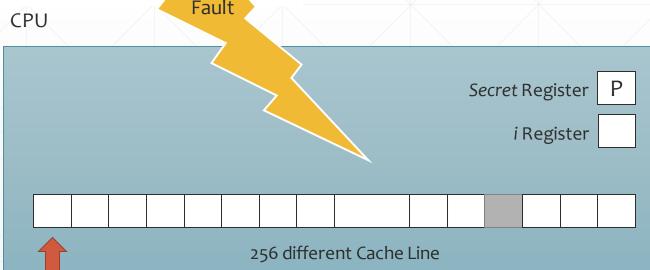


Oracle

oxf...81a0123 P A S S W O R D

Kernel Space

User Space

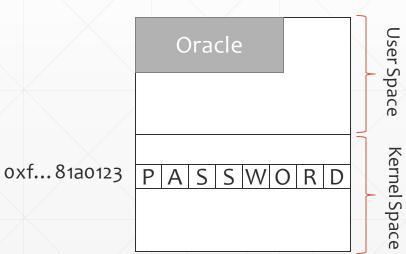


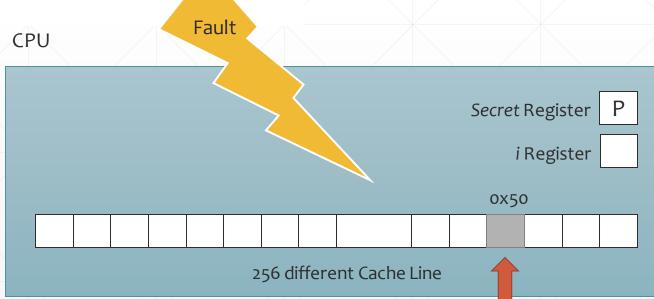


```
char oracle[4096 * 256];
char secret = *(char *) 0xffffffff81a0123;
char x = oracle[secret * 4096];
```



Virtual Address Space







Meltdown-style Attacks !!!

- What if we dereference addresses that causes other faults/assists?
- What if the Microarchitecture is in a specific state during the fault?
- Where does this data leak from?!







mov 0x401234, %rsi

mov (%rsi), %rax

Virtual Address

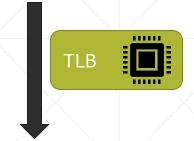


```
mov 0x401234, %rsi
```

mov (%rsi), %rax

Virtual Address

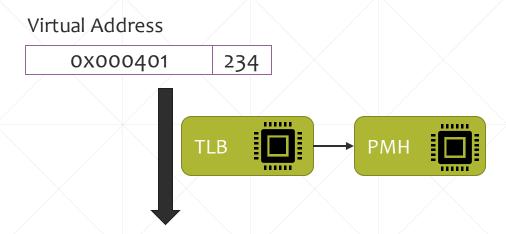
0x000401 234





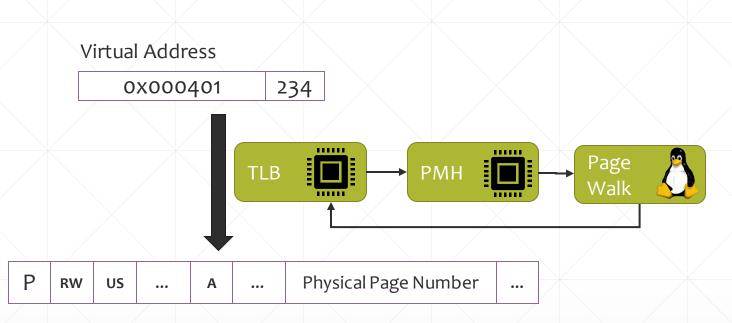
```
mov 0x401234, %rsi
```

mov (%rsi), %rax



mov 0x401234, %rsi

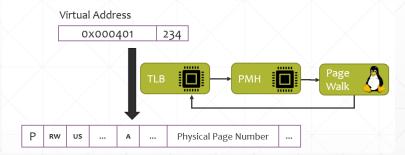
mov (%rsi), %rax





```
mov 0x401234, %rsi
```

mov (%rsi), %rax



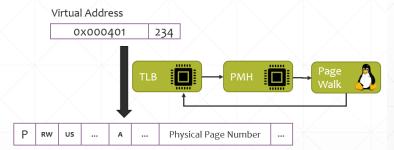
L₁D Cache

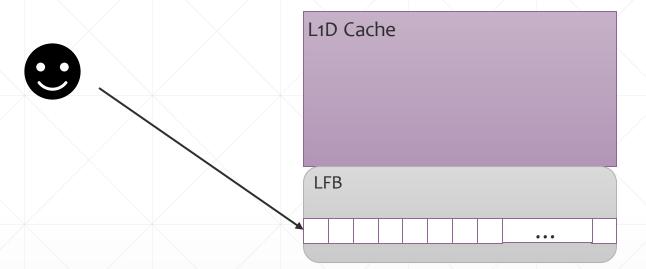
LFB



mov 0x401234, %rsi

mov (%rsi), %rax

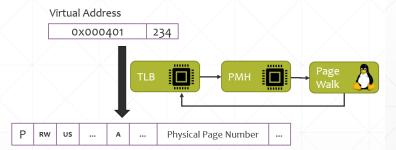


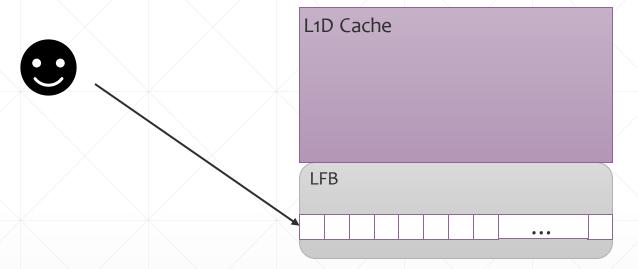




mov 0x401234, %rsi

mov (%rsi), %rax

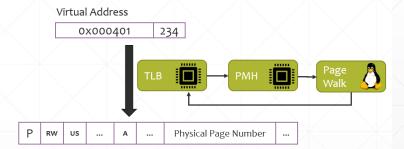


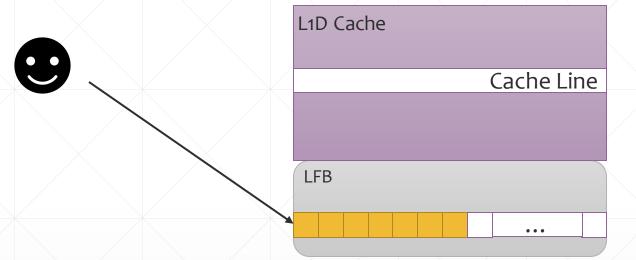




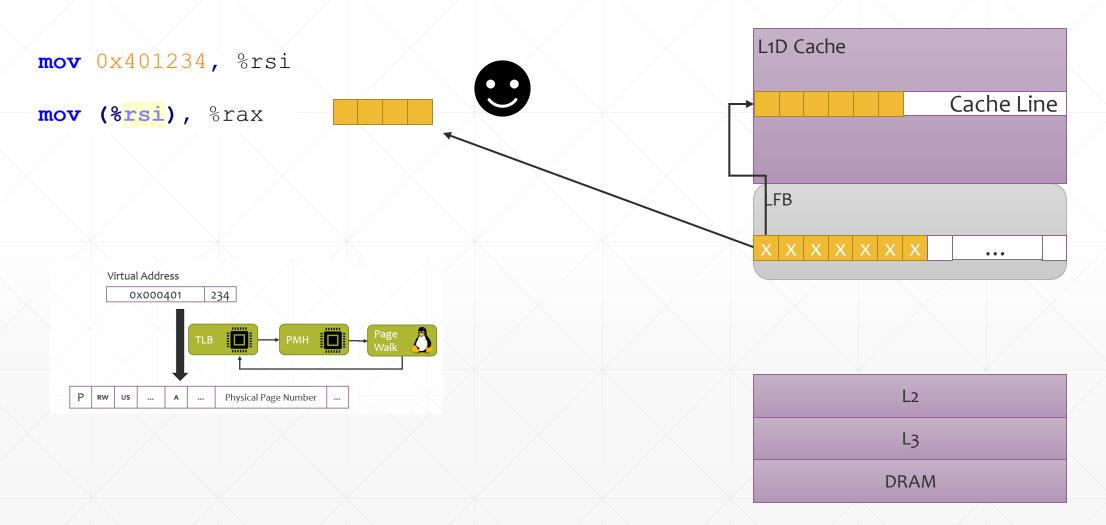
mov 0x401234, %rsi

mov (%rsi), %rax











P RW US ... A ... Physical Page Number ...

L₁D Cache

Cache Line

Cache Line

LFB (10 entries)



L2

L3





P RW US ... A ... Physical Page Number ...

L₁D Cache

Cache Line

LFB (10 entries)



L₃

L2





P RW US ... A ... Physical Page Number ...

L₁D Cache

Cache Line

LFB (10 entries)

X X X X X X X X X ...

L3

L2





P RW US ... A ... Physical Page Number ...

x x x x

L₁D Cache

Cache Line

LFB (10 entries)

X X X X X X X X ...

L₃

L2



P RW US ... A ... Physical Page Number ...

Cache Line

Cache Line

Cache Line

LFB (10 entries)

O O O X X X X X ... X



x x x x



P RW US ... A ... Physical Page Number ...

Cache Line

Cache Line

Cache Line

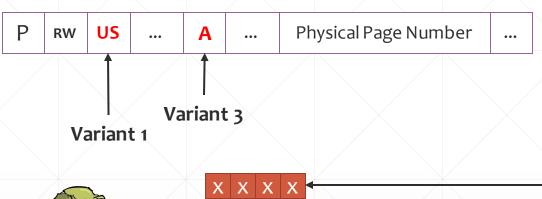
LFB (10 entries)

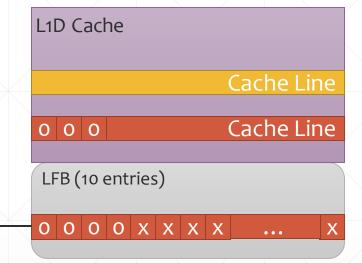
O O O X X X X X ... X



x x x x











Microcode Assist on 'A' Bit

- The CPU tells the OS if a page has been accessed or not by setting the Access Bit
- The OS can clear the bit and causes a microcode assist
- The microcode assist flushes the pipeline while setting the access bit



ZombieLoad VS. other Meltdown-Style Attacks

| | Page Number | | | Page Offset | |
|------------|-------------|---------------------|----------------|-------------|--|
| Meltdown | 51 | Physical Virtual | 12 11 | 0 | |
| Foreshadow | 51 47 | Physical Virtual | 12 11 | 0 | |
| Fallout | 51 47 | Physical Virtual | 12 12 | 0 | |
| ZombieLoad | 51 47 | Physical Virtual | 12 12 12 | 6 5 | |



What can we do with this data leakage?

- Attack across Process Context Switches
- Attack across Simultaneous Multithreading (SMT) AKA. Intel Hyperthreading



- We may leak bytes of data from other unimportant fill buffer entries
- Leak domino bytes to perform error correction

Target Secret

| 11010011 | 01111111 | 01111111 | ••• |
|----------|----------|----------|-----|
| | | | |



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- Leak domino bytes to perform error correction

Target Secret 11010011 0111111 01111111 ...

oxd3 ox10 ox4f



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- Leak domino bytes to perform error correction

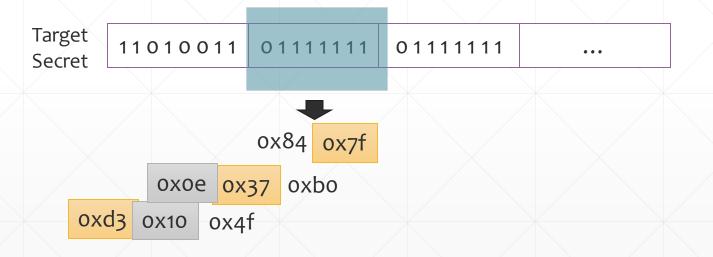


oxoe ox37 oxbo

oxd3 ox10 ox4f

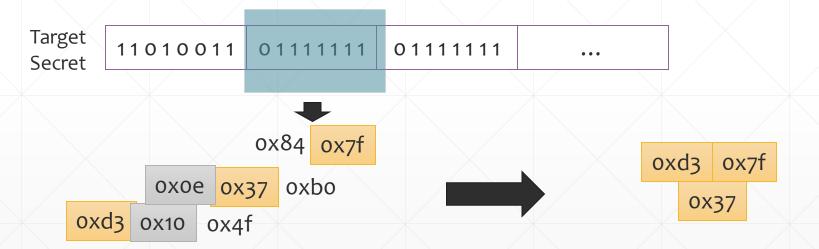


- We may leak bytes of data from other unimportant fill buffer entries
- Leak domino bytes to perform error correction





- We may leak bytes of data from other unimportant fill buffer entries
- Leak domino bytes to perform error correction





- Intel SGX allow developers to have hardware support for TEE
- Malicious OS is part of the threat model
- We can read register values of a trusted enclave with help of a malicious OS



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```
sgx-step
```

```
mov
add
xor
mov 0x4142434445464748, %rax
call
nop
jmp
```



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zstep



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```

zstep

jmp



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```
mov add xor mov 0x4142434445464748, %rax call nop jmp

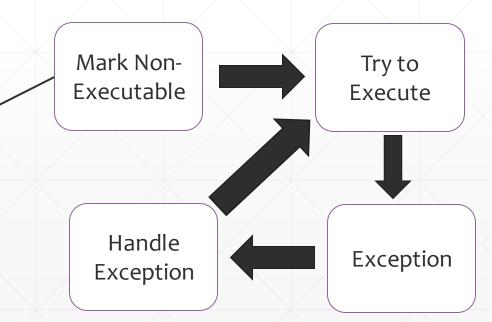
Exception
```

zstep



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```
mov
add
xor
mov 0x4142434445464748, %rax
call
nop
jmp
```



zstep



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- We can read register values of a trusted enclave with help of a malicious OS
- Repeated Context Switch in the transient domain w/ the same register values



ZombieLoad Demo! Recovering Linux Shadow



Is there any Mitigation?

- Intel suggested an instruction sequence to fill all the buffers across context switch
- Disable hyperthreading

Questions?!



https://zombieloadattack.com/