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MEMJAM: A FALSE DEPENDENCY ATTACK AGAINST CONSTANT-TIME CRYPTO IMPLEMENTATIONS IN SGX

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MemJam: A False Dependency Attack against Constant-Time Crypto Implementations in SGX

Ahmad "Daniel" Moghimi
Thomas Eisenbarth
Berk Sunar

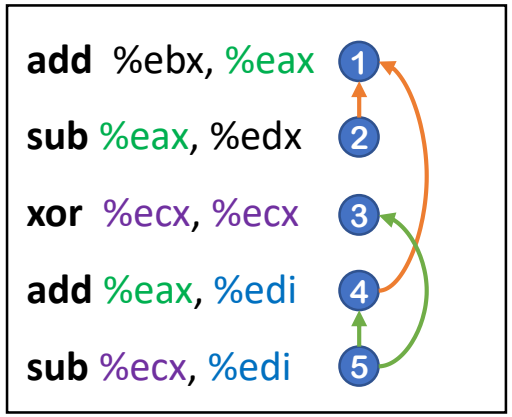
April 17, 2018

CT-RSA 2018 - San Francisco, CA

WPI

Data Dependency

- Data dependency: Instruction → Data of a preceding instruction



Data Dependency – Pipelined Execution

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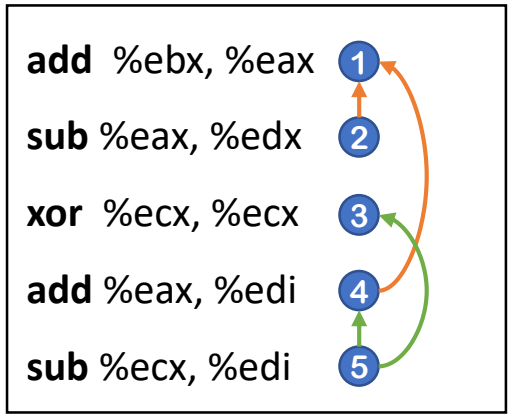

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EX Execute
WB Write Back

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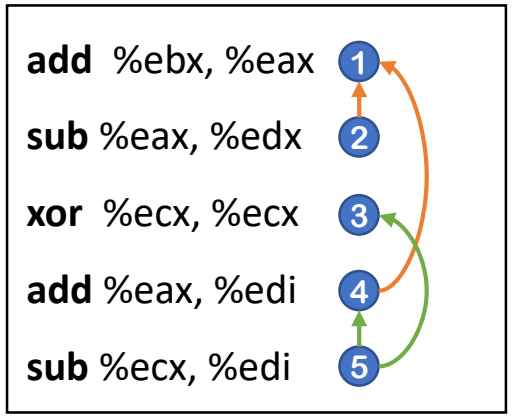

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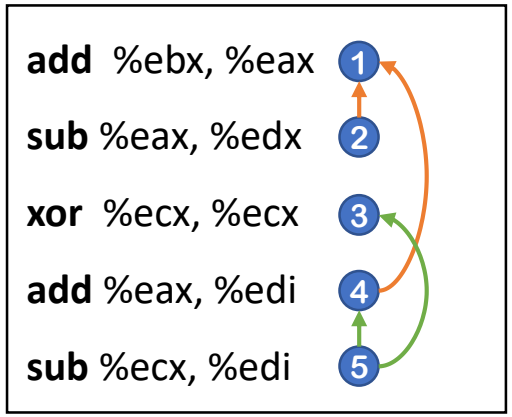

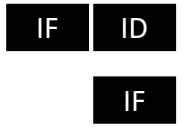

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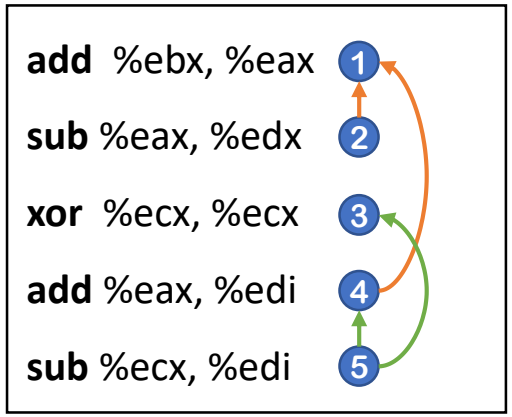

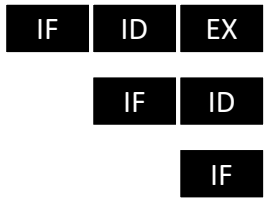

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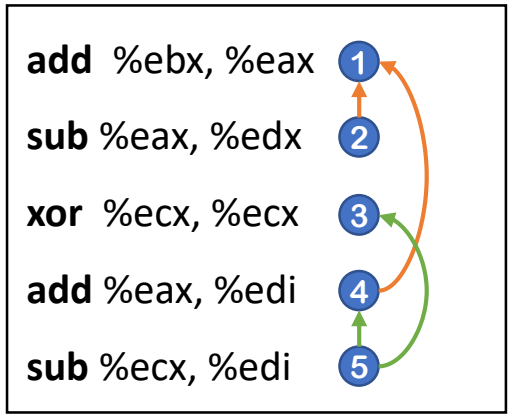

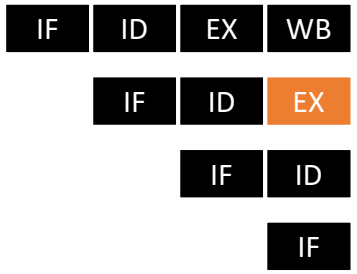

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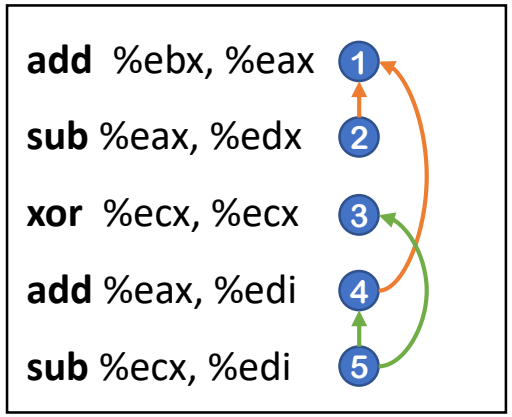

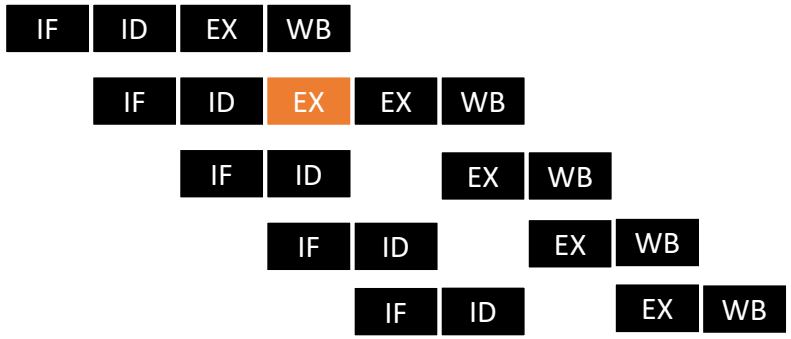

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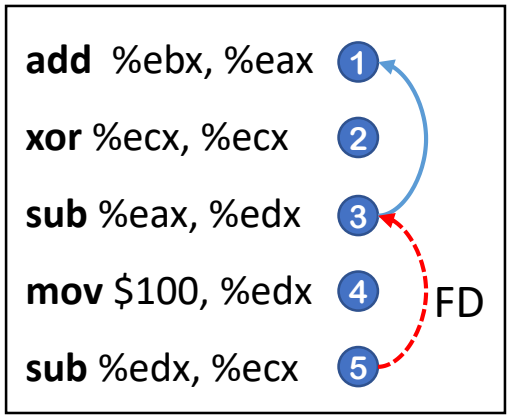
~~Data~~ False Dependency

- Pipeline stalls without true dependency.
- Reasons:
  - Register Reuse
  - Limited Address Space

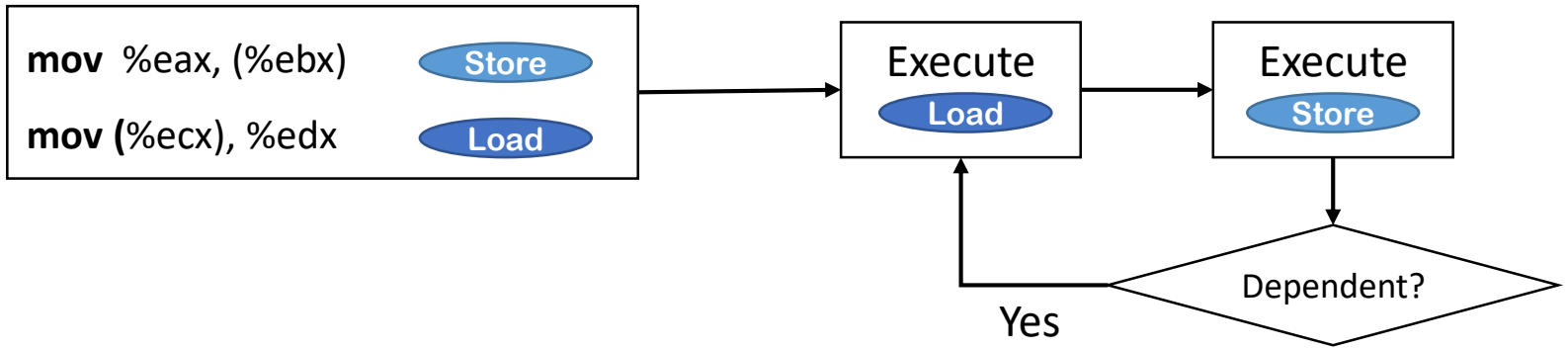


~~Data~~ False Dependency – Register Renaming

- Pipeline stalls without true dependency.
- Reasons:
  - Register Reuse
  - Limited Address Space

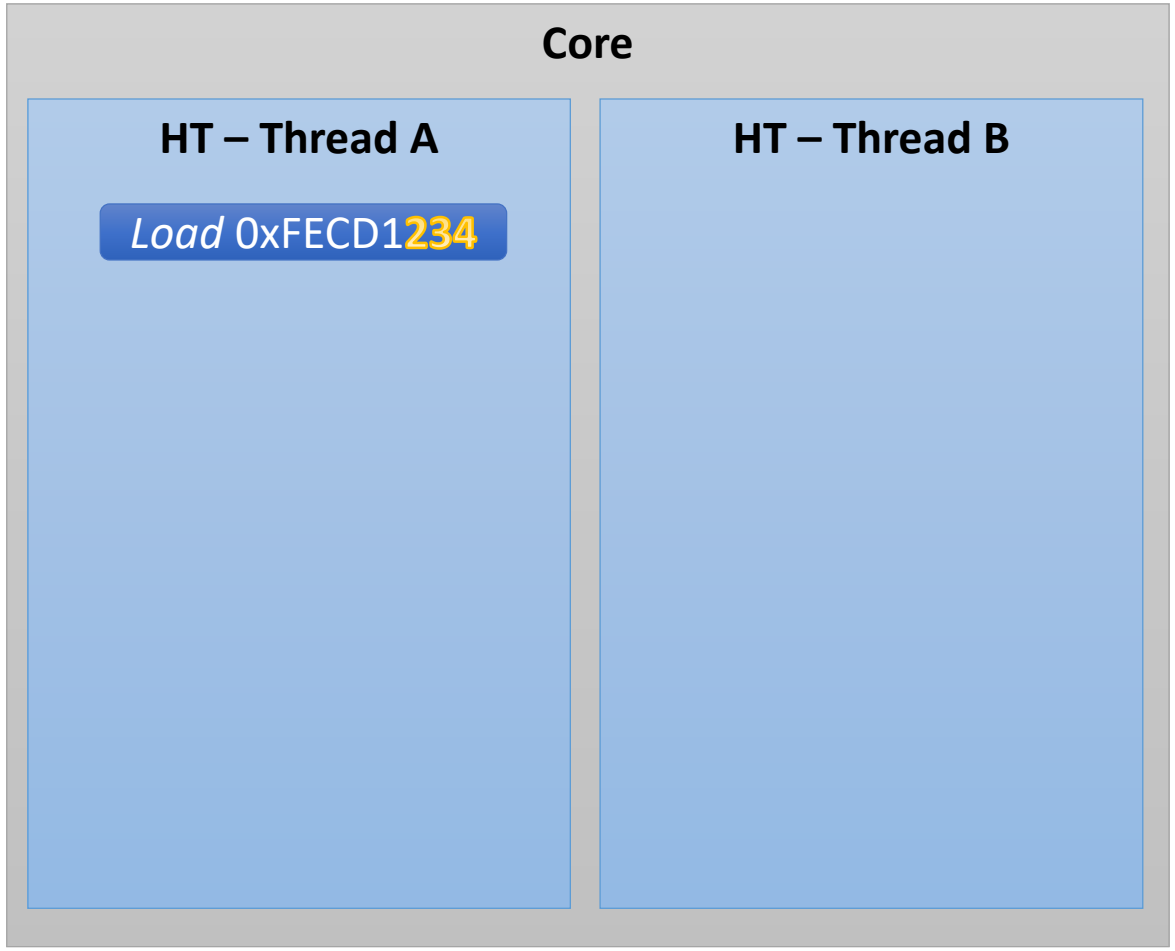
Memory False Dependency – 4K Aliasing

- Memory loads/stores are executed out of order and speculatively.
- The dependency is verified after the execution!

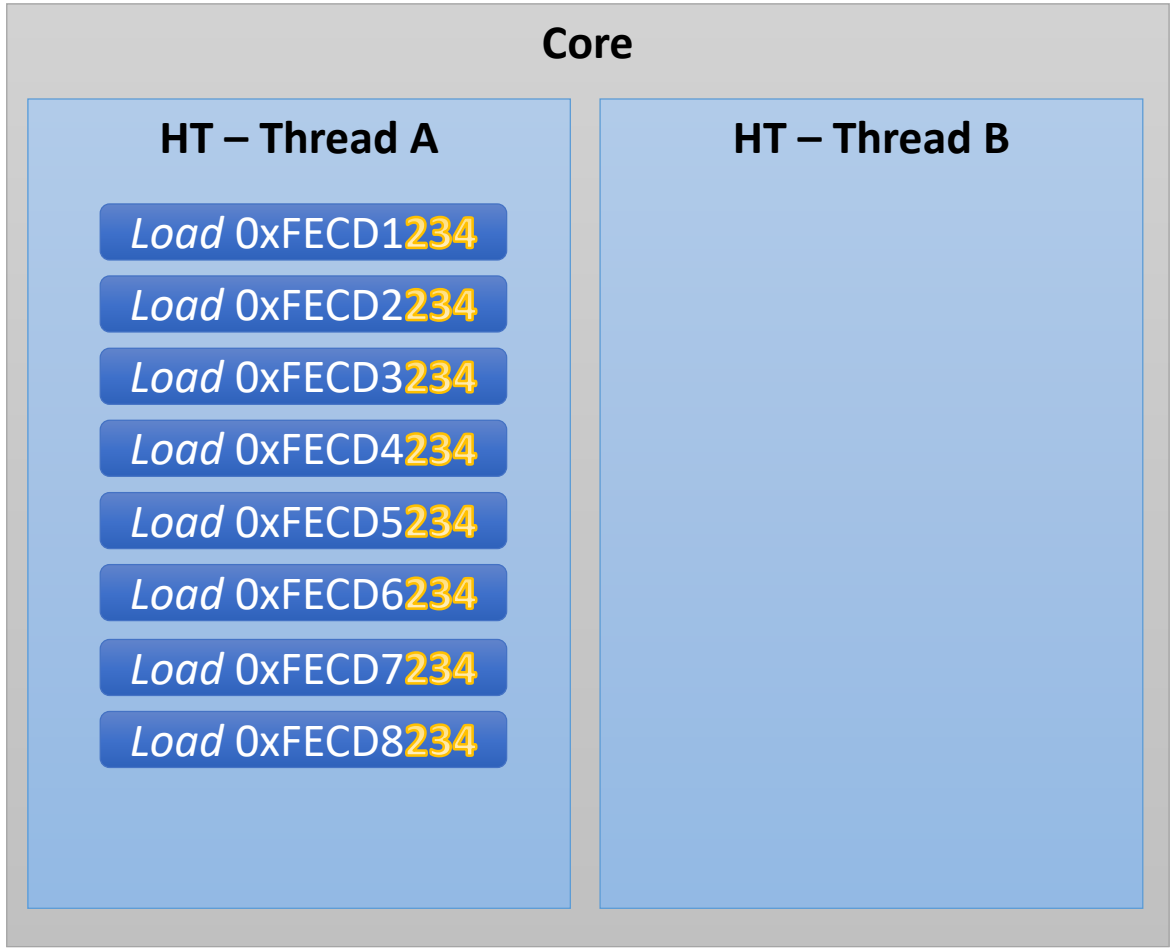


- 4K Aliasing: Addresses that are 4K apart are assumed dependent.
- Re-execute the **load** and corresponding instructions due to false dependency.
- Virtual-to-physical address translation → Memory disambiguation

4K Aliasing – Hyperthreading



4K Aliasing – Hyperthreading



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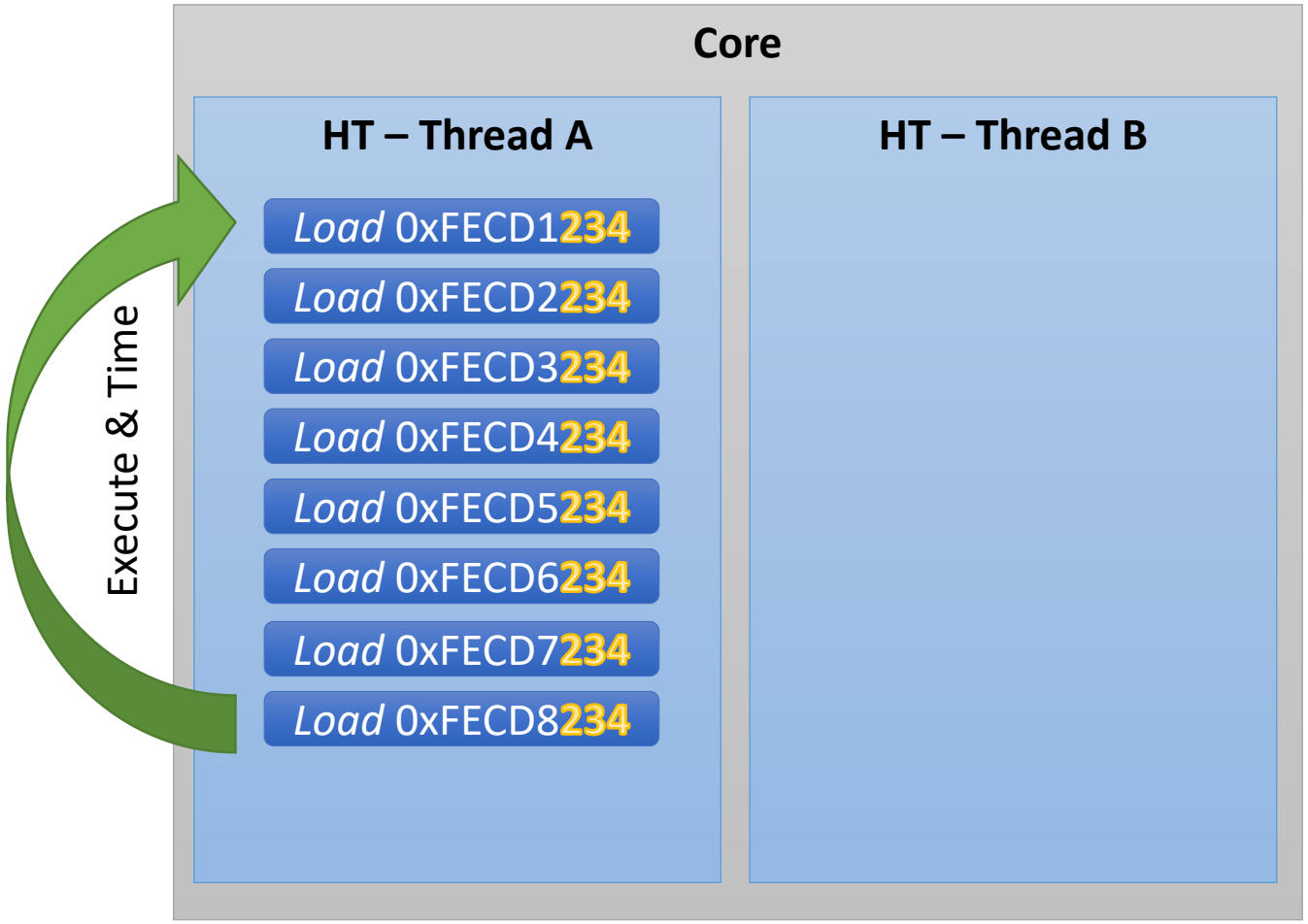

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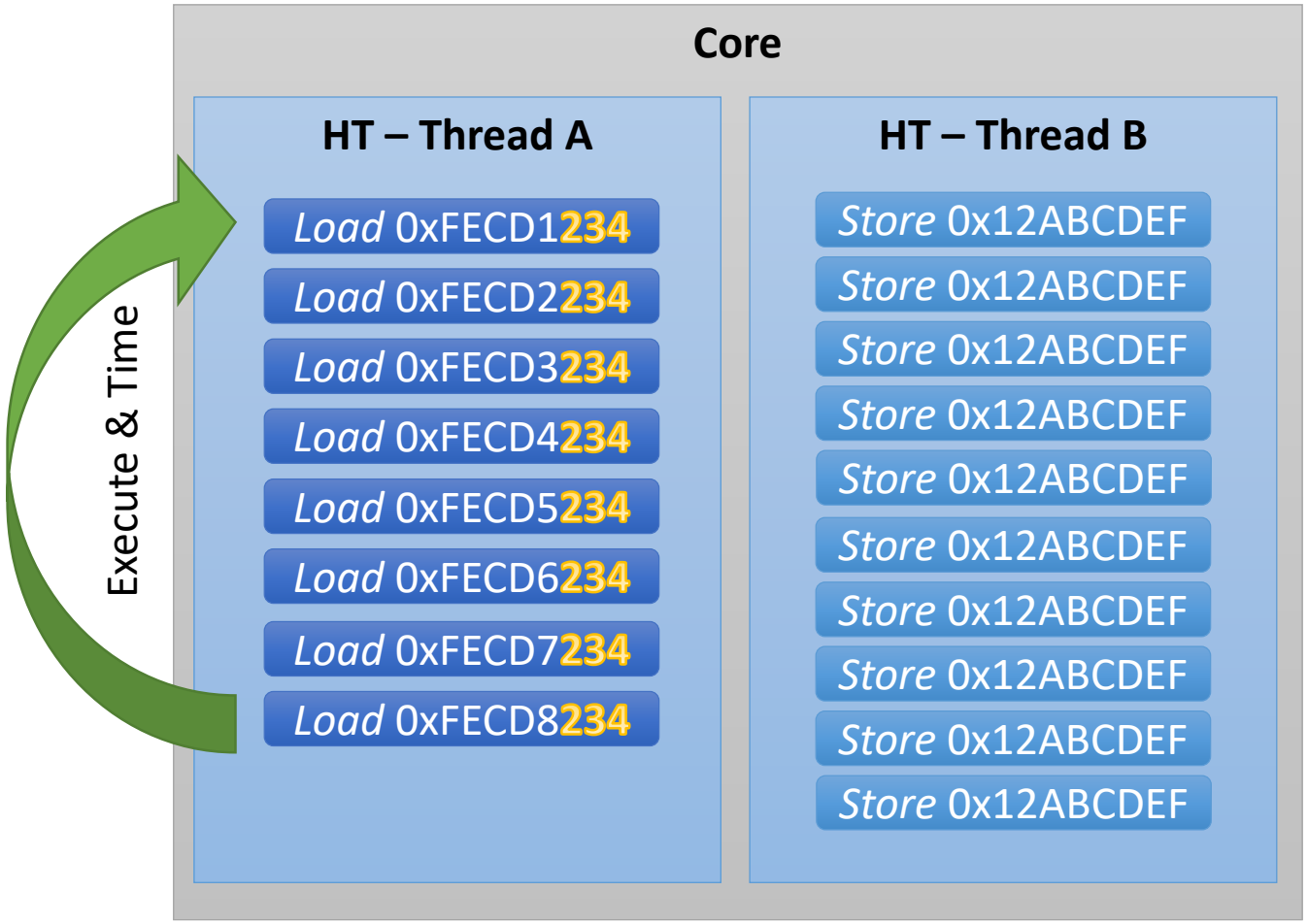

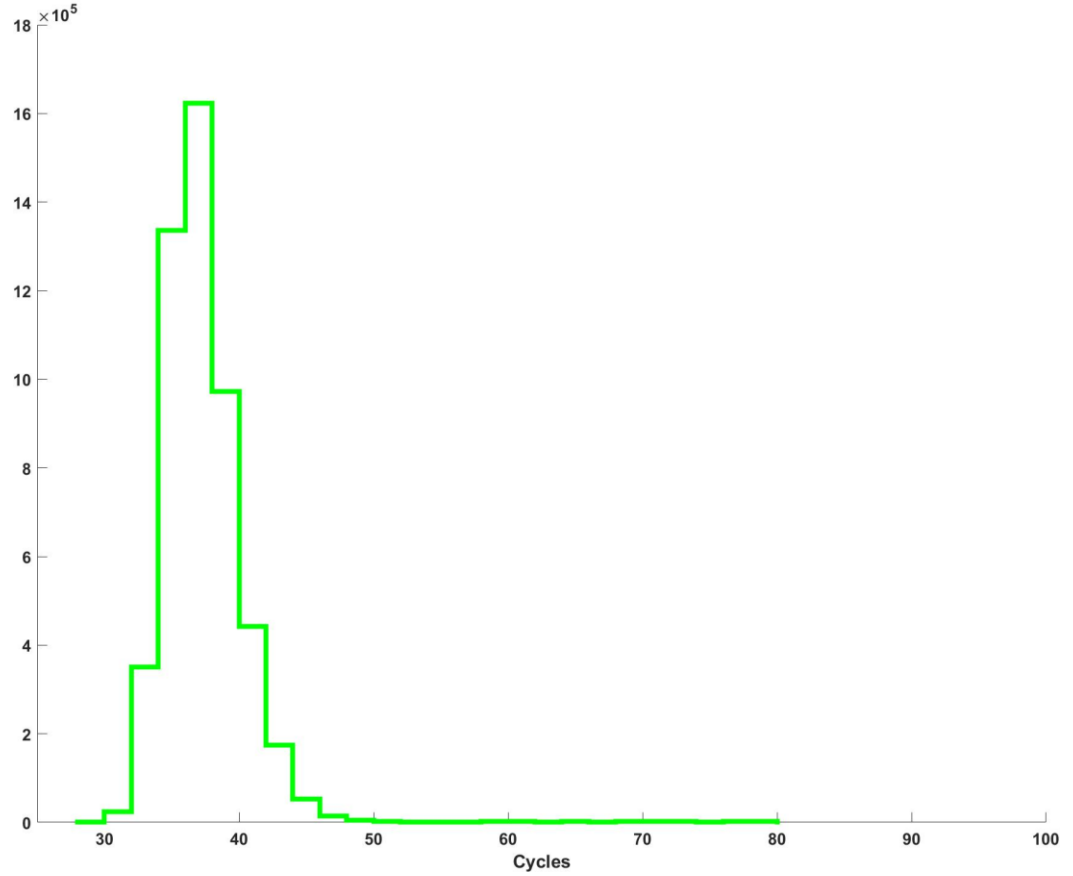

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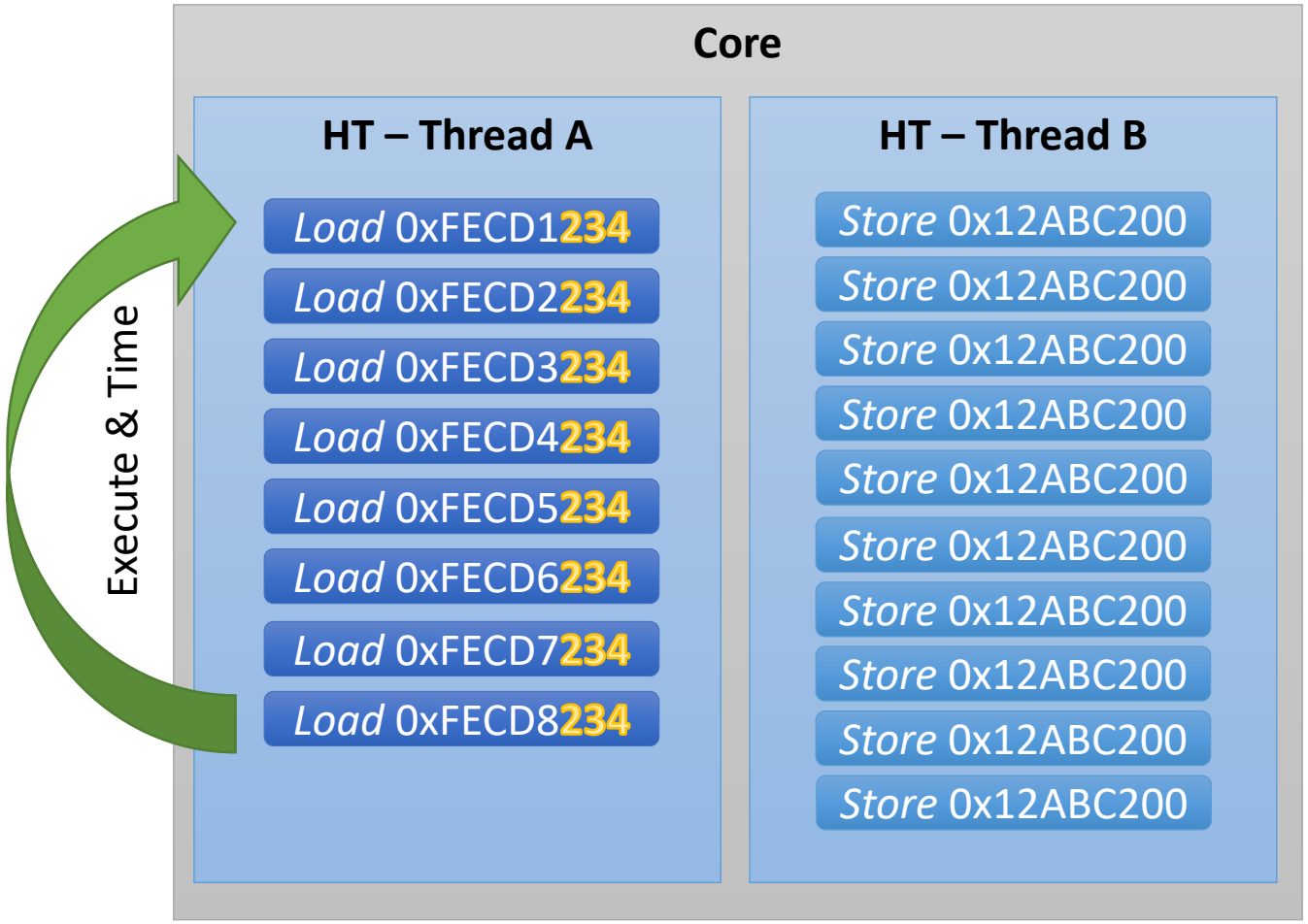

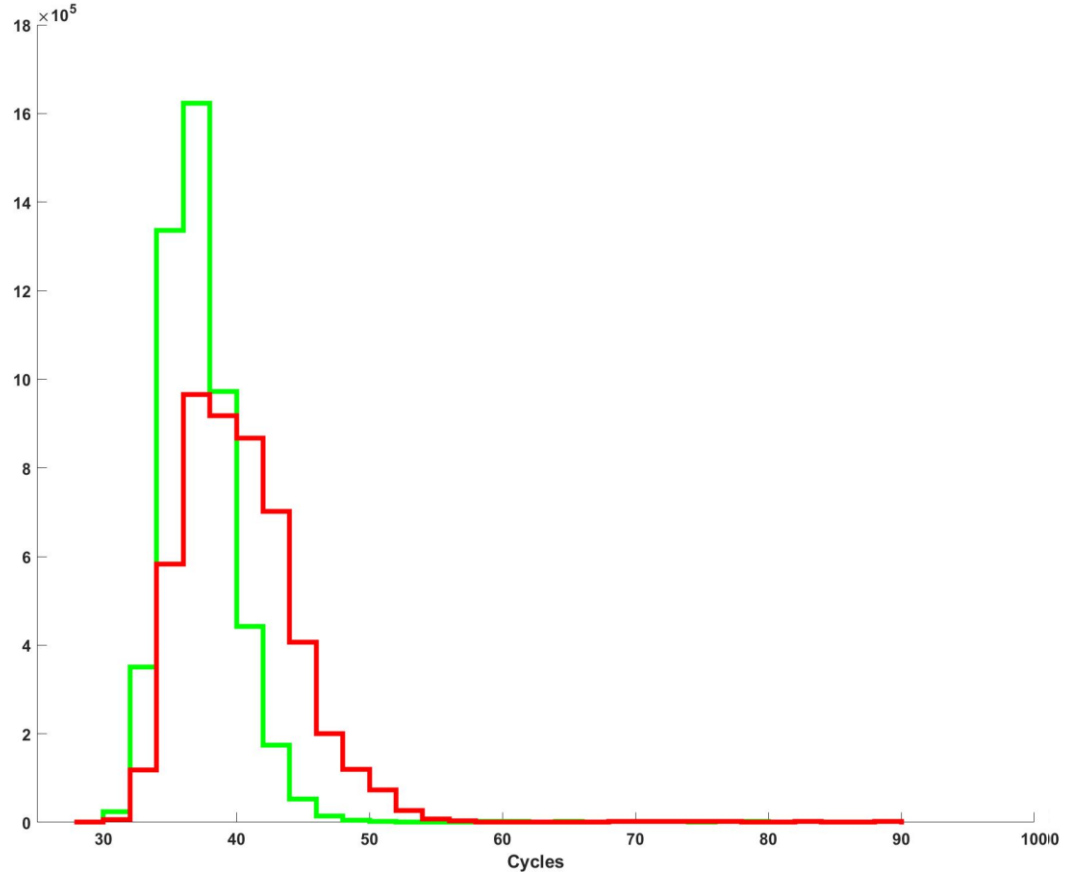

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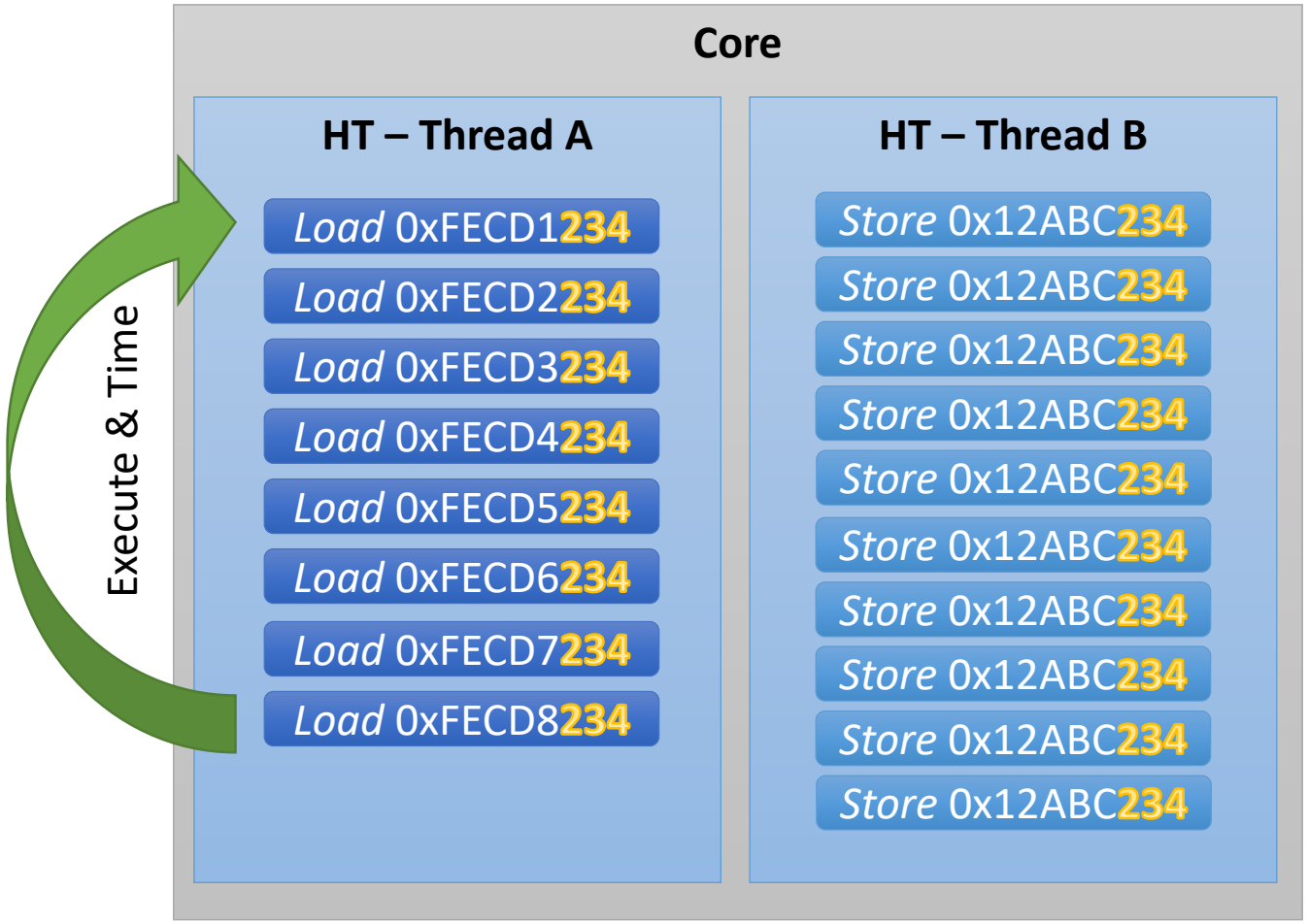

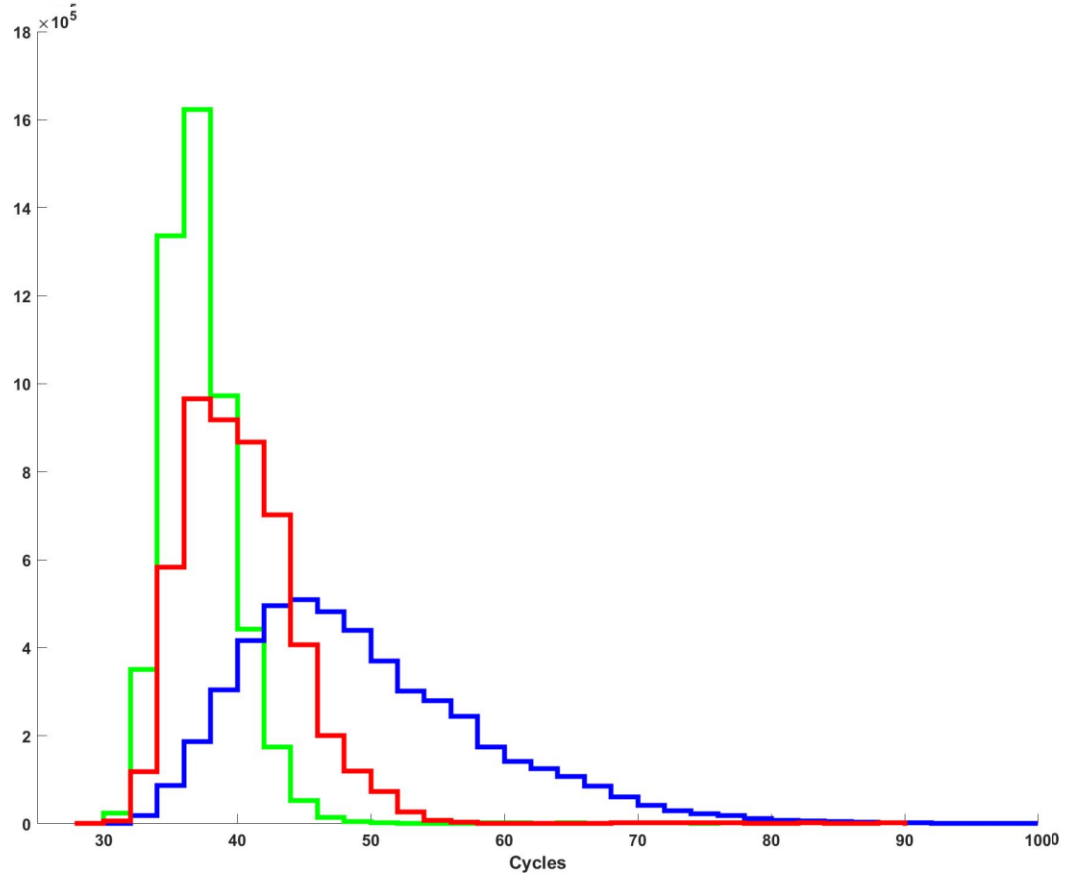

MemJam – Intra Cache Line Resolution

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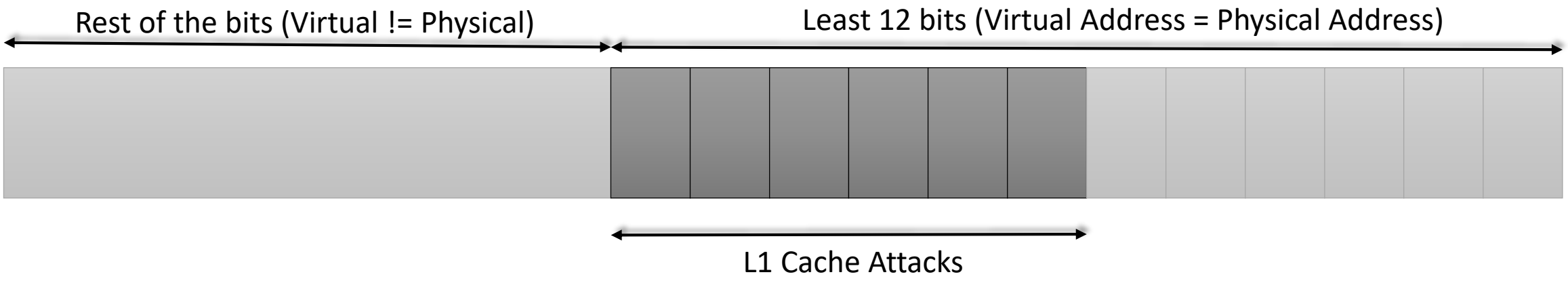

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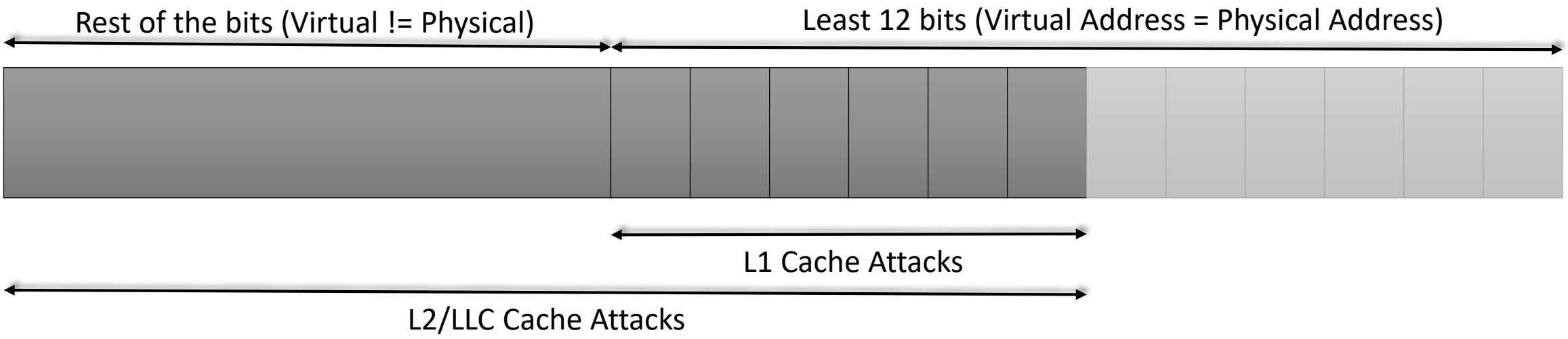

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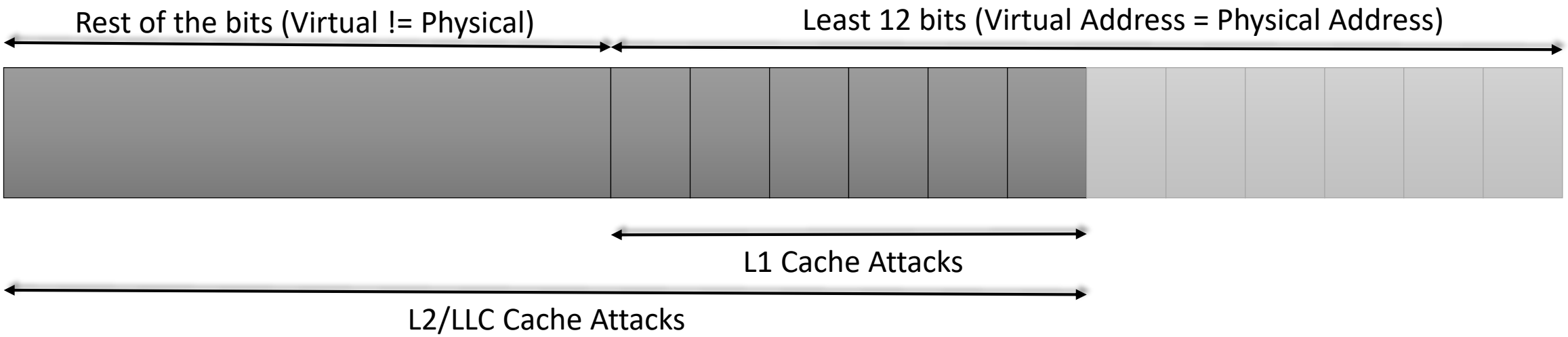

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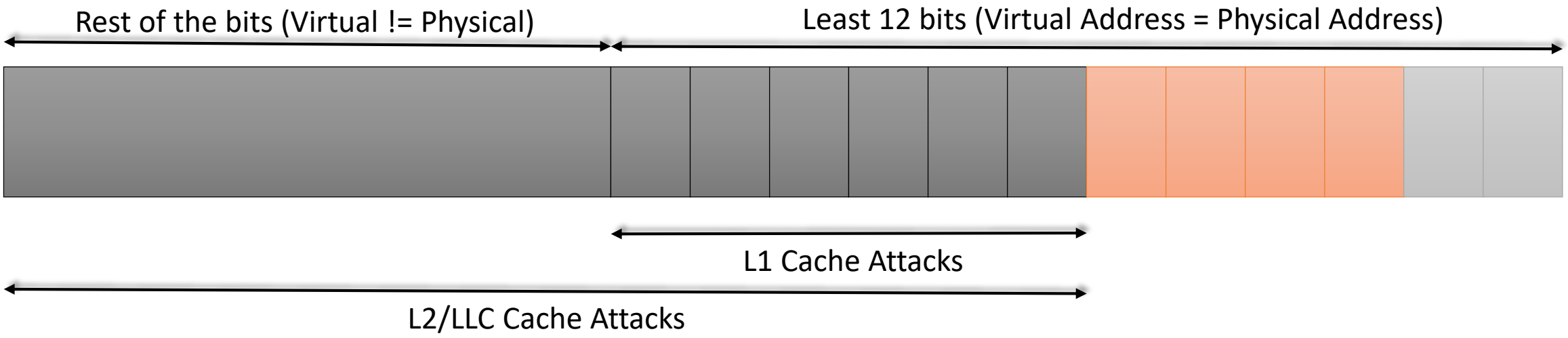
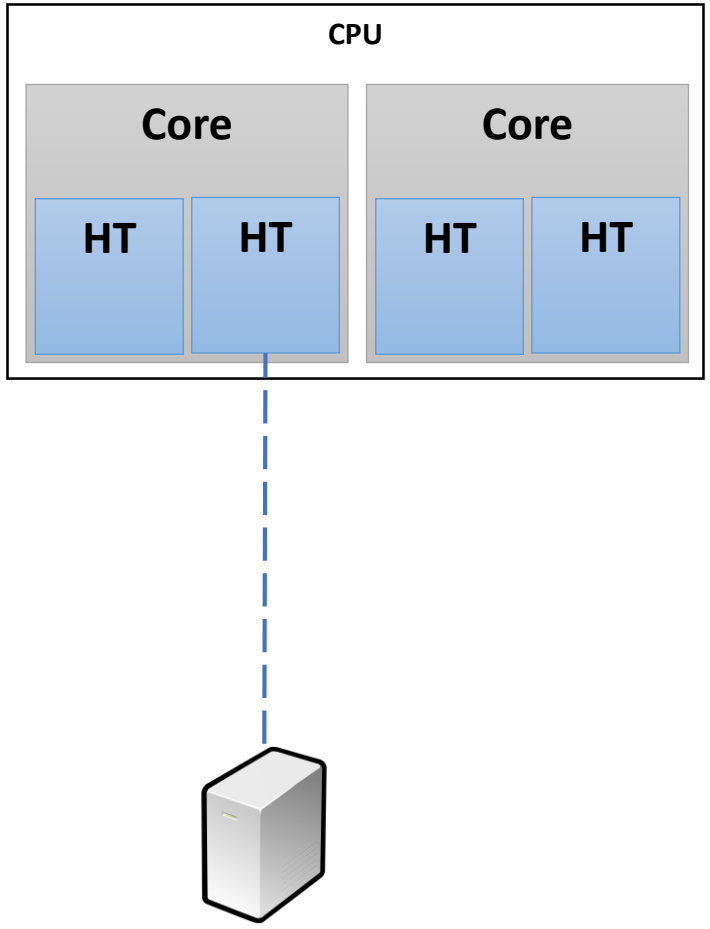


- Intra-cache line Leakage (4-byte granularity)
- Higher time **correlates**→ Memory accesses with the same bit 3 to 12
- 4 bits of intra-cache level leakage

MemJam Attack



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mov %[target], %rax;
write_loop:
   .rept 100;
   movb $0, (%rax);
   .endr;
jmp write_loop;
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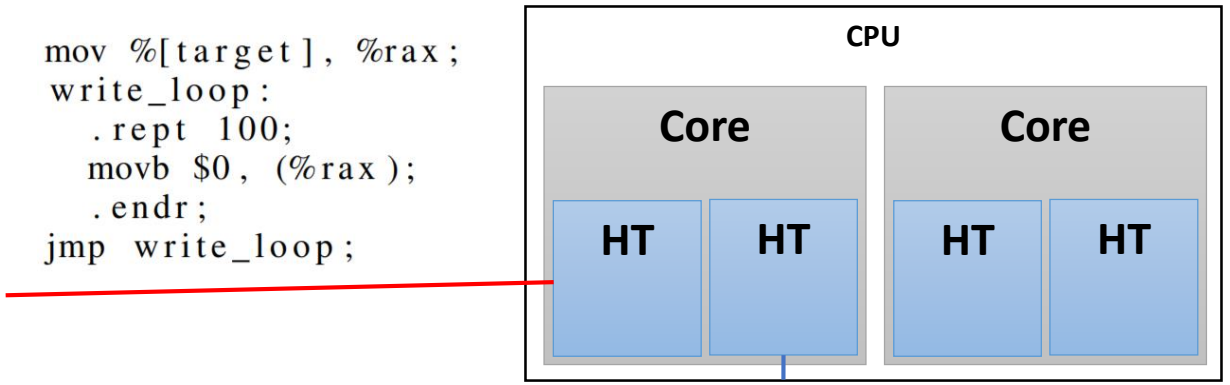

Encryption Service

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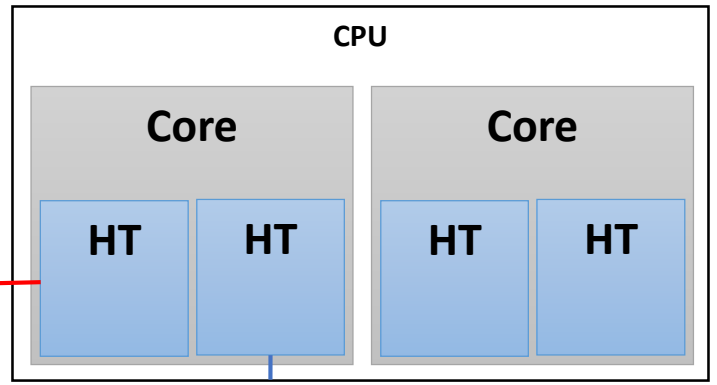

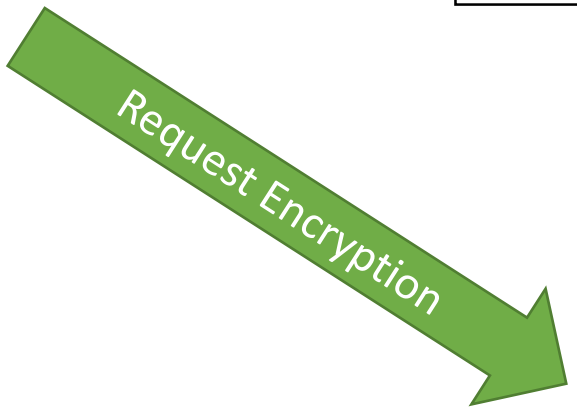

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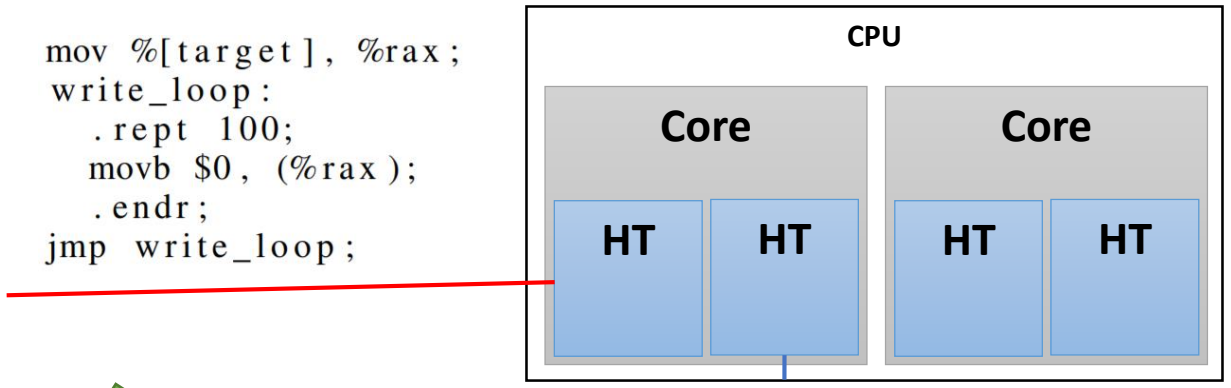

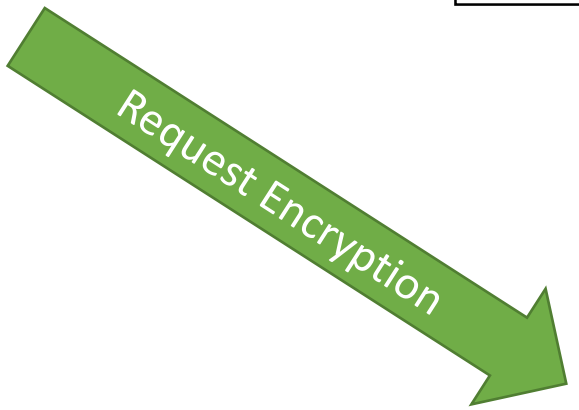

Encryption Service

Execute

load
compute
load
load
compute
load
compute
load
load

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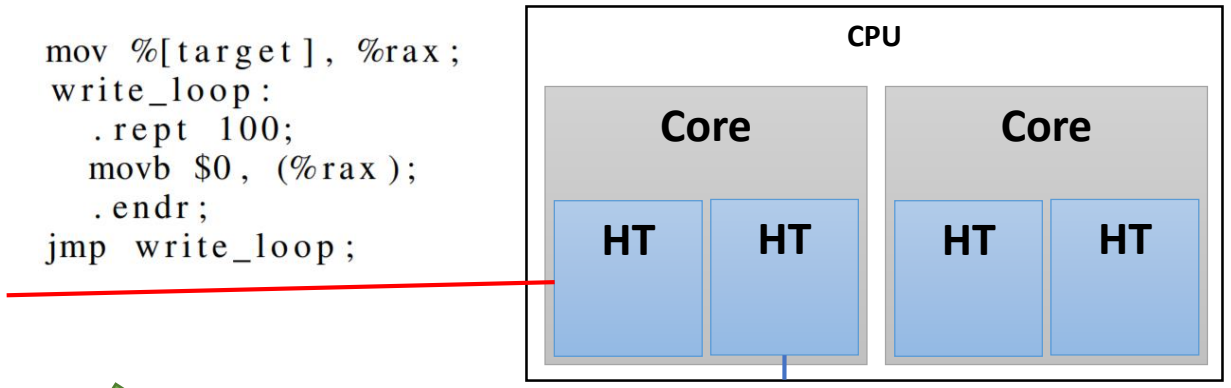

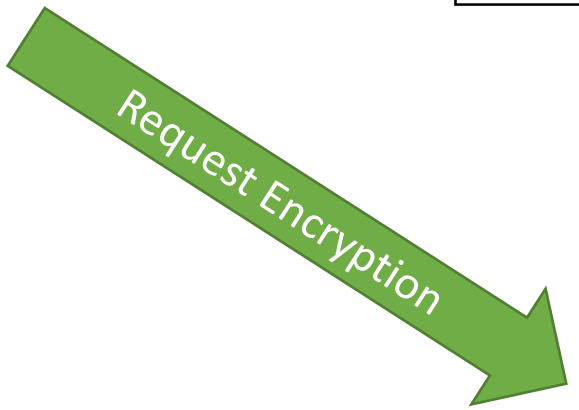

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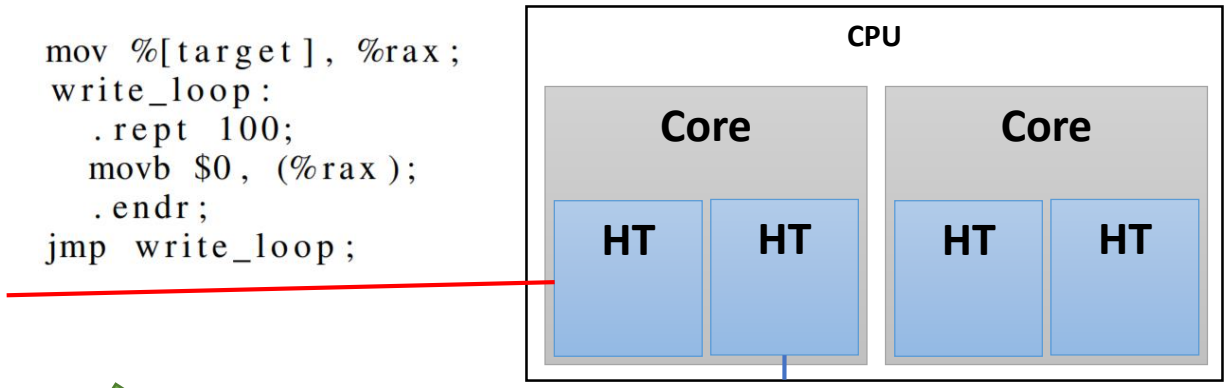

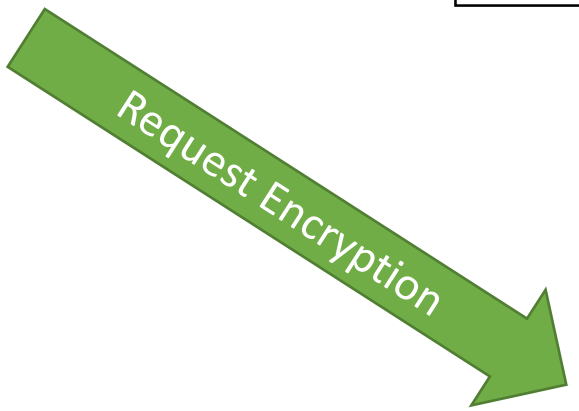

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~~compute~~
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compute
~~load~~
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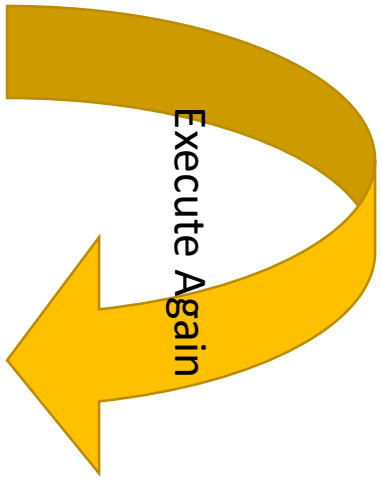
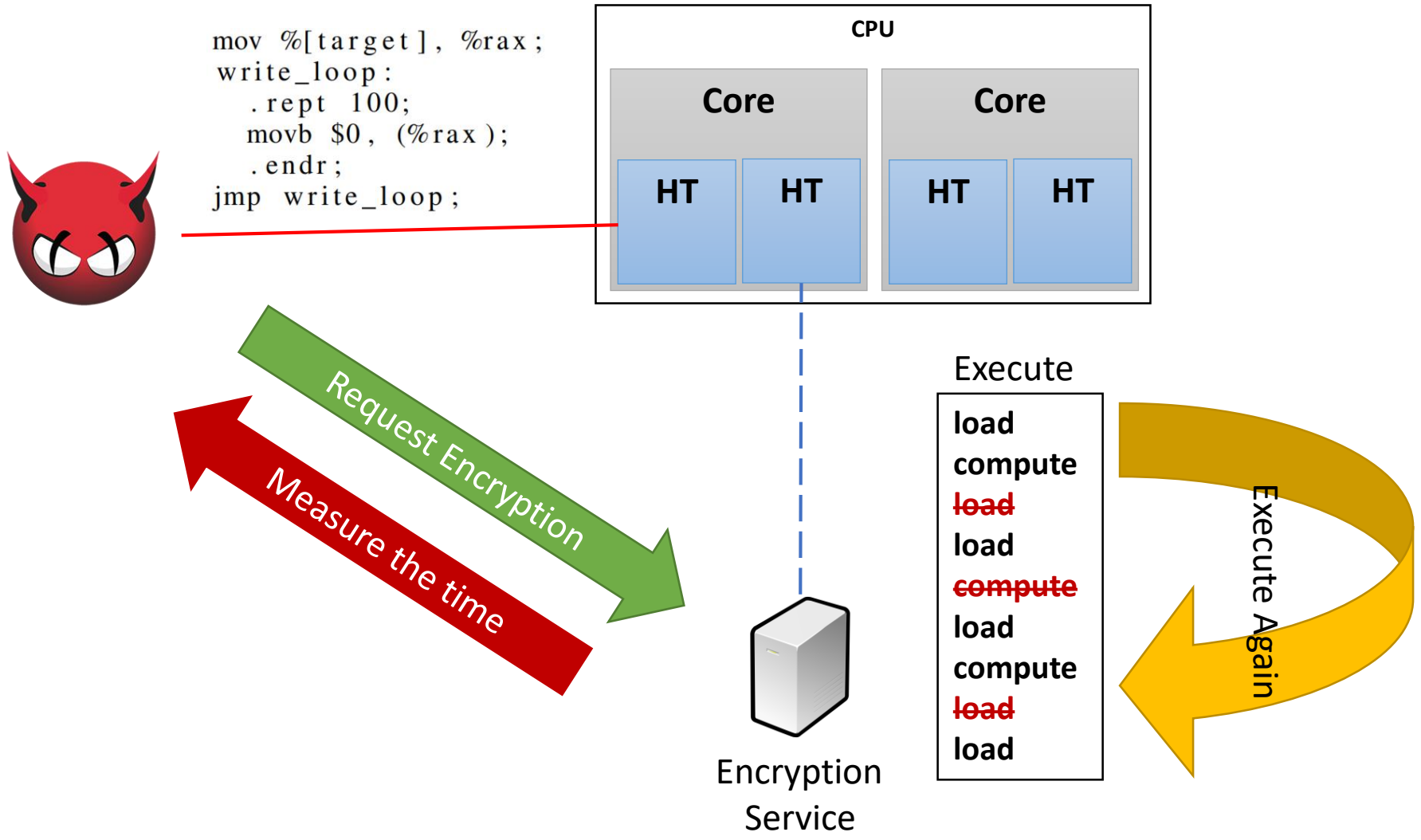


MemJam Attack



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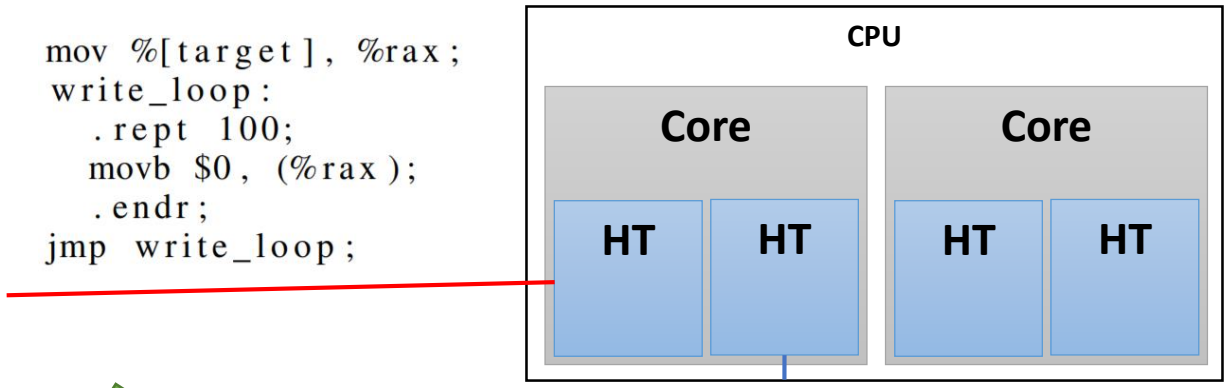
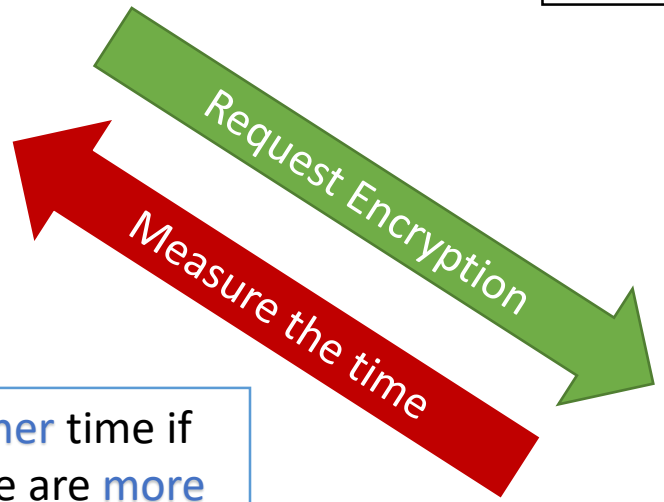


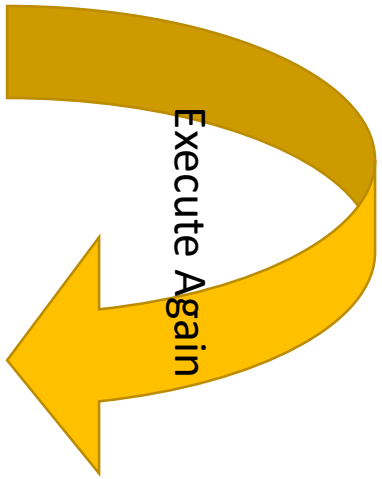


Higher time if there are more number of 4K conflicts

Encryption Service

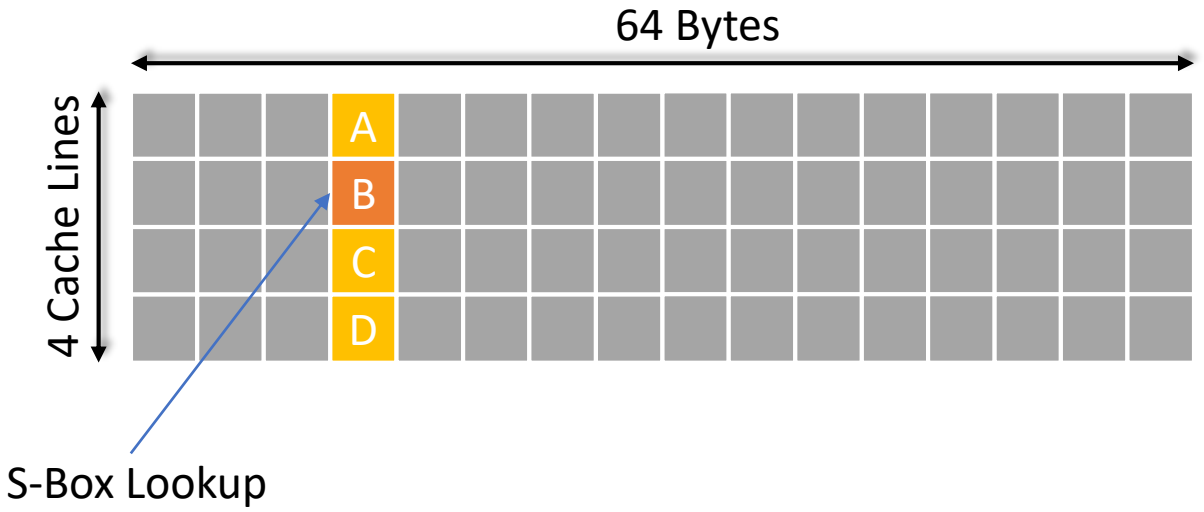
Execute

load
compute
~~load~~
load
~~compute~~
load
compute
~~load~~
load



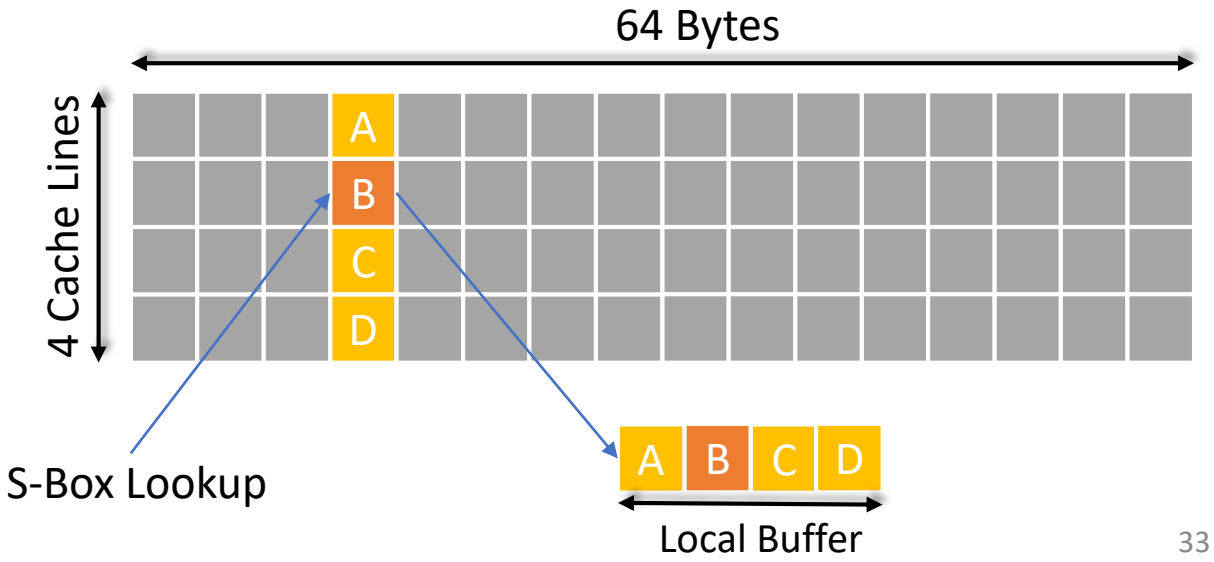
Constant time AES – Safe2Encrypt_RIJ128

- Scatter-gather implementation of AES
  - 256 S-Box – 4 Cache Line
  - Cache independent access pattern
- Implemented and distributed as part of Intel products
  - Intel SGX Linux Software Development Kit (SDK)
  - Intel IPP Cryptography Library



Constant time AES – Safe2Encrypt_RIJ128

- Scatter-gather implementation of AES
  - 256 S-Box – 4 Cache Line
  - Cache independent access pattern
- Implemented and distributed as part of Intel products
  - Intel SGX Linux Software Development Kit (SDK)
  - Intel IPP Cryptography Library



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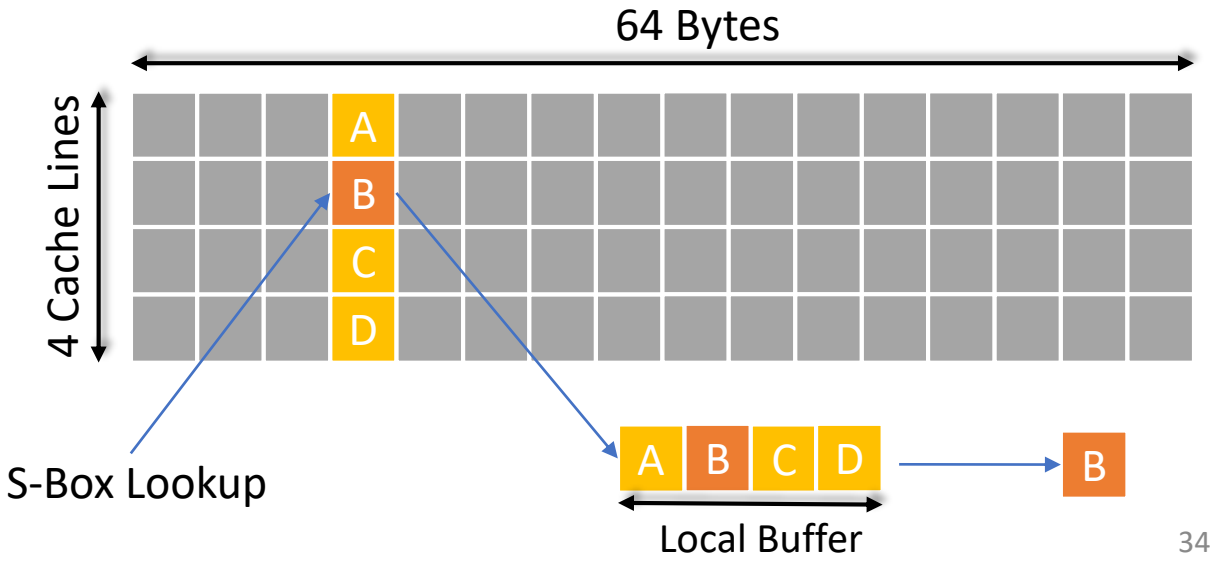
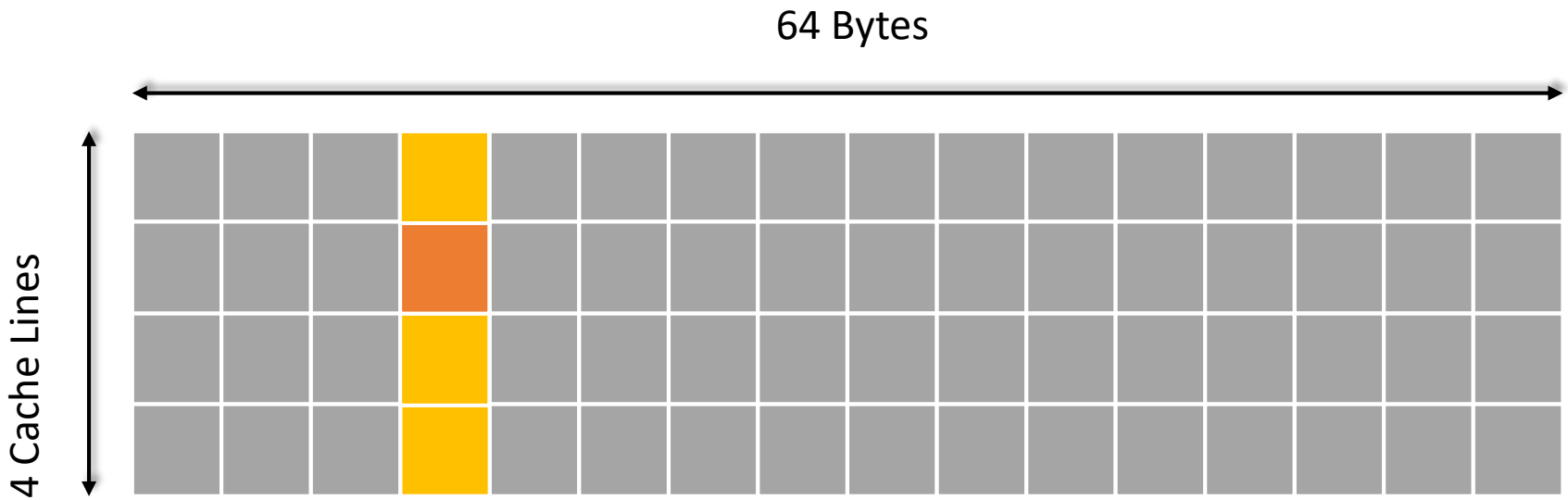


MemJam Attack on AES



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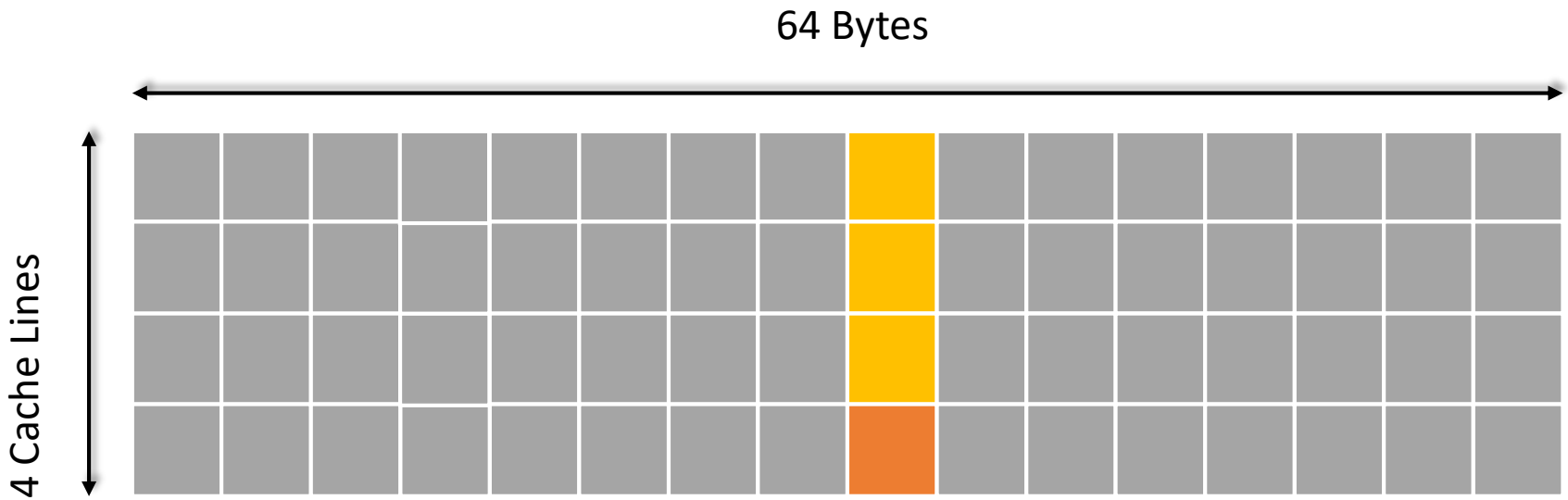

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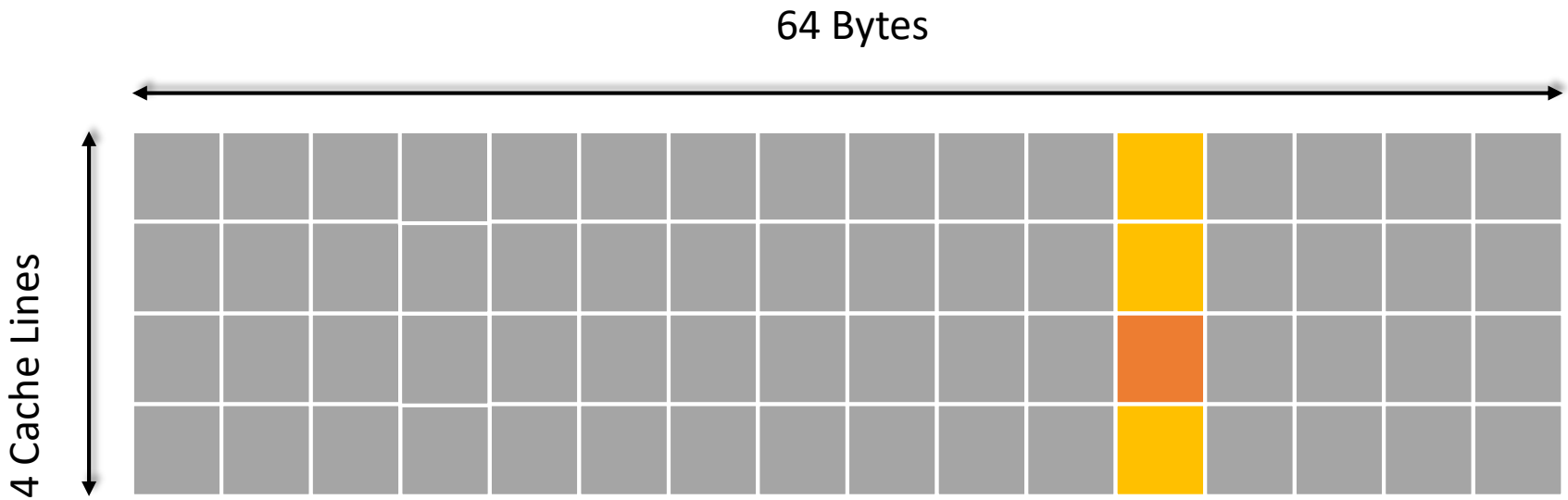

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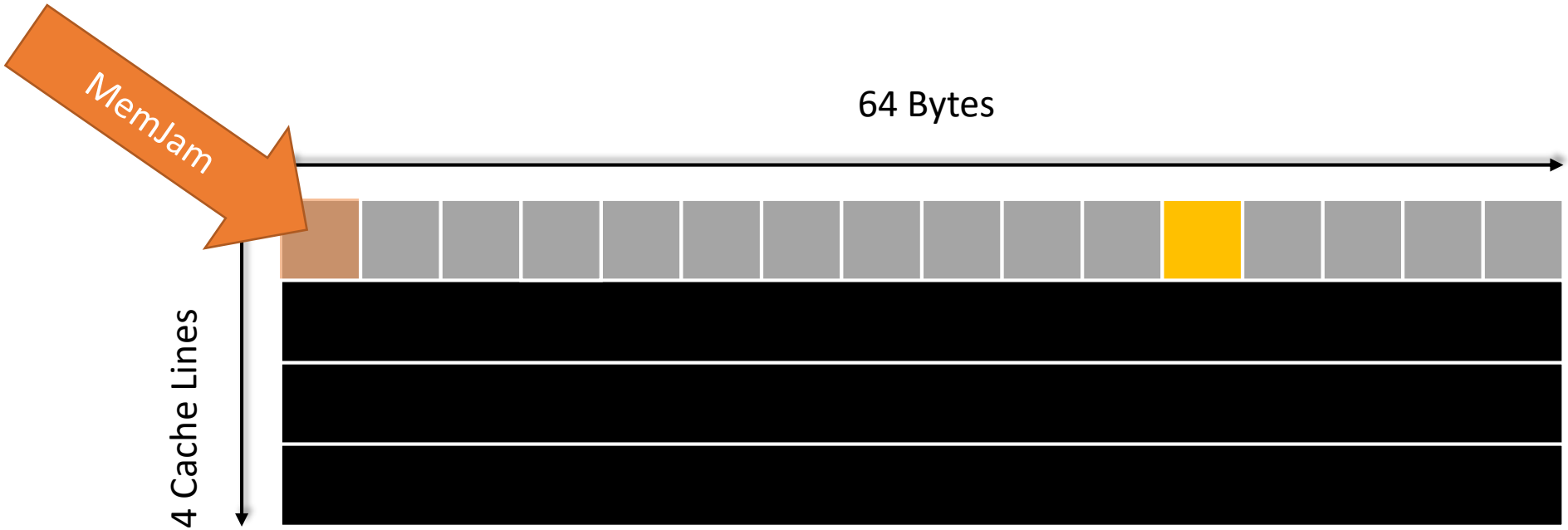
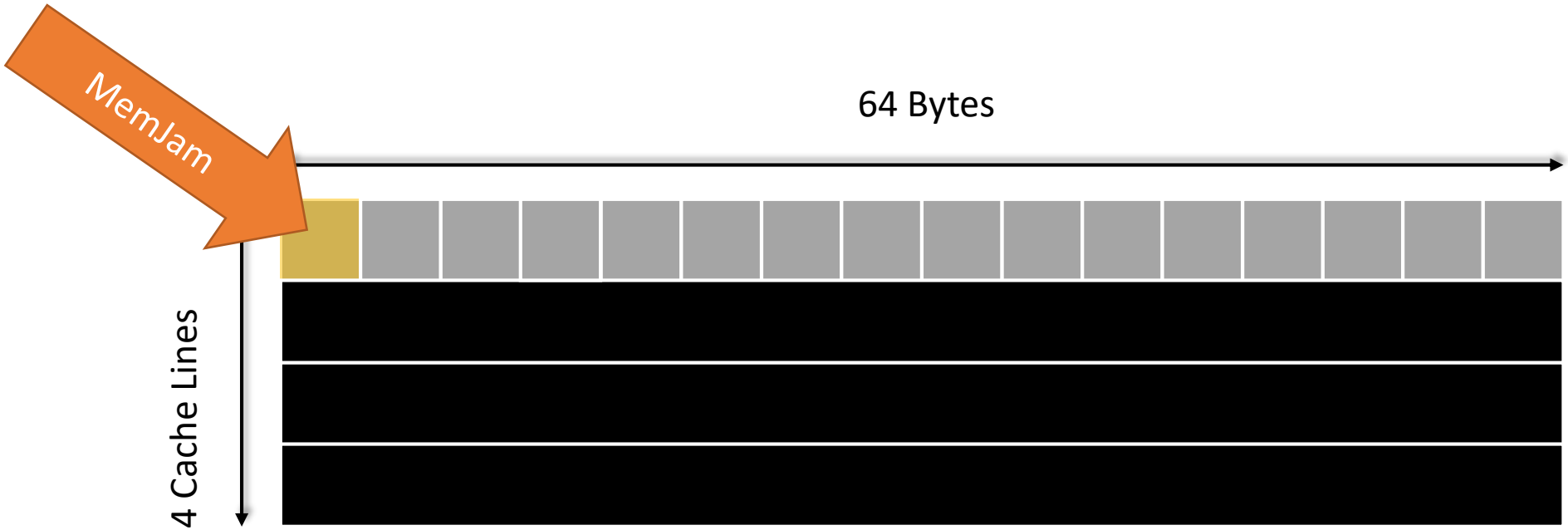


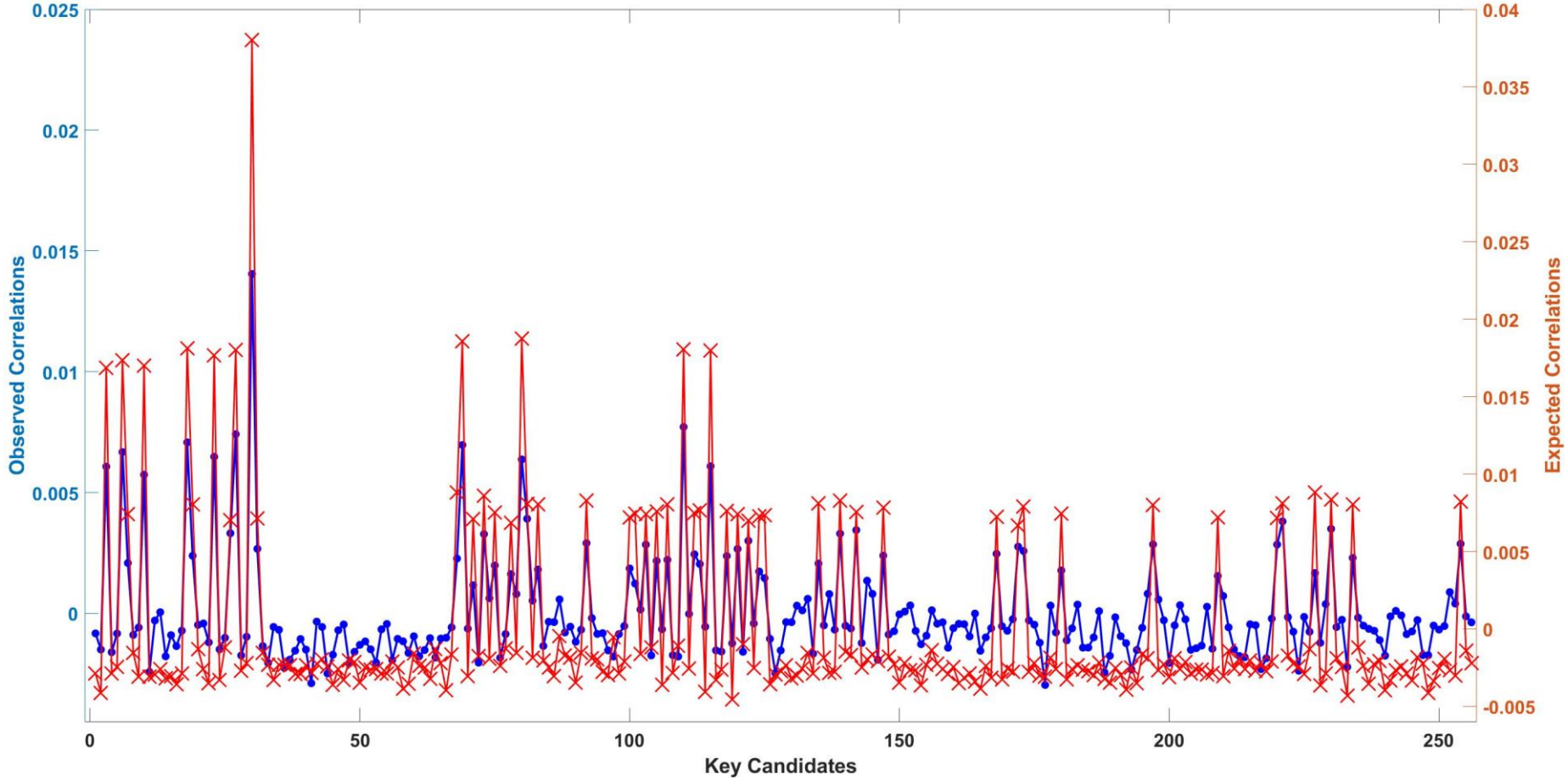
$$index = S^{-1}(c \oplus k)$$

MemJam Attack on AES

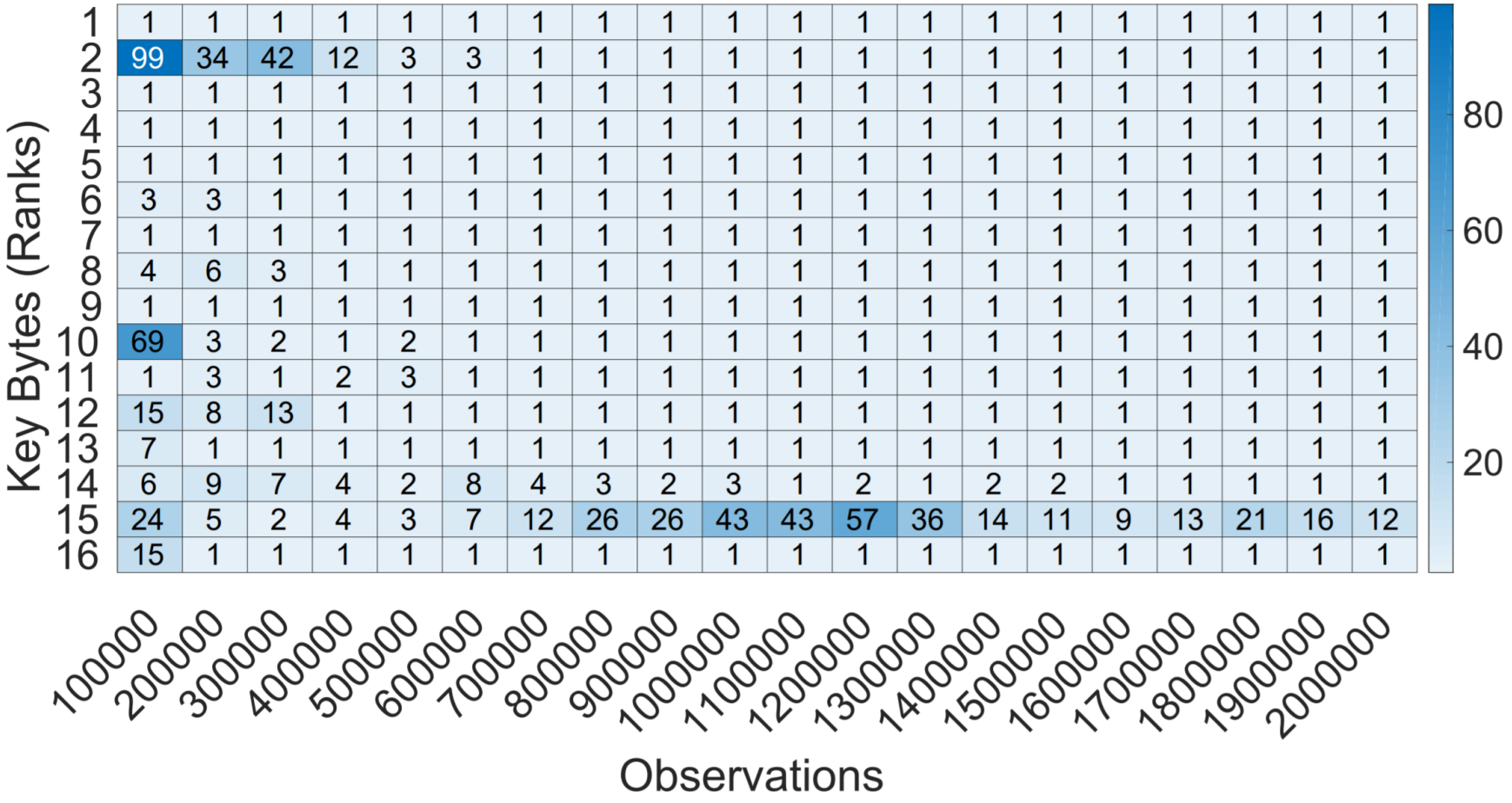


$$index = S^{-1}(c \oplus k) \longrightarrow index < 4$$

AES Key Recovery

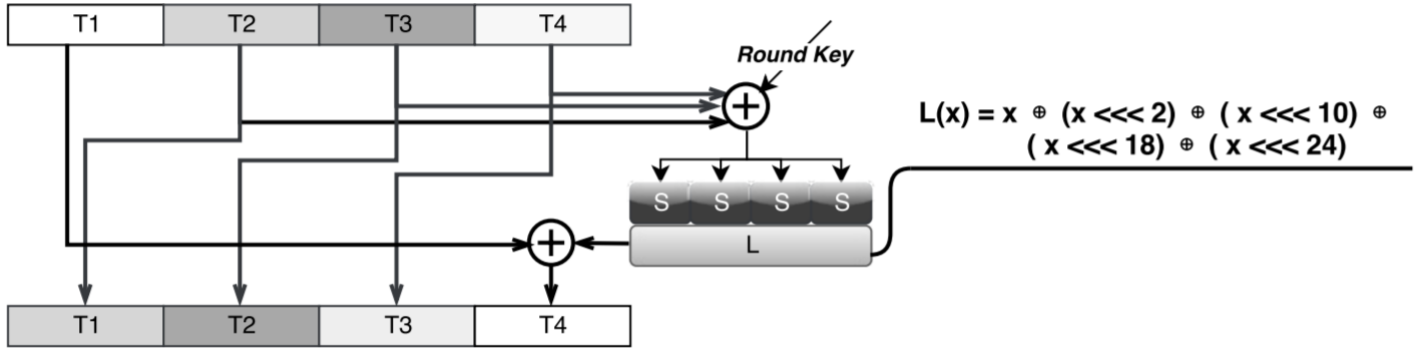


AES Key Recovery



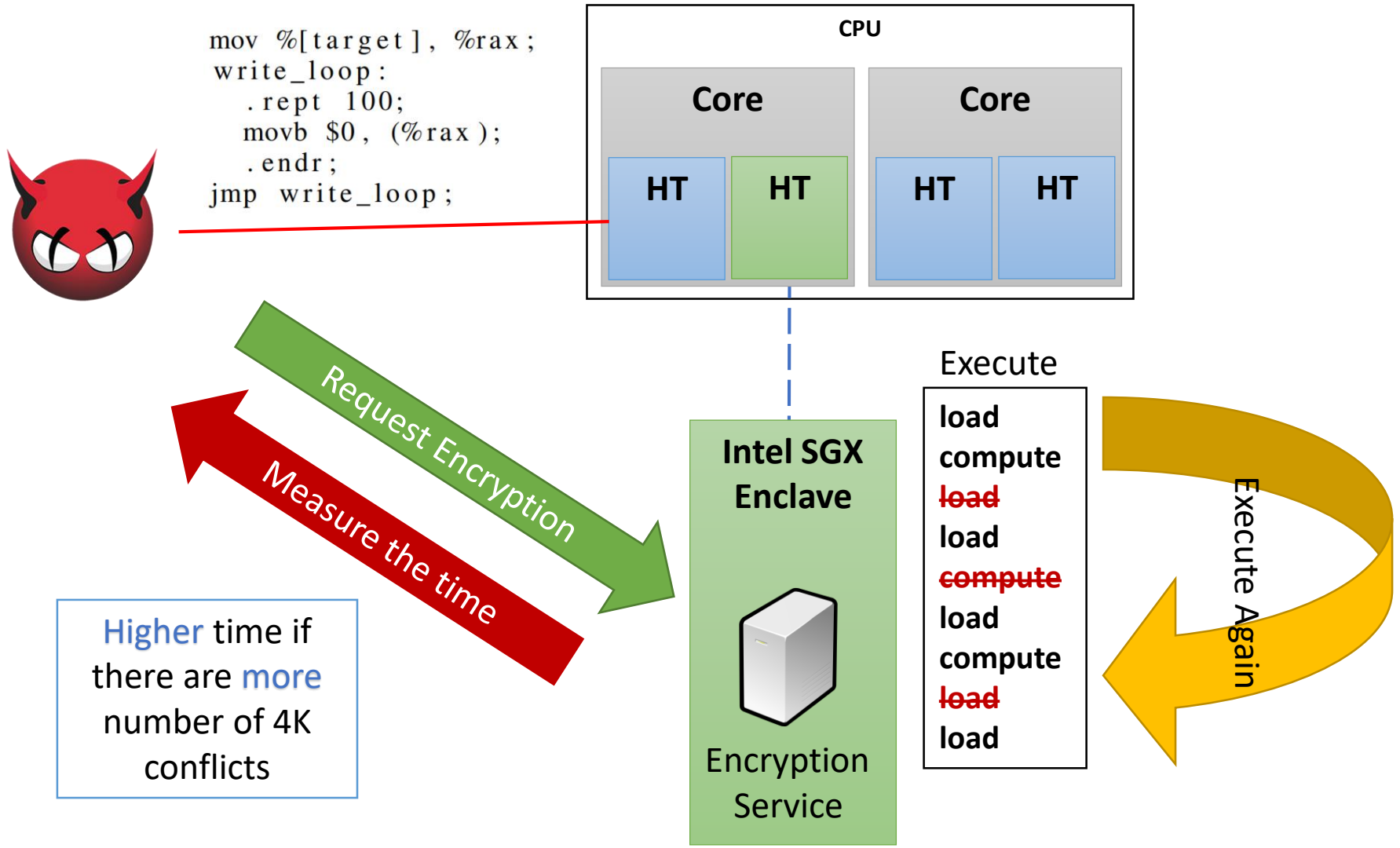
SM4 Block cipher – cpSMS4_Cipher

- Standard Cipher support by Intel
  - Chinese National Standard for Wireless LAN WAPI
- S-Box + Unbalanced Feistel Structure
- Protected by Cache State Normalization

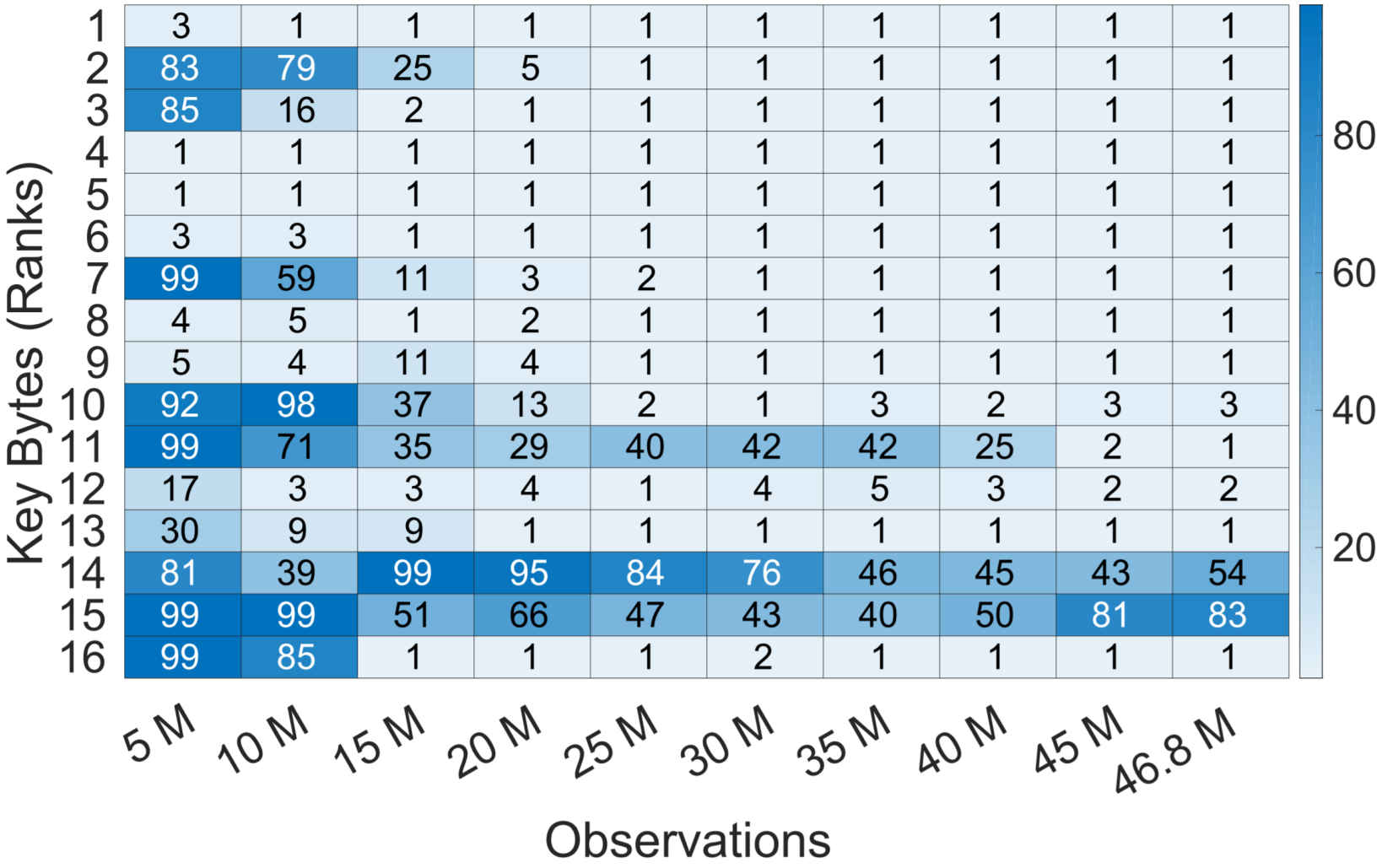


- Recursive attack → Full key recovery with 40K observations

MemJaming Intel SGX Secure Enclave



Intel SGX – AES Key Recovery



Conclusion

- New Side-Channel Attack Applicable to all Intel Processors
  - Intel SGX extensions
- Bypass of Constant-Time Implementations Techniques
  - Scatter-Gather
  - Cache State Normalization
- Agnostic to other Cache Attack Defense Mechanism

- Intel Trilogy
  - Intel Hardware
  - Intel Trusted Execution Environment
  - Intel Hardened Crypto Implementation

Responsible Disclosure

Date	Progress
08/02/2017	Reported
08/04/2017	Acknowledged
11/07/2017	Safe2Encrypt_RIJ128 got removed from SGX SDK.
11/17/2017	CVE-2017-5737 Assigned
work-in-progress	Patch

Questions?!

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Implementation Technique	Function Name	l9 n0 y8 k0 e9	m7 mx	n8	Linux SGX SDK
AES-NI	Encrypt_RIJ128_AES_NI	✓	×	×	✓ (pre-built)
AES Bitsliced	SafeEncrypt_RIJ128	✓	×	✓	✓ (pre-built)
AES Constant-Time	Safe2Encrypt_RIJ128	×	✓	×	✓ (source)
SM4 Bitsliced using AES-NI	cpSMS4_ECB_aesni	✓	×	×	N/A
SM4 Cache Normalization	cpSMS4_Cipher	✓	✓	✓	N/A

Release	Family	Cache Bank Conflicts	4K Aliasing
2006	Core	✓	✓
2008	Nehalem	×	✓
2011	Sandy bridge	✓	✓
2013	Silvermont, Haswell, Broadwell	×	✓
2015	Skylake	×	✓
2016	KabyLake	×	✓