

$V_{DSM} = 5200 \text{ V}$
 $I_{TAVM} = 2760 \text{ A}$
 $I_{TRMS} = 4340 \text{ A}$
 $I_{TSM} = 42000 \text{ A}$
 $V_{T0} = 1 \text{ V}$
 $r_T = 0.225 \text{ m}\Omega$

Phase Control Thyristor

5STP 25L5200

Doc. No. 5SYA1008-03 Jan. 02

- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate

Blocking

Maximum rated values ¹⁾

Symbol	Conditions	5STP 25L5200	5STP 25L5000	5STP 25L4600
V_{DSM}, V_{RSM}	$f = 5 \text{ Hz}, t_p = 10 \text{ ms}$	5200 V	5000 V	4600 V
V_{DRM}, V_{RRM}	$f = 50 \text{ Hz}, t_p = 10 \text{ ms}$	4400 V	4200 V	4000 V
V_{RSM1}	$t_p = 5 \text{ ms}, \text{ single pulse}$	5700 V	5500 V	5100 V
dV/dt_{crit}	Exp. to $0.67 \times V_{DRM}, T_j = 125^\circ\text{C}$	2000 V/ μs		

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DSM}	$V_{DSM}, T_j = 125^\circ\text{C}$			400	mA
Reverse leakage current	I_{RSM}	$V_{RSM}, T_j = 125^\circ\text{C}$			400	mA

V_{DRM}/V_{RRM} are equal to V_{DSM}/V_{RSM} values up to $T_j = 110^\circ\text{C}$

Mechanical data

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		63	70	84	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m			1.45		kg
Surface creepage distance	D_S		36			mm
Air strike distance	D_a		15			mm

¹⁾ Maximum Ratings are those values beyond which damage to the device may occur

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On-state

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. average on-state current	I_{TAVM}	Half sine wave, $T_c = 70^\circ\text{C}$			2760	A
RMS on-state current	I_{TRMS}				4340	A
Max. peak non-repetitive surge current	I_{TSM}	$t_p = 10\text{ ms}$, $T_j = 125^\circ\text{C}$, $V_D = V_R = 0\text{ V}$			42000	A
Limiting load integral	I^2t				8820	kA^2s
Max. peak non-repetitive surge current	I_{TSM}	$t_p = 8.3\text{ ms}$, $T_j = 125^\circ\text{C}$, $V_D = V_R = 0\text{ V}$			45000	A
Limiting load integral	I^2t				8404	kA^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	$I_T = 3000\text{ A}$, $T_j = 125^\circ\text{C}$			1.7	V
Threshold voltage	V_{TO}	$I_T = 1300\text{ A} - 4000\text{ A}$, $T_j = 125^\circ\text{C}$			1	V
Slope resistance	r_T	$T_j = 125^\circ\text{C}$			0.225	$\text{m}\Omega$
Holding current	I_H	$T_j = 25^\circ\text{C}$			125	mA
		$T_j = 125^\circ\text{C}$			60	mA
Latching current	I_L	$T_j = 25^\circ\text{C}$			500	mA
		$T_j = 125^\circ\text{C}$			250	mA

Switching

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	$T_j = 125^\circ\text{C}$, $I_{TRM} = 3000\text{ A}$, $V_D \leq 0.67 \cdot V_{DRM}$, $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$	Cont. $f = 50\text{ Hz}$		250	$\text{A}/\mu\text{s}$
Critical rate of rise of on-state current	di/dt_{crit}				1000	$\text{A}/\mu\text{s}$
Circuit-commutated turn-off time	t_q	$T_j = 125^\circ\text{C}$, $I_{TRM} = 3000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -5\text{ A}/\mu\text{s}$, $V_D \leq 0.67 \cdot V_{DRM}$, $dv_D/dt = 20\text{ V}/\mu\text{s}$,	700			μs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Recovery charge	Q_{rr}	$T_j = 125^\circ\text{C}$, $I_{TRM} = 3000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -5\text{ A}/\mu\text{s}$	5500		7500	μAs
Delay time	t_d	$V_D = 0.4 \cdot V_{DRM}$, $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$			3	μs

Triggering

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Gate power loss	P_G	For DC gate current			3	W
Average gate power loss	P_{GAV}		see Fig. 9			

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate trigger voltage	V_{GT}	$T_j = 25^\circ\text{C}$			2.6	V
Gate trigger current	I_{GT}	$T_j = 25^\circ\text{C}$			400	mA
Gate non-trigger voltage	V_{GD}	$V_D = 0.4 \times V_{DRM}$, $T_{vjmax} = 125^\circ\text{C}$	0.3			V
Gate non-trigger current	I_{GD}	$V_D = 0.4 \times V_{DRM}$, $T_{vjmax} = 125^\circ\text{C}$	10			mA

Thermal

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_j				125	$^\circ\text{C}$
Storage temperature range	T_{stg}		-40		140	$^\circ\text{C}$

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double side cooled			7	K/kW
	$R_{th(j-c)A}$	Anode side cooled			14	K/kW
	$R_{th(j-c)C}$	Cathode side cooled			14	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double side cooled			1.5	K/kW
	$R_{th(c-h)}$	Single side cooled			3	K/kW

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^n R_i (1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i (K/kW)	4.7	0.853	1.07	0.49
τ_i (s)	0.4787	0.0824	0.0104	0.0041

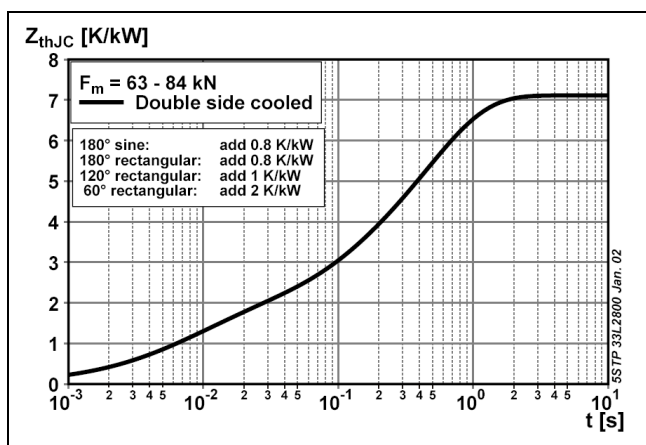


Fig. 1 Transient thermal impedance junction-to case.

On-state characteristic model:

$$VT = A + B \cdot iT + C \cdot \ln(iT + 1) + D \cdot \sqrt{IT}$$

Valid for $i_T = 500 - 10000$ A

A	B	C	D
-6.1840e-3	2.2000e-4	1.7329e-1	-6.4050e-3

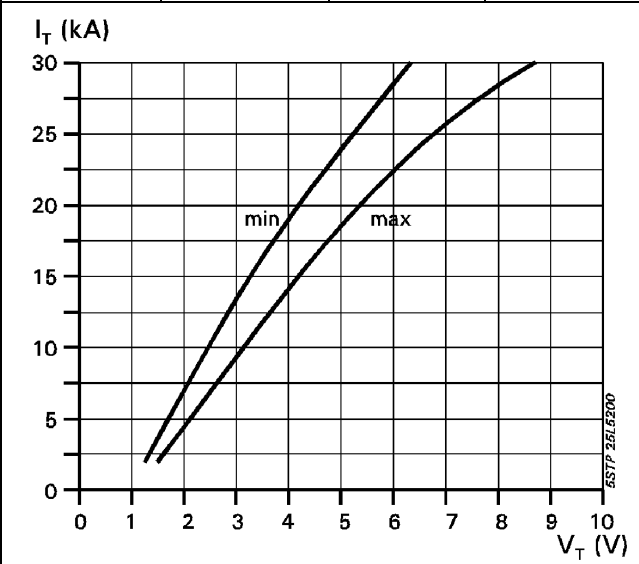


Fig. 2 On-state characteristics.
 $T_j = 125^\circ\text{C}$, 10ms half sine

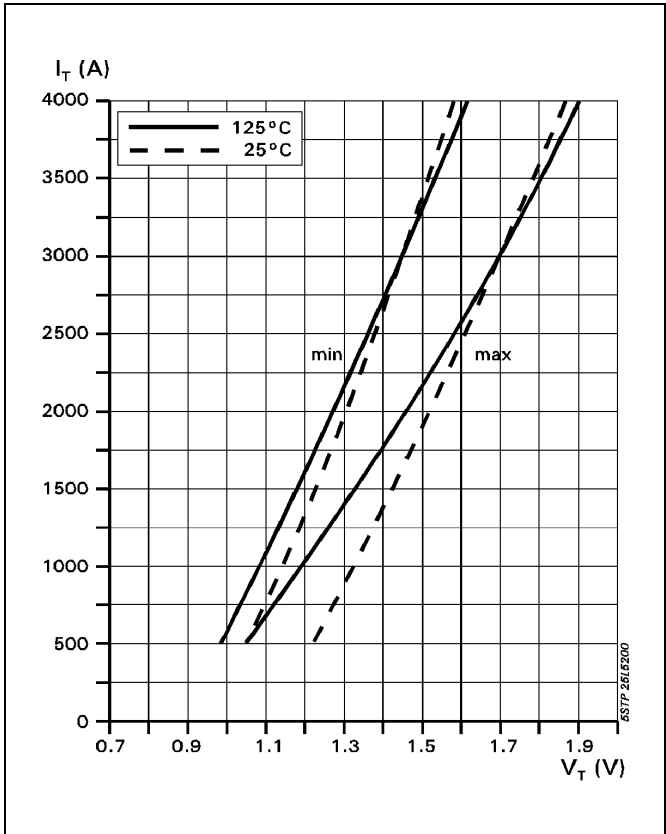


Fig. 3 On-state characteristics.

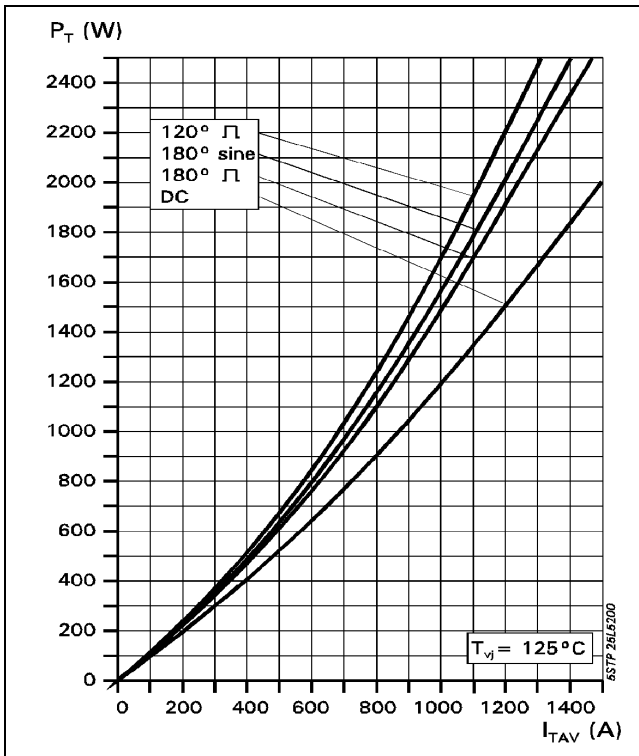


Fig. 4 On-state power dissipation vs. mean on-state current. Turn - on losses excluded.

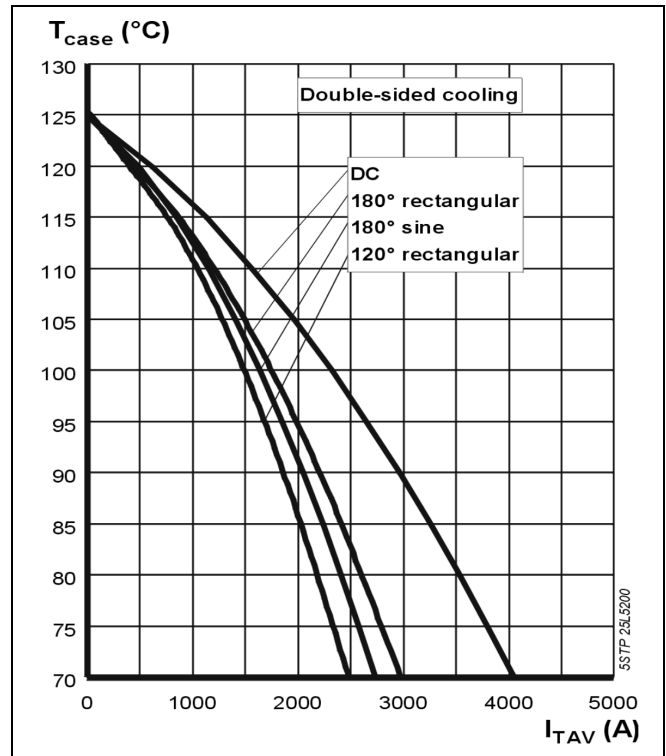


Fig. 5 Max. permissible case temperature vs. mean on-state current.

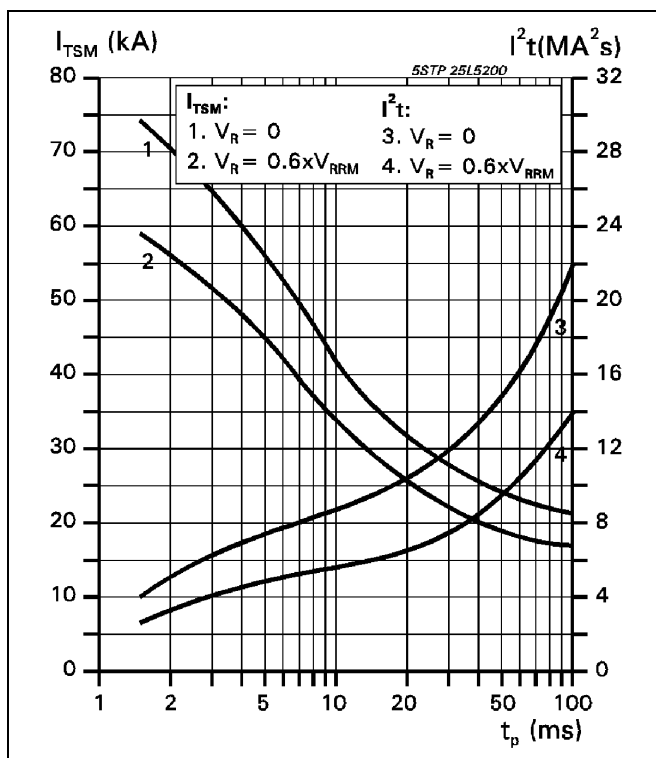


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

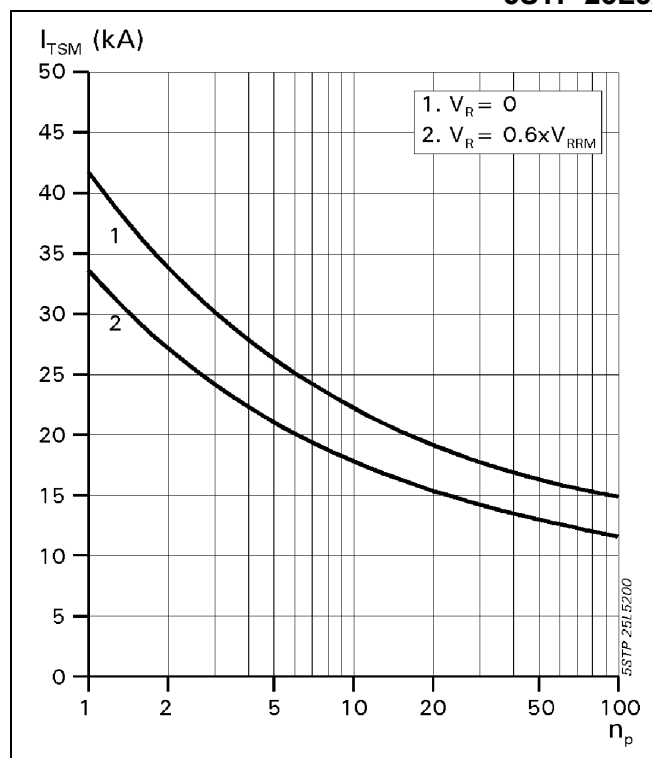


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

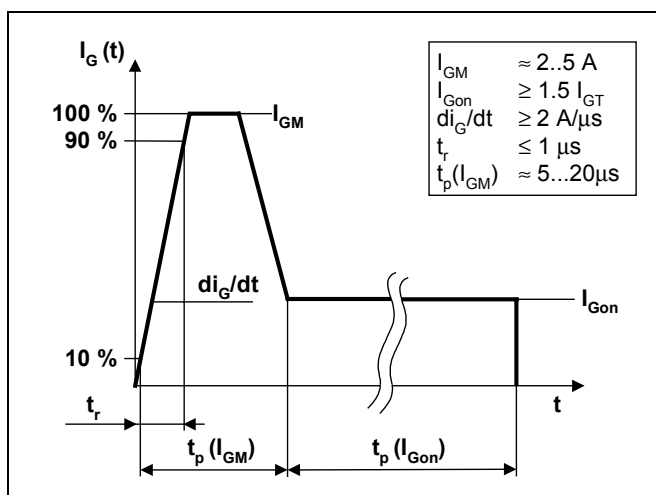


Fig. 8 Recommended gate current waveform.

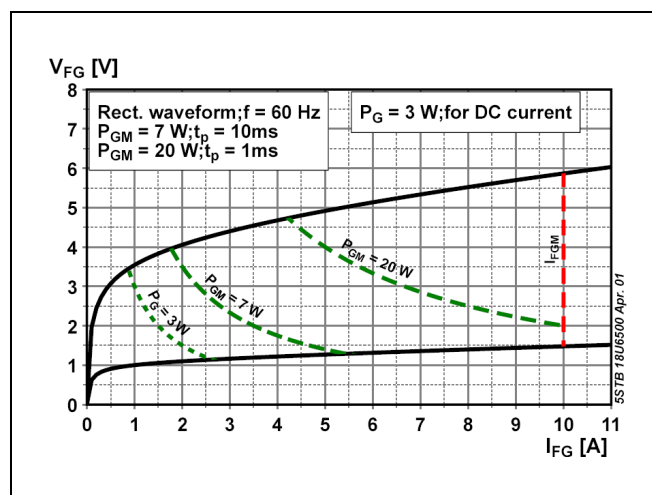


Fig. 9 Max. peak gate power loss.

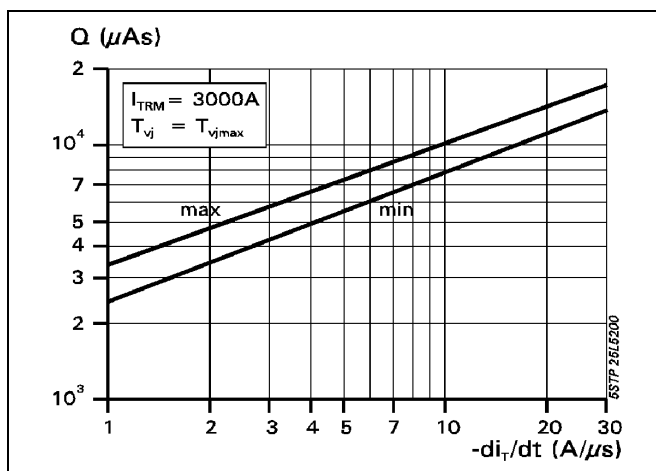


Fig. 10 Recovery charge vs. decay rate of on-state current.

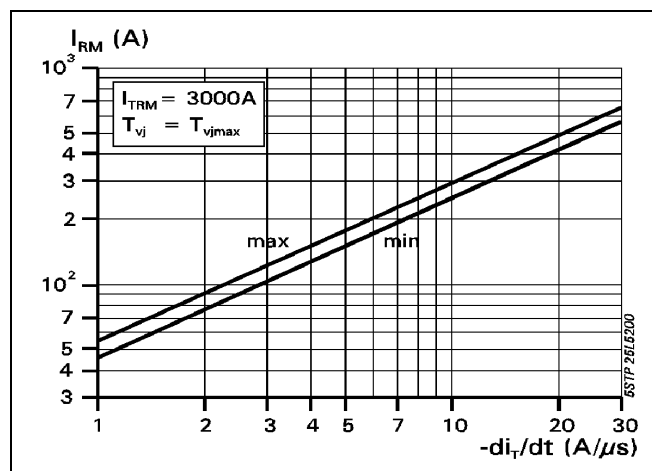


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

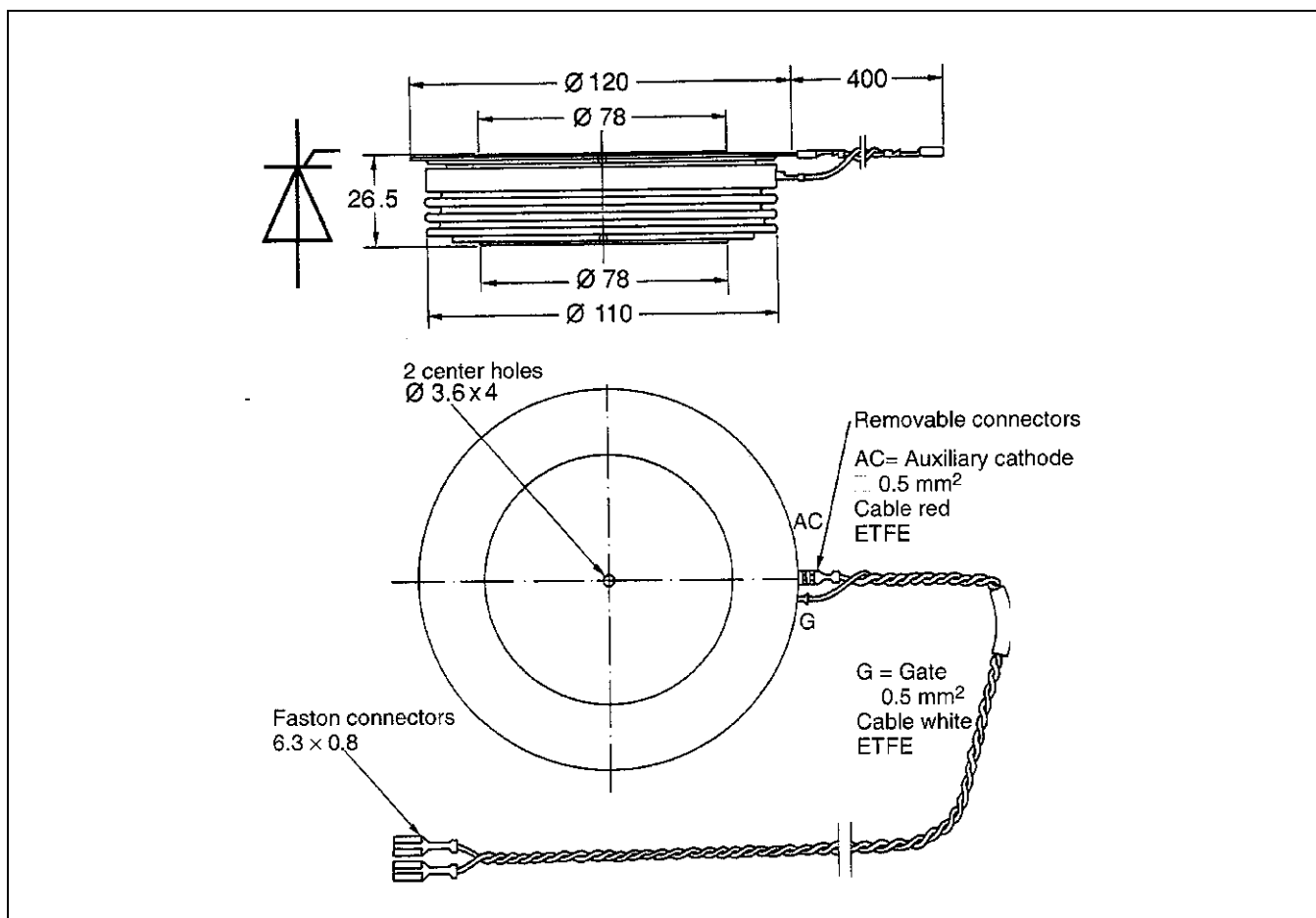


Fig. 12 Device Outline Drawing.

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