Intel 8085 Microprocessor

PIN DIAGRAM

The 8085A is an 8- bit microprocessor suitable for a wide range of application. It is a 40-pin DIP (Dual in package) chip, based on NMOS technology. It contains approximately 6200 transistors on a 164 x 222 mil chip. The pin configuration is shown in fig.3.1.

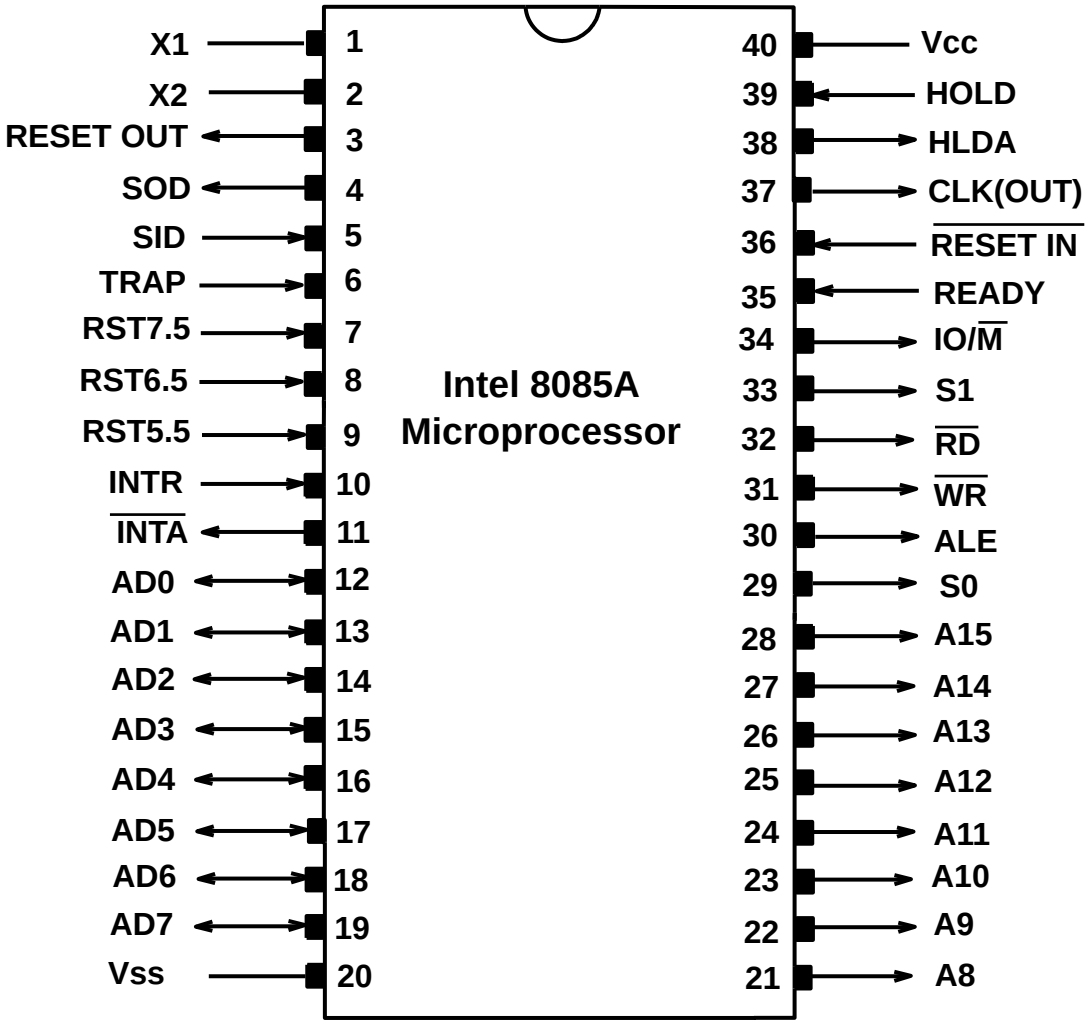

Fig.3.1 Pin Configuration of Intel 8085A Microprocessor

It requires a single +5V supply between V_{cc} at pin no. 40 and V_{ss} at pin no. 20.

Pin Configuration of Intel 8085A Microprocessor:

A_{15} – A_8 at pin no. 28 to pin no. 21:

The microprocessor can address directly 2^{16} memory locations or 65536 memory locations or 64k memory locations using 16-address lines (A_{15}-A_0). Pin no. 28 to pin no. 21 give us the higher order 8-bits of the address (A_{15}-A_8). These address lines are uni-directional, tri-state address lines. These address lines become tri-stated under three conditions namely:

(a) During DMA (direct memory access) operation.

(b) When a HALT instruction is executed.

(c) When microprocessor is being RESET.

AD_7–AD_0 at pin no. 19 to pin no. 12:

Pin no. 19 to pin no.12 marked AD_7–AD_0 are used for dual purpose. It is time multiplexed lower 8-bit address bus (A_7-A_0) and 8-bit data bus (D_7-D_0). Because at the time when this chip was developed, the practical limit on the numbers of pins was 40. The only solution was to multiplex part of the address bus with the data bus.

Before discussing, the functions of different pins, it is better to know few more points about the processor. The microprocessor, being a logic circuit, shall move from one state to the other state during it operation. There are ten (10) different possible states for the processor and the processor will be in one of these states as long as the power is ON. These states are:

1. RESET STATE: (T_{RESET}): Whenever microprocessor is reset, it enters in reset state. The microprocessor can be in T_{RESET} state for an integral multiple of clock cycle.
2. WAIT STATE: It can be in this state for an integral number of clock cycles, the duration being determined by an external content signal input marked READY.
3. HOLD STATE: (T_{HOLD}): As long as HOLD signal is active, microprocessor is in HOLD state.
4. HALT STATE: (T_{HALT}): Microprocessor enters in this state when an HALT instruction is executed by the processor. It remains in this state till such time when an external signal dictated by the user asked the microprocessor to perform further duties.
5. The other states the microprocessor can be in are marked T_1, T_2, T_3, T_4, T_5 & T_6 state. Each of these states is of one clock period duration. During each of these predetermined timing slots microprocessor performs very well defined activities.

Pin no.19 to pin no.12 are used by the microprocessor to send lower order 8-bits of the memory address during T_1 timing plot of a machine cycle. Therefore, the same 8-pins are utilized as bi-directional data bus for data transfer operation in the subsequent timing plots T_2 & T_3. Hence, these pins are designated as $AD_7 - AD_0$.

These 8 lines are also tri-state lines. They will be tri-stated during T_4, T_5 & T_6 states. They will also be restated during DMA operation, during RESET operation & when a HALT instruction is executed. These lines will also be tri-stated for a very short duration of time (few neon seconds) between T_1 &T_2 states.

ALE at Pin No 30:

The 8085A uses a time multiplexed address-data bus. This is due to limited number of pins on the 8085A. Low-order 8-bits of the address appear on the AD bus during the first clock cycle i.e., T_1 state of a machine cycle. It then becomes the data bus during the second and third clock cycles i.e., T_2 and T_3 states.

ALE stands for address latch enable. It is used to distinguish whether the $AD_7 – AD_0$ bus contains address bits $A_7 – A_0$ or data bits D_7- D_0. It is a single pulse issued during every T_1 state of the microprocessor as shown in fig.3.2.

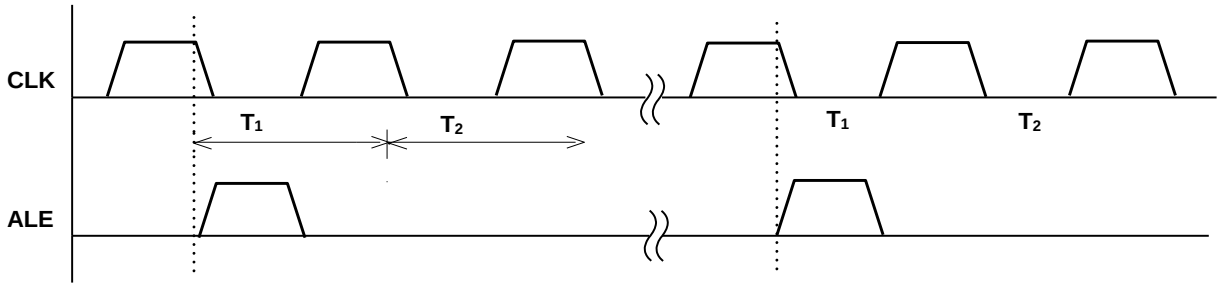

Fig.3.2 ALE Signal Issued in Every T_1 State

Since the lower 8-bits of the address information A_7 to A_0 is available at pin no.19 to pin no.12 only during T_1 period, therefore, ALE pulse can be can be used to latch address A_7 to A_0 in an external latch. ALE output is high during first half of the T_1 period and its falling edge can be used to latch the address bits A_7 to A_0 in an external latch e.g. 74LS373 register latch.

Fig.3.3a shows a schematic that uses a latch and the ALE signal to de multiplex the bus. The bus AD_7-AD_0 is connected as the input to the latch 74LS373. The ALE signal is connected to the enable (G) pin of the latch, and the output control (OC) signal of the latch is grounded. When ALE goes high during the T_1 state of a

machine cycle, the latch is transparent and the output of the latch changes according to the input. The CPU is putting lower-order bits of address during this time. When the ALE goes LOW, the address bits get latched on the output and remain so until the next ALE signal.

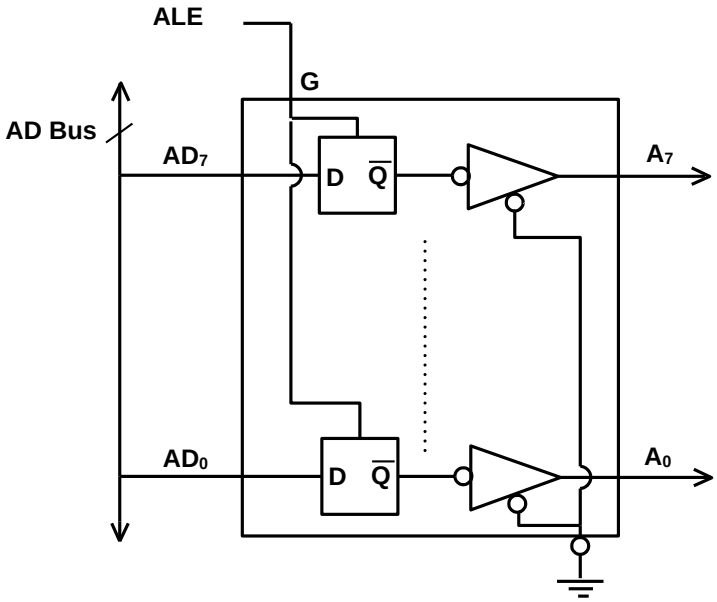

Fig.3.3a Latching of Lower Order Address in External Latch

Once saved in an external latch the lower order address A_7 to A_0 shall be available at the output of the register latch for the subsequent states T_2, T_3, T_4, T_5 & T_6, while pin no. 19 to pin no.12 can then be utilized by the microprocessor for bi-directional operation. The falling edge of the ALE can also be used to store status information being output by the 8085A during each machine cycle. The ALE output is never tri-stated in the 8085A. The manner of utilization of pins 19 to 12 is known as time multiplexed mode of operation.

The de-multiplexing of AD bus by latching lower byte of 16-bit address in external 8-bit latch 74LS373 is shown in fig.3.3b. Once the lower byte address is latched, the AD bus is available for bi-directional data transfer. The 8-bit higher order address issued by

microprocessor in every T1 state along with latched lower byte address constitutes unidirectional 16-bit address bus. The control signals put together constitutes bi-directional control bus, where some of the signals are always input and some are always output. The three buses, address bus, data bus and control bus together constitutes system bus.

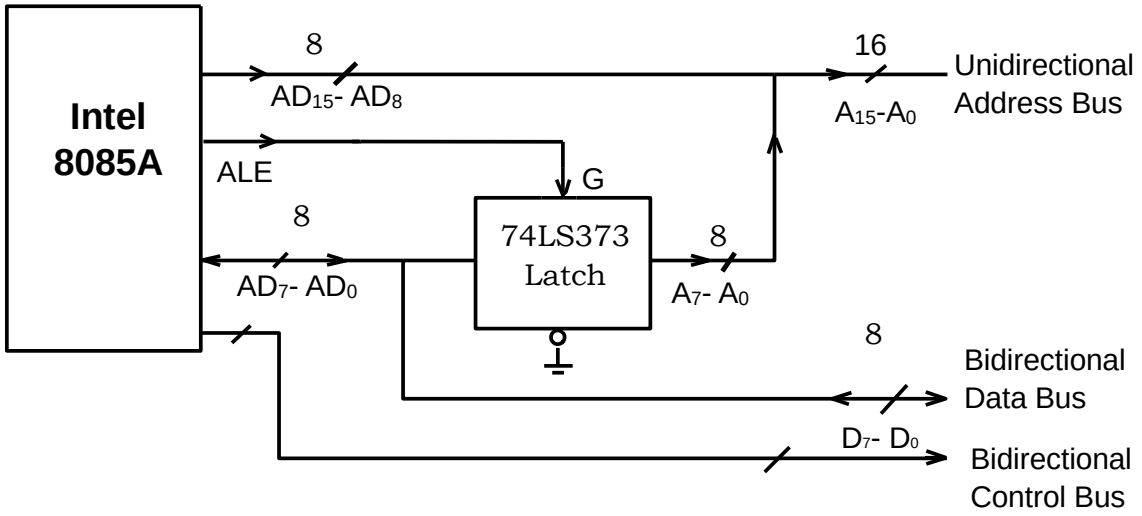

Fig.3.3b De-multiplexing of AD bus to Generate System Bus

The fact that ALE is required is a direct consequence of having a multiplexed data/address bus. This is unlike the Intel 8080 microprocessor which is similar to the 8085A but where these buses are not multiplexed. Some of the peripheral chips 8155/ 8156/ 8355/ 8755A have internal multiplexing facility, therefore, ALE input pin of these peripheral chips is connected to ALE output pin of the 8085 A, thus allowing a direct interface with the 8085 A. Thus IC chips internally de-multiplex the AD bus using the ALE signal. Since a majority of peripheral devices do not have the internal multiplexing facility, there is external hardware necessity for it.

$\overline{RD}$ & $\overline{WR}$ Control signals at pin no 32 and at pin no 31:

The BDB at pin no 19 to 12 are used for bi-directional data transfer operation during T_2 & T_3 states. When the BDB is inputting the information from the external world into the microprocessor, we say that μp is in READ mode and operation is READ operation. When the μp is outputting 8-bit of information to the external world through BDB we say μp is in WRITE mode and operation is WRITE operation.

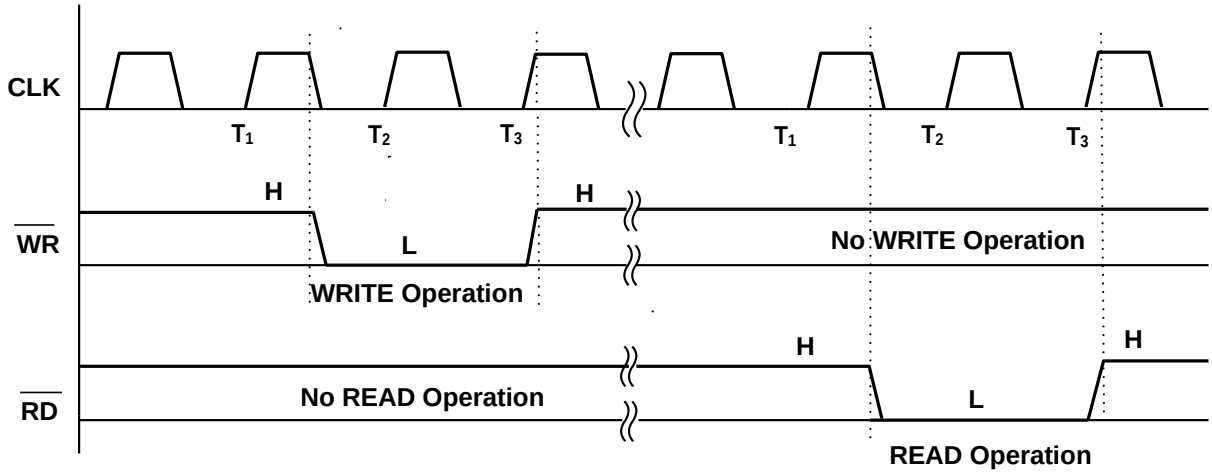

Fig.3.4 Read and Write Signals Issued During T_2-T_3 State

To tell the external world that μp is in WRITE mode, μp issues a control signal output $\overline{WR}$ at pin no. 31. It is normally HIGH & active LOW. It goes LOW during the beginning of T_2 state and goes HIGH again during middle of T_3 state of the microprocessor. This is shown is fig.3.4.

During WRITE operation, μp first send the desired address on the address bus during T_1 state, thereafter it places the desired data on BDB which is now in input mode and then issues a control signal, $\overline{WR}$. A low level on $\overline{WR}$ indicates that the data on data bus is to be written in to the selected memory location or I/O device. Data is setup

at the trailing edge. It is for the user to take appropriate action externally by the interfacing circuitry so that the data so placed goes to the appropriate device.

Similarly to tell the external world the microprocessor is in input mode for READ operation, it issues a control signal $\overline{RD}$ which is normally HIGH and active LOW. $\overline{RD}$ signal goes LOW during T_2 state and goes HIGH again during T_3 state similar to $\overline{WR}$ signal. A LOW level an $\overline{RD}$ indicates the selected memory or I/O device is to be read and the data bus is available for the data transfer. It is for the user to keep the appropriate 8-bit data either from the memory or I/O device during this period.

Both $\overline{RD}$ and $\overline{WR}$ are never made LOW at the same time. Both the signals are tri-stated during HOLD, HALT and RESET states.

IO/$\overline{M}$ at pin no 34:

IO/$\overline{M}$ is an output tri-state control signal. It is active both ways (HIGH as well as LOW). Whenever the address issued by the μp on the address lines refers to the memory then the μp makes IO/$\overline{M}$ LOW throughout T_1,T_2,T_3,T_4,T_5 & T_6 states of the machine cycle to indicate the external world that the address so sent belongs to the memory and data on the BDB refers to the memory.

Whenever the address on the address lines refers to an I/O device the μp makes IO/$\overline{M}$ control signal output HIGH to tell the external world that the address on the address bus refers to and I/O device and the data on the BDB refers to an I/O device.

Note that IO/$\overline{M}$ signal is LOW or HIGH as the case may be throughout six timing slots T_1,T_2,T_3,T_4,T_5 & T_6 states. It is for the user to make use of this feature to develop proper interfacing circuitry i.e., to generate the chip selected signals. In other words, a LOW IO/$\overline{M}$ signal enables the memory chips and a HIGH IO/$\overline{M}$ signal enables the I/O device.