SN74LV4052A-Q1 Dual 4-Channel Analog Multiplexers and Demultiplexers

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Supports Mixed-Mode Voltage Operation on All Ports
- Fast Switching
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Extremely Low Input Current

2 Applications

- Automotive:
  - Signal Gating
  - Chopping
  - Modulation or Demodulation (Modem)
  - Signal Multiplexing for Analog-to-Digital and Digital-to-Analog Conversion Systems

3 Description

These dual 4-channel CMOS analog multiplexers and demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The SN7LV4052A-Q1 devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak).

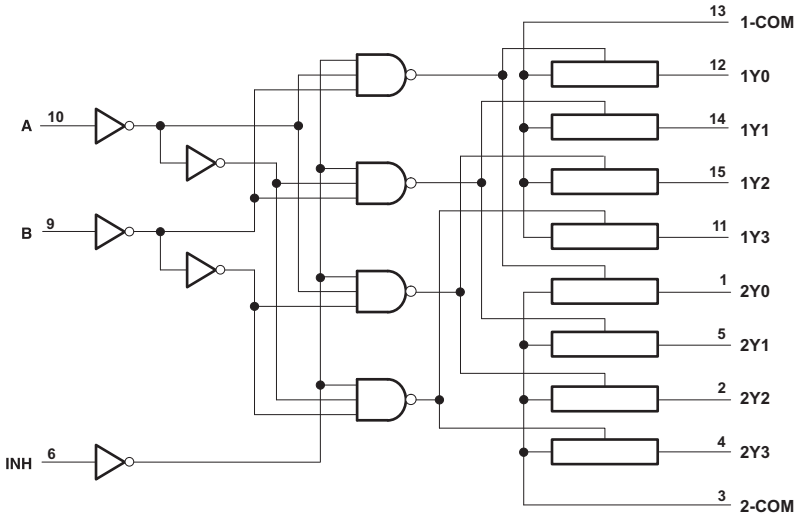
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV4052A-Q1	TSSOP (16)	5.00 mm × 4.40 mm
	SOIC (16)	9.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

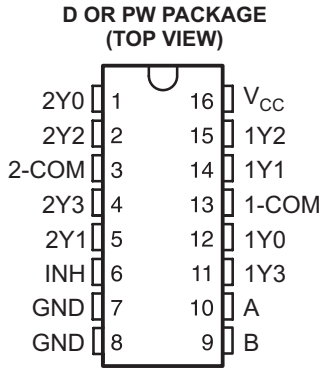
Changes from Revision E (November 2012) to Revision F **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4

Changes from Revision D (June 2011) to Revision E **Page**

- Deleted θ_{JA} row from Absolute Maximum Ratings table ... 4
- Added Thermal Information table ... 5
- Corrected second row of Function Table ... 11

5 Pin Configuration and Functions



Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	2Y0	I(1)	Input to mux 2
2	2Y2	I(1)	Input to mux 2
3	2-COM	O(1)	Output of mux 2
4	2Y3	I(1)	Input to mux 2
5	2Y1	I(1)	Input to mux 2
6	INH	I	Enables the outputs of the device. Logic low level with turn the outputs on, high level will turn them off.
7	GND	-	Ground
8	GND	-	Ground
9	B	I	Selector line for outputs (see Device Functional Modes for specific information)
10	A	I	Selector line for outputs (see Device Functional Modes for specific information)
11	1Y3	I(1)	Input to mux 1
12	1Y0	I(1)	Input to mux 1
13	1-COM	O(1)	Output of mux 1
14	1Y1	I(1)	Input to mux 1
15	1Y2	I(1)	Input to mux 1
16	Vcc	I	Device power input

(1) These I/O descriptions represent the device when used as a multiplexer, when this device is operated as a demultiplexer pins 1Y0, 1Y1, 1Y2, 1Y3, 2Y0, 2Y1, 2Y2, 2Y3 may be considered outputs (O) and pins 1-COM and 2-COM may be considered inputs (I).

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	
V_{IO}	Switch I/O voltage range(2) (3)		–0.5	V_{CC} + 0.5	
I_{IK}	Input clamp current	V_I < 0	–20		mA
I_{IOK}	I/O diode current	V_{IO} < 0	–50		
I_T	Switch through current	V_{IO} = 0 to V_{CC}		±25	
	Continuous current through V_{CC} or GND			±50	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The maximum limit for this value is 5.5 V.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (2Y0, GND, V_{CC}, and B)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2(2)		5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5			V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7			
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7			
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7			
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V			0.5	V
		V_{CC} = 2.3 V to 2.7 V			V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V			V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V			V_{CC} × 0.3	
V_I	Control input voltage		0		5.5	V
V_{IO}	Input/output voltage		0		V_{CC}	V
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V			200	ns/V
		V_{CC} = 3 V to 3.6 V			100	
		V_{CC} = 4.5 V to 5.5 V			20	
T_A	Operating free-air temperature	SN74LV4052ATDRQ1, SN74LV4052ATPWRQ1	–40		105	°C
T_A	Operating free-air temperature	SN74LV4052AQPWRQ1	–40		125	

(1) Hold all unused inputs of the device at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. TI recommends transmitting only digital signals at these low supply voltages.

6.4 Thermal Information

THERMAL METRIC		SN74LV4052A-Q1		UNIT
		D	PW	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.9	113.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.6	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.4	58.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.4	6.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.1	57.8	°C/W

6.5 Operating Characteristics

V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	11.8	pF

6.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = -40 to 105°C			T_A = -40 to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
r_{on}	On-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL} (see Figure 1)	2.3 V			225			225	Ω
			3 V			190			190	
			4.5 V			100			100	
$r_{on(p)}$	Peak on-state resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL}	2.3 V			600			600	Ω
			3 V			225			225	
			4.5 V			125			125	
Δr_{on}	Difference in on-state resistance between switch	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL}	2.3 V			40			40	Ω
			3 V			30			30	
			4.5 V			20			20	
I_I	Control input current	V_I = 5.5 V or GND	0 V to 5.5 V			±1			±2	μA
$I_{S(off)}$	Off-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_{INH} = V_{IH} (see Figure 2)	5.5 V			±1			±2	μA
$I_{S(on)}$	On-state switch leakage current	V_I = V_{CC} or GND, V_{INH} = V_{IL} (see Figure 3)	5.5 V			±1			±2	μA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5 V			20			40	μA

6.7 Switching Characteristics V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT	TEST CONDITIONS	T_A = -40 to 105°C			T_A = -40 to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF (see Figure 4)			12			14	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF (see Figure 5)			25			25	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF (see Figure 5)			25			25	ns

6.8 Switching Characteristics V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT	TEST CONDITIONS	T_A = -40 to 105°C			T_A = -40 to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF (see Figure 4)			8			10	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF (see Figure 5)			18			18	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF (see Figure 5)			18			18	ns

6.9 Analog Switch Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	T_A = 25°C			UNIT
						MIN	TYP	MAX	
Frequency response (switch on)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave)(1) (see Figure 6)		2.3 V		30		MHz
					3 V		35		
					4.5 V		50		
Crosstalk (between any switches))	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (seeFigure 7)		2.3 V		–45		dB
					3 V		–45		
					4.5 V		–45		
Crosstalk (control input to signal output)	INH	COM or Y	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)		2.3 V		20		mV
					3 V		35		
					4.5 V		65		
Feedthrough attenuation (switch off)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz(2) (see Figure 9)		2.3 V		–45		dB
					3 V		–45		
					4.5 V		–45		
Sine-wave distortion	COM or Y	Y or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	V_I = 2 Vp-p	2.3 V		0.1%		
				V_I = 2.5 Vp-p	3 V		0.1%		
				V_I = 4 Vp-p	4.5 V		0.1%		

(1) Adjust f_{in} voltage to obtain 0-dBm output. Increase fin frequency until dB meter reads −3 dB.
(2) Adjust f_{in} voltage to obtain 0-dBm input.

7 Parameter Measurement Information

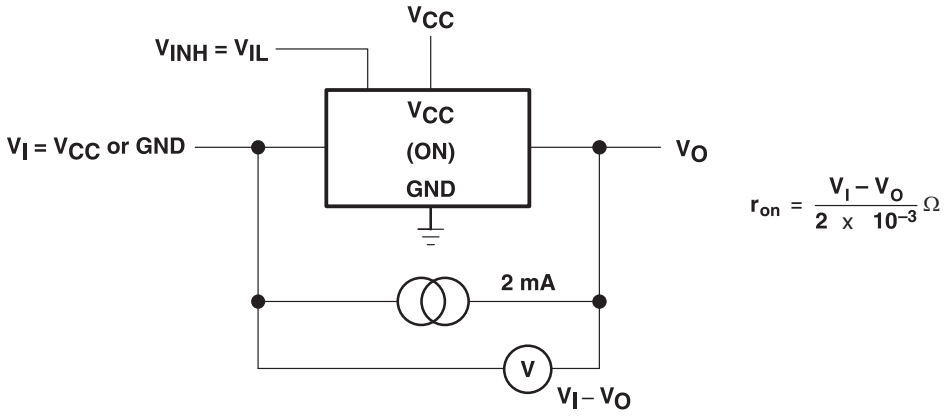
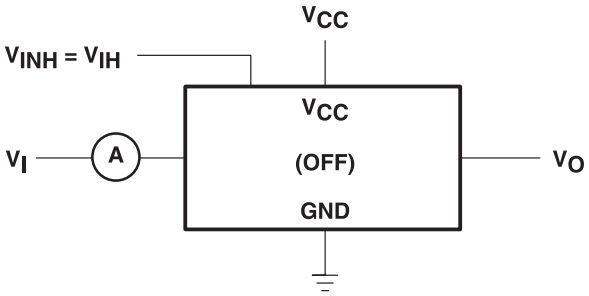


Figure 1. On-State Resistance Test Circuit



Condition 1: V_I = 0, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = 0

Figure 2. Off-State Switch Leakage-Current Test Circuit

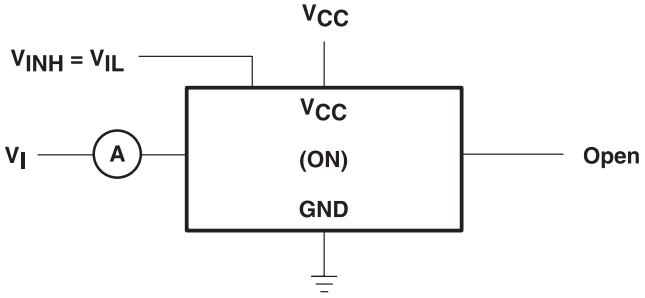


Figure 3. On-State Switch Leakage-Current Test Circuit

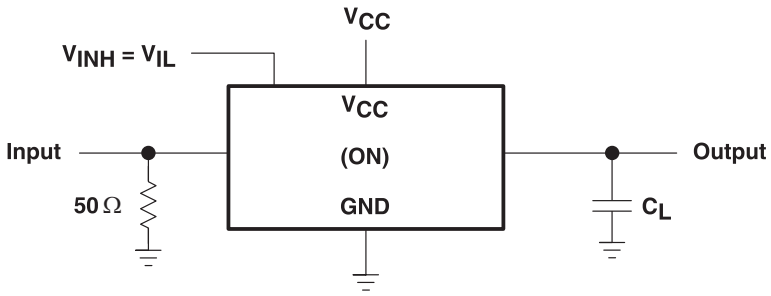
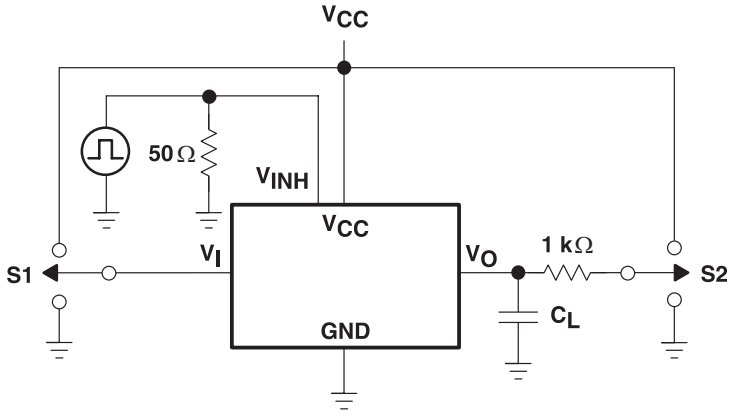


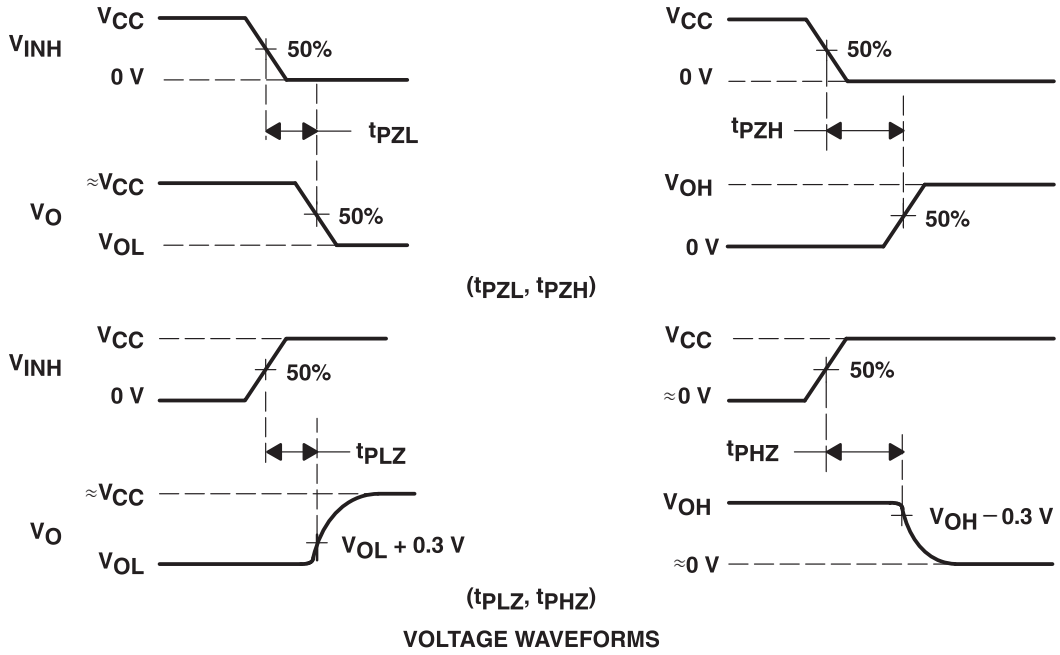
Figure 4. Propagation Delay Time, Signal Input to Signal Output

Parameter Measurement Information (continued)



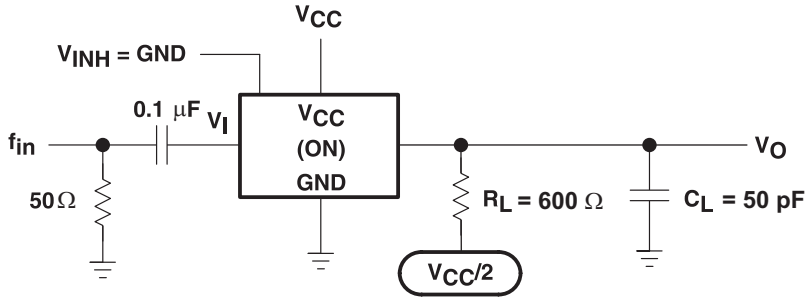
TEST	S1	S2
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	GND V_{CC}	V_{CC} GND

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

Parameter Measurement Information (continued)

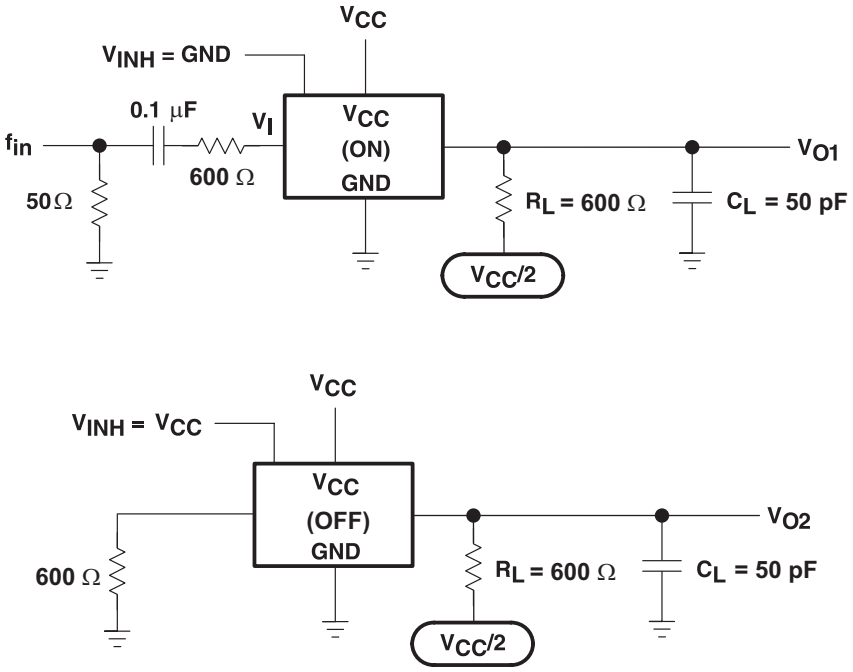


Figure 7. Crosstalk Between Any Two Switches

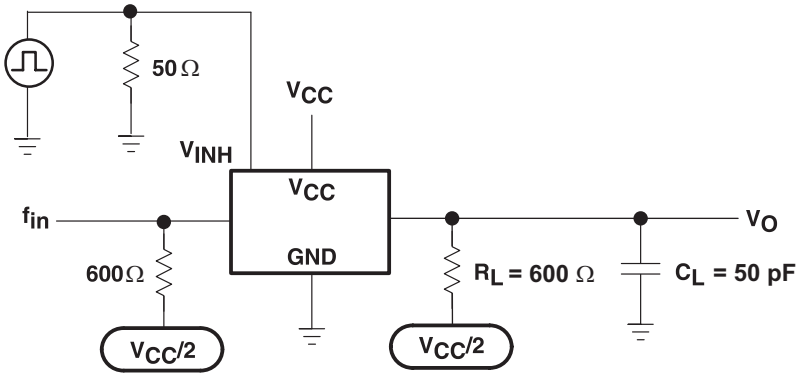


Figure 8. Crosstalk Between Control Input and Switch Output

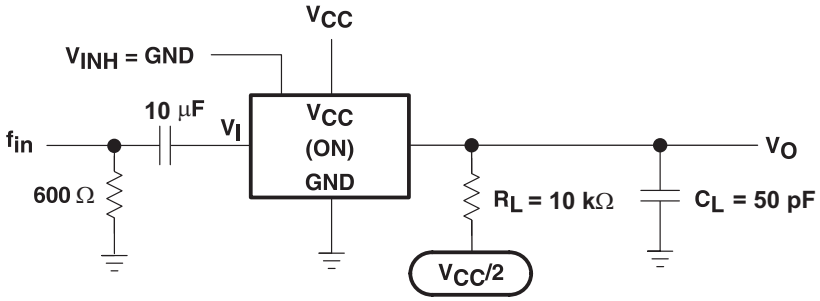


Figure 9. Feedthrough Attenuation (Switch Off)

Parameter Measurement Information (continued)

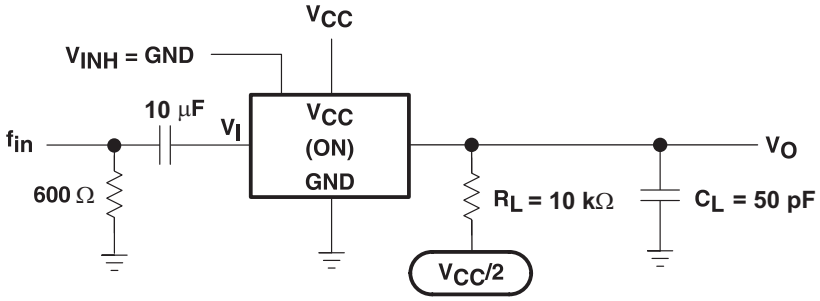


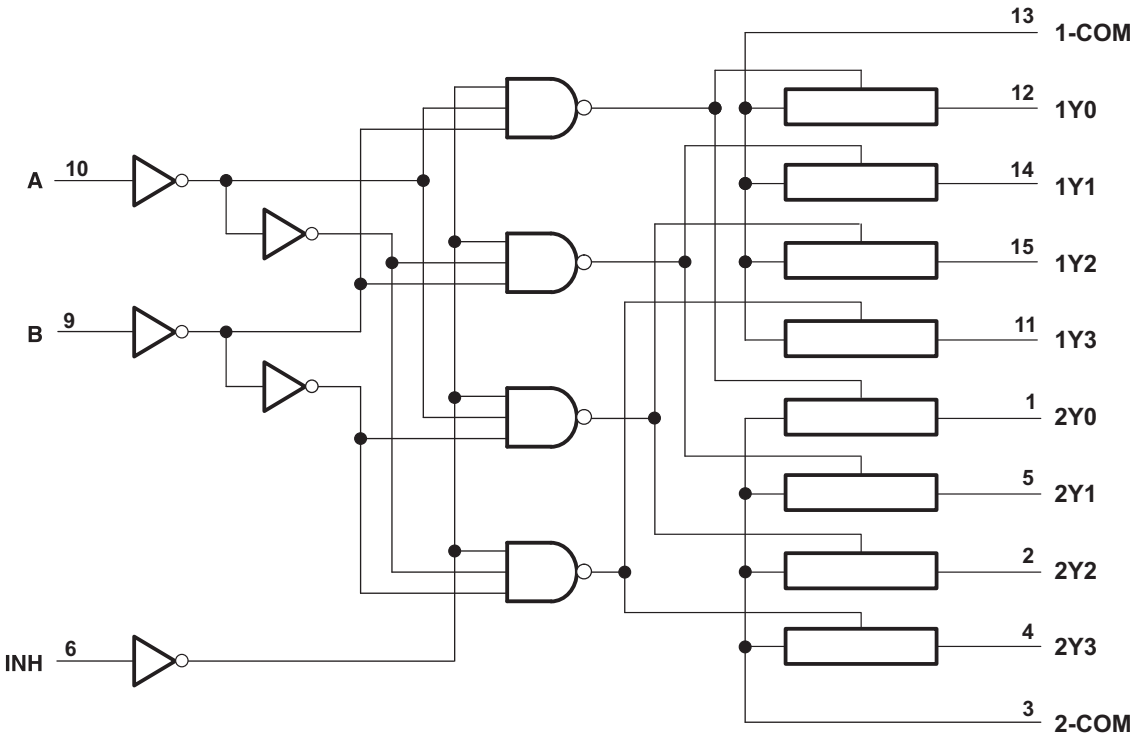
Figure 10. Sine-Wave Distortion

8 Detailed Description

8.1 Overview

This device is a dual 4-channel analog multiplexer. A multiplexer is often used when several signals need to share the same device or resource. This device allows the selection of one of these signals at a time for analysis or propagation.

8.2 Functional Block Diagram



8.3 Feature Description

This device contains 2 separate 4-channel multiplexers for use in a variety of applications. The 4-channel multiplexers can also be configured as demultiplexers by using the COM pins as inputs and the 1Yx or 2Yx pins as outputs. This device is qualified for automotive applications and has an extended temperature range of -40C to 125C (maximum depends on package type).

8.4 Device Functional Modes

Table 1. Function Table

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A multiplexer is used in applications where multiple signals share a resource. In the example below, several different sensors are connected to the analog-to-digital converter (ADC) of a microcontroller (MCU).

9.2 Typical Application

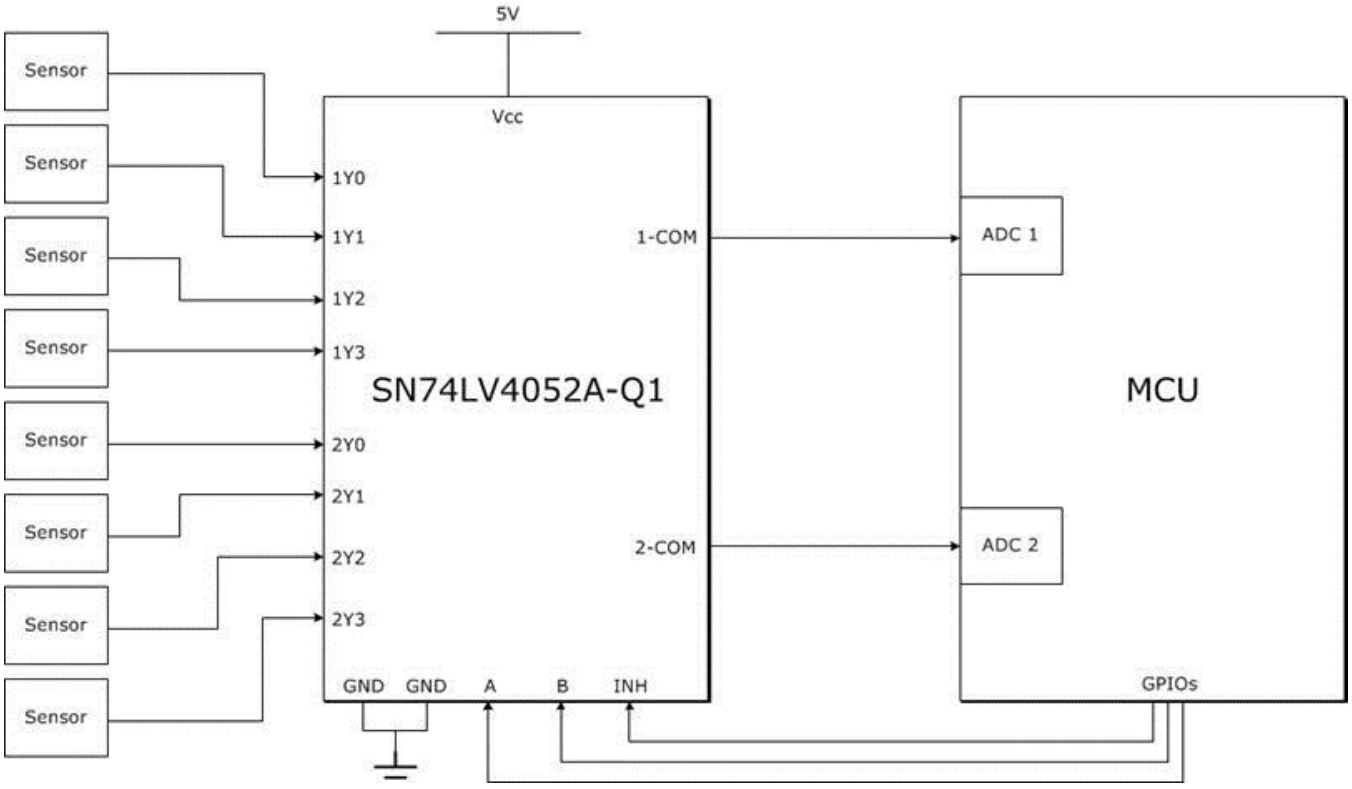


Figure 11. Typical Application Schematic

9.2.1 Design Requirements

Normally processing 8 different analog signals would require 8 separate ADCs, but this figure shows how to achieve this using only 2 ADCs and 3 GPIOs (general purpose input/outputs).

9.2.2 Detailed Design Procedure

To design with the SN74LV4052A-Q1, a stable input voltage between 2V (see *Recommended Operating Conditions*(1) for details) and 5.5 V must be available. Another important design consideration would be the characteristics of the signal that is being multiplexed to make sure no important information is lost due to timing or voltage level incompatibility with this device.

(1) Hold all unused inputs of the device at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

10 Power Supply Recommendations

Most systems have a common 3.3 V or 5 V rail that may be used to supply the V_{CC} pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) may be used to supply this device from a higher voltage rail.

11 Layout

11.1 Layout Guidelines

In general, it is best to keep signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω,as required by the application. Be careful placing this device too close to high voltage switching components, as they may cause interference.

11.2 Layout Example

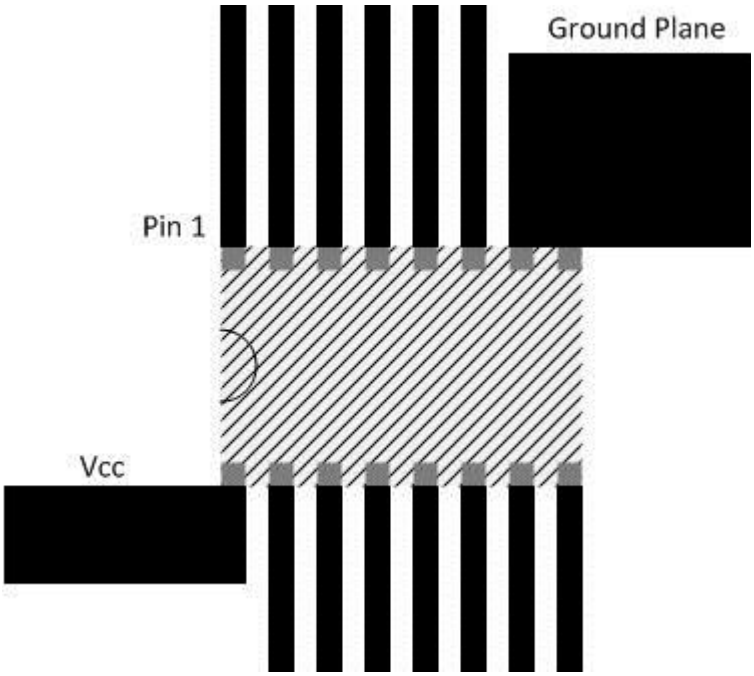


Figure 12. Layout Example Schematic

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLV4052ATPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4052AQ	Samples
SN74LV4052AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	4052AQ1	Samples
SN74LV4052ATDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4052AQ	Samples
SN74LV4052ATPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4052AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LV4052A-Q1 :

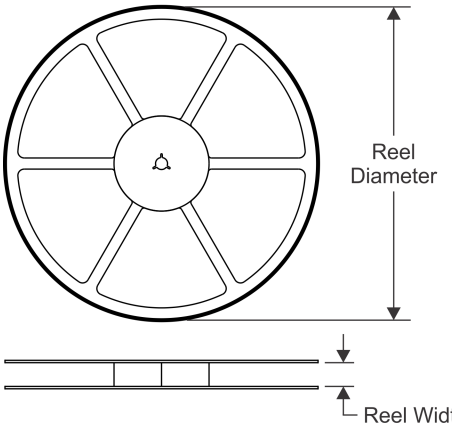
- Catalog: SN74LV4052A
- Enhanced Product: SN74LV4052A-EP

NOTE: Qualified Version Definitions:

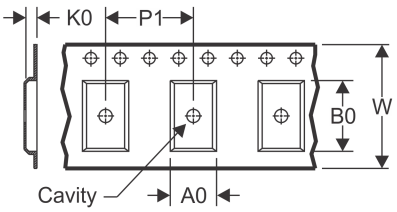
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

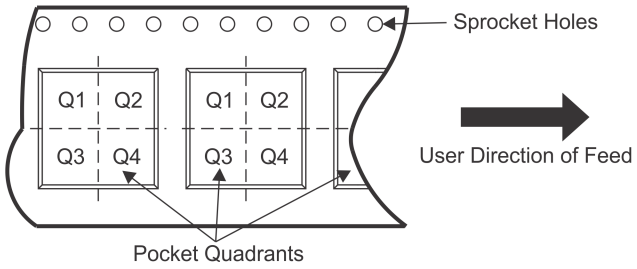


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

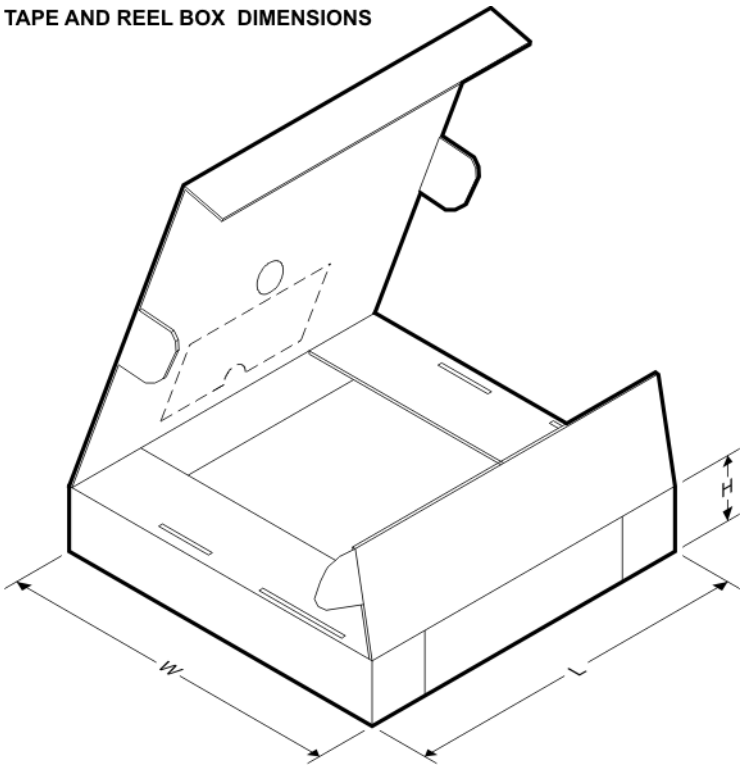
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLV4052ATPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052ATPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

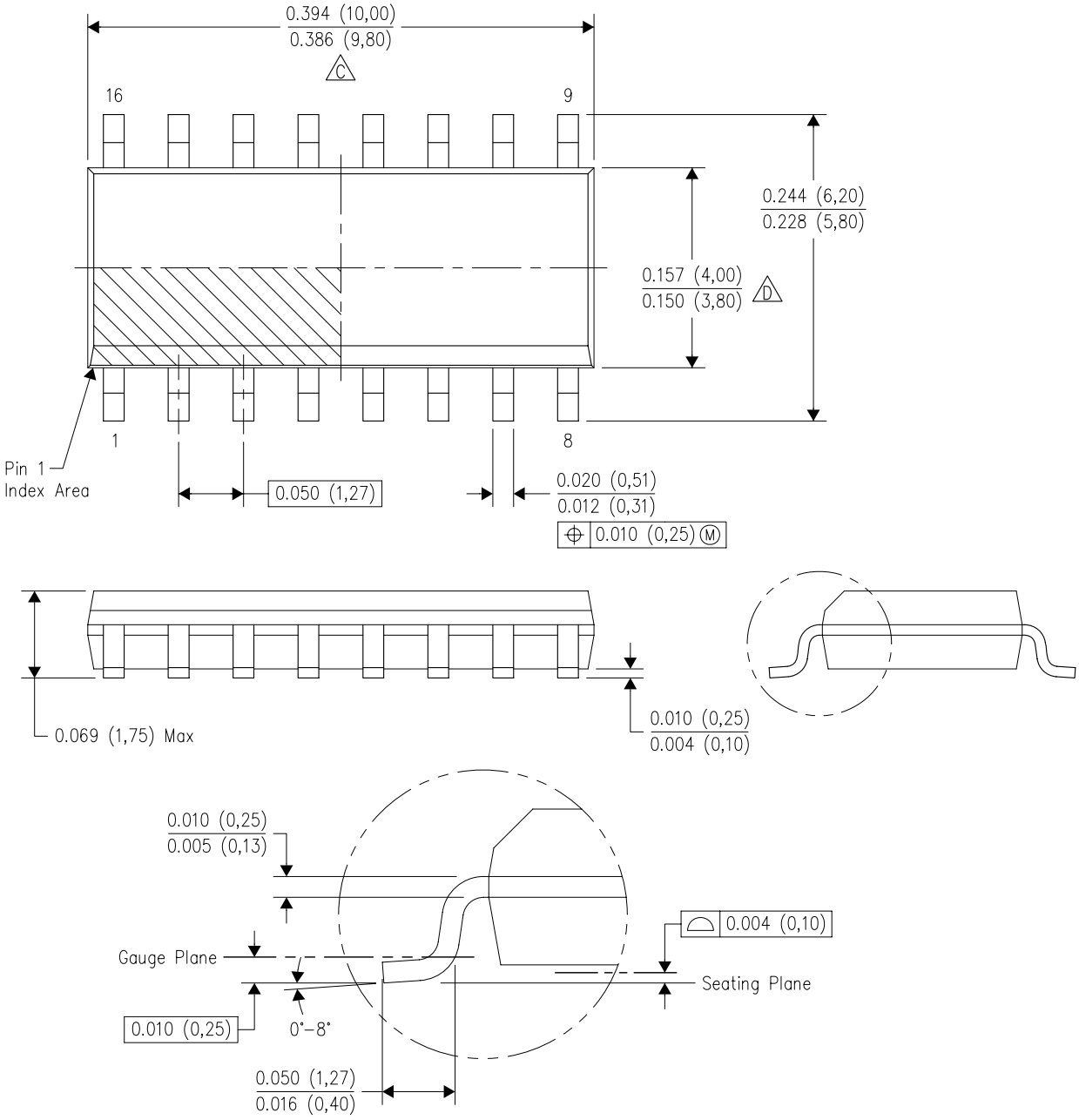
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

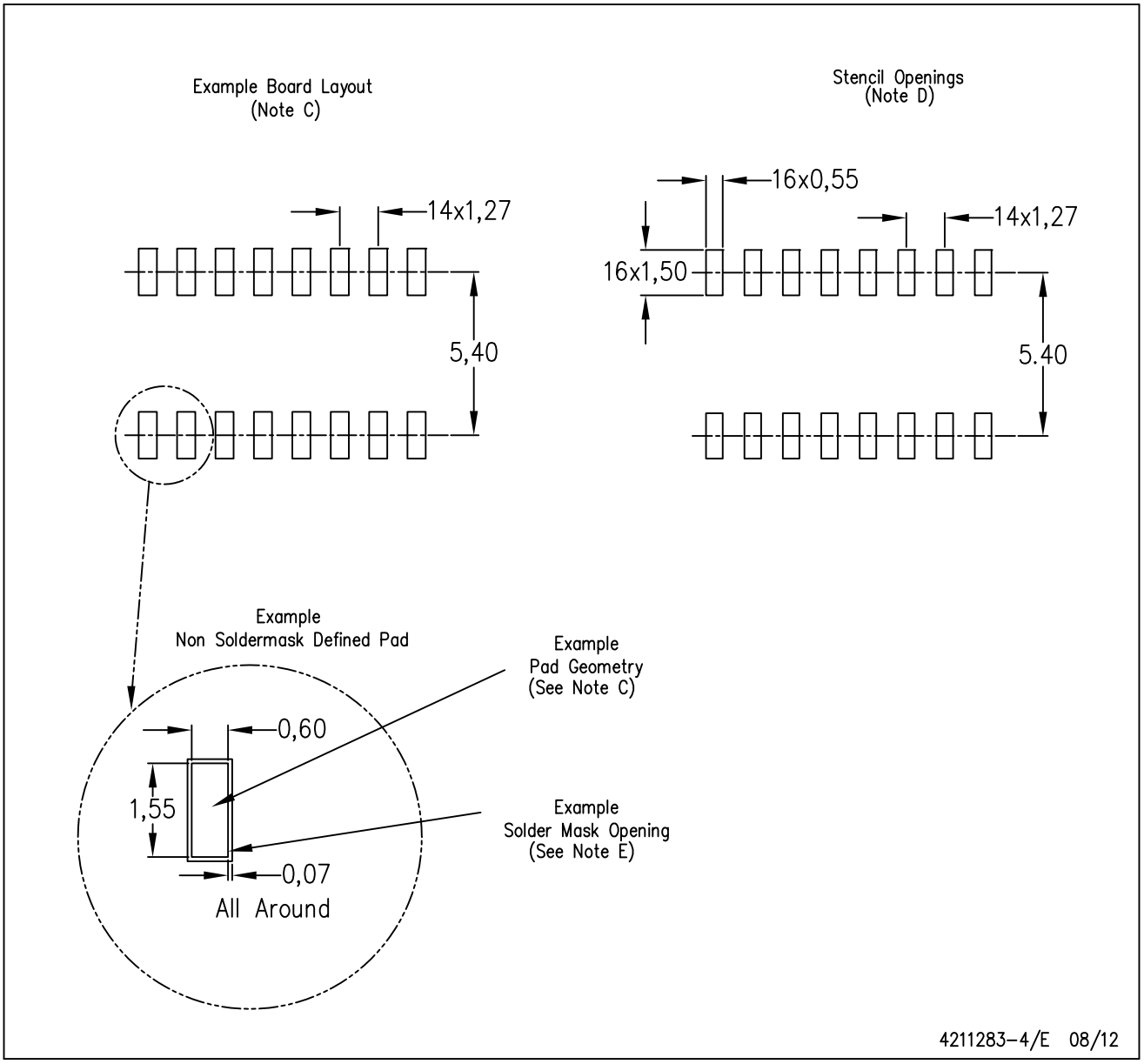
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLV4052ATPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4052AQPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4052ATPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



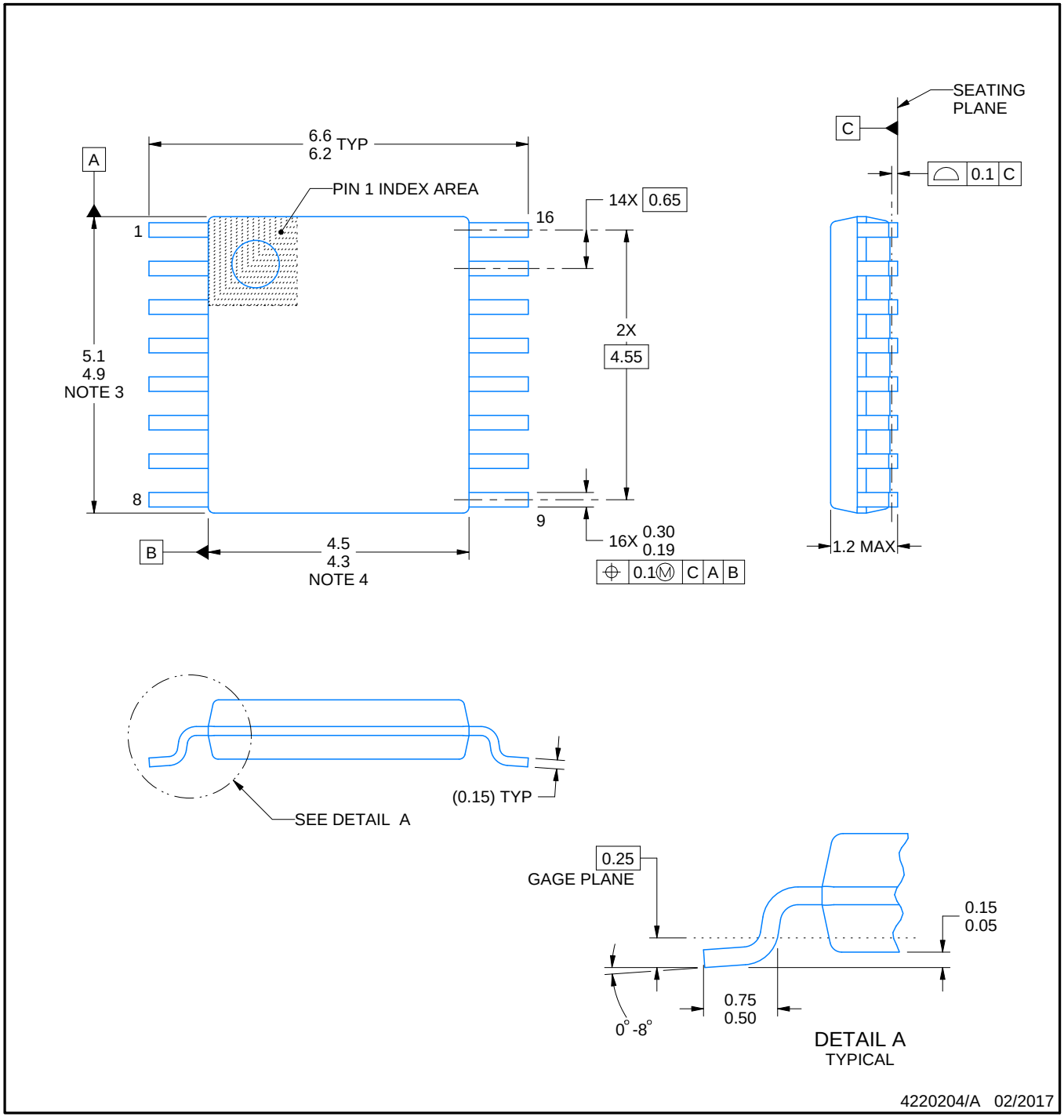
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

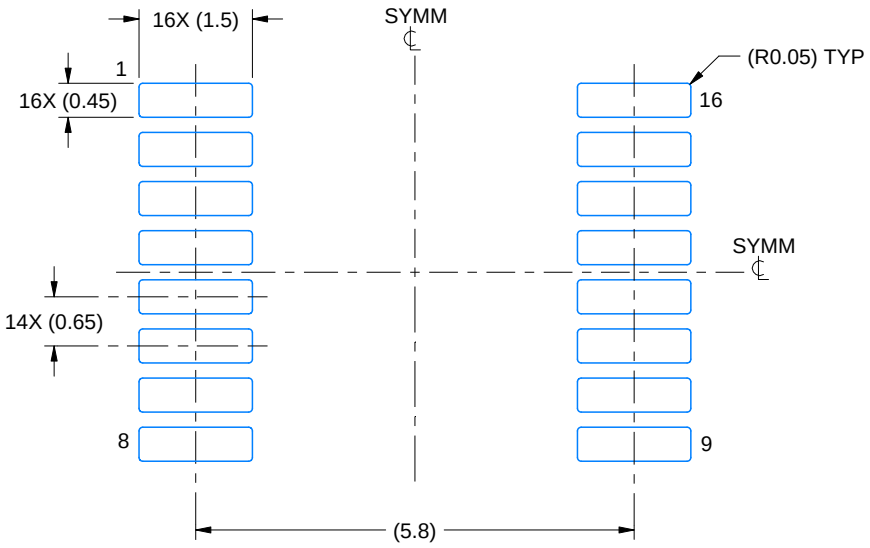
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

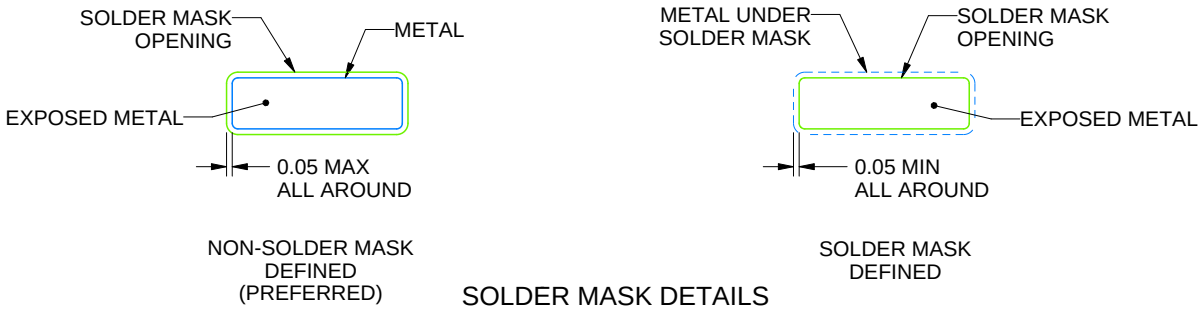


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

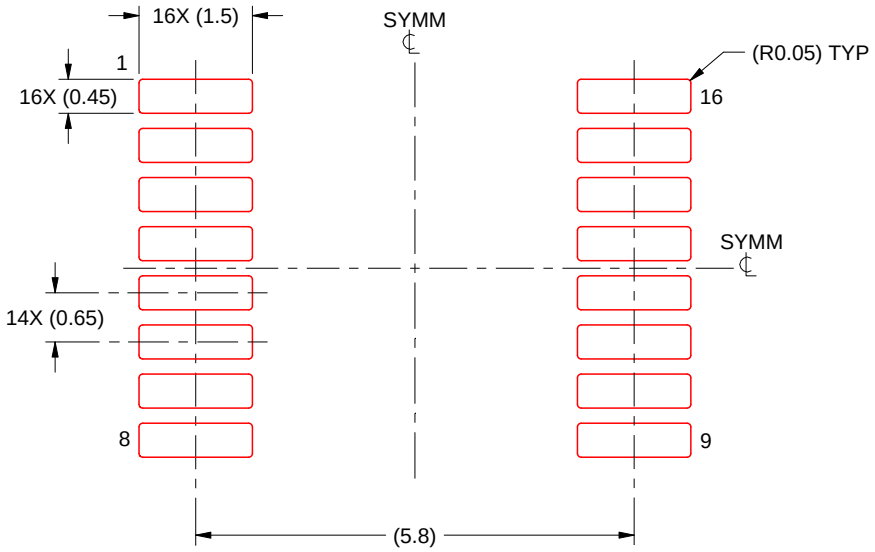


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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