David Basil Akang Analogue Coursework.pdf

by David Akang

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101CDE 2018/19 Academic Year, Semester 2 Coursework

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Section 1: PN Junction

Basic Semiconductor Concept:

1.1.1

P-type doping refers to the addition of P-type semiconductor materials to intrinsic semiconductors. The 'P' refers to positive; which arises from excess holes or electron vacancies. The charge carriers in p-type materials are Holes.

Two elements which can be used for P-type doping are:

- Boron (^{5}B)
  Electronic configuration: ($1s^2 2s^2 2p^1$)
- Aluminium (^{13}AL)
  Electronic configuration: ($1s^2 2s^2 2p^6 3s^2 3p^1$)

The common characteristic of both elements include:

The elements are trivalent in nature due to the fact that they have three electrons in its outmost shell as seen in its electronic configuration.

1.1.2

N-type doping refers to the addition of N-type semiconductor materials to intrinsic semiconductors. The 'N' refers to negative; which arises when N-type materials are bonded with silicon or germanium, an extra electron would remain free to roam. The charge carriers in N-type materials are 'electrons'.

Two elements which can be used are:

- Phosphorus **(^{15}P)**
  Electronic configuration: ($1s^2 2s^2 2p^6 3s^2 3p^3$)
- Arsenic **(^{33}As)**
  Electronic configuration: ($1s^2 2s^2 2p^6 3s^2 3p^6 4s^2 3d^{10} 4p^3$)

The common characteristics of both elements include:

1. The elements are pentavalent in nature due to the fact that they have five electrons in its outmost shell.

1.2 PN Junction (Diode) Basic:

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1.2.1

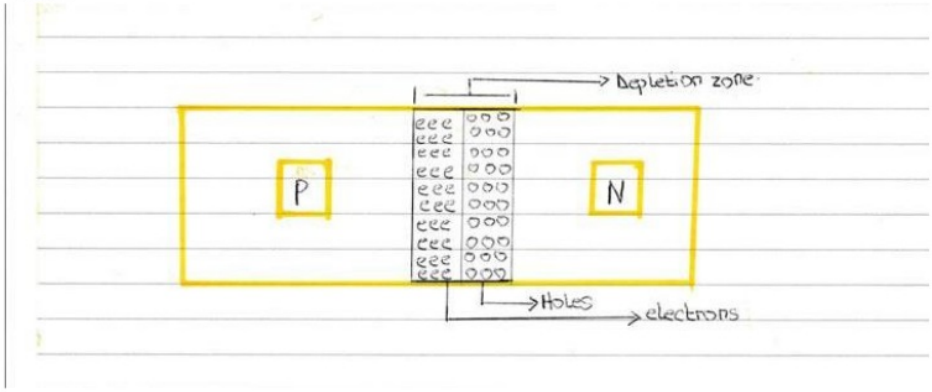

Figure 1: PN Junction

When a p-type semiconductor having excess holes is connected to an n-type semi-conductor having extra electrons, electrons from the n-side would diffuse to the p- side, and, holes from the p side would also move to the n side. The current that arises when holes and electrons transverse is referred to as *'Diffusion Current'*. The diffusion that occurs results in a space that is void of any charged particles, as seen in Figure 1. This leads to an electric field which arises from there; being a region of positively ionized impurities (0) and a region of negatively ionized impurities (e). Also, drift current is the current due to the flow of charge carriers resulting from the electric field. The potential difference across the field creates a barrier across the electrons and holes. This area is referred to as the **depletion zone**. This is expressed mathematically as shown in Equation 1

$I_{diffusion} = I_{drift}$ ……..Equation 2 (Where $I_{diffusion}$ = Diffusion Current and I_{drift} = Drift Current)

The potential difference across this zone for silicon is 0.7Volts and 0.3Volts for germanium.

1.2.2

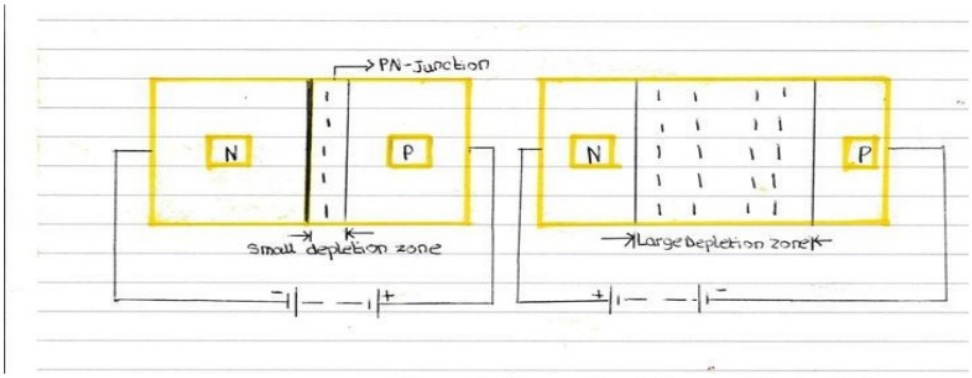

Figure 2: Forward and Reverse Biasing Voltage

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As depicted, in figure 2; when a positive voltage is applied to the P-region and a corresponding negative voltage is applied to the n-region. The positive voltage repels the holes and the negative voltage repels the electrons which leads to a reduction in the depletion zone.
On the other hand, when a positive voltage is applied to the N-region and a corresponding negative voltage is applied to the P-region. The positive voltage attracts electrons, while the holes which arise from electron vacancies are attracted to the negative terminal. This results in an enlarged depletion layer which prevents current from flowing through the material.

1.2.3

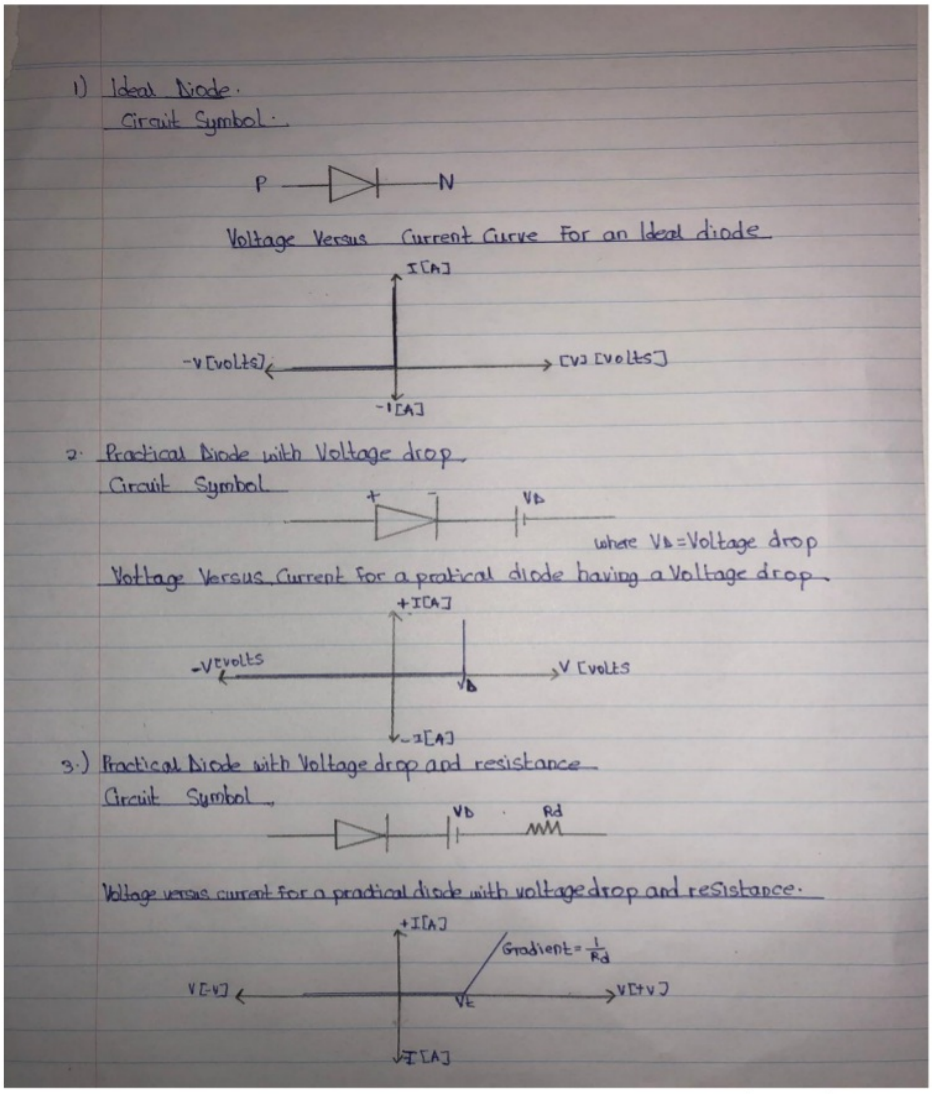

Figure 3: Diode Applications

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1.3 PN Junction (Diode) Applications

1.3.1

$$Is = \frac{Vs - Vd}{R + Rd}$$

$$Is = \frac{5 - 0.6}{100 + 10}$$

$$Is = 0.04A$$

1.3.2

The circuit is a Clipper.

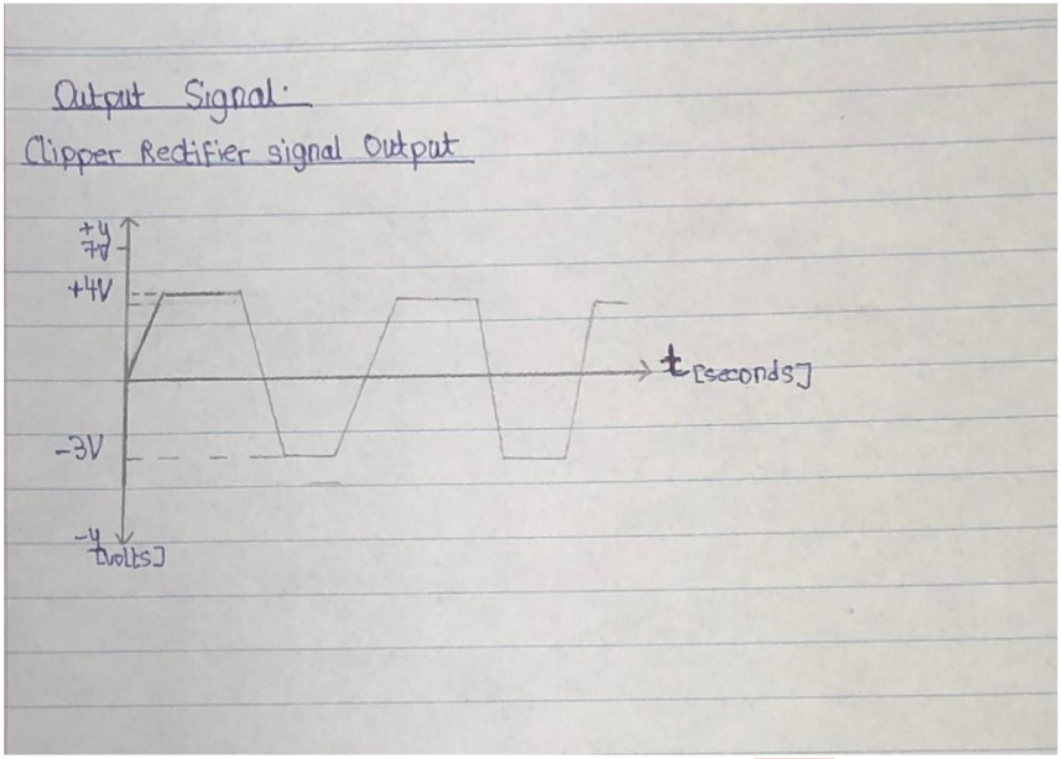

Figure 4: Rectifier Signal Output

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1.3.3

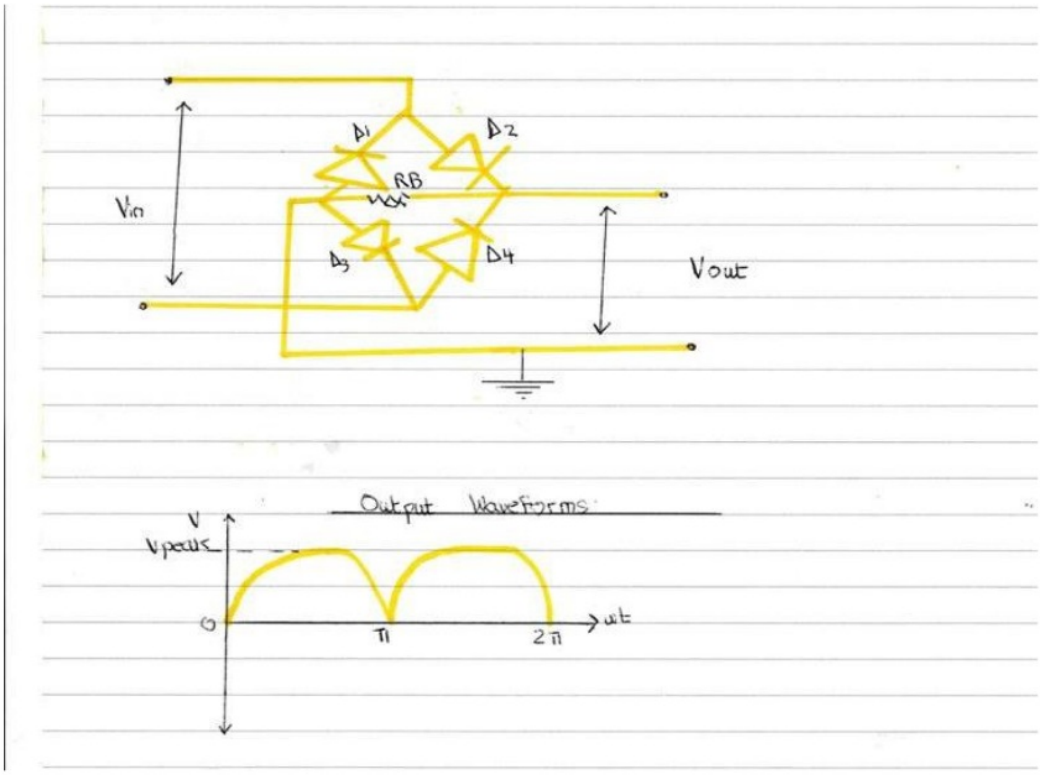

Figure 5: Full Wave Rectifier Output

As shown in the figure above, the type of rectifier shown is a full wave rectifier. During the positive half cycle, diode (D1) and (D3) will be conducted and forward biased. So the current will flow from (+Vin – D2 – RB- D3). On the other hand, during the negative half cycle and the polarities are reversed, current will flow through (-Vin – D4 – RB – D1). The output waveform for both the negative and positive half cycle is also shown in the figure above.

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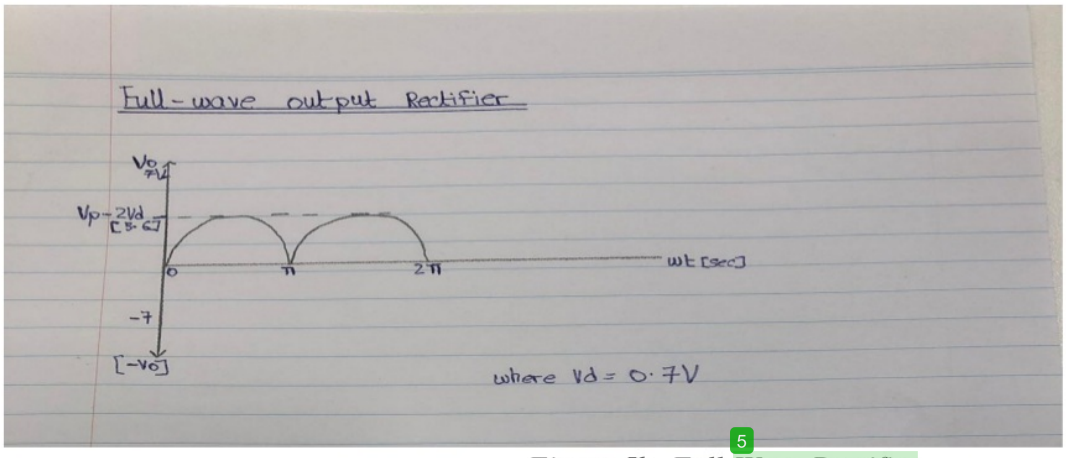

Figure 5b: Full-Wave Rectifier

During the positive half cycle, the diodes that are conducted are **D2** and **D3**, and also during the negative half cycle, the diodes that are conducted are **D1** and **D4**;

Two diode drops causes loss of 1.4V at the output. Peak voltage is $\sqrt{2} \times V$.

$Vp = \sqrt{2} * Vrms$;

$Vrms = \frac{Vp}{\sqrt{2}}$

$\frac{Vp}{\sqrt{2}} = \frac{7-2(0.7)}{\sqrt{2}}$

= 3.959V

1.4

AC/DC Converter

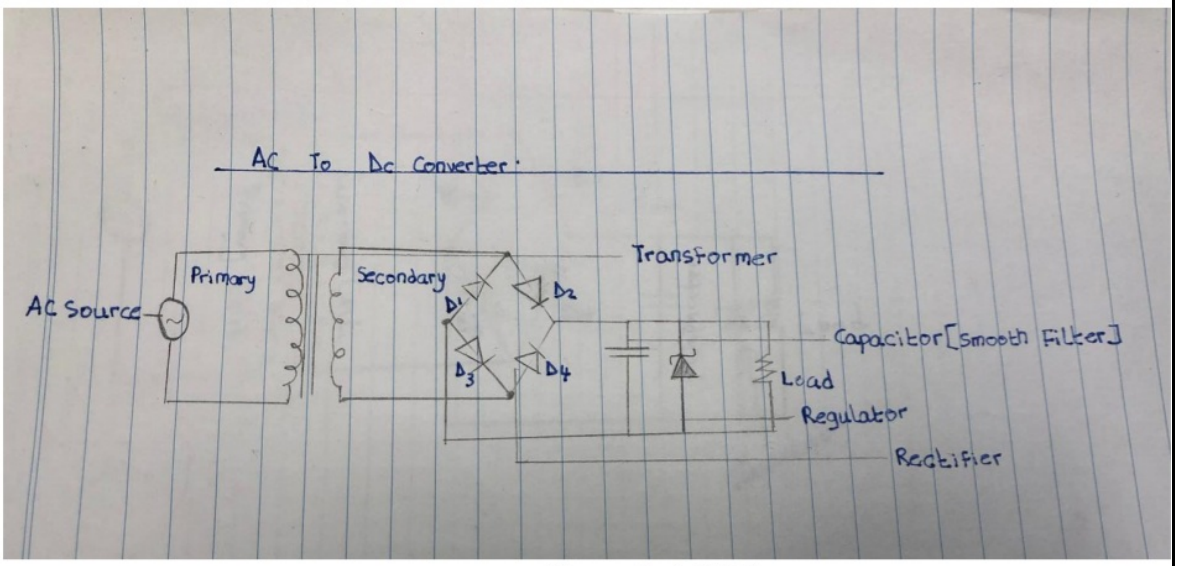

Figure 6: AC/DC converter

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The main parts of the AC to DC converter include:

- **Transformers**: they switch from a high potential difference (voltage) to a low potential difference (voltage); it can also convert a low voltage level to a high voltage level. In order, to step down voltage there will have to be more primary coils in relation to secondary coils.
- **Capacitor**: it helps to smoothen and even out fluctuations in the signal.
- **Regulator**: for regulation, a zenner diode is used; its main use is to protect the circuit by having a low and specified reverse breakdown voltage.
- **Full wave rectifier**: it helps convert alternative current to direct currents which flows in one direction. This part of the circuit also incorporates four diodes.

Section 2: Bipolar Junction Transistor

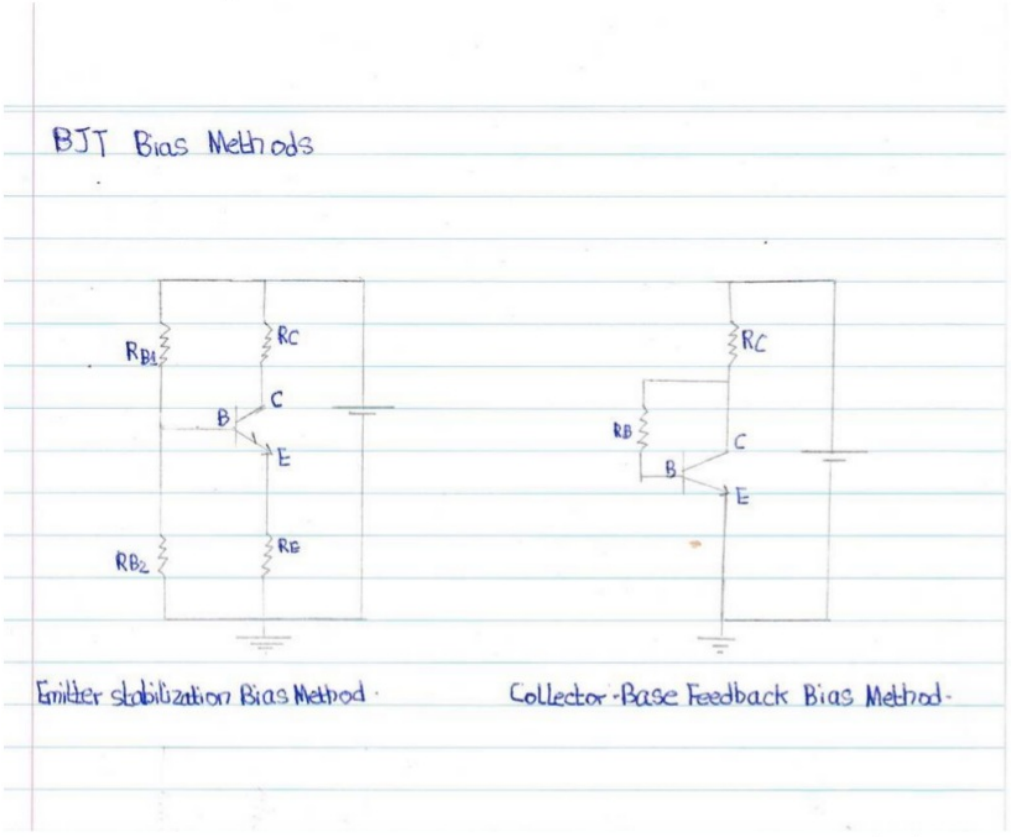

Figure 7: BJT Bias Methods

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The operating point of the transistor is referred to as the Q-point, the 'q' refers to 'quiescent'; while using devices the q point has to be stabilized correctly so its mode of operation would work well. The value (hfe/B), which is the AC current gain of a BJT varies with temperature; so an increase in temperature would lead to a corresponding increase in Ic. This is expressed mathematically as shown in equation 3:

Current Gain (B) = $\frac{Ic}{IB}$ ……..Equation 3

Where B = DC current gain of BJT, Ic = Collector Current and IB= Base Current.

This change in Ic, will shift the Q-point to shift to the saturation region which is not expected for the transistor, while it is in analogue mode and may also damage the transistor.

While stabilizing the Q point, the first circuit in Figure 7 shows an emitter stabilization bias method; for this arrangement, the emitter resistance (RE) causes a voltage drop in its direction which helps to reverse bias the emitter junction. Also, the total forward bias of Emitter – Base Junction is equated to the voltage drop across RE subtracted from the voltage across the base. The voltage across base is shown mathematically in equation 4

VB = $Vcc * \frac{RB2}{RB1+RB2}$ ……..*Equation 4*

(Where VB = Voltage across base, Vcc= source voltage and RB are resistors)

Therefore, the dc bias is not dependent on the current gain (Ic) as seen earlier.

The second circuit shown in figure 7 shows a Collector-Base Feedback Bias Method. This configuration uses negative feedback to stabilize the q point by preventing thermal energy loses. As shown in figure 7, an RB resistor is connected to the Collector and Base; this ensures that any thermal voltage drop would be dropped across RC resistor and not affect the transistor's base current.

2.2 BJT DC Mode

2.2.1 Cut-off Condition

$Ic = 0;$

$VCE = VCC$

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Saturation Condition

$VCE = 0$

$\text{Ic} = \frac{Vcc}{Rc+Re} = \frac{20}{5000+4000} = 2.222mA$

$\text{Vce} = \frac{1}{2}Vcc$

Q point = 10V

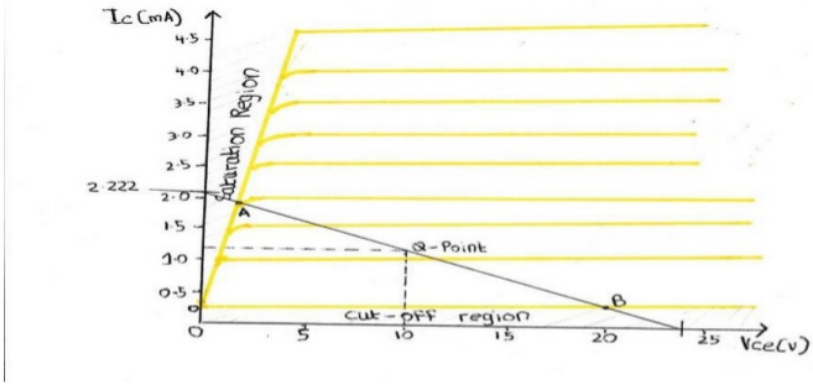

Figure 8: DC load line

2.2.2

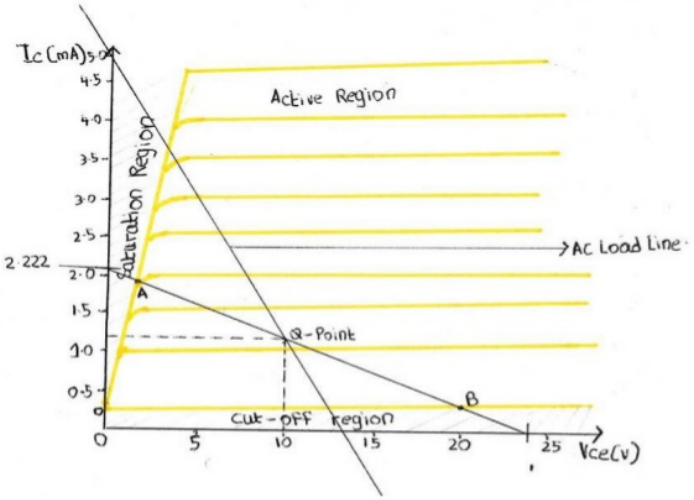

Figure 9: AC load line

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While calculating the DC load line as shown in figure 8, the emitter resistance is considered and the potential divider circuit is used to calculate the collector current (Ic); on the other hand while calculating the AC load line shown in figure 9, the emitter resistance is not considered due to the parallel connected capacitor so as current goes through the least resistive path, this would consequently short out the emitter resistance.

2.3 BJT AC Model/Hybrid-pi Model

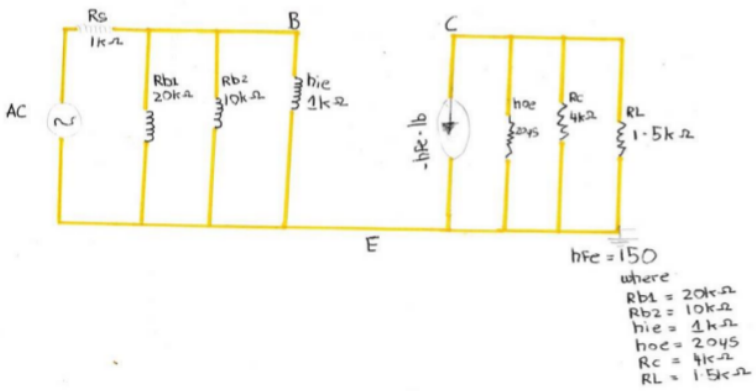

Figure 10: BJT AC Model/Hybrid-pi Model

The AC voltage gain (Gv) is given by

$$Gv = \frac{Vout}{Vs} = \frac{-hfe}{hie} \cdot \frac{(Rb1//Rb2//hie)}{Rs+(Rb1//Rb2//hie)} \cdot \left(\frac{1}{hoe} // R_c // R_l\right)$$

$$Gv = \frac{-150}{1K\Omega} \cdot \frac{(20K\Omega//10K\Omega//1K\Omega)}{1K\Omega+(20K\Omega//10K\Omega//1K\Omega)} \cdot \left(\frac{1}{20\mu s} // 4k\Omega // 1.5K\Omega\right)$$

$$Gv = -0.15 \cdot \frac{869.565}{1869.565)} \cdot (1067.615)$$

$$= \mathbf{-74.484V}$$

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Section 3: Field Effect Transistor

3.1 Semiconductor basic of FET

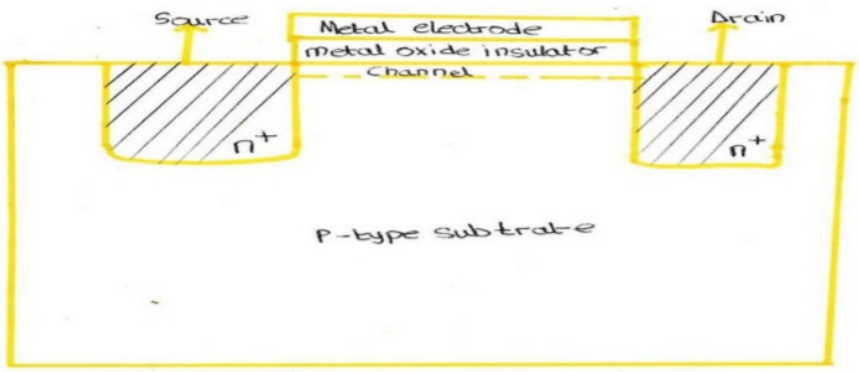

Figure 11: N-type Channel enhancement mosfet

N-type channel enhancement MOSFET has 3 terminals as depicted in figure 11, they are 'source', 'gate' and 'drain'. When a positive voltage is applied to the gate, it repels the positive holes (electron vacancy) in the substrate, by this action, electrons would be formed directly beneath the gate and thus would create a path for the movement of electrons in the n+ region to flow from the source to drain. Therefore, as the gate voltage increases, the drain current increases. This is why n channel enhancement MOSFET are referred to as voltage control current components.

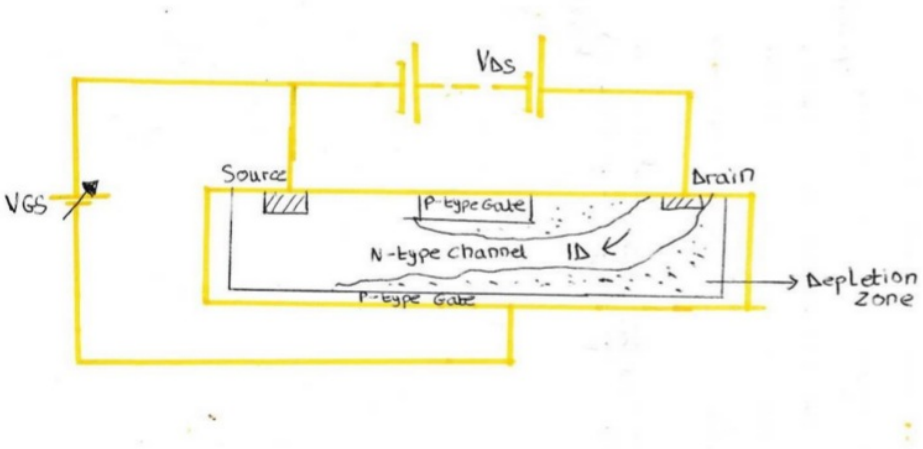

Figure 12: N-channel JFET

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Also, figure 12 shows an n-channel JFET, it shows the combination of two PN junctions, a voltage is applied between the drain and source (V_{DS}) which makes a current (Id) to flow as shown. The n-type channel shown,varies in voltage as the channel goes from source to drain. This creates a depletion layer, due to the reverse biasing of the PN junction. The current flowing through the channel (Id) is controlled by the voltage applied to the gate terminal.

Field Effect transistors are often used in measuring devices because of its high input impedance; this arises from the reverse biased PN junction. This impedance lessens interference with signals when measurements like voltage are being taken.

3.2 FET DC Model

3.2.1

Given I_d = 5mA; V_{DS}=5V; V_T= -3.5V; R1+R2=100K; I_{DSS} = 12 mA; Rs = 500ohms; V_{DD}= 10V

$$I_d = I_{DSS}\left(1 - \frac{VGS}{VT}\right)^2$$

Making V_{GS} the subject;

$$V_{GS} = -V_T\left(\sqrt{\frac{Id}{IDSS}} - 1\right)$$

$$= -3.5\left(\sqrt{\frac{5*(10^{-3})}{12*(10^{-3})}} - 1\right)$$

$$= \mathbf{-1.240V}$$

$$V_S = Id*Rs$$

$$= \mathbf{2.5V}$$

$$V_{GS} = V_G - V_S$$

$$V_G = V_{GS} + V_S$$

$$= -1.240 + 2.5$$

$$= \mathbf{1.26V}$$

$$V_G = \left(\frac{R2}{R1+R2}\right) * VDD$$

$$1.26 = \left(\frac{R2}{100000}\right) * 10$$

R2 = **12,600ohms**

R1 = 100,000-12,600 = **87,400ohms**
Using Kirchhoff's voltage law for the loop:
$V_{DD} = V_s + V_{DS} + I_D R_D$, making Rd subject
$R_D = \frac{VDD - Vs - Vds}{ID}$
$= \frac{10V - 2.5V - 5V}{5mA}$
$= \mathbf{500\Omega}$

3.2.2
To make the JFET, work in linear mode and not saturation mode, the V_{GS} is reverse biased. The V_{GS} must be greater than the threshold voltage (Vt)

VGS ≥ VT…….. Condition 1

So when the V_{DS}, is less than the V_{DSSAT}, the JFET would work in the linear region. V_{DSSAT} got by V_{GS} - V_T. The Also increasing the Rd value ensures the JFET stays in the linear region.

0 ≤ VDS ≤ VGS-VT…….Condition 2

3.3 FET AC Model/Hybrid-pi Model

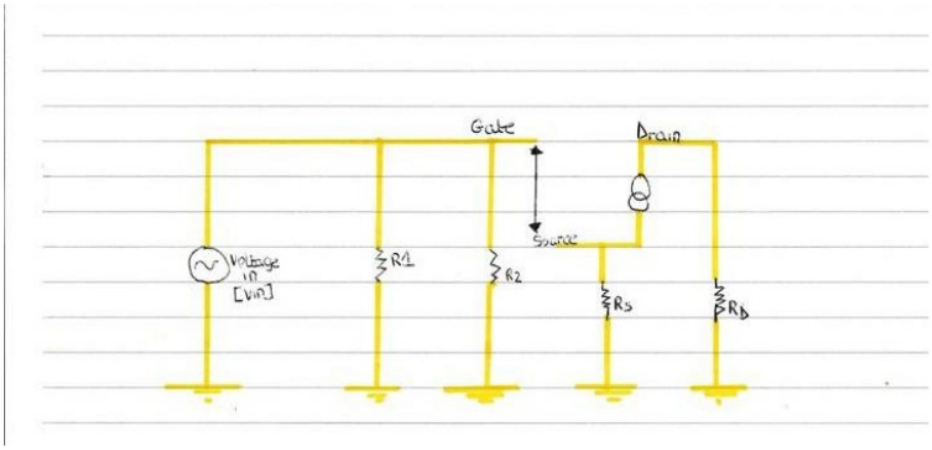

Figure 13: FET AC Mode/Hybrid Pi Model

$gm = \frac{-2}{Vt} . \sqrt{Idss} . Id$
$= \frac{-2}{-3.5} . \sqrt{(12 * 10^{-3})} . \sqrt{(5 * 10^{-3})}$
$= 4.426mA$
Also,

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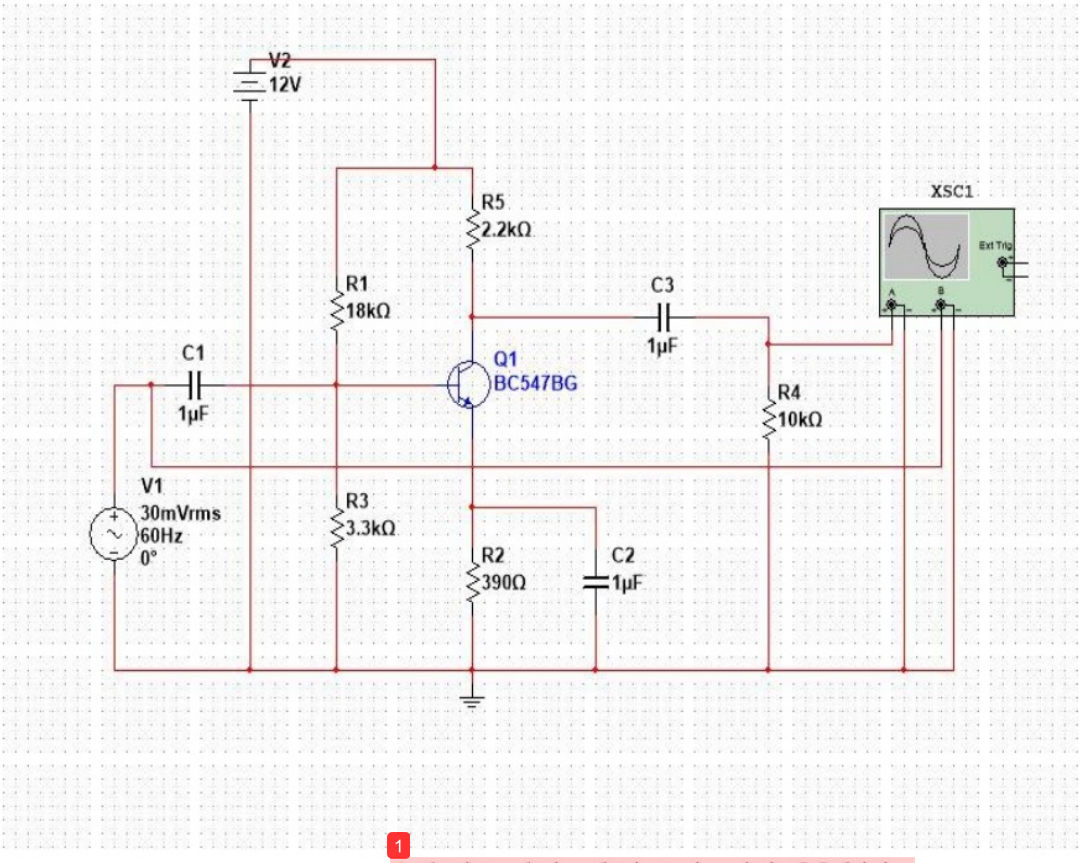
$$Gv = gm \cdot \frac{(R1//R2)}{(Rs//R1//R2)} \cdot (R_d // R_l)$$

$$= (4.426*10^{-3}) \cdot \frac{(11012.4)}{(11512.4)} \cdot (500)$$

$$= \mathbf{2.116volts}$$

Boost Section:

1. **A designed simulation circuit in Multisim**



A designed simulation circuit in Multisim

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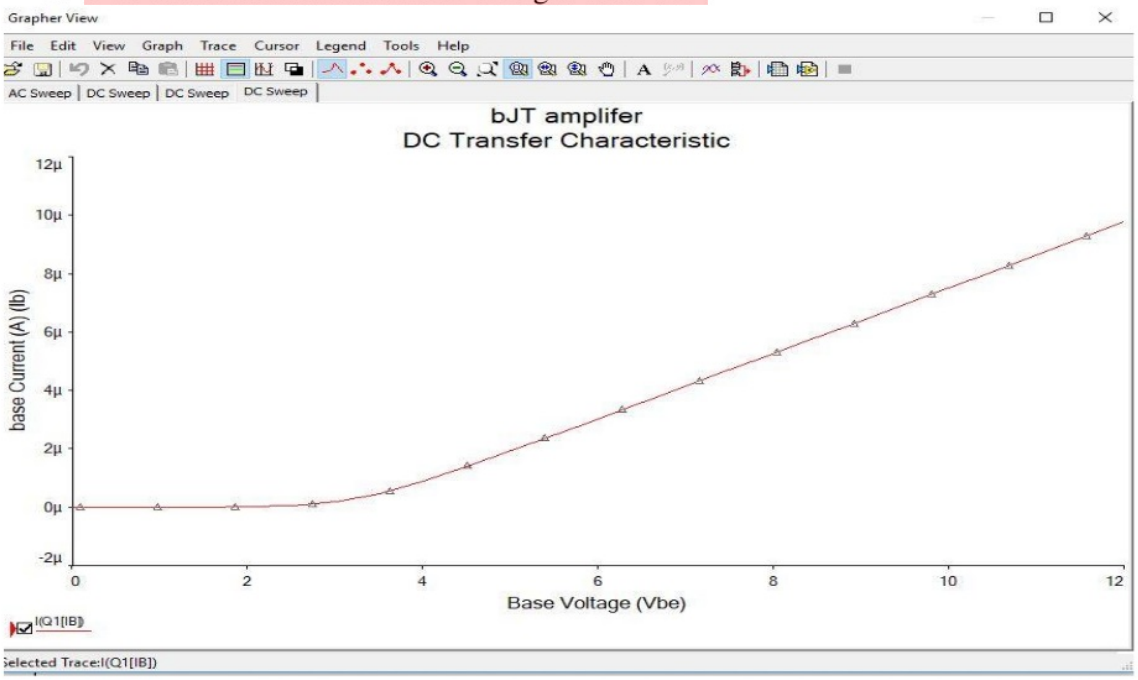
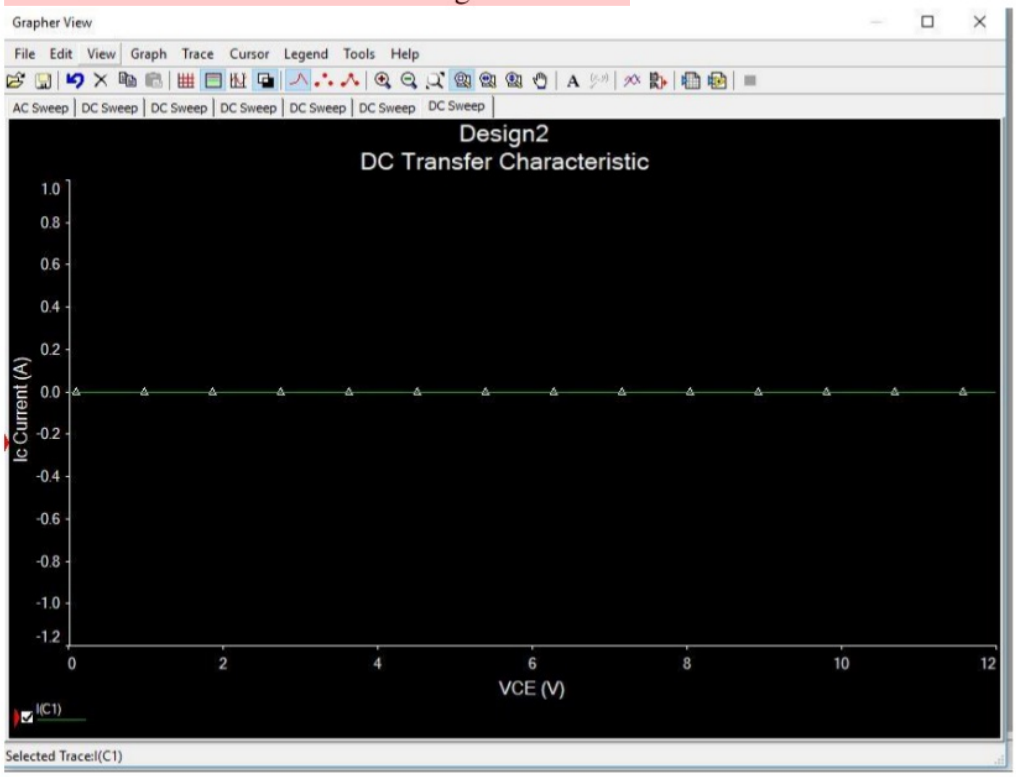
2. **B-E Characteristics:** How IB changes with VBE



3. **C-E Characteristics:** How IC changes with VCE



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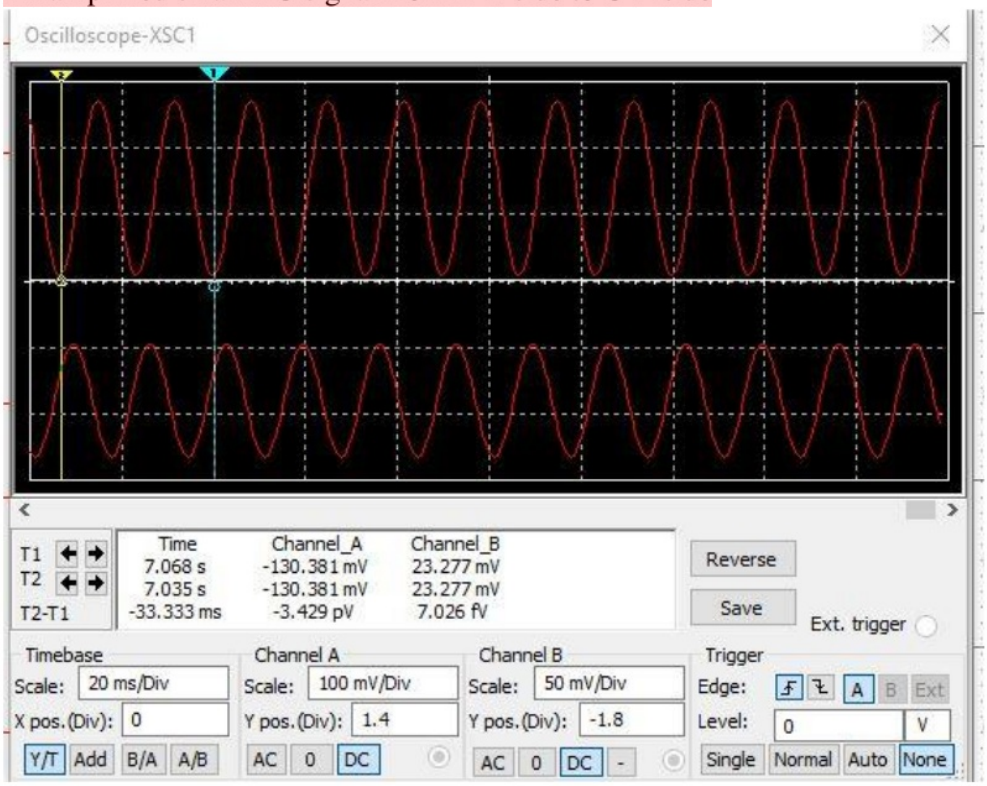
4. An amplified small AC signal from B-E side to C-E side



In order to calculate the voltage gain of the amplified AC signal:

Gv = $\frac{Channel\ A}{Channel\ B}$ = $\frac{-130.381}{23.277}$ = **-5.601V**

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