DIGITAL LOGIC SYSTEMS - SPRING 2019
PROJECT 3: VARIABLE LENGTH ADDER

Deadline: Thursday 23rd May, 2019

A variable length adder is an adder which splits the addend strings into two parts — prefix and postfix — and performs two separate additions on the prefixes and postfixes. In this project you must design a variable length adder and implement it in Logisim.

Specifications

The general specification of this adder, hereinafter denoted as $VLA(n)$ is

Input: $A[n-1:0], B[n-1:0] \in \{0,1\}^n$, and $P[k-1:0] \in \{0,1\}^k$, where $n = 2^k$

Output: $S[n-1:0] \in \{0,1\}^n$ and $D, E \in \{0,1\}$

Functionality: Let $p \triangleq \langle P[k-1:0] \rangle$. Then, the outputs D, E, and S must satisfy

$$\langle A[p-1:0] \rangle + \langle B[p-1:0] \rangle = \langle S[p-1:0] \rangle + 2^p \cdot D$$
$$\langle A[n-1:p] \rangle + \langle B[n-1:p] \rangle = \langle S[n-1:p] \rangle + 2^n \cdot E$$

Your Assignment

Design and implement a variable length adder for 4 bits, i.e. $VLA(4)$. *Hint: Think what information flows from right part to the left part of the addition. In order to decouple between the left and the right additions, how can you "cut" this flow of information?*

Submission Instructions

(1) Submit a single Logisim (".circ") file. No prints/screenshots. This file must be named `ID1_ID2_varlenadder.circ` with `ID1` and `ID2` replaced by each partner's 9 digit ID number.
(2) Use the provided `template_varlenadder.circ` file as a template, and implement your designs in the circuit named `VarLenAdder`. Do not move or modify the input/output ports, the "blackbox" layout, and the names of the circuits!
(3) Only one of the students in a pair needs to upload the submission. Do not upload the same work twice!
(4) You may not use gates with *fan-in* larger than 2. Exception is for Logisim's MUX2:1, which has fan-in of 3, however is allowed to be used.
(5) You are allowed to use the *data-bits* attribute of the gates to perform bitwise operations.