**Computer Science 605.611**

Problem Set 3

Module 3 defines and describes basic logic gates such as AND, OR, XOR, NOT, etc.

1. The following truth table defines the output C as a function of the two inputs A and B:

Table

Description automatically generated

a) (5) Write down the expression for the logical product of the zero maxterms.

Maxterms were defined in module 3.

**(A + B) (A’ + B’)**

b) (5) Use only Boolean identities (not truth tables) to show that the logical sum of the non-zero minterms for this function is equivalent to the logical product of the zero maxterms. Minterms and maxterms were defined in module 3.

Minterms = (AB’) + (A’B)

First Not the Equation = (AB’ + A’B)’

Demorgans Law = (A’ + B’’) (A’’+B’) = (A’+B)(A+B’)

Distribution = (A’A + A’B’ + (A+B’)B = (A’B’ + (A+B’)B)

Distribution = (A’B’ + BA + BB’) = A’B’ + BA

Not the equation again = (A’B’ + BA)’

Demorgans Law = (A’’ + B’’) (B’ + A’) = (A+B)(B’+A’) = maxterms

2. (5) Which one of the following individual logic gates is equivalent to the circuit shown below?

That is, given the same two single-bit data inputs A and B, which one of the 6 logic gates listed below generates the same output as the circuit? (The answer is F, I bolded it)

a) AND d) NAND

b) OR e) XNOR

c) NOR f) **XOR**

A blue line drawing of a diagram

Description automatically generated

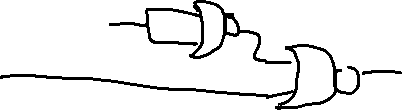
3 a) (5) Show how the following 3-input NOR gate can be implemented using a minimum number of 2-input NOR gates. Only NOR gates should be included in your solution.

**(those are all meant to be NOR gates, I am not good at drawing in word)**

Output

A blue line drawing of a half moon

Description automatically generated



A

B

C

b) (5) Show how the following 3-input AND gate can be implemented using a minimum number of 2-input AND gates. Only AND gates should be included in your solution.

**(Also these are meant to be AND gates, still cant draw)**

Output

1A blue line drawing of a bulb

Description automatically generated



A

B

C



4. (5) The output generated by the logic circuit shown below corresponds to logic expression containing a single term. Write down that simplified logic expression. Output = \_\_\_\_(X+Y)Y\_\_\_\_

Chart

Description automatically generated with medium confidence

5. (5) What signal is used by the control system to determine when the ALU has produced the sum of two CPU registers?

The Zero Signal

6. a) (5) Multiplication and division can be implemented using three simpler ALU operations. What are those three operations?

**Adding, Subtracting, and Shifting**

b) (5) Write down one or more MIPS true-op instructions (excluding any subtraction instruction) to place the arithmetic difference $4 - $5 into register $6. No register other than $6 should be modified by your solution.

(step one, change $5 into its negative value, then add it to $4)

**mult $5 -1**

**add $6 $4 $5**

7. (5) Is the circuit shown below a combinational circuit or is it a sequential circuit? Explain your answer.

A picture containing antenna

Description automatically generated

I believe this circuit is a sequential circuit. This is because the circuit relies on the output of the last logic. This means it has a “memory” of the last run.

8. (5) The truth table on the left below corresponds to a half adder where A and B are the two input data bits, X is the sum and Y is the carry. Complete the truth table on the right by filling in the entries to make the table correspond instead to a half subtractor. For the half subtractor, X is the difference (A - B) and Y is the borrow.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | X | Y |  | A | B | X | Y |
| 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |  | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |  | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |  | 1 | 1 | 0 | 0 |

9. (5) Is the circuit shown below an example of a decoder, an encoder or a multiplexer? Explain how the outputs are related to the inputs.

Diagram

Description automatically generated

The Circuit shown above is an example of a multiplexer. The outputs are related to the input by this, n inputs and log­2(n) control lines gives us one output.

10. Consider the following circuit:

Diagram

Description automatically generated

a) (5) Is this a combinational circuit or is it a sequential circuit? Explain your answer.

This is a sequential circuit. This is because if one wanted to shift a number multiple times they would have to send the output back through, thus it could only be run once the last run is done.

b) (5) If S=0, show the value for each of the 4 outputs if initially

I3, I2 , I1  I0 = 1111.

O3 = \_\_1\_\_\_

O2 = \_\_1\_\_\_\_

O1 = \_1\_\_\_\_

O0 = \_\_0\_\_\_\_

c) (5) If S=1, show the value for each of the 4 outputs if initially

I3, I2 , I1  I0 = 1011.

O3 = \_\_\_0\_\_\_

O2 = \_\_\_1\_\_\_\_

O1 = \_\_\_0\_\_\_\_

O0 = \_\_\_\_1\_\_\_

11. (5) Is the circuit shown below an example of a decoder, an encoder or a multiplexer? Explain how the outputs are related to the inputs.

Diagram

Description automatically generated

This circuit is a decoder. The outputs are related to the inputs with a formula of n inputs (2) to 2^n outputs (4).

12. (5) Is the circuit shown below an example of a decoder, an encoder or a multiplexer? Explain how the outputs are related to the inputs.

Diagram

Description automatically generated

This circuit is an encoder. The input and outputs are related by 2^n inputs to n outputs, or the opposite of a decoders relation. In this case we have 8 or 2^3 inputs and 3 outputs.

13. (5) Consider the logic circuit shown below:

Icon

Description automatically generated

Which one of the following individual logic gates is equivalent to this circuit? That is, which one of the 6 logic gates listed below generates the same output as the circuit above with A and B as its two inputs? **It would be the same as an AND gate**

**a) AND** d) NAND

b) OR e) XNOR

c) NOR f) XOR

14. (5) Write down a single MIPS instruction to place into register $7, the quotient of the signed integer in register $4 divided by the constant 256. Your solution should not use any of the MIPS division instructions.

**Srl $7 $4 8**

15. (5) Let b31, b30, b29, . . . b1, b0 correspond to the 32 bits within a CPU register. The unsigned integer represented by this 32-bit pattern corresponds to the following polynomial in powers of two:

P\_unsigned = b31\*(2^31) + b30\*(2^30) + b29\*(2^29) + . . . + b1\*(2^1) + b0\*(2^0)

where, of course, each bn is either 0 or 1

The two’s complement signed integer represented by the 32-bit pattern corresponds to the following polynomial in powers of two where the leftmost bit (b31) is multiplied by –(2^31):

P\_signed = b31\*[-(2^31)] + b30\*(2^30) + b29\*(2^29) + . . . + b1\*(2^1) + b0\*(2^0)

Evaluate P\_unsigned and P\_signed for the 32-bit pattern: 11000000000000110100001000111010

and express your answer in decimal.

P\_unsigned = \_\_3221225473\_\_\_\_

P\_signed = \_\_-1073741823\_\_\_\_\_