

Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.21 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.21 secs

--> Reading design: mux_proper.prj

TABLE OF CONTENTS

- 1) Synthesis Options Summary
- 2) HDL Parsing
- 3) HDL Elaboration
- 4) HDL Synthesis
 - 4.1) HDL Synthesis Report
- 5) Advanced HDL Synthesis
 - 5.1) Advanced HDL Synthesis Report
- 6) Low Level Synthesis
- 7) Partition Report
- 8) Design Summary
 - 8.1) Primitive and Black Box Usage
 - 8.2) Device utilization summary
 - 8.3) Partition Resource Summary
 - 8.4) Timing Report
 - 8.4.1) Clock Information
 - 8.4.2) Asynchronous Control Signals Information
 - 8.4.3) Timing Summary
 - 8.4.4) Timing Details
 - 8.4.5) Cross Clock Domains Report

```
=====
*           Synthesis Options Summary           *
=====

---- Source Parameters
Input File Name      : "mux_proper.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters
Output File Name       : "mux_proper"
Output Format          : NGC
Target Device          : xc7a100t-3-csg324

---- Source Options
Top Module Name        : mux_proper
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation    : No
FSM Style              : LUT
RAM Extraction         : Yes
RAM Style              : Auto
ROM Extraction          : Yes
Shift Register Extraction : YES
ROM Style              : Auto
```

```
Resource Sharing           : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block             : Auto
Automatic Register Balancing : No
```

---- Target Options

```
LUT Combining            : Auto
Reduce Control Sets       : Auto
Add IO Buffers            : YES
Global Maximum Fanout     : 100000
Add Generic Clock Buffer(BUFG) : 32
Register Duplication      : YES
Optimize Instantiated Primitives : NO
Use Clock Enable          : Auto
Use Synchronous Set        : Auto
Use Synchronous Reset       : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES
```

---- General Options

```
Optimization Goal          : Speed
Optimization Effort         : 1
Power Reduction              : NO
Keep Hierarchy                : No
Netlist Hierarchy             : As_Optimized
RTL Output                   : Yes
Global Optimization           : AllClockNets
Read Cores                     : YES
Write Timing Constraints      : NO
Cross Clock Analysis          : NO
Hierarchy Separator            : /
Bus Delimiter                  : <>
Case Specifier                  : Maintain
Slice Utilization Ratio        : 100
BRAM Utilization Ratio         : 100
DSP48 Utilization Ratio        : 100
Auto BRAM Packing               : NO
Slice Utilization Ratio Delta   : 5
```

```
=====
```

```
=====
```

* HDL Parsing *

```
=====
```

Analyzing Verilog file "D:\BRB\dds-mini\W4_1.v" into library work
Parsing module <mux_proper>.

```
=====
```

* HDL Elaboration *

```
=====
```

Elaborating module <mux_proper>.

WARNING:HDLCompiler:413 - "D:\BRB\dds-mini\W4_1.v" Line 10: Result of 2-bit expression is truncated to fit in 1-bit target.

WARNING:HDLCompiler:413 - "D:\BRB\dds-mini\W4_1.v" Line 12: Result of 32-bit expression is truncated to fit in 1-bit target.

WARNING:HDLCompiler:413 - "D:\BRB\dds-mini\W4_1.v" Line 13: Result of 32-bit expression is truncated to fit in 1-bit target.

```
=====
*                      HDL Synthesis                      *
=====
```

```
Synthesizing Unit <mux_proper>.
Related source file is "D:\BRB\dds-mini\W4_1.v".
Summary:
    no macro.
Unit <mux_proper> synthesized.
```

```
=====
HDL Synthesis Report
```

```
Found no macro
```

```
=====
*                      Advanced HDL Synthesis                     *
=====
```

```
=====
Advanced HDL Synthesis Report
```

```
Found no macro
```

```
=====
*                      Low Level Synthesis                     *
=====
```

```
Optimizing unit <mux_proper> ...
```

```
Mapping all equations...
```

```
Building and optimizing final netlist ...
```

```
Found area constraint ratio of 100 (+ 5) on block mux_proper, actual ratio is 0.
```

```
Final Macro Processing ...
```

```
=====
Final Register Report
```

```
Found no macro
```

```
=====
*                      Partition Report                     *
=====
```

```
Partition Implementation Status
```

```
-----
No Partitions were found in this design.
```

```
=====
*                      Design Summary                     *
=====
```

```
Top Level Output File Name      : mux_proper.ngc
```

Primitive and Black Box Usage:

```
-----  
# BELS : 3  
# GND : 1  
# LUT2 : 1  
# VCC : 1  
# IO Buffers : 12  
# IBUF : 3  
# OBUF : 9
```

Device utilization summary:

```
-----  
Selected Device : 7a100tcsg324-3
```

Slice Logic Utilization:

Number of Slice LUTs:	1	out of	63400	0%
Number used as Logic:	1	out of	63400	0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used:	1			
Number with an unused Flip Flop:	1	out of	1	100%
Number with an unused LUT:	0	out of	1	0%
Number of fully used LUT-FF pairs:	0	out of	1	0%
Number of unique control sets:	0			

IO Utilization:

Number of IOs:	12			
Number of bonded IOBs:	12	out of	210	5%

Specific Feature Utilization:

```
-----  
Partition Resource Summary:  
-----
```

No Partitions were found in this design.

```
-----  
=====  
Timing Report
```

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-----  
No clock signals found in this design
```

Asynchronous Control Signals Information:

```
-----  
No asynchronous control signals found in this design
```

Timing Summary:

```
-----  
Speed Grade: -3
```

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 0.765ns

Timing Details:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis
Total number of paths / destination ports: 8 / 6

Delay: 0.765ns (Levels of Logic = 3)
Source: I1 (PAD)
Destination: out<8> (PAD)

Data Path: I1 to out<8>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	2	0.001	0.383	I1_IBUF (out_1_OBUF)
LUT2:I0->O	2	0.097	0.283	_n00231 (out_6_OBUF)
OBUF:I->O		0.000		out_8_OBUF (out<8>)
Total		0.765ns (0.098ns logic, 0.667ns route) (12.8% logic, 87.2% route)		

=====

Cross Clock Domains Report:

=====

Total REAL time to Xst completion: 14.00 secs
Total CPU time to Xst completion: 14.81 secs

-->

Total memory usage is 4616540 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 3 (0 filtered)
Number of infos : 0 (0 filtered)