```
Release 14.7 - xst P.20131013 (lin64)
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-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Reading design: mux_proper.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "mux_proper.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "mux_proper"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324

---- Source Options
Top Module Name                    : mux_proper
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
```

```
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "/home/ishaan/dds/DDS_MINI_FINAL/DDS_MINI_FINAL/MUX_PROPER.v" into
library work
Parsing module <mux_proper>.

=========================================================================
*                           HDL Elaboration                             *
=========================================================================

Elaborating module <mux_proper>.

=========================================================================
*                          HDL Synthesis                                *
=========================================================================

Synthesizing Unit <mux_proper>.
    Related source file is "/home/ishaan/dds/DDS_MINI_FINAL/DDS_MINI_FINAL/MUX_PROPER.v".
    Summary:
        no macro.
Unit <mux_proper> synthesized.
```

```
=========================================================================
HDL Synthesis Report

Found no macro
=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Found no macro
=========================================================================

=========================================================================
*                       Low Level Synthesis                             *
=========================================================================

Optimizing unit <mux_proper> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block mux_proper, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
=========================================================================

=========================================================================
*                          Partition Report                             *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

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=========================================================================
*                           Design Summary                              *
=========================================================================

Top Level Output File Name         : mux_proper.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 4
#      INV                         : 1
#      LUT2                        : 2
#      LUT3                        : 1
# IO Buffers                       : 12
#      IBUF                        : 3
#      OBUF                        : 9

Device utilization summary:
---------------------------
```

```
Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice LUTs:                    4  out of  63400     0%
    Number used as Logic:                 4  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:      4
   Number with an unused Flip Flop:       4  out of      4   100%
   Number with an unused LUT:             0  out of      4     0%
   Number of fully used LUT-FF pairs:     0  out of      4     0%
   Number of unique control sets:         0

IO Utilization:
 Number of IOs:                          12
 Number of bonded IOBs:                  12  out of    210     5%

Specific Feature Utilization:

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

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================================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 0.917ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

================================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 13 / 9
--------------------------------------------------------------------------------
Delay:               0.917ns (Levels of Logic = 3)
  Source:            S (PAD)
  Destination:       out<8> (PAD)
```

```
  Data Path: S to out<8>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             7   0.001   0.539  S_IBUF (out_2_OBUF)
     LUT3:I0->O            1   0.097   0.279  out<8>1 (out_8_OBUF)
     OBUF:I->O                 0.000          out_8_OBUF (out<8>)
    ----------------------------------------
    Total                      0.917ns (0.098ns logic, 0.819ns route)
                                       (10.7% logic, 89.3% route)

=========================================================================

Cross Clock Domains Report:
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=========================================================================


Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 6.88 secs

-->


Total memory usage is 482728 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```