Final Project Report

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Abstract

The project goal is aimed towards developing a reliable high-speed signaling system that can work at the highest possible bit rate before failure. This system must have at least 70 channels with a signaling rate of at least 1 Gb/s, and the voltage swing may have a maximum voltage swing of 800 mV. The signal must travel a trace with a minimum of 40 cm in length which could spa across multiple PCBs.

Overall Design Approach

Description:

Using Intel's Cyclone FPGA chips, the Cyclone X GX FPGA will be used for this project due to its high-speed capability and ability to route at least 70 LVDS I/O pins.

For this project, the transmitter will emit a differential bipolar signal of +/- 400mV, through a 40cm PCB trace, and then to the receiver. The receiver will simply be a comparator by using a high-speed diff amp. Ideally, that resulting value would be capable of going to a microcontroller, or another FPGA. It will be controlled by a pipeline of two d flip flops to control the bit rate more consistently. The design will include capacitance and inductance sourced from vias/pads and connectors to help gain a more accurate design.

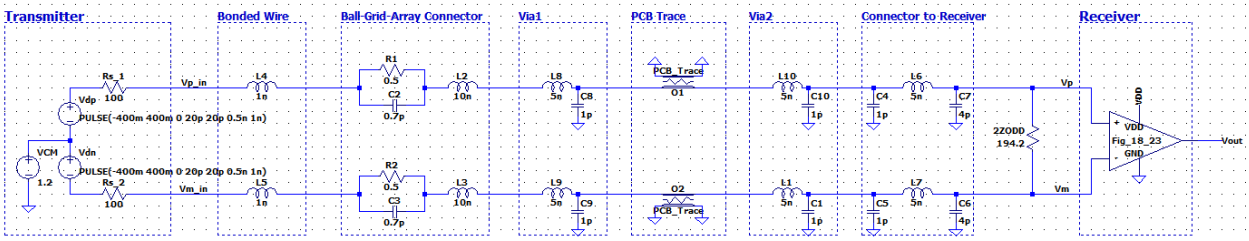

Fig. 1: Schematic of Design

Signaling (including equalization and crosstalk control):

Signaling Parameters		
Parameters	**Values/Comments**	**Units**
Unidirectional vs Bidirectional	This project design uses Bidirectional Signaling	--
Single-ended vs Differential	This project design uses Differential Signaling	--
Number of Signal Levels	There are only two signal levels. It will either be a bit '1' or a bit '0'.	--
Signals	'1' = 400	mV
	'0' = -400	mV
Signaling Rate	1	Gbps

Voltage/Current Mode	Current Mode	--
Voltage Swing	800	mV
Equalization	Not included in this project design	--
Crosstalk Control	Not included in this project design	--
C(parallel)	9.68	pF/m
C(fringing)	23.7	pF/m
C(total)	33.4	pF/m
L	333	nH/m
Z0	100	Ω
Velocity	3.0	m/ns
Time Delay	133	Ps
Cd	0.92	pF/m
M	9.17	nH/m
Cc	32.48	pF/m
Zeven	102.6	Ω
Zodd	97.1	Ω
Serial Resistance	100	Ω
Terminal Resistance	100	Ω
R1	102.6	Ω
R2	3622.7	Ω

Table 1: Signaling parameters summary

The goal when creating these signals were to create as much of a homogenous system as possible to avoid crosstalk and reflections. This would allow the design to transfer the signals through the 40cm line evenly with minimal distortion or disturbances.

Timing:

The timing concept will be clock forwarding mainly due to it being mesochronous. The receiver will receive the two voltage signals from the two differential lines and proceed to output either a bit '1' or '0' based on the comparison, and then go through a couple of d flip flops that's synchronous to the Cyclone X's clock.

Timing Parameters		
Parameters	**Values/Comments**	**Units**
Rise Time	196	ps
Fall Time	144	ps
Minimum Aperture Time	177	ps
Clock Period Jitter	-40 (min), 40 (max) (refer to Table 7, Appendix A)	ps
Transmitter Jitter	200 (max) (refer to Table 6, Appendix A)	ps
Cycle-to-Cycle Jitter	-40 (min), 40 (max) (refer to Table 7, Appendix A)	ps
Duty Cycle Jitter	-40 (min), 40 (max) (refer to Table 7, Appendix A)	ps

Table 2: Timing parameters summary

Performance and Noise Summary:

Noise Parameters		
Parameters	**Values/Comments**	**Units**
Transmitter Offset	+/-5%	--
Receiver Offset	+/-5%	--
Receiver Sensitivity	10	mV
Voltage Swing Noise	31.84	mV
Total Noise (Bounded)	121.84	mV
Gross Margin	400.0	mV
Net Margin	278.16	mV
BER	9.15*10^-33	bits/error
VSNR	12.15	--
MTBF	3.456*10^15	years/error

Table 3: Performance and noise parameters summary

Intersymbol Interference:

Bandlimited Channels are channels where the frequency response is zero above the cutoff frequency. When out of range, removed frequency components are considered an incomplete signal. As a result, the channel is unable to use the attenuated frequency. Since this type of interference is not limited to wireless devices, the design must take it under consideration. Some sources of this interference could be truncated signals sent through the channel or the physical properties of the medium.

Through plugging in approximate values of the design to find KnVs, intersymbol interference comes out to be 31.84 mV.

Gaussian Noise:

Using the equation, V = (4kTBR)^0.5 (to find thermal noise where T is temperature, B is bandwidth, and R is resistance, the measured thermal noise comes out to be 40 uV which is negligible in comparison to other sources of noise.

For unrelated backplane noise and added Gaussian from termination resistors, perpendicular crosstalk, etc., a value of 5mV and 10 mV was used respectively.

Power supply noise is also a source of Gaussian noise and is approximately 5% of the signal swing. So, for our design, it is about 20 mV.

Calculating total Gaussian noise with the above values yields a total of 22.9 mV RMS.

Board Specs

Line Width and Spacing, and Layer Stackup:

According to the datasheet for the Cyclone X chip, the "total current per LVDS I/O bank must not exceed 100 mA" (refer to (8), Work Cited) and a standard 1.4 mils (0.03556mm) copper thickness will be used. Assuming worst case, the minimum required trace width would be 1.26 mils (0.032004mm).

Also, according to the datasheet, "voltage levels must not exceed 1.89V" (refer to (8), Work Cited). Using this information and Appendix A, Table 1, the internal layers spacing between traces will be 0.05mm (2 mils), external conductors uncoated spacing is 0.1mm (4 mils), and the external conductors coated spacing at 0.05mm (2 mils) and then the spacing between layers will be around 0.15mm (6 mils).

The U484 packaging plan, comes with a 484-pin UBGA (ultra fineline ball grid array). With 188 GPIO's, 70 LVDS', and 6 XCVR pins, that means there are 264 signal pins, and 220 power and ground pins. Therefore, roughly 54.5% of the pins will be used as signal pins. Using these values with Appendix B, Equation 1, the number of layers in the stackup can be estimated. (refer to equation 1, Appendix B)

With four signal layers, an eight-layer stack up would be suggested where the four layers will be used for signaling, one for power, and one for ground.

Electrical Model of the Line:

Given the distances in and around traces, the capacitance and inductance between each trace can be calculated. (refer to Table 4, Appendix A)

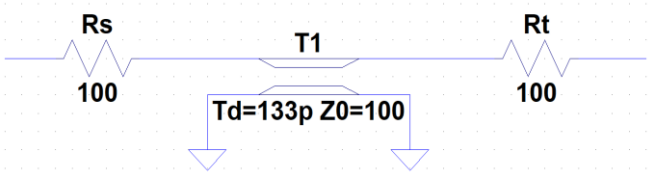

Fig. 1: This is the transmission line with Rs and Rt

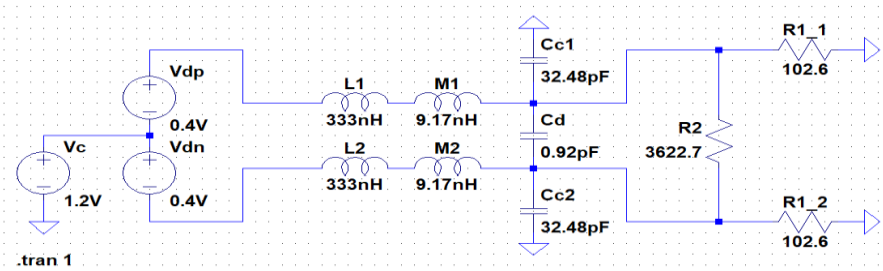

Fig. 2: Model of the Transmission Line

Signaling

Unidirectional vs. Bidirectional signaling:

Transmitter and Receiver pins are designated to either send or receive signals respectively. They are not capable of doing both and, as such, considered unidirectional pins. GPIO pins, on the other

hand, can behave as either one in each instance, but not both at the same time. This versatility is what makes the Cyclone X GX FPGA chip's pins bidirectional.

Single-ended vs. Differential signaling:

LVDS/Differential	Minimum Voltage (V)	Maximum Voltage (V)
Differential Mode Output	0.247	0.6
Common Mode Output	1.125	1.375

Table 4: Differential Signaling Voltage Values

The device has 188 single-ended signaling pins, and 70 LVDS pins, if using the U484 package plan. Otherwise, the number of pins increases for both if using larger package plans.

The information in Table 5 was provided (refer to Table. 3, Appendix A). After comparing the differences, LVDS (HSTL) is most ideal for the design.

Number of signal levels:

The common mode output voltage will be between 1.125V and 1.375V, and the differential mode output voltage will be between 0.247V and 0.6V. (refer to Table 3, Appendix A)

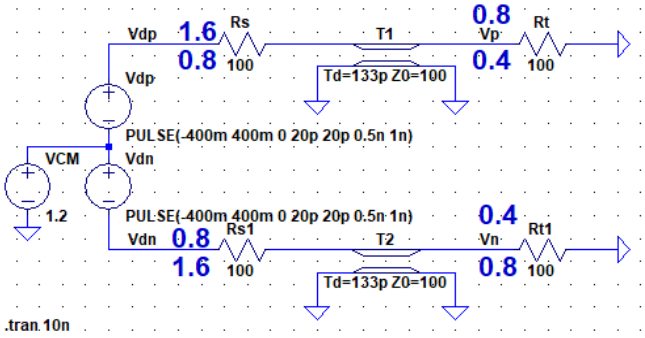

Fig. 3: Schematic shows hand calculation values above

	Voltage (mV)	
	Bit Value '0'	Bit Value '1'
V_{CM}	1200	1200
V_D	-400	400
Vp	800	400
Vn	400	800
Vp-Vn	400	-400
Vs	400 - (-400) = 800	

Table 5: Voltage Swing Calculation via Differential Analysis.

Signaling Rate:

Based on the signal levels mentioned and on Appendix A, Table 4, the 1 Gbps on the backplane will be the device's signaling rate.

It should be noted that, in order to make receiver performance optimal, "the receiver voltage input must be within 1.0 V to 1.6 V for data rates above 700 Mbps and 0 Vt to 1.85 V for data rates below 700 Mbps." (Note 25, Intel Cyclone 10 GX Device Datasheet)

Voltage/Current Mode:

The device will be in current mode.

Current mode was chosen to reduce noise from the Power Supply. Unfortunately, the current mode driver couldn't be implemented. This will be further discussed in the future improvements.

Equalization (if appropriate):

Unnecessary due to the homogenous medium.

Crosstalk Control (if appropriate):

Unnecessary due to the homogeneous medium.

Signaling Details - e.g., Levels, Rise-Time, Impedance: Rise time given by Table 22 of Device Datasheet.

Rise time and fall time have slightly larger values than aperture time which cause the signal to go from a square wave to more of a sine wave. (refer to Fig. 3)

Attenuation was considered through the lossy transmission line in LTSpice. (refer to Fig. 8)

The chip offers a signaling rate of 1.43 Gbps; a minimum of 1 Gbps and maximum of 6.6 Gbps on the backplane. (refer to Table 4, Appendix A)

If the backplane has a maximum of 6.6 Gbps, then we can safely assume voltage of the receiver is approximately 1.03 V and the rise time is 400 ps based on Appendix A, Table 5. This value would suggest that the chip-to-chip data rate is 12.5 Gbps.

Timing and Synchronization

Overall Timing Concept (e.g., clock forwarding, etc.):

Currently no flip flops have been implemented, but when getting around to it, clock forwarding architecture is what is planned. Particularly because it is a mesochronous system.

Some limitations of this concept are that clock skew can limit the performance, and low pass channels can cause jitter amplification.

A description of any manual or automatic timing adjustments (control loops):

A control loop will not be used throughout the design but discussed further in the "Future Improvements".

Noise Budget/BER

Transmitter Offset:

Appendix The offset for the transmitter would be +/- 5%.

Receiver Offset and Sensitivity:

For now, the assumed receiver offset is +/- 5%, and the receiver sensitivity is 10mV based on our design.

Crosstalk:

For the project, there would ideally be no crosstalk as there are no resistors that could potentially reflect voltage back onto the upper channel.

Coefficients	Ratio
Capacitive Coupling	0.28
Inductive Coupling	0.028
Near-End	0.0138
Far-End	0

Table 6: Coefficient Ratios

Inter-Symbol Interference (of all types and depending on your design):

The primary causes of intersymbol interference is Multipath Propagation and Bandlimited Channels.

Multipath Propagation is when a wireless transmitted signal reaches a receiver through multiple paths. Seeing how our project is not wireless, this interference is not accounted for in our design.

Bandlimited Channels are channels where the frequency response is zero above the cutoff frequency. When out of range, removed frequency components are considered an incomplete signal. As a result, the channel is unable to use the attenuated frequency. Since this type of interference is not limited to wireless devices, this project's design must take it under consideration. Some sources of this interference could be truncated signals sent through the channel or the physical properties of the medium.

Based on values found earlier, the differential signal can vary from -400 mV to 400 mV. From this, a voltage swing of approximately 400 mV is assumed.

Variable	Value
Gross Margin (Vs/2)	400mV
Worst Case Reflection	0.026
Reflection Crosstalk	0.0138
Kn	0.0398
KnVs	31.84mV
Transmitter Offset (Vs*+/-5%)	40mV
Receiver Offset (Vs*+/-5%)	40mV
Receiver Sensitivity	10mV

Bounded Noise	121.84mV
Net Margin (VNM)	278.16mV

Table 7: Intersymbol Interference Calculations

Accounting for Gaussian Noise:

Thermal NoiseVt = 4kTBR (Electronics Notes) where T is temperature, B is bandwidth, and R is resistance.

Using the given values, thermal Noise comes out to be approximately 40 uV which is almost negligible. There is 5 mV for unrelated backplane noise. 10 mV for added Gaussian noise due to termination resistors, perpendicular crosstalk, etc.

Noise Source	Voltage (mV)
Thermal	0.04
Backplane	5.00
Gaussian	10.00
PS V_{RMS}	20.00
Total V_{RMS}	22.90

Table 8: Sources of Gaussian Noise

Power Supply Noise:

Power supply noise is considered the "difference between the local voltage references of the driver and receiver" (Elgamel & Bayoumi) and is also considered a source of Gaussian noise. It can be approximated to roughly around 20mV.

There are several methods that can be employed to counteract power supply noise:

1. Increase the power and ground pins.
2. Use decoupling capacitors in Power and Ground lines.
3. Size up Power and Ground lines in order to minimize the IR and L di/dt voltage variations as well as compensate for large current peaks.
4. Perform clock skew scheduling to reduce the quantity of concurrent switching.

BER and MTBF calculations:

BER and MTBF Calculations	
VSNR	12.15
BER	9.15*10^-33
MTBF	3.456*10^15 years/error

Table 9: Bit Error Rate and Mean Time Between Failures

Timing Budget

Overall:

According to the high speed I/O specifications listed on Appendix A, Table 6 indicates a jitter of 200 ps. Additionally, under Appendix A, Table 7 regarding DDR3 protocol, the jitter for clock period, cycle-to-cycle period, and duty cycle can vary from -40 to 40 ps each.

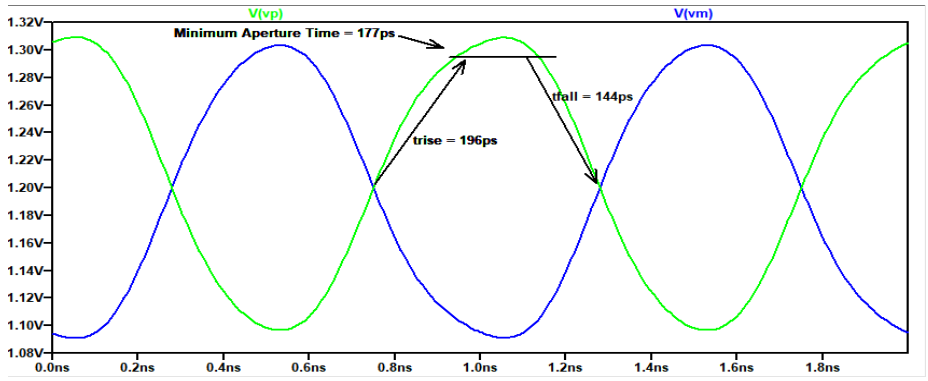

Fig. 3: LTSpice Simulation representing the rise/fall time and minimum aperture time

A list of all Sources of Jitter:

Ideally, the project design has no crosstalk and thus no jitter caused by it. However, there is a possibility of intersymbol interference if the bandwidth is not twice the frequency as $2/\tau$ is needed for reliable transmission. By differential I/O specifications given by Appendix A, Table 6 & 7, there are 4 given sources of jitter as listed in Table 12.

A list of Cancelled and Uncancelled Sources of Skew:

Channel-to-channel skew (TCCS) is the timing difference between the fastest and slowest output edges. As seen on Table 37 of the Cyclone X datasheet, The TCCS is 150 ps. It should be noted that the skew can be compensated for with PCB trace length (Note 59). Unfortunately, a control loop was not implemented to help get rid of uncancelled sources of skew. This means, the current design has no cancelled sources of skew.

Power & Cost

Power Estimate (per channel & overall):

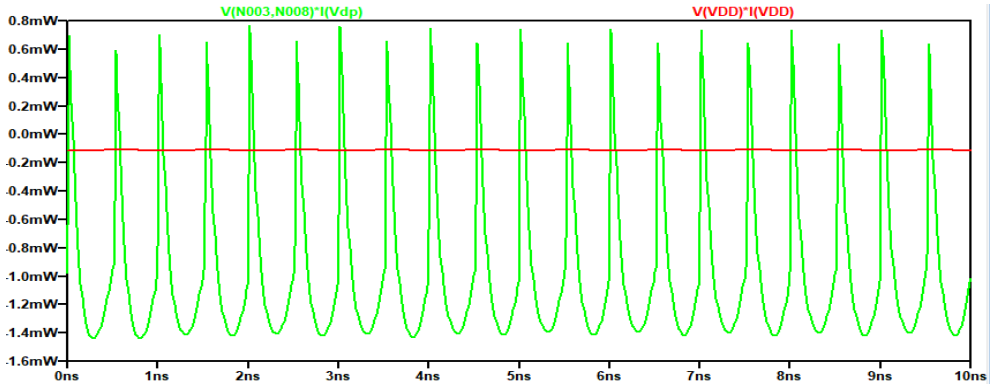

Fig. 4: Power Dissipation Waveforms through LVDS I/O (Green) and Receiver VDD (Red)

Using LTSpice simulation tools, the average power dissipated for the LVDS I/O is 977uW and for the Receiver's VDD is 112uW. This means, the total power dissipation is equal to 1.089mW.

Cost estimate (per channel & overall):

484UBGA Cyclone X x 1 ... $135.52
Cost of Comparator x 70 ... $0.53
PCB Board 8 Layer x 1…. $12.09
Total Cost = $184.71

SPICE or other simulations showing at least the following

Eye Diagram:

Using the same figure from Fig. 1, a PWL will be applied to the differential voltages to discover the eye in the system.

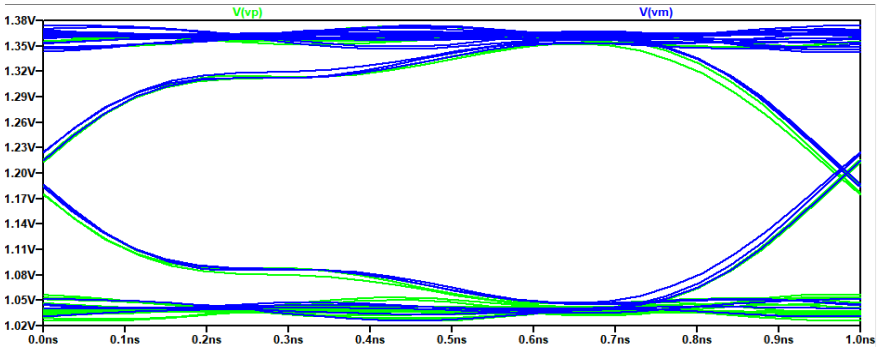

Fig. 6: Waveform of the Eye Diagram

TDR (Waveform at Source) and TDT (Waveform at Receiver):

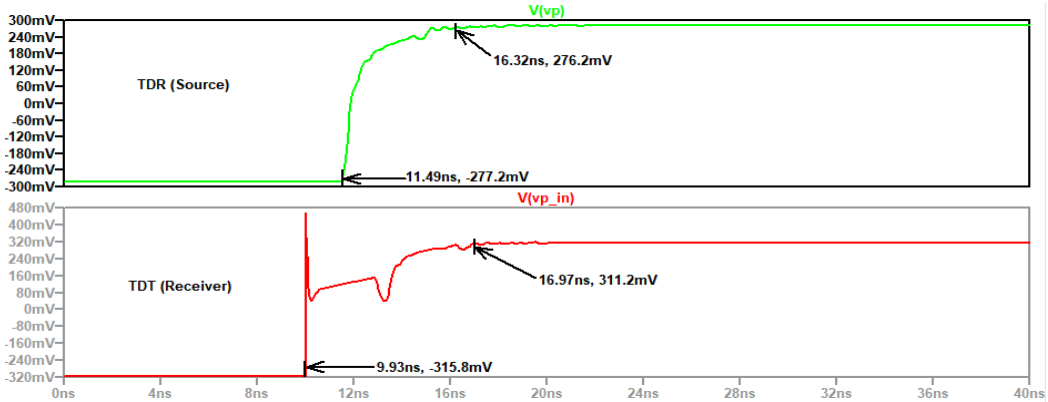

Fig. 7: Simulation of the schematic above

Using the worst-case, where the transmission line is offset by -5%, a reflection above appears.
As soon as the signal from Vp (0.133ns) travels back to Vi (0.267ns), the signal Vi gets updated to its correct value of 200mV at 0.286ns (0.19ns to update reflection).

Conclusion

It's difficult to keep the signal stable through a line with no current/voltage driver. With all the parasitic capacitances/inductances/resistances, it all hinders the signals input towards the receiver. Because of that, a not so very favorable output may occur.

The bit error rate can change significantly with the slightest change of any of the variables. As a result, the MTBF also fluctuated wildly.

Future Improvements

In order to get a much more desirable output the transmission line needs to be driven with all the parasitic capacitances it gets involved in. If a voltage/current driver were to have been applied, the receivers input waveform would've looked cleaner and maintained its shape and form as a square wave.

If a control loop were to have been applied, the eye diagram (refer to Fig. 4) potentially could have had a larger maintainable eye.

Appendix A: Tables/Simulations

	Internal layers		External conductors, uncoated		External conductors coated	
Vpk,V	mm	inch	mm	inch	mm	inch
15	0.05	0.002	0.1	0.004	0.05	0.002
30	0.05	0.002	0.1	0.004	0.05	0.002
50	0.1	0.004	0.6	0.024	0.13	0.006
100	0.1	0.004	0.6	0.024	0.13	0.006
150	0.2	0.008	0.6	0.024	0.4	0.016
170	0.2	0.008	1.25	0.05	0.4	0.016
250	0.2	0.008	1.25	0.05	0.4	0.016
300	0.2	0.008	1.25	0.05	0.4	0.016
500	0.25	0.01	2.5	0.1	0.8	0.032
1000	1.5	0.06	5	0.2	2.33	0.092
2000	4	0.158	10	0.4	5.38	0.22
3000	6.5	0.256	15	0.6	8.43	0.34
4000	9	0.355	20	0.79	11.48	0.46
5000	11.5	0.453	25	0.99	14.53	0.58

Table 1. IPC-2221 standard table for recommended clearance between two traces from

Rozenblat, Lazar. “PRINTED CIRCUIT BOARD (PCB) SPACING / CLEARANCE vs. VOLTAGE.”

Table 26. Transmitter Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	—	High Speed Differential I/O (44)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
Rise time (45)	20% to 80%	20	—	130	ps
Fall time (45)	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate setting of SLEW_R5 (46)	—	—	15	ps

Table 2. Transmitter Specifications Table 26 from *“Intel Cyclone 10 GX Device Datasheet.”* Intel.

Table 17. Differential I/O Standards Specifications for Intel Cyclone 10 GX Devices

Differential inputs are powered by V_{CCPT} which requires 1.8 V.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) (23)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (24)			V_{OCM} (V) (24)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (25)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0	D_{MAX} ≤700 Mbps	1.85	0.247	—	0.6	1.125	1.25	1.375
							1	D_{MAX} >700 Mbps	1.6						
RSDS (HIO) (26)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) (27)	1.71	1.8	1.89	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL (28)	1.71	1.8	1.89	300	—	—	0.6	D_{MAX} ≤700 Mbps	1.7	—	—	—	—	—	—
							1	D_{MAX} >700 Mbps	1.6						

Table 3. Differential I/O Standards Specifications for Intel Cyclone 10 GX Devices Table 17 from *“Intel Cyclone 10 GX Device Datasheet.”* Intel.

Signaling Details

Table 18. Transmitter and Receiver Data Rate Performance

Symbol/Description	Condition	Datarate	Unit
Chip-to-Chip (29)	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.03 V	12.5	Gbps
	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 0.95 V	11.3	Gbps
	Minimum Data Rate	1.0 (30)	Gbps
Backplane	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.03 V	6.6	Gbps
	Minimum Data Rate	1.0 (30)	Gbps

Table 4. Transmitter and Receiver Data Rate Performance Table 18 from *“Intel Cyclone 10 GX Device Datasheet.”* Intel.

Table 22. Reference Clock Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL (31)			
	RX pin as a reference clock	CML, Differential LVPECL, and LVDS			
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		25 (32) / 50	—	800	MHz
Rise time	20% to 80%	—	—	400	ps
Fall time	80% to 20%	—	—	400	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX pin as a reference clock	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} = 0.95 V	—	0.95	—	V
	V_{CCR_GXB} = 1.03 V	—	1.03	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) (33)	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 MHz to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R_{REF}	—	—	2.0 k ±1%	—	Ω
Maximum rate of change of the reference clock frequency $T_{SSC\text{-}MAX\text{-}PERIOD\text{-}SLEW}$ (34)	Max SSC df/dt			0.75	ps/UI

Table 5. Reference Clock Specifications from *"Intel Cyclone 10 GX Device Datasheet."* Intel.
-A list of all sources of Jitter

Table 37. High-Speed I/O Specifications for Intel Cyclone 10 GX Devices

When serializer/deserializer (SERDES) factor J = 3 to 10, use the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

The Intel Cyclone 10 GX devices support the following output standards using true LVDS output buffer types on all I/O banks:

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	–E5, –I5			–E6, –I6			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40 (57)	10	—	700	10	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards		Clock boost factor W = 1 to 40 (57)	10	—	625	10	—	525	MHz
f_{HSCLK_OUT} (output clock frequency)		—	—	—	700 (58)	—	—	625 (58)	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate) (59)	SERDES factor J = 4 to 10 (60)(61)(62)	(62)	—	1434	(62)	—	1250	Mbps
		SERDES factor J = 3 (60)(61)(62)	(62)	—	1076	(62)	—	938	Mbps
		SERDES factor J = 2, uses DDR registers	(62)	—	275 (63)	(62)	—	250 (63)	Mbps
		SERDES factor J = 1, uses DDR registers	(62)	—	275 (63)	(62)	—	250 (63)	Mbps
	$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	—	—	200	—	—	250	ps
		Total jitter for data rate, < 600 Mbps	—	—	0.12	—	—	0.15	UI
	t_{DUTY} (64)	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	%
	t_{RISE} & t_{FALL} (61) (65)	True Differential I/O Standards	—	—	180	—	—	200	ps
	TCCS (64)(59)	True Differential I/O Standards	—	—	150	—	—	150	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 (60)(61)(62)	150	—	1434	150	—	1250	Mbps
		SERDES factor J = 3 (60)(61)(62)	150	—	1076	150	—	938	Mbps
	f_{HSDR} (data rate) (without DPA) (59)	SERDES factor J = 3 to 10	(62)	—	(66)	(62)	—	(66)	Mbps
		SERDES factor J = 2, uses DDR registers	(62)	—	(63)	(62)	—	(63)	Mbps
		SERDES factor J = 1, uses DDR registers	(62)	—	(63)	(62)	—	(63)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	10000	—	—	10000	UI
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	± ppm
Non DPA mode	Sampling Window	—	—	—	300	—	—	300	ps

Table 6. High-Speed I/O Specifications for Intel Cyclone 10 GX Devices from *"Intel Cyclone 10 GX Device Datasheet."* Intel.

Table 43. Memory Output Clock Jitter Specifications for Intel Cyclone 10 GX Devices

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 10 ps peak-to-peak is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

Protocol	Parameter	Symbol	Data Rate (Mbps)	Min	Max	Unit
DDR3	Clock period jitter	$t_{JIT(per)}$	1,866	–40	40	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	1,866	–40	40	ps
	Duty cycle jitter	$t_{JIT(duty)}$	1,866	–40	40	ps

Table 7. Memory Output Clock Jitter Specifications for Intel Cyclone 10 GX Devices from High-Speed I/O Specifications for Intel Cyclone 10 GX Devices from *"Intel Cyclone 10 GX Device Datasheet."* Intel.

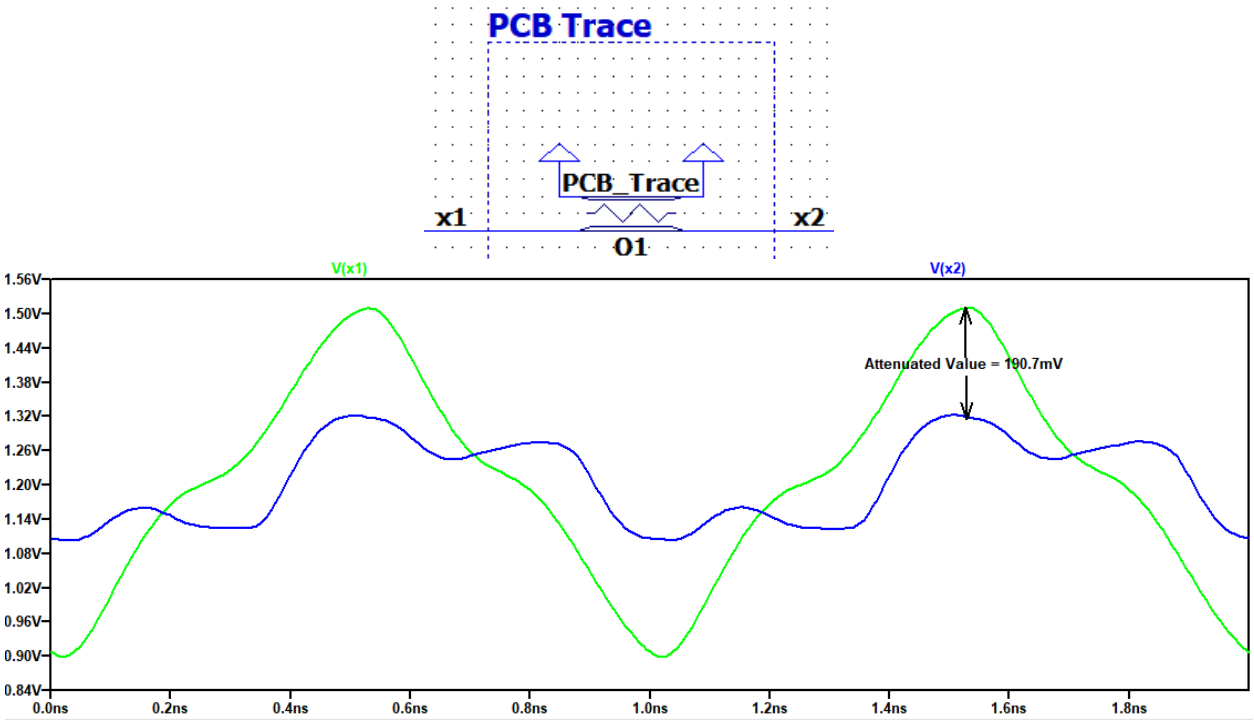

Fig. 8 Finding the attenuated value between the transmission line

Thermal Noise Variables	
Boltzmann Constant (k)	1.38*10^-23
Temperature	293 degrees
Bandwidth	1 GBPS
Resistance	100uV

Table 8: Values to plug into Thermal Noise Equation

Parameter	Distance (mils)
Trace Width	1.53
Copper Thickness	1.40
Internal Distance Between Traces	2.00
External Distance Between Traces	4.00
Spacing Between Layers	6.00

Table 9: Parameters for the Electrical Model of the Line

Appendix B: Equations, Calculations, and extra tables

$$\text{Layers} = \frac{Signals}{Routing\ Channels\ x\ Routes\ Per\ Channel} \quad (1)$$

(refer to (3), Work Cited)

Signals = (484 * 54.5%) = 264 signal pins
Routing Channels = (sqrt(484) - 1) * 4 = 84
Routes per Channel = 1 (because the spacing between each channel is small)
Therefore,
Layers = 264/(84*1) = 3.143 (round up) = 4 signal layers
Therefore, an 8 layer board is required

$$C = C(\text{parallel plate}) + C(\text{fringing}) = w\varepsilon/d + 2\pi\varepsilon / \ln(s/r) \quad (2)$$

where,
w = Trace width
s = h + d = spacing between layers + copper thickness
r = d/2 = copper thickness
ε = εo * εr
C = 9.68 pF/m + 23.7 pF/m = 33.4 pF/m

$$CL = \varepsilon\mu \quad (3)$$

L = (8.854x10^-12 * 4πx10^-7) / 33.4 pF/m = 333 nH/m

$$Z0 = \text{sqrt}(L/C) \quad (4)$$

Z0 = sqrt(351nH/m / 33.4pF/m) = 99.85 ohms ≈ 100 ohms

$$\text{Velocity} = 1 / \text{sqrt}(LC) \quad (5)$$

Velocity = 299850412 m/s or 3.0 m/ns

$$\text{Time Delay} = \text{length/velocity} \quad (6)$$

Time Delay = (40 cm) / (3.0 m/ns) = 133 ps

$$Cd = \varepsilon A/d = (\text{permittivity} * (\text{length} * \text{width})) / (\text{height}) \quad (7)$$

Cd = (8.854*10^-12 * (40cm * 0.038862mm)) / (0.15mm)
Cd = 0.92 pF/m

$$L/M = C/Cd \tag{8}$$

M = (Cd * L) / C
M = (0.92pF/m * 333nH/m) / 33.4pF/m = 9.17 nH/m

$$Cc = C - Cd \tag{9}$$

Cc = 33.4 pF/m - 0.92 pF/m = 32.48 pF/m

$$Zeven = sqrt((L + M) / (C - Cd)) \tag{10}$$

Zeven = sqrt((333nH/m + 9.17nH/m) / (33.4pF/m - 0.92pF/m))
Zeven = 102.6 ohms

$$Zodd = sqrt((L - M) / (C + Cd)) \tag{11}$$

Zodd = sqrt((333nH/m - 9.17nH/m) / (33.4pF/m + 0.92pF/m))
Zodd = 97.1 ohms

$$R1 = Zeven \tag{12}$$

R1 = 102.6 ohms

$$R2 = 2((Zeven * Zodd) / (Zeven - Zodd)) \tag{13}$$

R2 = 2((102.6 * 97.1) / (102.6 - 97.1)) = 3622.7 ohms

$$Kcx = Cd / C \text{ (Capacitive Coupling)} \tag{14}$$

Kcx = 0.92pF/m / 33.4pF/m
Kcx = 0.28

$$KIx = M / L \text{ (Inductive Coupling)} \tag{15}$$

KIx = 9.17nH/m / 333nH/m
KIx = 0.028

$$Krx = (Kcx + Klx) / 4 \text{ (Reflection Crosstalk Coefficient)} \tag{16}$$

Krx = (0.028 + 0.028) / 4
Krx = 0.0138

$$Kfx = (Kcx - Klx) / 2 \text{ (Far-end Crosstalk Coefficient)} \tag{17}$$

Kfx = (0.028 - 0.028) / 2
Kfx = -0.0000037 = 0

$$\text{Gross Margin} = Vs/2 \tag{18}$$

Gross Margin = 400 mV

$$Kn = \text{Crosstalk} + \text{Reflection} \tag{19}$$

Kn = 0.0398

$$\text{Intersymbol Interference} = KnVs \tag{20}$$

KnVs = 0.1238 * 800 = 31.84 mV

$$\text{Transmitter offset} = Vs*+/-5\% \tag{21}$$

Transmitter offset = 40mV

$$\text{Receiver offset} = Vs*+/-5\% \tag{22}$$

Receiver offset = 40mV

$$\text{Bounded Noise} = 31.84mV + 10mV + 40mV + 40mV \tag{23}$$

Bounded Noise = 121.84mV

$$\text{Net Margin (VNM)} = \text{Gross Margin} - \text{Bounded Noise} \tag{24}$$

Net Margin (VNM) = 278.16 mV

$$\text{TOTAL VRMS} = \text{sqrt}((5mV)^2 + (10mV)^2+(20mV)^2) \tag{25}$$

TOTAL VRMS = 22.9 mV RMS

$$VSNR = VNM / VRMS \tag{26}$$

VSNR = 278.16 mV / 22.9 mV = 12.15

$$BER = e^{-((VSNR)^2 / 2)} \tag{27}$$

BER = e^-((12.15)^2 / 2) = 3.91*10^-19

$$MTBF = (1/BER) / 1gbps \tag{28}$$

MTBF = (1/(3.91*10^-19)) / 1gbps = 3.456x10^15 years/error

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