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EE421-1001 F19

Switching Power Supply Boost Converter

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Summary of the Boost SPS

A boost SPS is a type of switch mode power supply circuit. It is designed to “boost” a lower DC voltage to a higher one. For example, a boost SPS can convert an input of 5V to an output of 12V. In short, a boost SPS is a step-up regulator. For this design, the input VDD ranges from 3.75V to 5.25 and will output a steady voltage of 7.5V.

The boost SPS consists of 6 general on-chip: a voltage divider, the bandgap, a comparator, a ring oscillator, a 3-stage buffer, and an NMOS switch. It also has an input terminal for an input voltage, and an input-output terminal connected to the drain of the NMOS.

A voltage divider takes the circuits boosted voltage and sends $1/6^{th}$ of it to the comparator where it is compared to a consistent voltage (1.25V) generated by the bandgap. The comparator’s output is high when the bandgap output voltage exceeds that of the divided input voltage, and the output is low when the divided input voltage exceeds the bandgap output. This signal is sent to the ring oscillator to enable its operation. When enabled, the ring oscillator creates a waveform to be sent to the 3-stage buffer of 8x incrementation (73 short-length inverters). The resulting waveform has a frequency of 9.63 MHz (a period of 103.8238ns), and a duty cycle of approximately 74% (an active high for 77.0895ns). This final signal is then connected to the gate of the NMOS where it will ground the wire that its drain is connected to whenever the NMOS is activated.

Design Tradeoffs

1N5819 Schottky Diode

This diode has a maximum voltage of 40V and a rectified forward current of average of 1A. It is perfect for the operation of this circuit as it has a dissipation of 1.25W of power and a maximum thermal resistance of 100 degrees Celsius per watt. In addition to being able to operate in temperatures of up to 100 degrees Celsius, it also has little to no thermal runway when operating at 90 degrees Celsius. This is far more than enough for the used power supply. Thermal runway can cause a significant amount of damage to a circuit or even destroy it. It is the result of the circuit's internal heat increasing faster than its ability to dissipate excess heat. The specifications of this diode make it an ideal choice for this circuit.

NMOS switch

The NMOS must switch quickly which makes it require a considerably large width. This influenced my choice of choosing a MOSFET with a width of 150um and a multiplier of 8 to create a 2000:1 ratio between the width and the length. The chosen NMOS has a resistance of 10ohms and a capacitance of 1.8pF. Due to the smaller internal gate resistances from the large width, the MOSFET can carry high current and be used as a high-speed switch.

Adjusting the width of the NMOS causes a tradeoff between the internal resistance and its capacitance. The NMOS must have a lower resistance if it is to be used as a high-speed switch. The greater the width, the lower the resistance. However, this negatively affects the internal capacitance by increasing it as the width increases, resulting in additional delay. To reduce this, a buffer is required to drive the signal at a faster rate. This can further be reduced by using multiple fingers, hence the use of a multiplier.

Capacitor

The overall circuit oscillates near 7.5V with some ripple. The reduced ripple is due to the size of the chosen capacitor. In this case, 3um is well over the minimal amount needed for the circuit. Capacitors can be used to reduce noise in power supply circuits as it helps smooth the signal. The amount of ripple current capacitor contains is closely related to temperature. For this reason, a ceramic capacitor should be used when this chip is fabricated because ceramic capacitors can operate at higher temperatures over other conventional capacitors. The amount of ripple is dependent on the input voltage. When operating at the minimum voltage of 3.75V, the circuit's output oscillates between 7.477V and 7.554V. At maximum voltage of 5.25V, the output instead oscillates at a slightly higher voltage of 7.507 and 7.646.

The main tradeoff is the capacitance's size depends on the chosen speed of the circuit. Higher frequencies demand larger capacitors as large quantities of current are produced. Having larger capacitors can significantly increase delay. This delay is compensated for by using a buffer to help reduce it.

Inductor

Like the capacitor, the inductor's size is also reliant on the frequency of the circuit. This results in a tradeoff between frequency and impedance. At higher frequencies, an inductor's impedance will also increase causing lower current in the load resistor. To adjust for this, a smaller inductor is necessary to ensure higher current to the load resistor and less overall impedance in the circuit.

Details of On-chip components

General Information

Table 1: Inverters

Inverter	Size (W_P/W_N)	Use
Short-Length	12u/6u	General Purpose Standard Inverter
Long-Length	6u/6u	Signal Delayer Found in Ring Oscillator
8x Inverter	96u/48u	Buffer Stage 2 of 3-stage Buffer
64x Inverter	768u/384u	Buffer Stage 3 of 3-stage Buffer

Table 2:

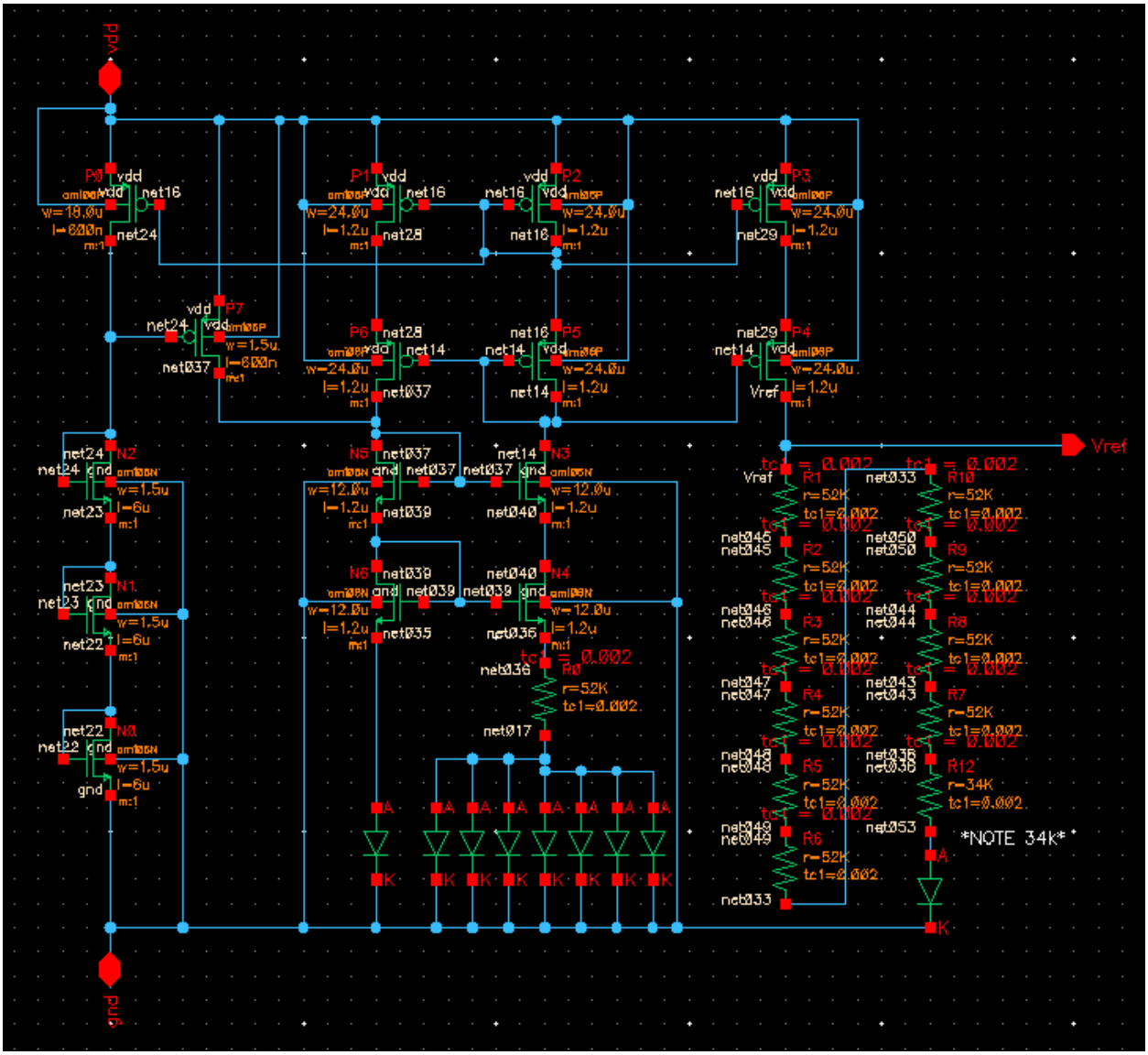
Ring Oscillator Specifications		
Frequency	9.63 MHz	
Duty Cycle	Before Buffer	After Buffer
	26%	74%

Bandgap

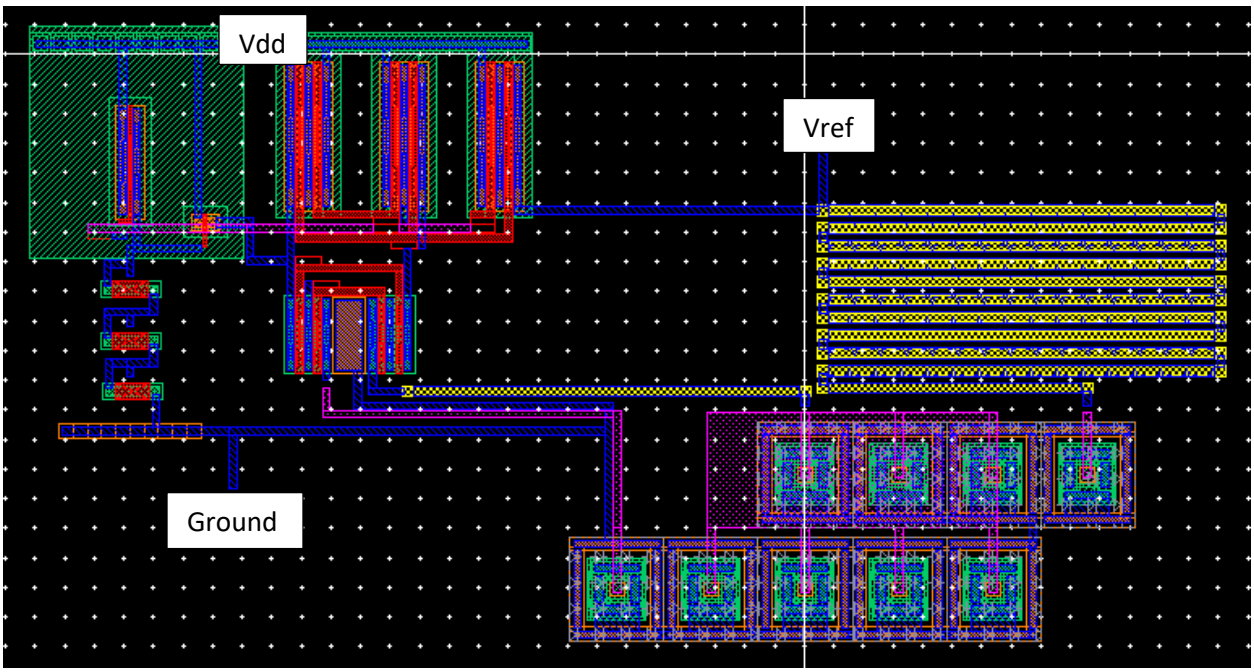
The purpose of the bandgap circuit is to consistently output a steady voltage of 1.25V regardless of how much Vdd may vary. This output is connected to one of the two input terminals of the comparator to always check if the overall voltage output of the whole circuit goes below a certain threshold.

Schematic, Layout, and Symbol of Bandgap:

Schematic:

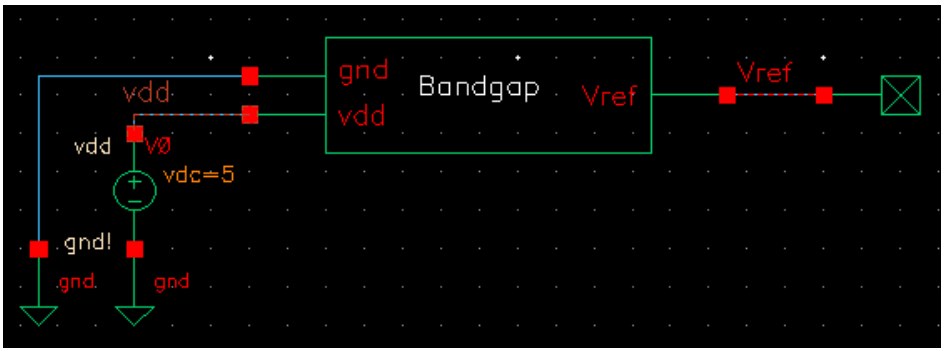


Layout:

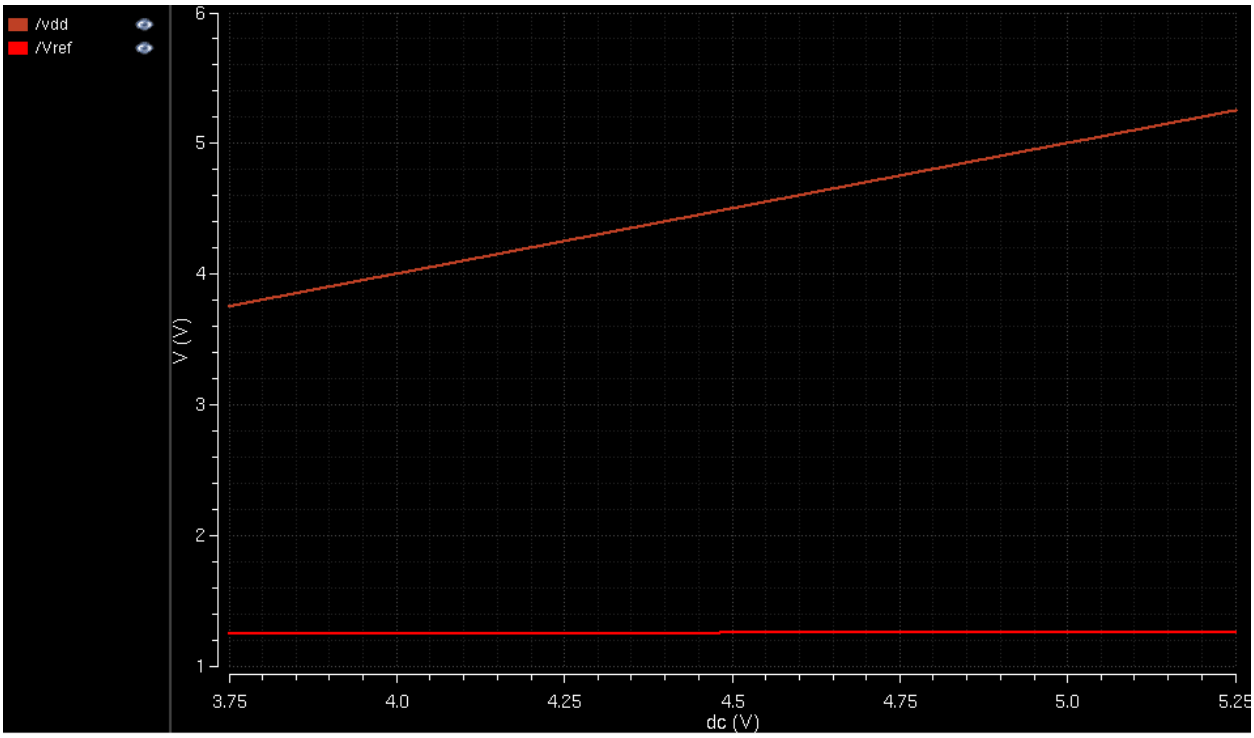


Symbol:

Bandgap Simulation:



Running a dc analysis from 3.75V to 5.25V, we can see that even as vdd increases overtime, the bandgap outputs a consistent 1.25V with minimal variation. From this, we can safely assume it works as intended.

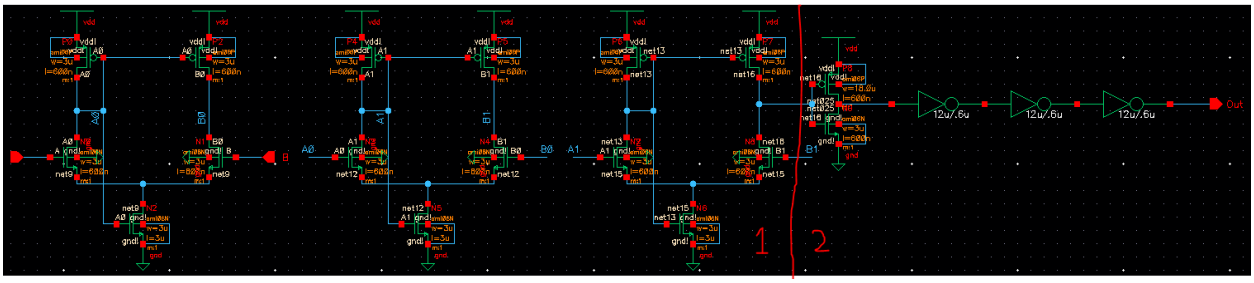


Comparator

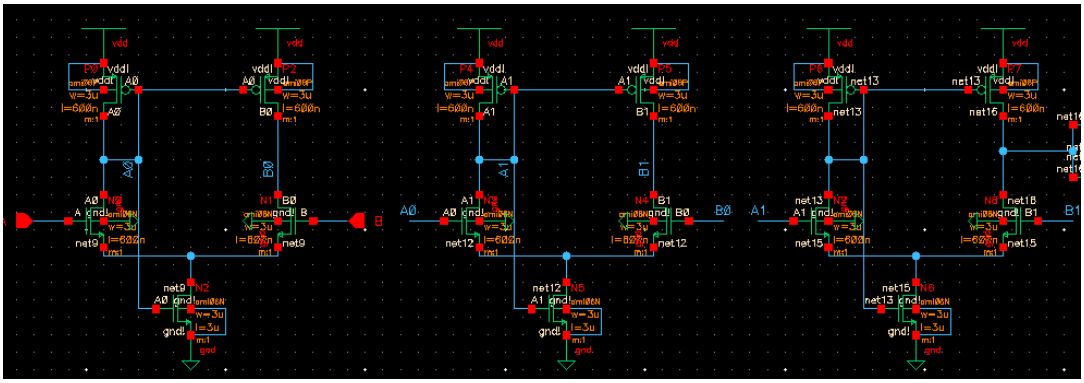
A comparator outputs a signal depending on the comparison between two inputs. The signal is set to high when the input voltage at the positive terminal surpasses the input voltage. Shown below is the entirety of the comparator schematic. The first portion of the circuit, or segment 1, consists of three cascading self-biased differential amplifiers. All 3 act as hysteresis devices but take the output of the previous device as their respective inputs. The 3 NMOS' located at the bottom of Segment 1 are all 3u/3u widths and lengths while the rest are of 3u/.6u dimension. Segment 2, also seen below, consists of primarily inverters to square up the output. The 3 right most inverters are the standard 12u/.6u inverters. The inverter between the standard inverters and the hysteresis devices has a PMOS of 18u/.6u and an NMOS of 3u/.6u. This is in order to reduce the delay of the output signal.

Schematic, Layout, and Symbol of Comparator:

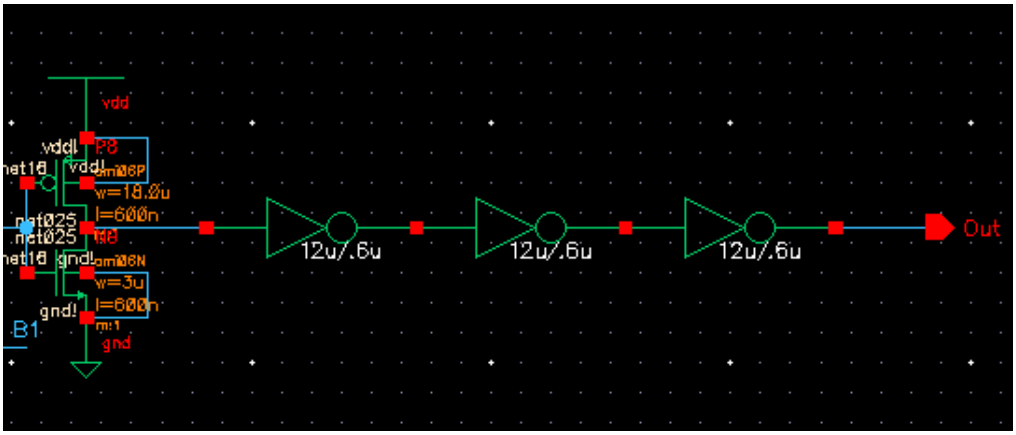
Total Schematic:



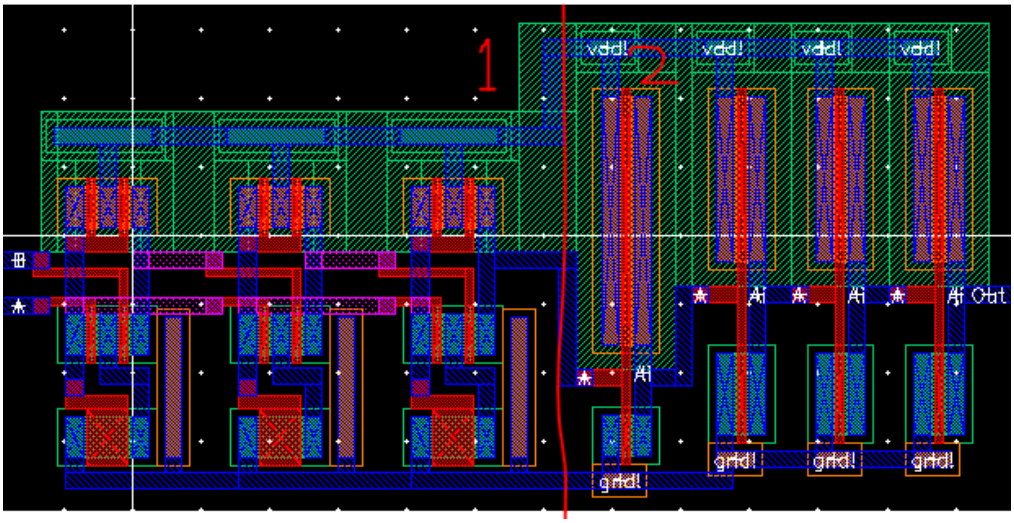
Segment 1:



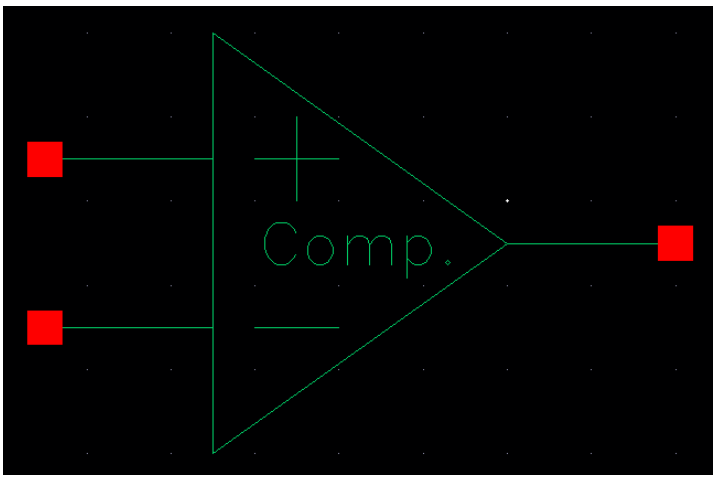
Segment 2:



Layout:

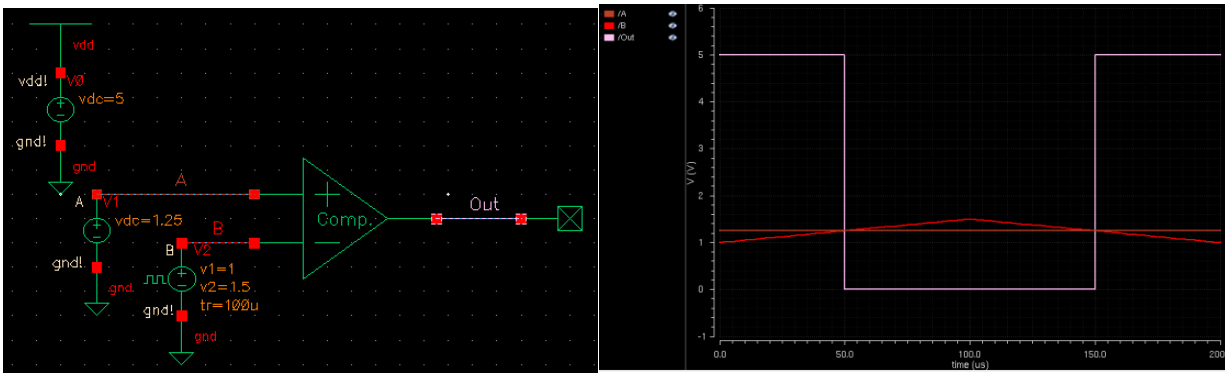


Symbol:



Comparator Simulation:

Using the comparator symbol and a regular transient simulation set for 200us, I connected the positive terminal to a vdc of 1.25V as a way of representing the bandgap, and the negative terminal to a pulse signal varying between 1V and 1.25V.

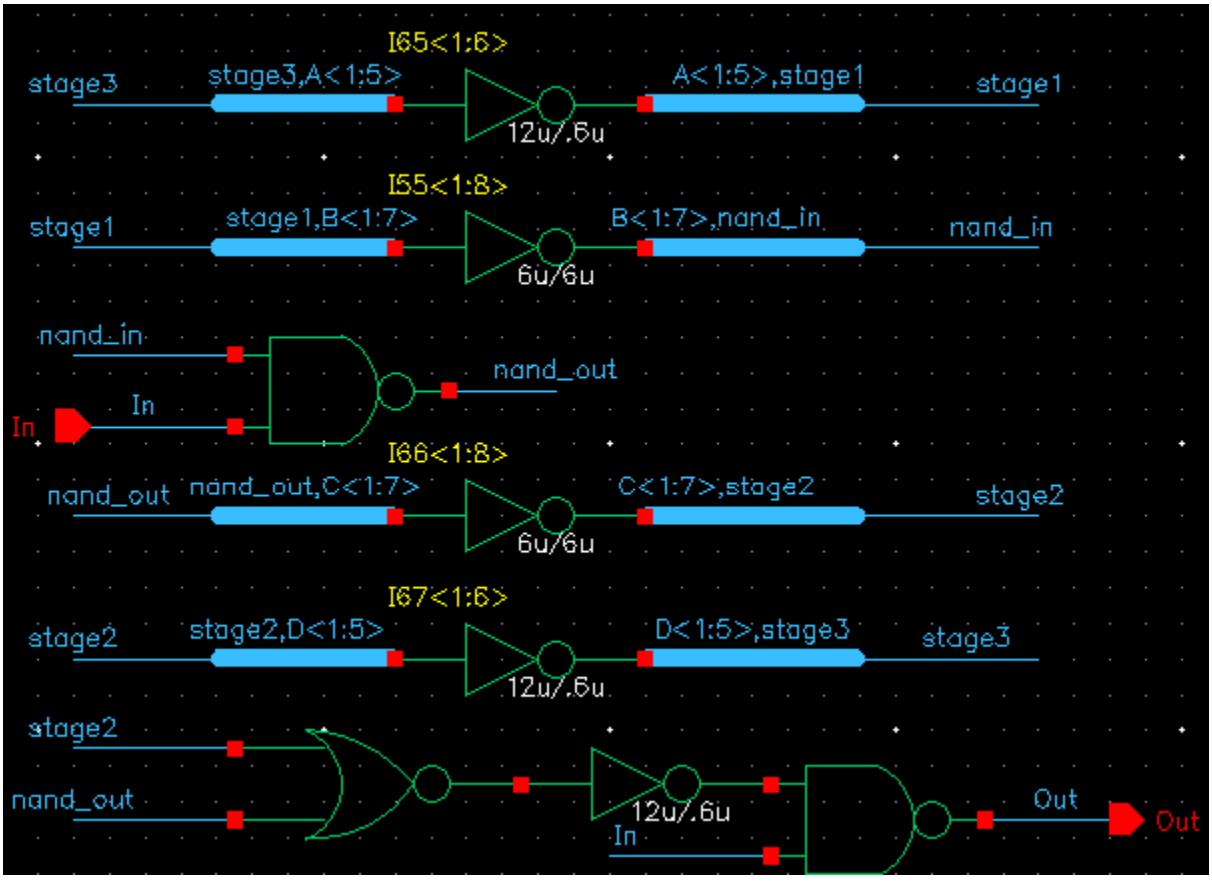


As seen in the graph, the comparator's output is high until the moment the input voltage of the negative terminal surpasses that of the positive terminal. At this point, the comparator quickly switches to low.

Ring Oscillator

All components of the SPS hold an important role, but the ring oscillator is the determinant for multiple off-chip components. It determines the frequency and duty cycle of the entire circuit which is essential in nearly all calculations regarding efficiency. In total, the oscillator for this design is made up of 13 short-length inverters, 16 long-length inverters, 2 nand gates, and 1 nor gate. The assembly of all parts can be seen below in the schematic. The signal taken in from the comparator acts as an enable for both the oscillator as well as its output.

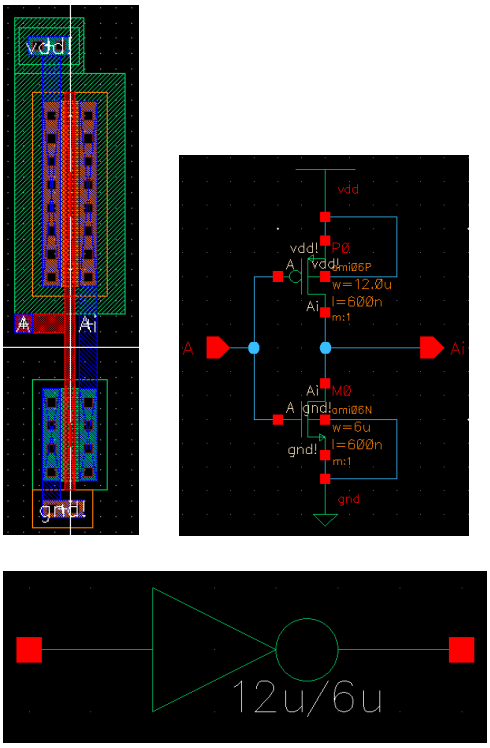
Schematic of Ring Oscillator:



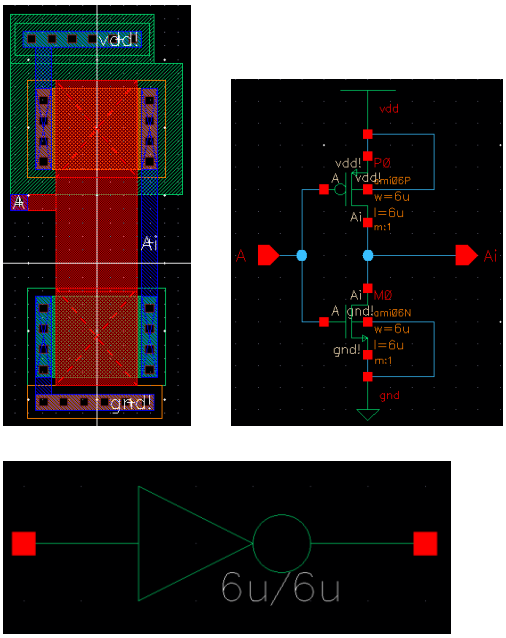
General Layouts of Involved Components:

It is important to note how many various parts there are inside of the ring oscillator and how to identify each of the individual parts. Given below are the schematics, layouts, and symbols of the inverters, as well as the NAND and NOR gates for reference.

12u/.6u Inverter Layout:

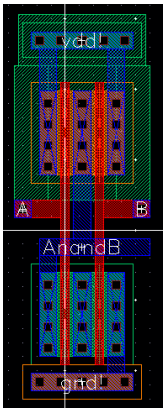


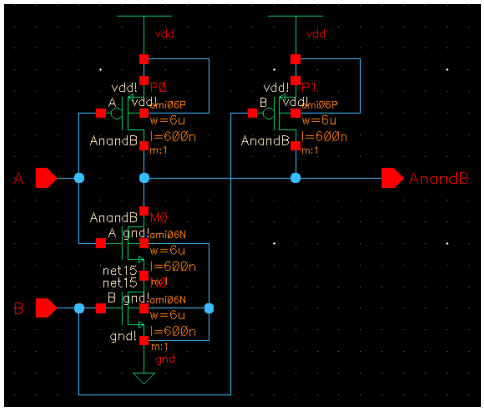
6u/6u Inverter Layout:

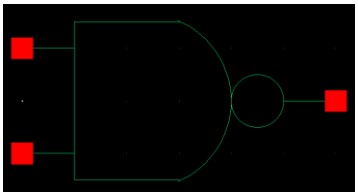


NAND Gate:

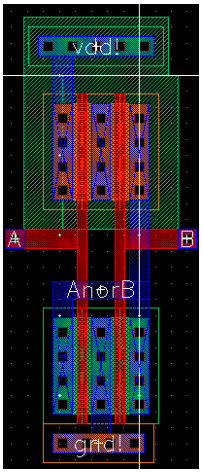
The NAND gate uses 2 PMOS's and 2 NMOS's of 6um width

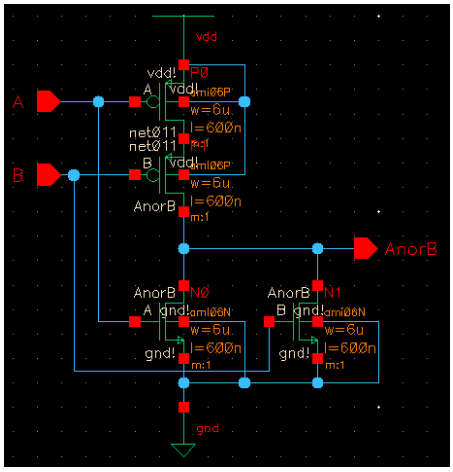


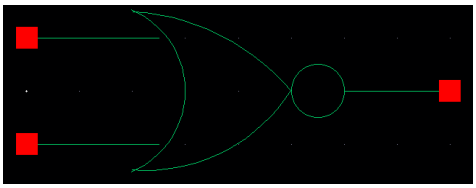




NOR Gate:

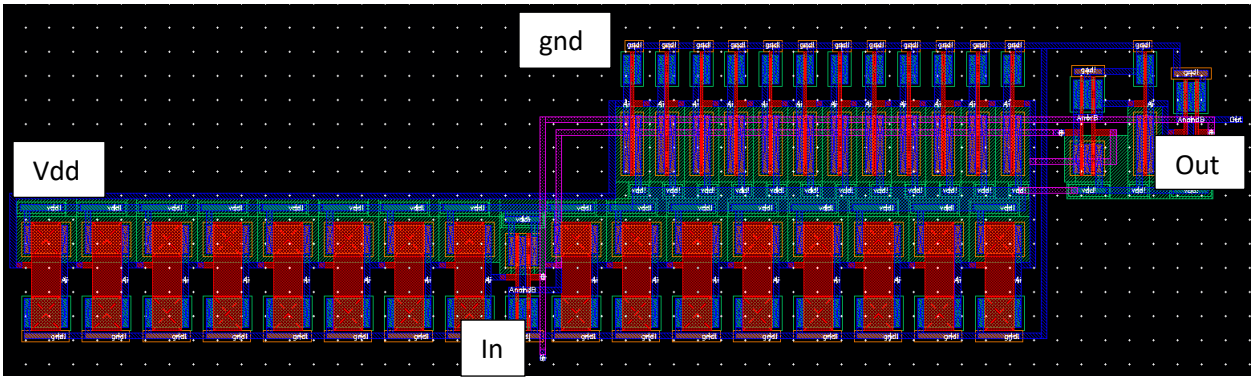




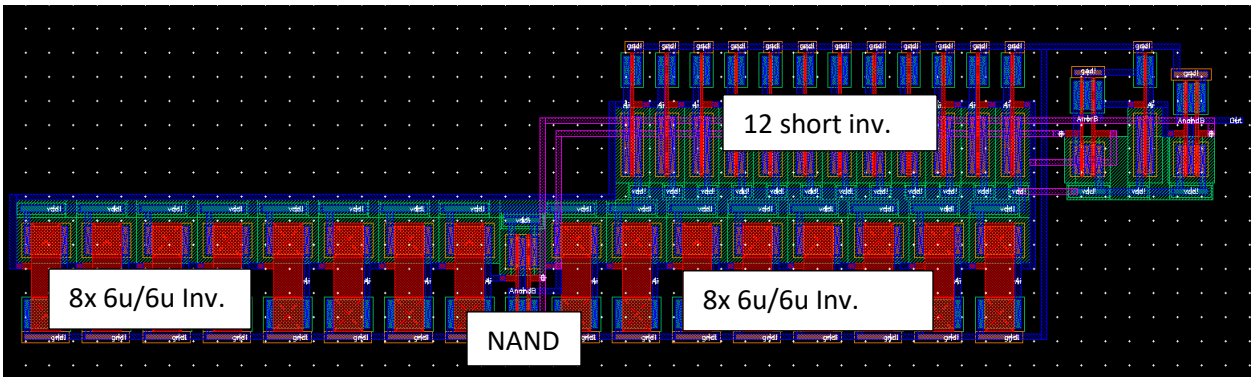


Layout and Symbol of Ring Oscillator:

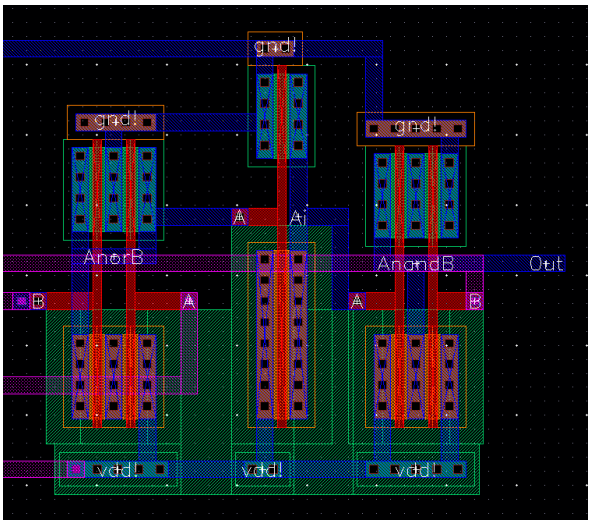
Terminals:



Inverter and Gate:



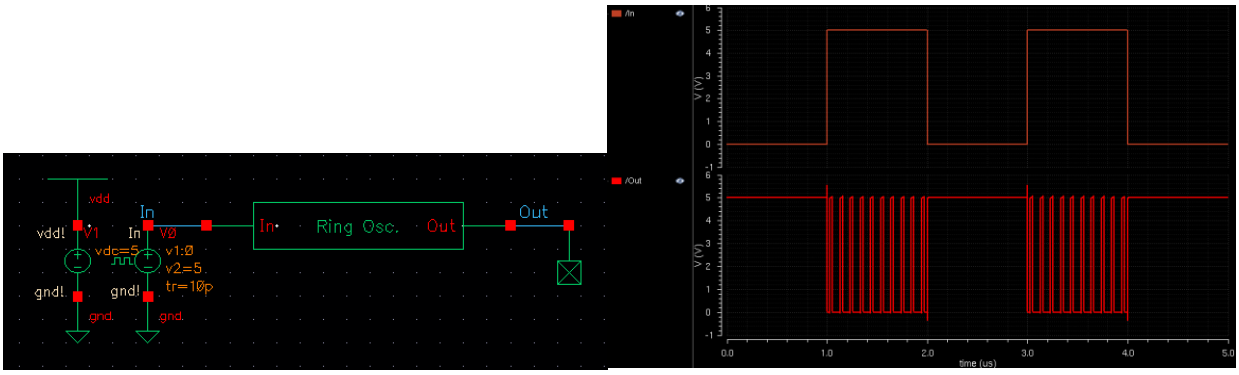
The NOR Gate, Inverter, and NAND Gate located at top right corner of layout leading to the output terminal of the oscillator is given below along with the symbol:



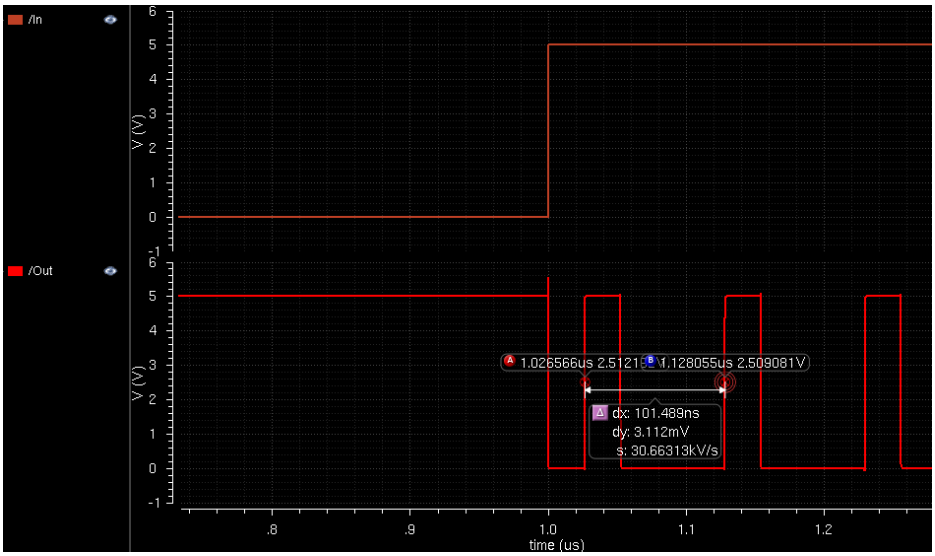
Symbol:

Ring Oscillator Simulation:

In order to simulate the Ring Oscillator, its input is connected to a pulse signal to represent the enable signal that is output from the comparator as shown below. From what it looks like, it generates a duty cycle below 50%. This is solved through the 3-stage buffer.



Zoomed in, we can see that the ring oscillator on its own creates a frequency of 9.63MHz and has a duty cycle of about 24%.



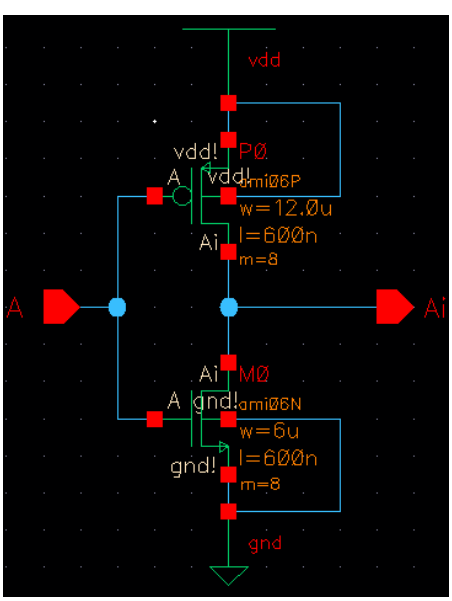
3-Stage Buffer

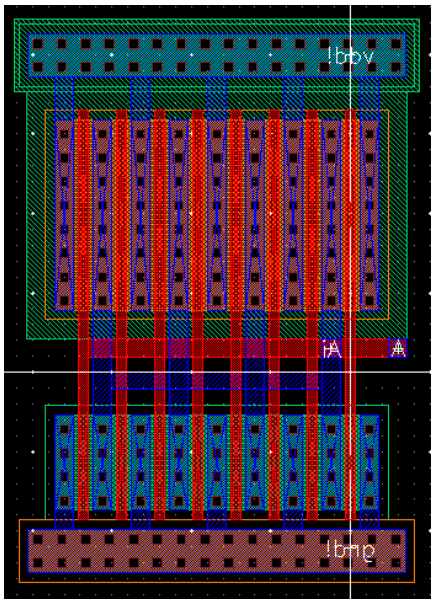
The 3-Stage Buffer for this circuit is designed to fulfill multiple purposes. One is to invert the ring oscillator's signal so that the NMOS receives a signal with a duty cycle above 50% rather. This is because the quantity of inverters used for this buffer is odd, causing the signal to finally output as an inversion. Another is to counter the high capacitance of the switch itself as well as the capacitance of the capacitor in which both would give significant delay. Every stage of the buffer is 8 times the previous stage.

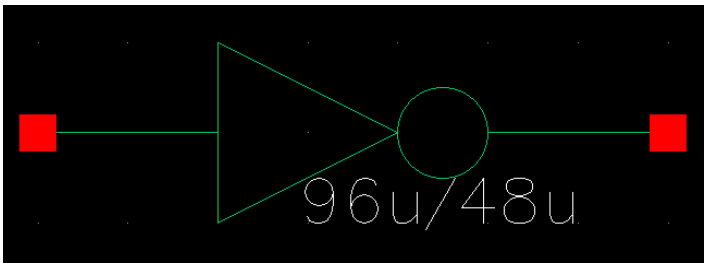
The first stage of the buffer is that of a 12u/6u short-length inverter. The schematic, layout, and symbol of this can be referenced in the earlier section discussing the ring oscillator. The second stage is another 12u/6u inverter except with a multiplier of 8. This results in an inverter equal to having dimensions of 96u/48u but with 8 fingers. The third and final stage is yet another multiplier of 8x the previous one resulting in a final inverter with the equivalence of 768u/384u. This is still made with the standard 12u/6u inverter, but this time with a final multiplier of 64x.

Schematic, Layout, and Symbol of 3-Stage Buffer:

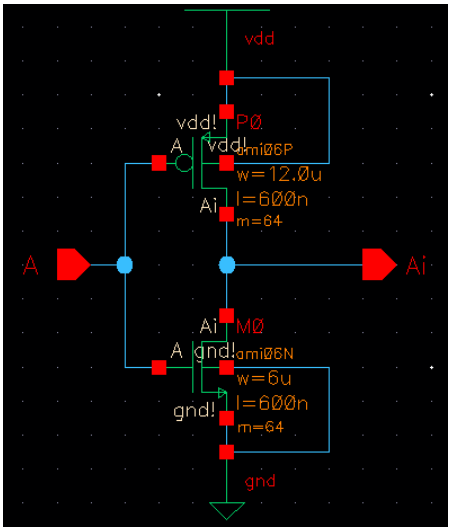
2nd Stage of buffer:

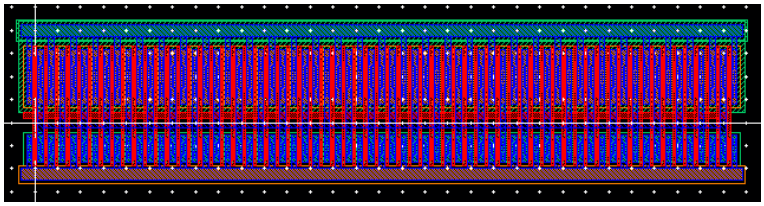


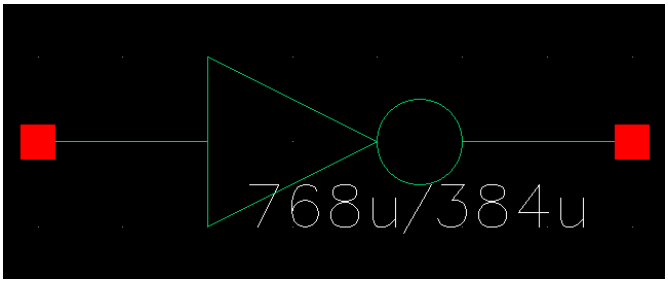




3rd Stage of Buffer:

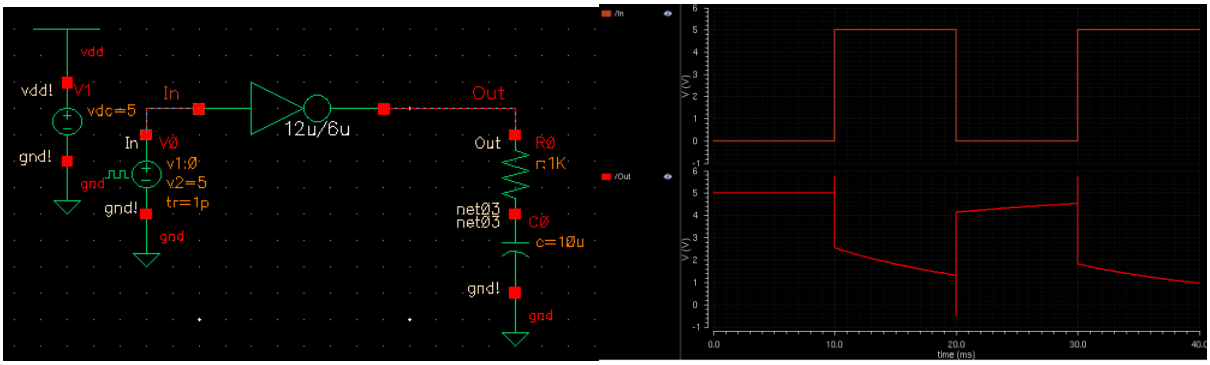




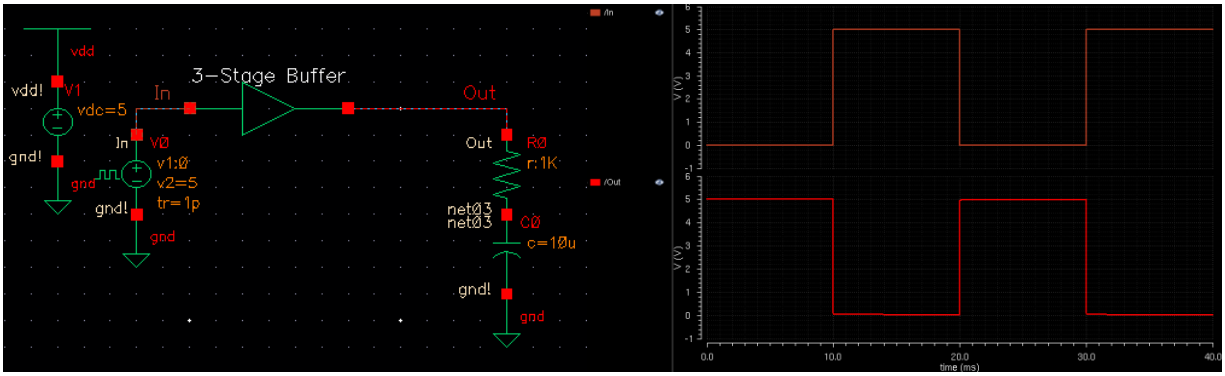


3-Stage Buffer Simulation:

To simulate the 3-stage buffer, a pulse signal is attached to the input terminal to represent the ring oscillator output. The signal will pulse every 10ms with a period of 20ms. On the output is a resistor followed by a capacitor which normally would give a delay to the signal. This can be seen in the following where, instead of a buffer, a single inverter is used.



However, if we replace the inverter with a 3-stage buffer, the wave manages to reach steady state quickly and closely resembles a proper inversion of the input wave.



NMOS Switch

The NMOS switch is responsible for the grounding of the anode of the Schottky diode, and thus, the charging and discharging of the capacitor. As described in the tradeoffs, the NMOS switch must be high-speed to ensure proper functionality of the circuit. This makes the necessary NMOS switch have a large width in order to encompass small internal gate resistance and be capable of carrying high currents. In order to satisfy this condition, the SPS for this design is an NMOS with a width of 15um and length of 600nm, as well as a multiplier of 8.

The resistance of the MOSFET can be calculated using the following:

$$R = Rsquare * (\frac{L}{W})$$

Knowing that Rsquare is 20k, plugging in the chosen dimensions results in:

$$R = 20kohms * \left(\frac{600nm}{8 * 150um}\right) = 10ohms$$

10 ohms is small in comparison to other resistors in the circuit that is considered negligible or redundant.

Knowing C'ox is equal to 25fF/um^2, we can also calculate the capacitance of the NMOS given by the equation:

$$Cox = C'ox(L * W)$$

Plugging in what we have into the equation:

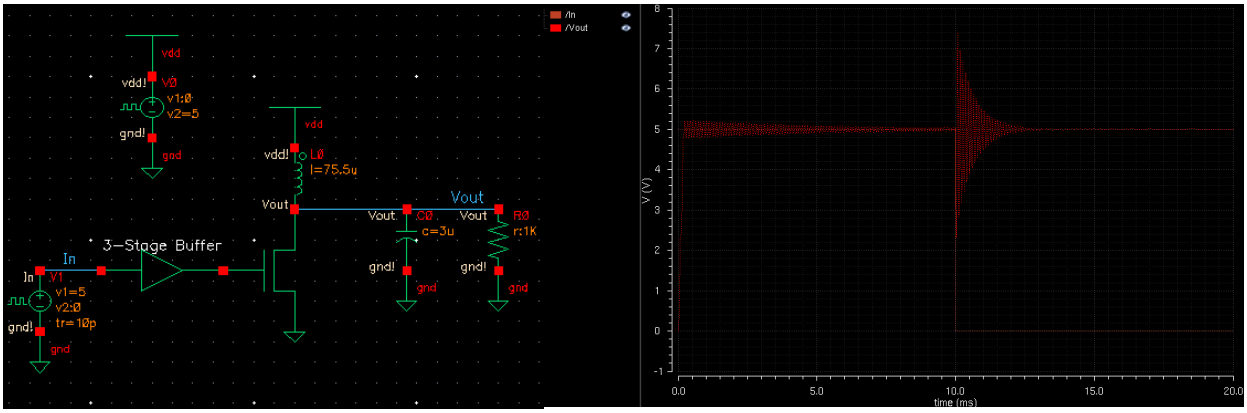
$$Cox = \left(\frac{2.5fF}{um^2}\right) * 600nm * (8 * 150)um = 1.8pF$$

1.8pF capacitance is quite significant. This is the tradeoff of the NMOS switch; a lower resistance is desirable, but it comes at the cost of increased capacitance. This is compensated for using the buffer's application to drive the signal as mentioned before.

Schematic, Layout, and Symbol of NMOS Switch:

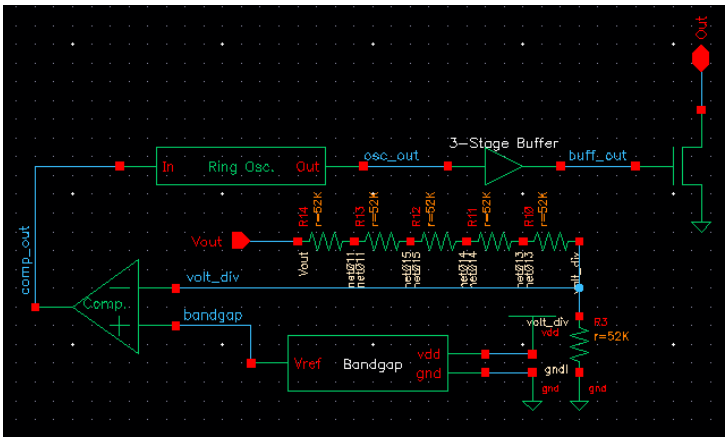
NMOS Simulation:

When the signal “In” is high, the NMOS is switched off, allowing the capacitor to charge up. Once switched on, the switch closes and Vout is pulled to ground. However, the capacitor is trying to discharge causing a current through the Vout wire. This creates an oscillation as the current bounces between the inductor and the capacitor causing resonance.



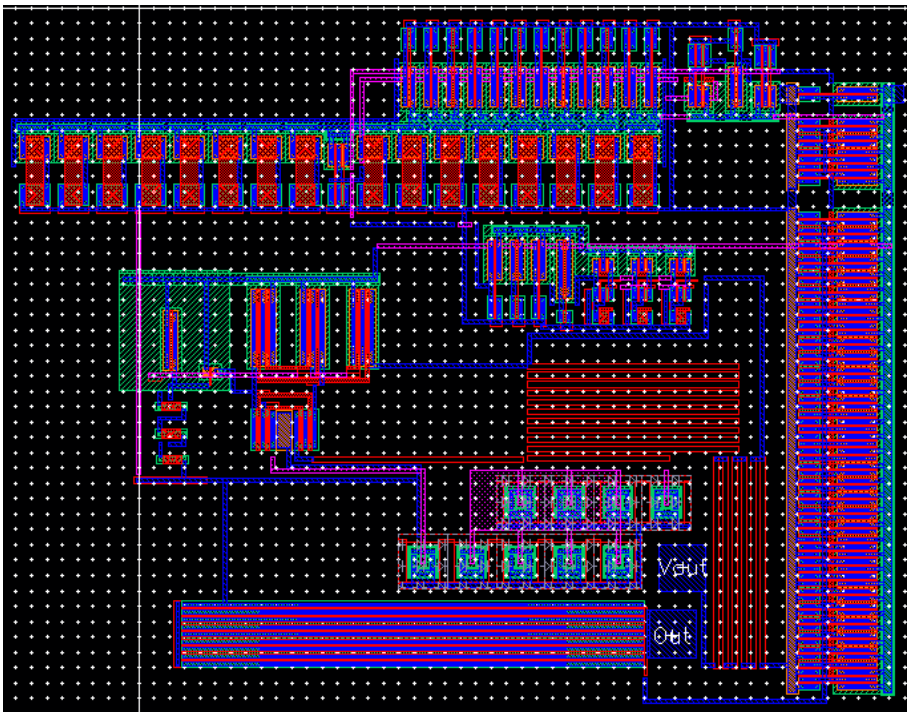
Final Schematic of SPS and Layout

Putting together all the described parts in the order of description creates the following schematic of the SPS and Layout:

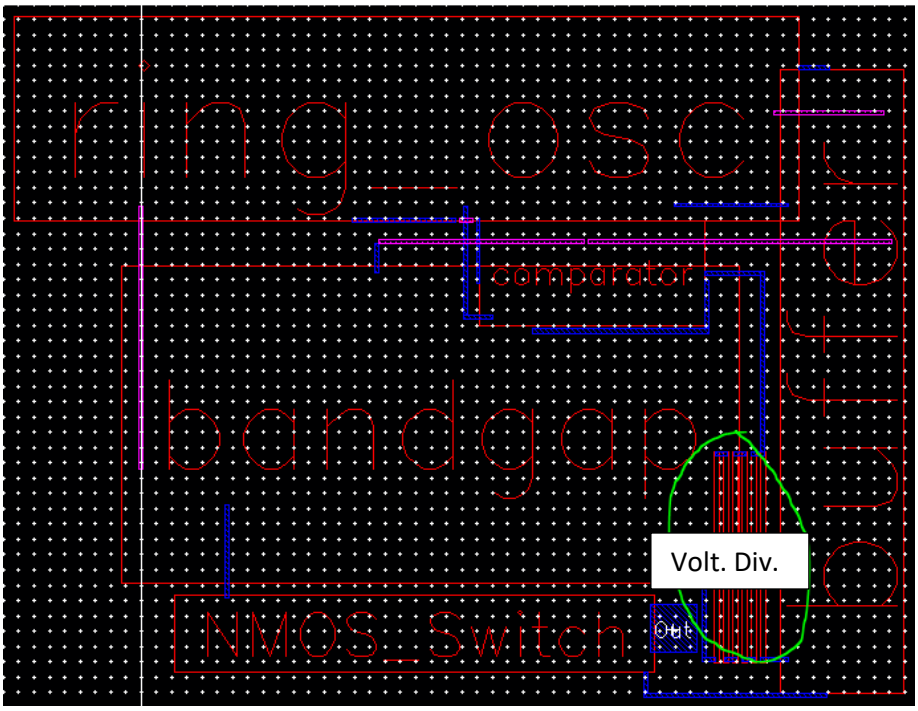


This is the full layout of the SPS. The various component parts that make it up are visible by making the start and stop of display levels in display options 0 as shown below the full layout.

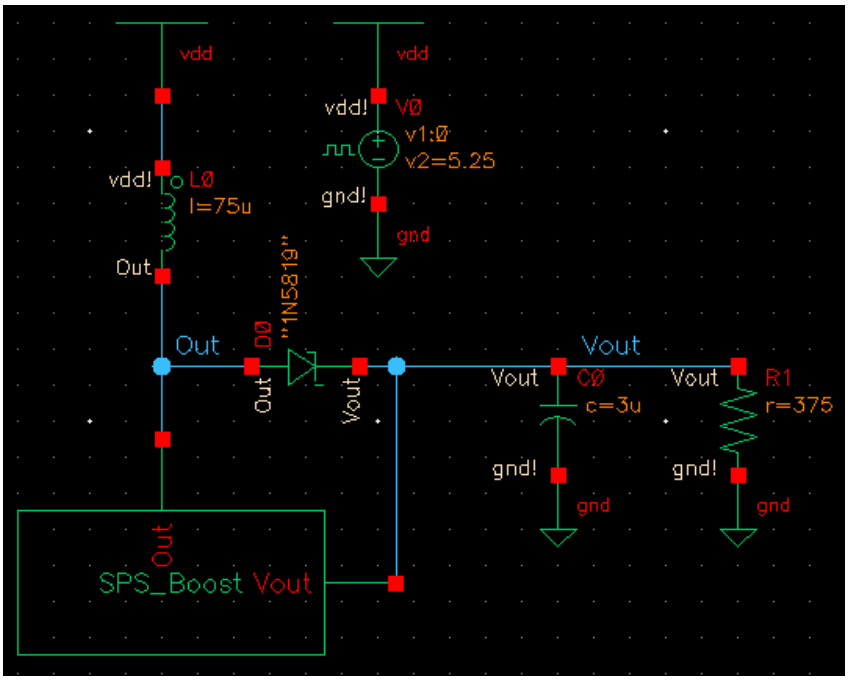
Layout:



Layout with 0 Display Levels:

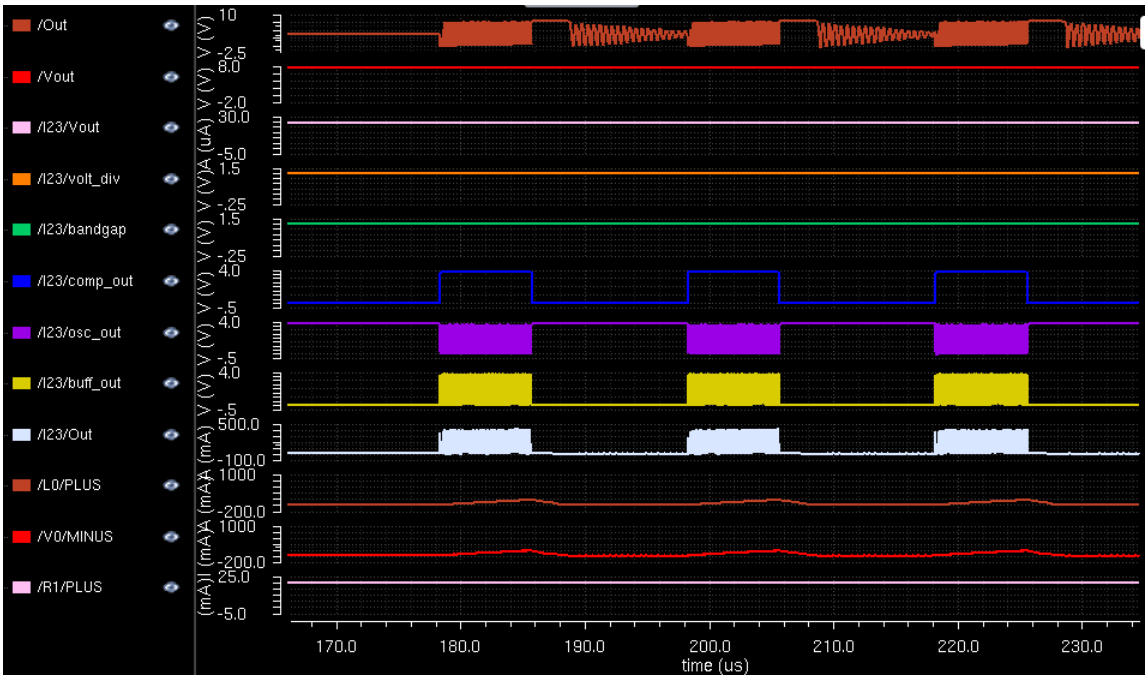


Simulation of SPS with Off-Chip components

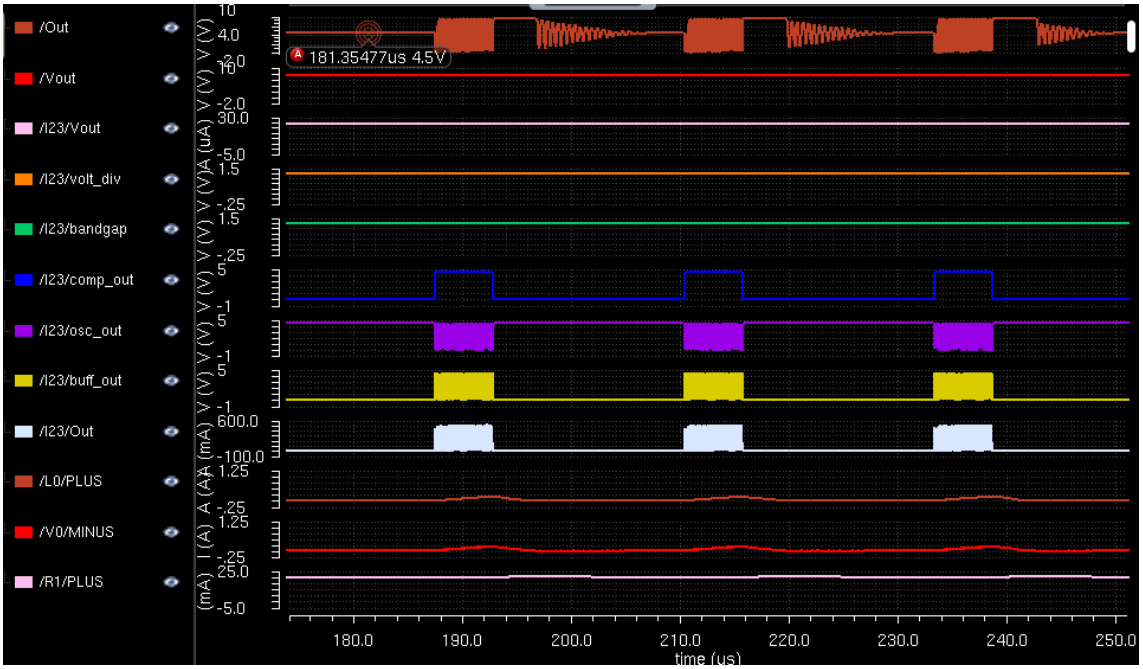


Schematic Simulations:

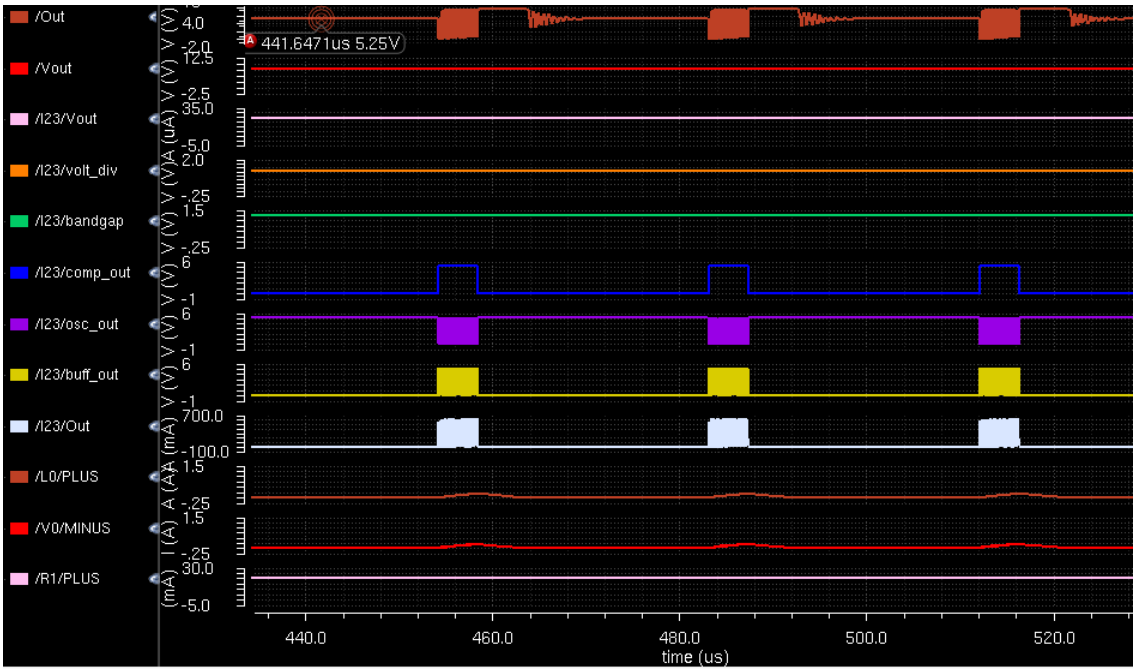
Transient Simulation at 3.75V:



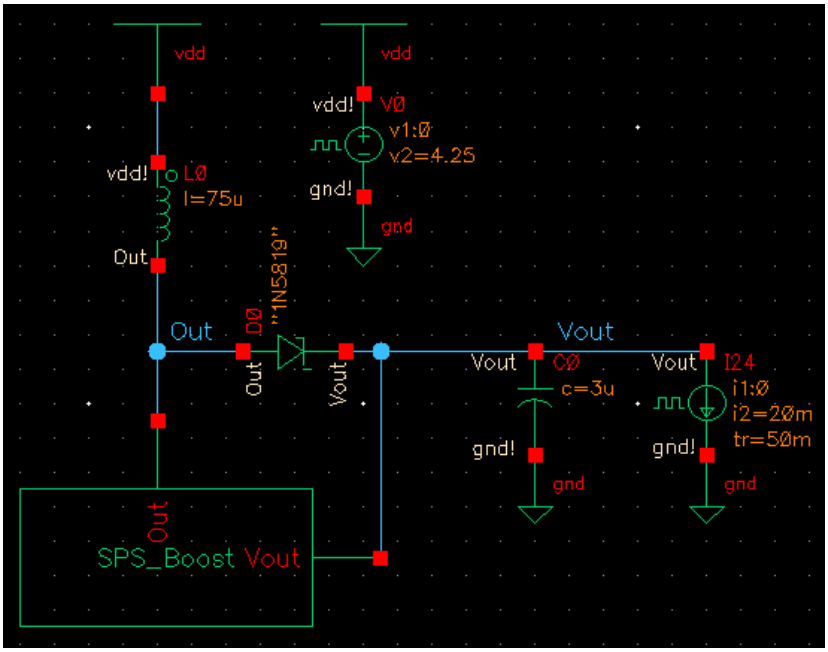
Transient Simulation at 4.5V:



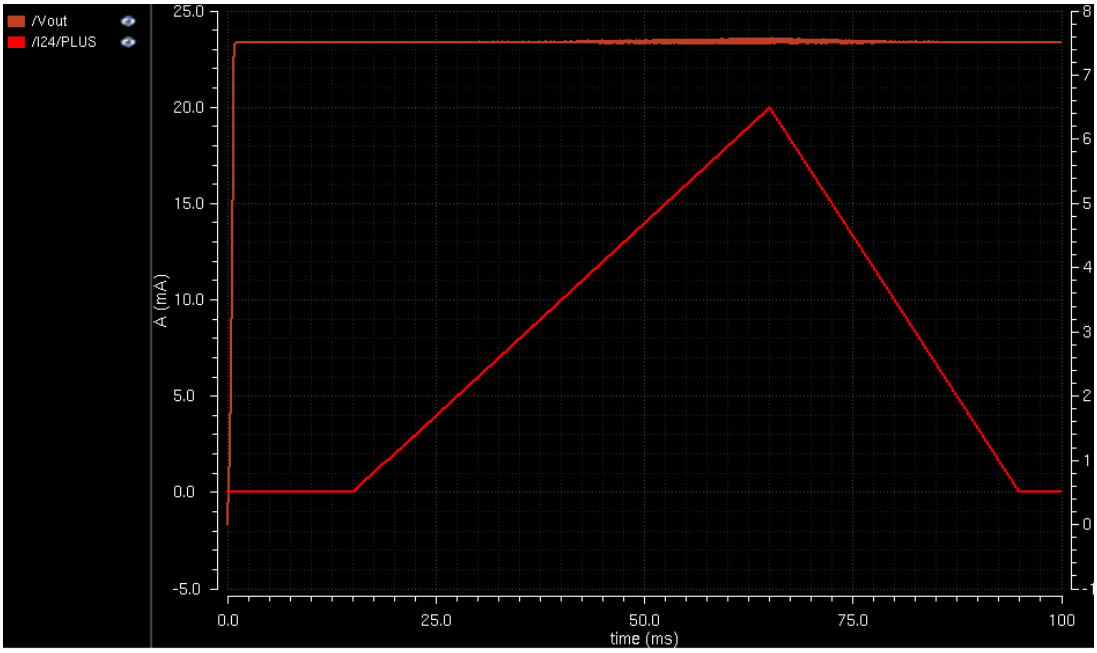
Transient Simulation at 5.25V:



Load Current Simulation over a 100ms period (4-hour simulation):

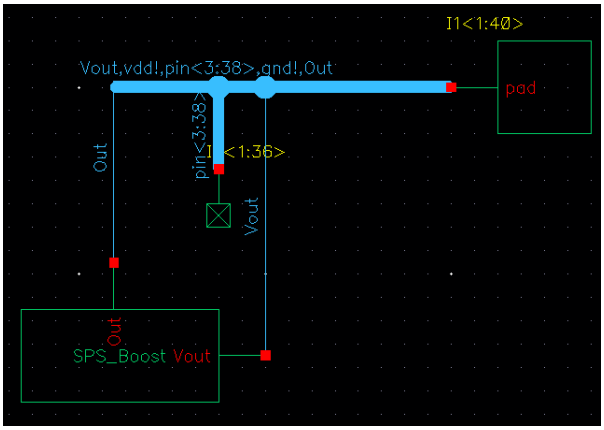


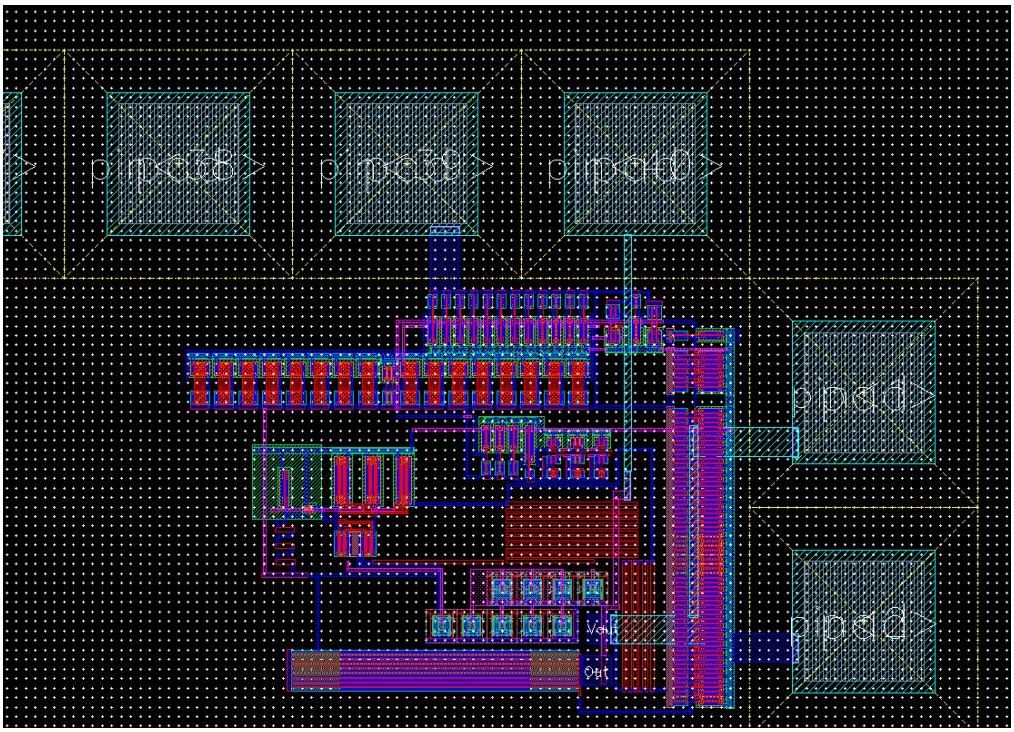
Ran a current load of 0A to 20A across the circuit with a delay time of 15ms, a rise time of 50ms, and a fall time of 30ms. The transient ran for 100ms. A shorter time could have been chosen, but it was necessary to run the current over a long period so as to see the various changes the current has overtime.



Padframe Schematic and Layout:

For the layout, I chose to have a number convention that started from the top of the right side pins and count clockwise. I connected Vout to pad<1>, V_{DD} to pad<2>, gnd to pad<39>, and Out to pad<40>. The reason I chose to designate the pads this way was to keep vdd and gnd a distance away from each other to minimalize the risk of user error shorting the two together.



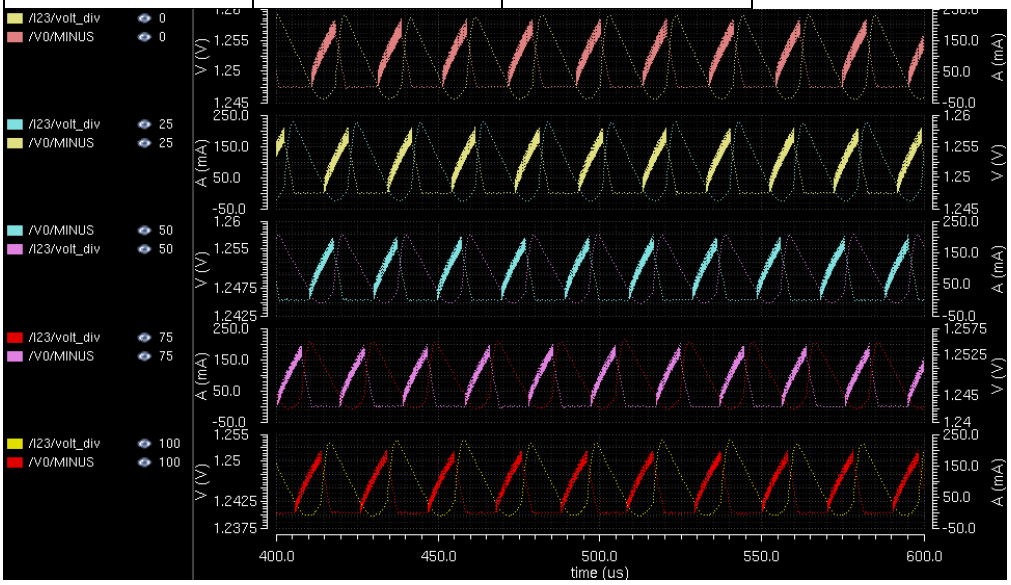


Efficiency and Temperature Calculations

VDD at 3.75V:

$$E = \frac{7.5 * 20mA}{3.75 * \ Avg(I(VDD))}$$

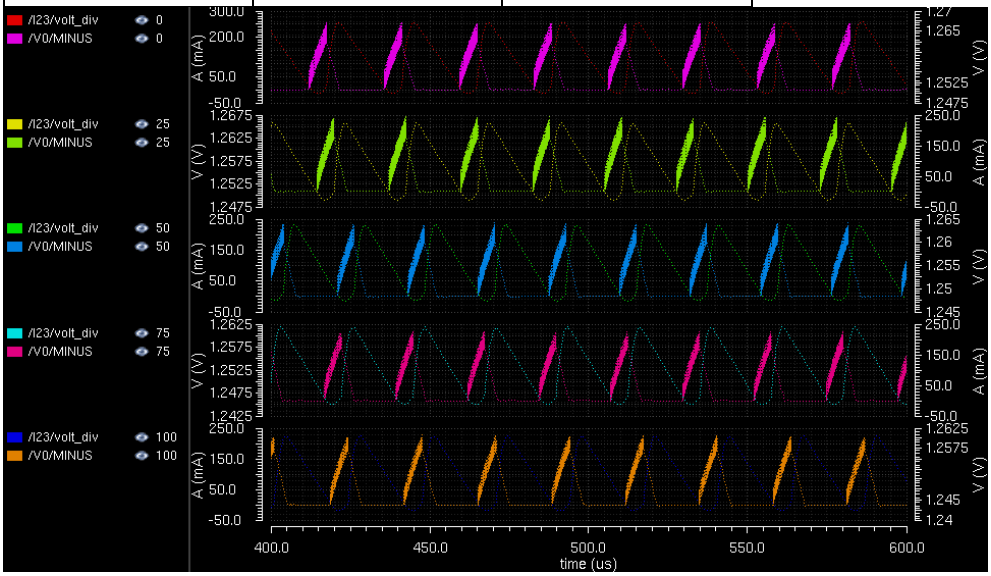
Temperature	Avg($I(V_{DD})$)	Efficiency
0	45.27mA	88.35%
25	48.66mA	82.20%
50	46.31mA	86.37%
75	47.48mA	84.25%
100	49.56mA	80.71%



VDD at 4.5V:

$$E = \frac{7.5 * 20mA}{4.5 * \ Avg(I(VDD))}$$

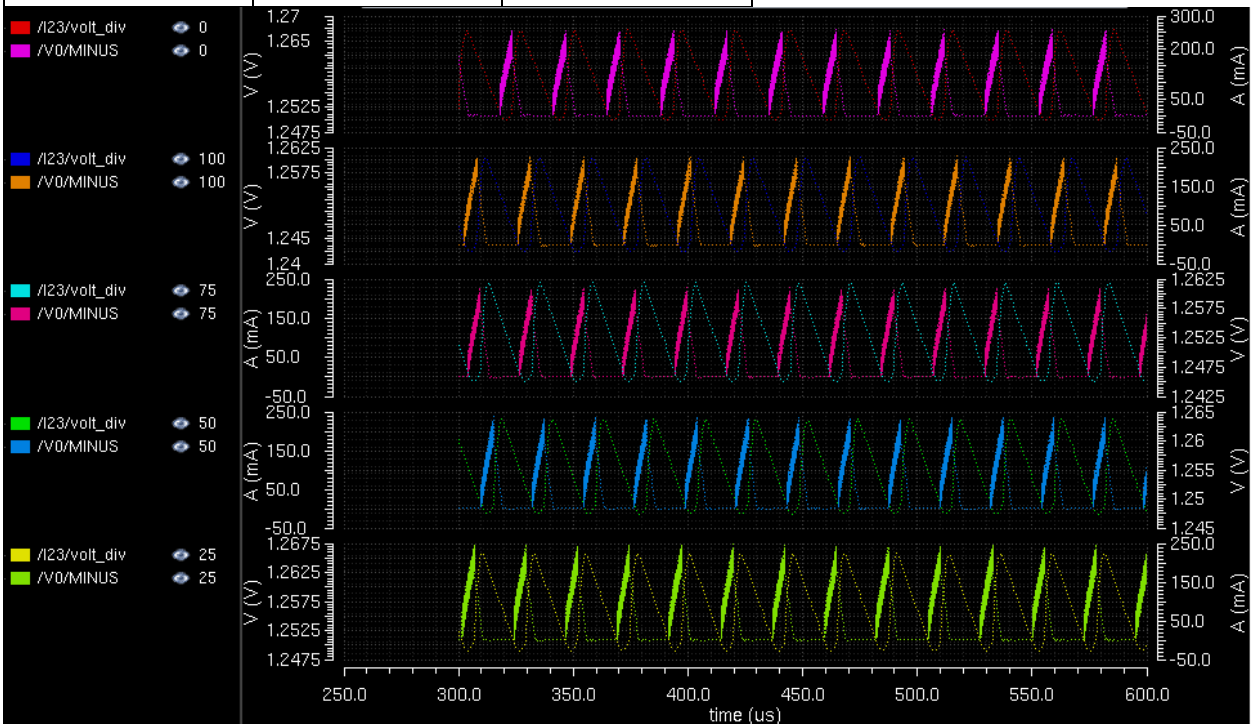
Temperature	Avg($I(V_{DD})$)	Efficiency
0	46.92mA	85.25%
25	47.83mA	83.63%
50	48.31mA	82.80%
75	48.50mA	82.47%
100	49.41mA	80.96%



VDD at 5.25V:

$$E = \frac{7.5 * 20mA}{5.25 * \ Avg(I(VDD))}$$

Temperature	Avg(I(V_{DD}))	Efficiency
0	47.52mA	84.18%
25	48.66mA	82.20%
50	49.07mA	81.52%
75	49.95mA	80.08%
100	50.38mA	79.40%



Conclusion:

Problems Encountered:

The greatest challenge I encountered with this project was the creation of the ring oscillator. At first, I had made a ring oscillator with a frequency of approximately 50% duty cycle. The circuit worked around this frequency until I needed to modify it so the duty cycle would be great enough to allow the NMOS to close for longer periods. However, even after doing so, a lot of debugging had to be done as the output signal was going high instead of low when the enable was low. This was fixed by implementing a second NAND gate into the ring oscillator's design. The ring oscillator was modified several times even after the final layout had been created causing several pauses in progress to fix the issue.

Potential Future Improvements:

A strikingly obvious improvement I could make is decreasing the frequency of the ring oscillator. This would greatly increase the efficiency of the circuit. Additionally, I could look more into finding an optimal balance between the capacitance and resistance in my NMOS switch. While a 10ohm resistance makes it a fast switch, 1.2pF is notorious for an internal capacitance size. On top of these improvements, I would investigate choosing an inductor and capacitor value that is most optimal for the frequency I set from the improved ring oscillator.