1 Design Summary

The design requirements for PWM filter are as follows:

- Input: 3.3 Vpp square wave to simulate 50% duty cycle PWM
- Filter output: DC with 12-bit resolution (Maximum ripple: 403uVpp)

The design requirements for Post Amp are as follows:

- Supply Voltage: ±15 V dc (for post amplifier)
- Post amplifier gain: 1024 V/V, ac coupled

The design goals and performance for 12bit, system resolution are summarized in **Table 1**. **Figure 1** depicts the measured ripple for 12bit system resolution with 1024 times gain of the RC low pass filter design.

Table 1: Comparison of Design Goals, Simulated Performance, and Measured Results

System Resolution	Goal Max Ripple	Simulated Ideal Components	Measured Results
12bit (filter out)	403uVpp	344.48uVpp	347.66uVpp
12bit (post amp out)	412mVpp	396mVpp	404mVpp

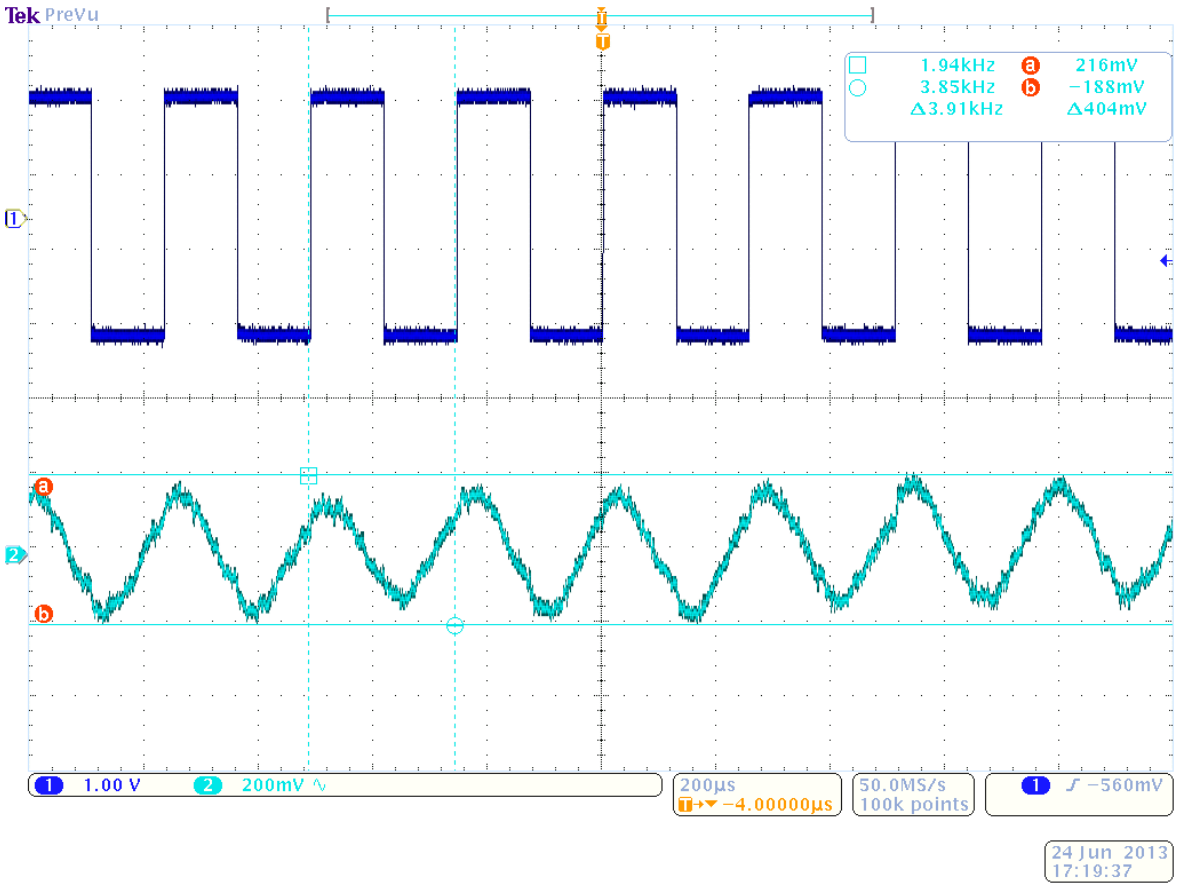

Figure 1: PWM Output Ripple Verification for 12 bit System (Gain = 1024V/V)

2 Theory of Operation

2.1 Design Overview

Pulse Width Modulation (PWM) is a technique where the width of digital pulses is adjusted to generate different average dc voltages. Most microcontrollers have a built-in timer that can be used to generate a PWM signal. PWM outputs can be converted to a dc voltage by using a series of RC low pass filters to average the pulses. Thus, a filtered PWM circuit is a simple low cost method to convert digital to analog (i.e. create a DAC). The main goal of this design is to convert PWM to analog output and achieve a 12 bit resolution with a ripple signal less than one half LSB. A secondary goal is to develop a circuit that amplifies the output ripple (error) to a level that an oscilloscope can measure. A system block diagram is shown in Figure 2.

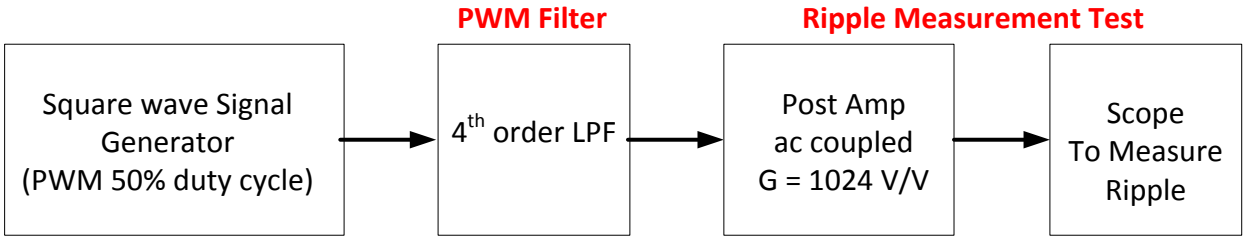

Figure 2: System block diagram

The PWM output from a microcontroller is a square wave that has a programmable pulse width (duty cycle). The output of a simple RC filter connected to the PWM output will charge to the average voltage of the PWM signal. **Figure 3** shows a 10% and 90% duty cycle PWM signal connected to a simple RC filter. Note that the output charges to approximately 90% of the square wave's amplitude for a 90% duty cycle. In general, the ideal average dc output is PWM amplitude multiplied by the duty cycle (i.e. Vout = V_{PWM} x Duty_Cycle). The charge and discharge of the filter capacitor can also be seen in **Figure 3**. The peak-to-peak amplitude of the variations caused by the charge and discharge of the filter capacitor is called the ripple. The objective is to convert the PWM signal to a dc voltage so ideally the ripple would be zero. The results shown in **Figure 3** are for a single pole RC filter; adding additional filter stages will further minimize the ripple. The ripple can be thought of as an error that limits the resolution of the signal. As a rule of thumb the ripple should be kept to half the voltage resolution. To achieve our resolution objective (12 bits) we will have to determine the number of filter stages and the cutoff frequency required to reduce the ripple to half of the voltage resolution.

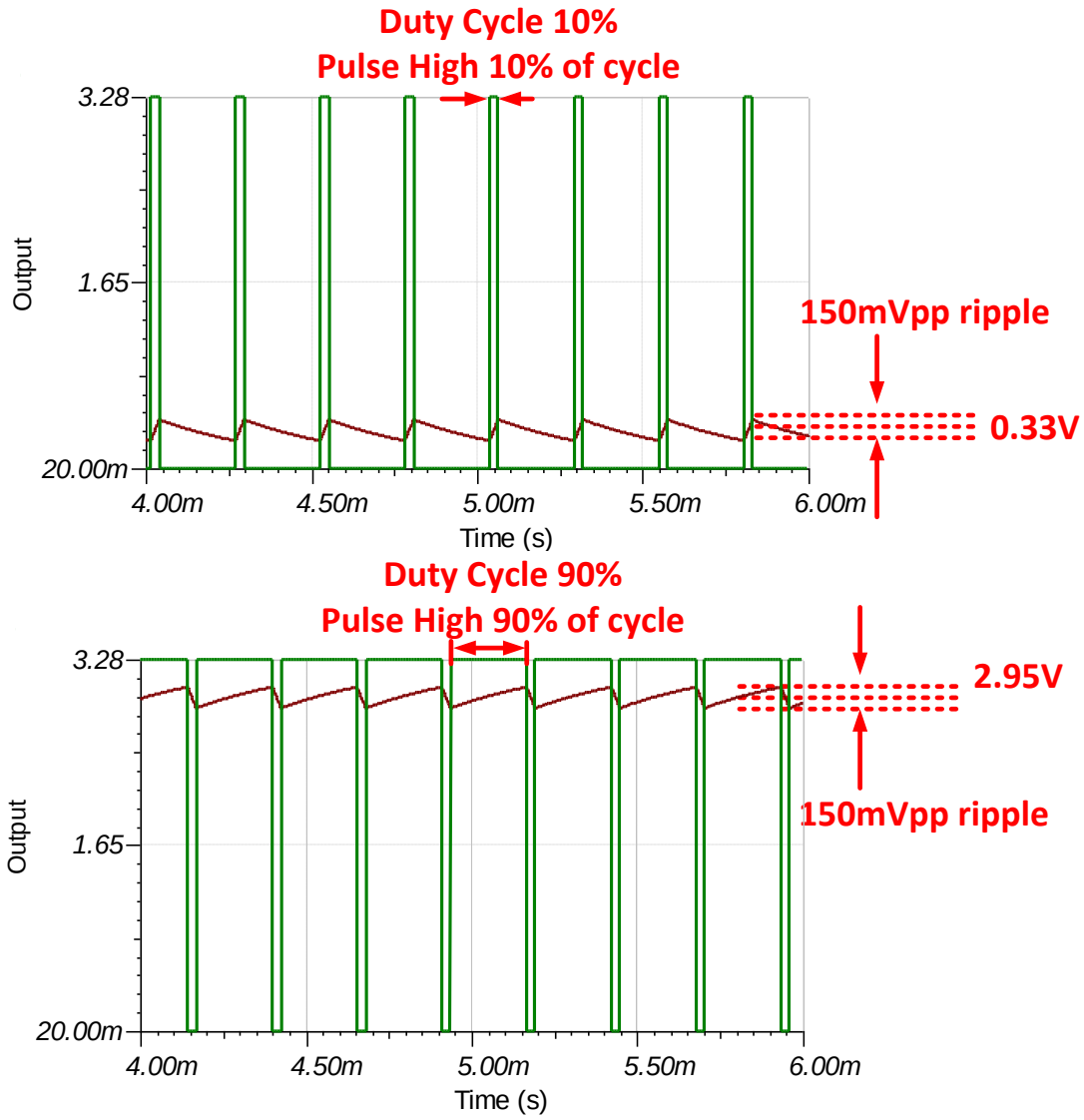

Figure 3: PWM Signal and dc Output for 10% and 90% Duty Cycle

Another factor that controls the resolution is the degree by which the width of the PWM signal can be adjusted. A common method for generating PWM signals it to use a binary counter. **Figure 4** shows the generation of two different PWM signals with an 8 bit counter. The counter output remains high until the desired duty cycle is met and then it is reset. The MSP430 microcontroller uses this principle with a 16 bit counter. The number of bits in the counter corresponds to the bits of resolution in the analog output if the signal is properly filtered. For this design our goal is 12 bit resolution, so a 12 bit counter is needed to achieve 12 bits of resolution. Later in this document we will discuss the trade-offs associated with higher resolution systems.

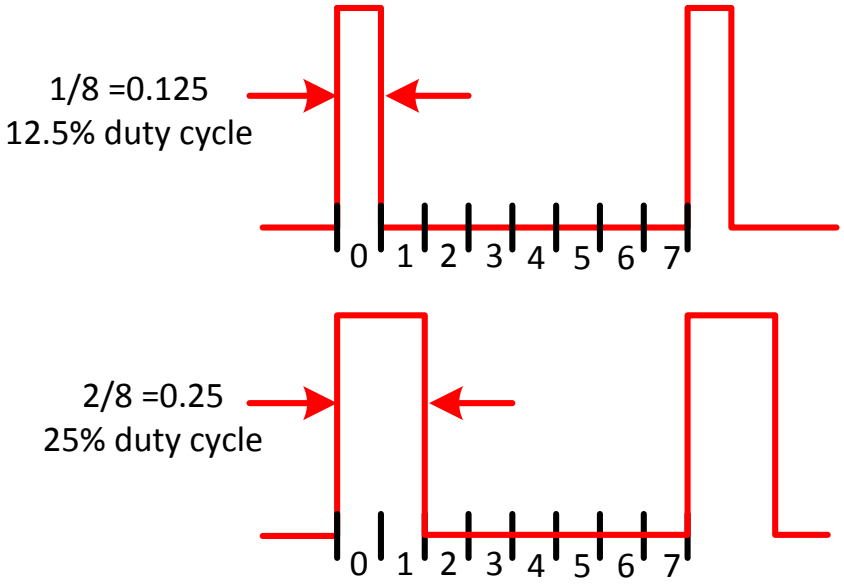

Figure 4: PWM for an 8 Bit Counter

Figure 5 illustrates the PWM (counter) output on the MSP430. In this figure the full 16 bit (i.e. 65,536) counter is being used. In **Figure 5** the PWM output is configured for the minimum duty cycle (i.e. 1 count in 65,536 or 0.00153% duty cycle). The period of one count is 62.5ns for the MSP430 at a master clock frequency of 16MHz. The period of the entire 16 bit clock cycle is 4.096ms (62.5 ns x 65536). The PWM frequency is 244Hz (T_{PWM_Cycle} = 4.096ms).

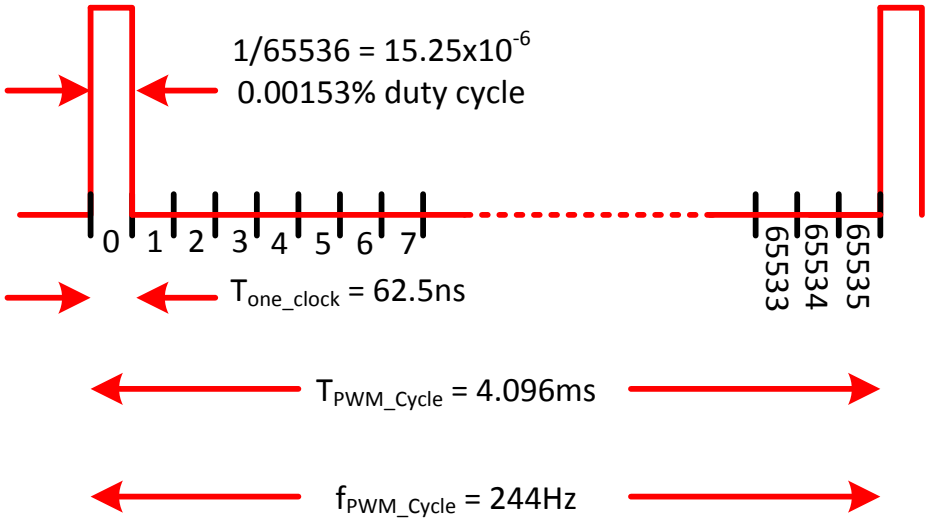

Figure 5: PWM for a 16 bit Counter (Frequency, Period, and Duty Cycle shown)

In the case of this design our resolution objective is 12 bits, so we only need 12 bits of the 16 bit counter in the MSP430. **Figure 6** shows the PWM signal where the counter is reset after 12 bits. The resolution is now 1/4096 or a 0.0244% duty cycle. Limiting the counter to 12 bits also affects the period and frequency of the PWM signal. The frequency of the 12 bit PWM signal is 3.91kHz which is substantially higher than the 16 bit PWM frequency (244Hz). The PWM frequency is the frequency by which analog output can be adjusted. The PWM frequency also determines the cutoff frequency of the filter.

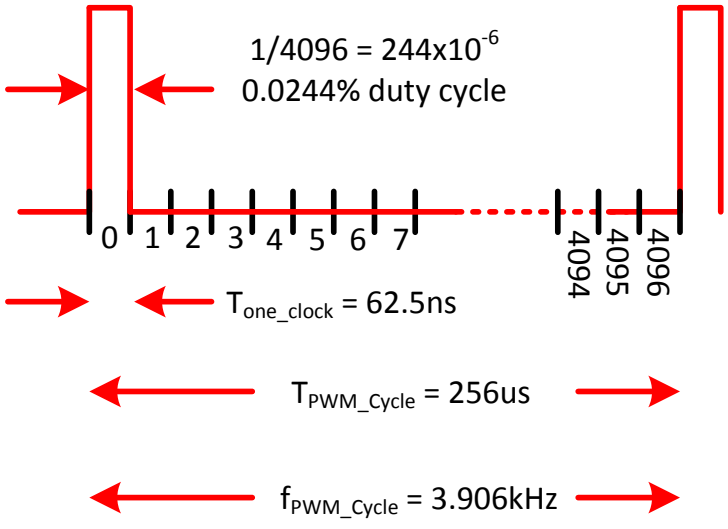

Figure 6: PWM for a 12 bit Counter (Frequency, Period, and Duty Cycle shown)