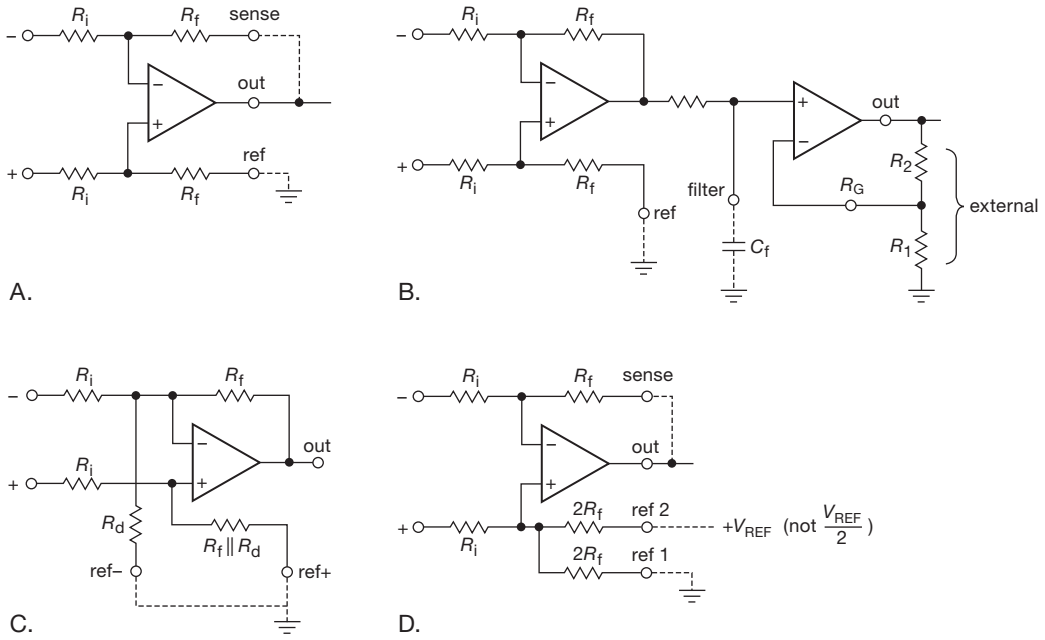

Figure 5.75. Circuit configurations for the difference amplifiers in Table 5.7 on page 353 (identified in the "Config" column). The "E" form is shown in Figure 5.89. The "C" form is used for high voltages (e.g., ±270 V for the AD629B).

C. CMRR trim

Likewise, you can trim out residual CMRR (caused by slight mismatch of resistor ratios R_f/R_i in the two paths) with the circuit of Figure 5.74B. It's important to limit the trim range, to permit an accurate and stable trim to something considerably better than the off-the-shelf 80 dB (worst-case) CMRR specification. You can't get any old value of trimmer, and it's best not to use values less than 100 Ω (even if you can find them) if you care about stability. Here we've chosen standard resistor values and a 100 Ω trimmer to produce a resistance range of 20–30 Ω from the REF terminal to ground, providing a ±5 Ω symmetrical variation around R_1. For the 25k resistor values of this unity-gain difference amplifier (rather typical; see Table 5.7 on page 353), this corresponds to a trim range adequate to null an initial CMRR of 75 dB. You can, of course, add an offset null to this circuit, as indicated.

D. Single-supply offset

One of the difference amplifiers in Table 5.7 (page 353) helpfully splits the reference feedback resistor into a parallel pair (Figure 5.75D), so it's easy to offset the output voltage range. For example, you could run the amplifier on a single +5 V supply, with REF2 driven from a clean reference of that same voltage. With no difference signal the output will be +2.5 V. The amplifier can accommodate input signals over a ±10 V range, and its gain of 0.2 takes a ±10 V differential input to a 0–4 V output. You can, of course, use a lower reference voltage. It's often convenient to use $V_{ref} = 4.096$ V when driving an ADC; this makes the step size come out in round numbers, e.g., 1 mV/step for a 12-bit conversion.

5.15 Instrumentation amplifier

The difference amplifiers of the previous section are inexpensive, and fine for many applications; and they have the nice feature of accepting inputs beyond the rails. But they have limited gain ($\leq$10) and CMRR ($\lesssim$85 dB min), their resistors make them somewhat noisy (20 nV/$\sqrt{\text{Hz}}$ to 50 nV/$\sqrt{\text{Hz}}$), and their relatively low input resistance ($\sim$10k to $\sim$100k) limits their utility to situations where the driving signals are of low impedance (op-amp outputs, low-Z balanced lines, low-R sense resistors).

If you need lots of gain, or a high input impedance, or superior CMRR, you need something different. It's called an *instrumentation amplifier*. These impressive devices have input impedances upward of 10^9 Ω, gains from unity to 1000 or so, low voltage noise (down to $\sim$1 nV/$\sqrt{\text{Hz}}$), and worst-case CMRRs of 100–120 dB (look ahead to Table 5.8 on page 363).

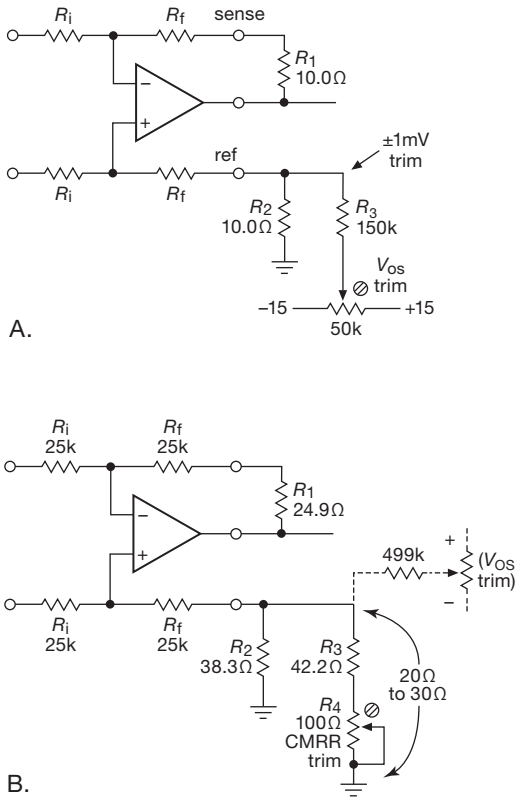

Figure 5.74. Trimming the offset and CMRR of a difference amplifier.

5.15.1 A first (but naive) guess

High input impedance – that's easy, just add op-amp followers to the difference amplifier (Figure 5.76); and then the resistors R_i and R_f can be smaller, reducing their Johnson noise contribution.

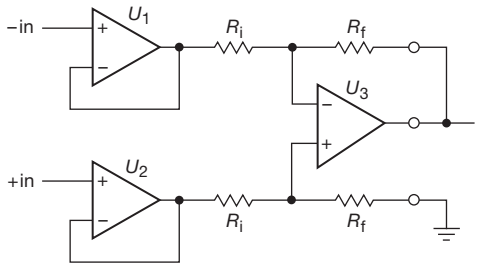

Figure 5.76. A first stab at improving the difference amplifier.

Indeed, this circuit has the enormous input impedance we expect from an op-amp follower, so there is no longer a problem from any reasonable source impedance.[70] But it does not improve the CMRR, which is still limited by the resistor ratio matching of R_f/R_i: it's really hard to do better than 100,000:1 with on-chip laser trimming (both initial trim and stability with time and temperature). In fact, this circuit degrades the CMRR somewhat, with two more amplifiers in the signal path.

5.15.2 Classic three-op-amp instrumentation amplifier

The circuit in Figure 5.77 is much better. It is the standard "three-op-amp instrumentation amplifier," one of several configurations that provide the desirable combination of high CMRR, high R_{in}, low e_n, and plenty of gain when you need it. The input stage is a clever configuration of two op-amps that provides high differential gain and unity common-mode gain without requiring close resistor matching. Its differential output represents a signal with substantial reduction in the comparative common-mode signal (when configured for $G_{diff} \gg 1$), and it is used to drive a conventional differential amplifier circuit. The latter is usually arranged for unity gain and is used to generate a single-ended output while removing the common-mode signal.

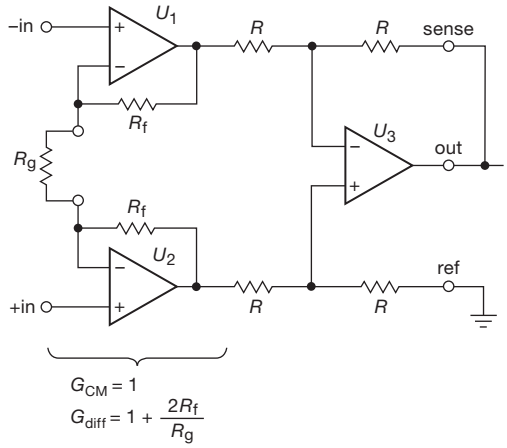

Figure 5.77. The classic three-op-amp instrumentation amplifier.

It's worth looking more closely at this circuit. We've hinted that it can deliver very high CMRR and very low e_n. But that is true *only when configured for large differential*

[70] At least at dc. At higher frequencies it again becomes important to have matched source impedances relative to the common-mode signal, because the input capacitance of the circuit forms a voltage divider in combination with the source resistance. "High frequencies" may even mean 60 Hz and its harmonics, because common-mode ac powerline pickup is a common nuisance.

gain. To see why, imagine we configure it for $G_{\rm diff} = 1$, by omitting the gain-setting resistor $R_{\rm g}$. Then we've just got the previous circuit (Figure 5.76), i.e., a buffered unity-gain difference amplifier. It has the same limitations of CMRR (set by resistor matching) and noise (from U_3's resistors).

Now imagine we set $G_{\rm diff} = 100$. We would do this by choosing $R_{\rm g}$ so that $1 + 2R_{\rm f}/R_{\rm g} = 100$, i.e., $R_{\rm g} = 2R_{\rm f}/(G-1)$. For the INA103, for example, $R_{\rm f} = 3\,{\rm k}\Omega$, so we'd use $R_{\rm g} = 60.6\,\Omega$. The INA103 conveniently includes a resistor of that value,[71] so for $G_{\rm diff} = 100$ you need only tie a pair of pins together. Let's look again at the CMRR and noise scene.

First, the CMRR: the front end has a differential gain of 100 and a common-mode gain of unity. In other words, it passes on to the difference amplifier stage a signal that has received 40 dB of CMRR blessings. Another 80 dB of CMRR in the output stage, and we've got the promised 120 dB CMRR. These numbers are typical of available instrumentation amplifiers, as listed in Table 5.8 (page 363) and graphed in Figure 5.82. For the INA103, for example, the datasheet lists CMRR=86 dB/72 dB (typ/min) for $G = 1$, and 125 dB/100 dB (typ/min) for $G = 100$.

Second, the noise voltage: the output stage still contributes Johnson noise from its resistor array, along with noise inherent in its amplifier. That cannot be helped. But that noise is combined with the *already-amplified* input signal, so the effect, *relative to the input signal* (RTI), is $100\times$ less. For the INA103, for example, the datasheet lists the noise density (typical, at 1 kHz) as $e_{\rm n}$=65 nV/$\sqrt{\rm Hz}$ for $G = 1$ and 1.6 nV/$\sqrt{\rm Hz}$ for $G = 100$.[72]

5.15.3 Input-stage considerations

Several preliminary comments here on the all-important input stage (about which a well-known circuit guru remarked "instrumentation amplifiers are all about their inputs"), with more to come later in §5.16.

A. Resistor matching

The circuit looks handsome with its symmetrical matched $R_{\rm f}$'s, but that requirement did not intrude in the discussion above. What is the effect of mismatched feedback resistors in the first stage? The common-mode gain remains unity (if you tie both inputs together, both outputs follow); and the differential gain expression is the same as before, but with $2R_{\rm f}$ not surprisingly replaced with the sum $R_{\rm f1} + R_{\rm f2}$. What changes, though, is that a purely differential input causes a differential output (amplified by $G_{\rm diff}$, as before) combined with some common-mode output.

You can see how this goes by imagining that U_2's feedback resistor is replaced with a short and U_1's resistor with $2R_{\rm f}$, and a symmetrical dc input signal $\pm\Delta V$ is applied to the inputs: U_2's output goes down ΔV, while U_1's goes up $(1 + 4R_{\rm f}/R_{\rm g})\Delta V$. That's the correct differential output, but with a common-mode offset of $(2R_{\rm f}/R_{\rm g})\Delta V$. This is not of great concern, providing that the $R_{\rm f}$'s are reasonably matched; they do not require the precise matching needed for the output stage.

B. The input amplifiers

It is essential that U_1 and U_2 have excellent CMRRs in order that a purely common-mode input signal is not converted to a differential signal (which would then be passed on to the output). Stated more precisely, they must have *matched* CMRRs, so that the voltage across $R_{\rm g}$ accurately tracks the differential input voltage. Viewing the circuit operation more generally in this light, the input amplifiers need not have extremely low individual offset voltages – what matters is that their offset voltages are accurately *matched* and remain so with changes in common-mode voltage. This gives rise to several circuit variants in which the "op-amps" U_1 and U_2 are configurations with well-matched base–emitter drops between each input and the corresponding $R_{\rm g}$ pin; see for example Figure 5.88C below.

C. Input-stage overload

The input stage amplifiers U_1 and U_2 will clip if their outputs are forced close to their supply rails, even though the output of the full circuit (U_3's output) would be expected to stay within safe bounds. Put another way, $V_{\rm CM} \pm 0.5V_{\rm diff}(1 + 2R_{\rm f}/R_{\rm g})$ must not reach either supply rail.

D. Signal guards

Instrumentation amplifiers are used with low-level signals, often conveyed by shielded cables to minimize noise. This adds input capacitance, thereby limiting the bandwidth (particularly with signals of moderate to high source impedance). Of perhaps greater importance, it degrades the CMRR at signal frequencies: the cable's shunt capacitance forms a voltage divider with the signal's source impedance, separately for each input; so if you have a

[71] More precisely, it includes an on-chip resistor, ratio matched to $R_{\rm f}$, to produce an overall guaranteed gain of 100.0±0.25%.

[72] The datasheet separates out the front-end and second-stage contributions, 1 nV/$\sqrt{\rm Hz}$ and 65 nV/$\sqrt{\rm Hz}$, respectively. From these you can calculate the input-referred noise $e_{\rm n}({\rm RTI}) = \left\{e_{\rm n}({\rm in})^2 + [e_{\rm n}({\rm out})/G]^2 + 4kTR_{\rm g}\right\}^{1/2}$. The last term is the square of the Johnson noise voltage $e_{\rm n} = 0.13\sqrt{R_{\rm g}}\,{\rm nV}/\sqrt{\rm Hz}$.