Session





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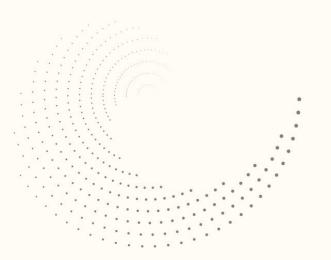
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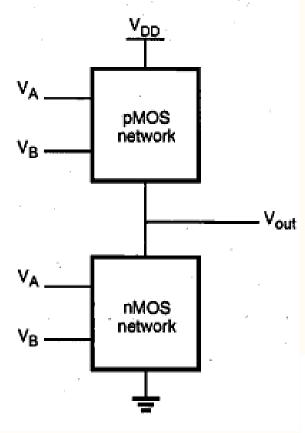
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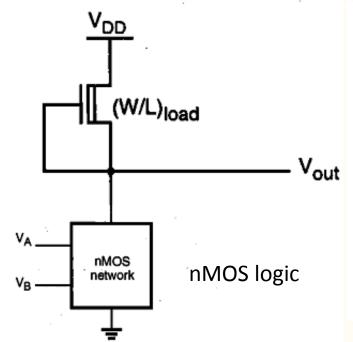
VLSI DESIGN 23EC2211A

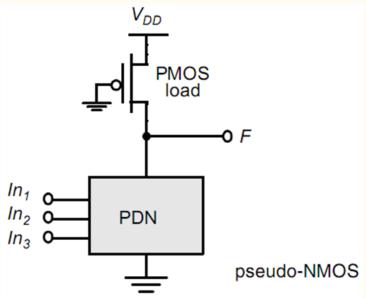
TOPIC CO-3-4-5

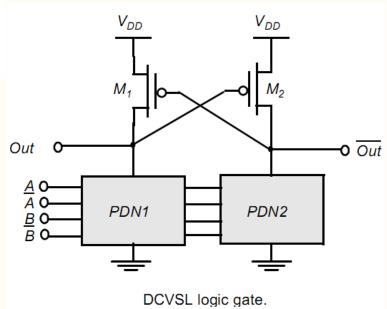


CO-3



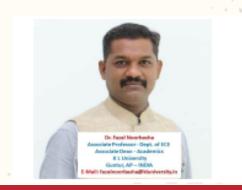






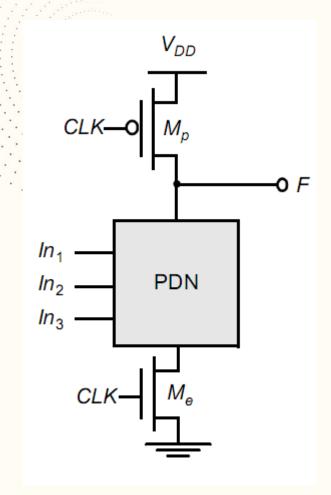
CLK M_p In_1 In_2 In_3 PDN CLK M_e

Dynamic CMOS logic

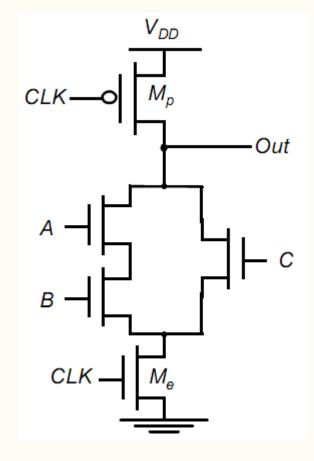


Differential Cascade Voltage Switch Logic (or DCVSL)

Draw and explain Dynamic CMOS Logic using $Y = (\overline{AB + C})$.

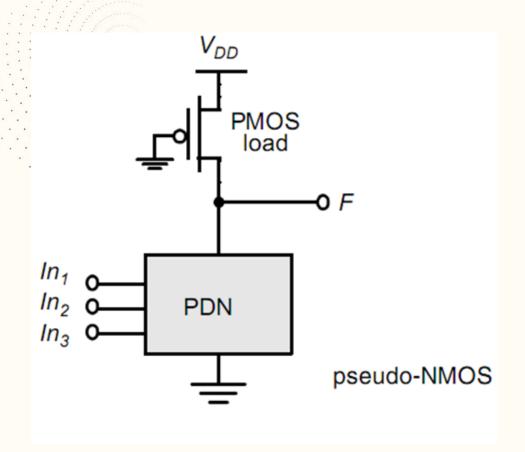


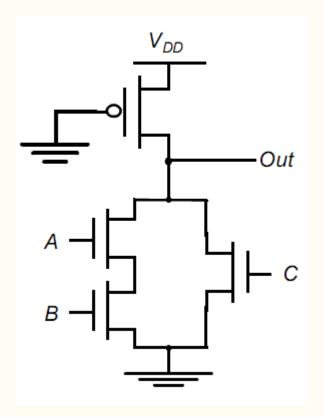
this circuit is divided into two major phases: precharge and evaluation, with the mode of operation determined by the clock signal CLK.





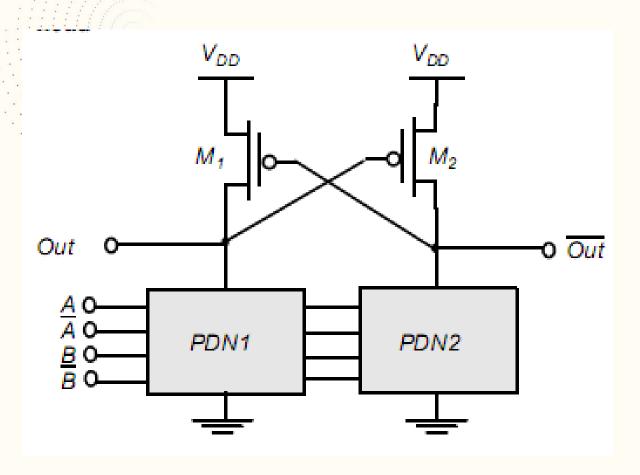
Draw and explain pseudo-NMOS logic using $Y = (\overline{AB + C})$.

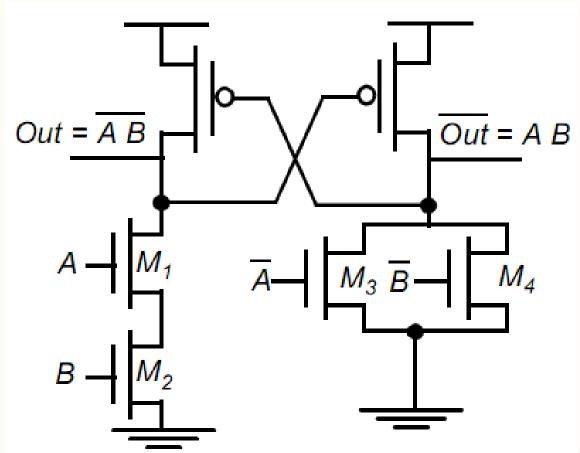




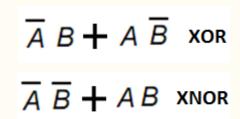


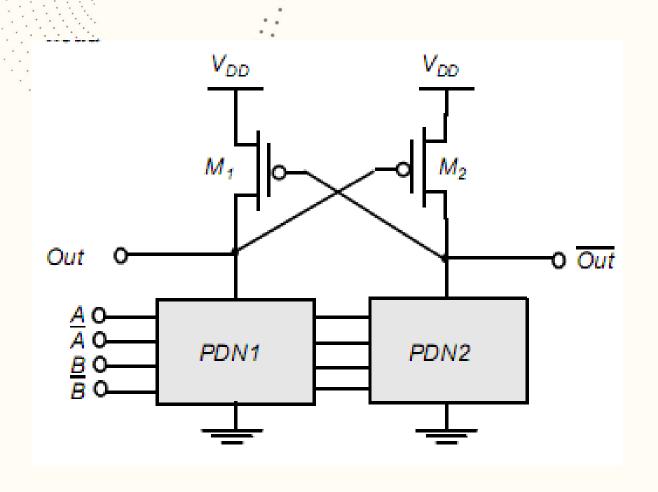
Draw and explain Differential Cascode Voltage Switch logic (DCVSL) using NAND and AND.

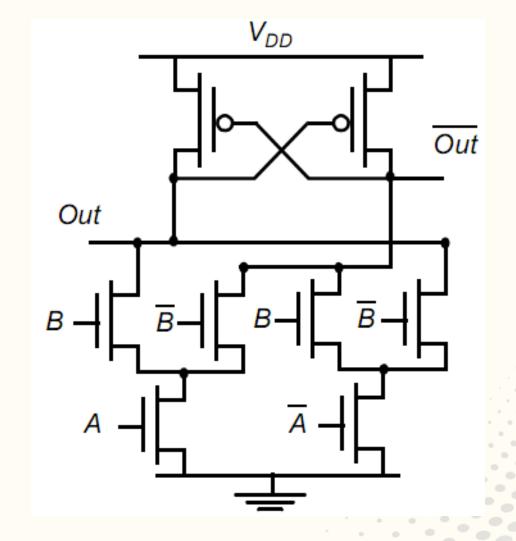




Draw and explain Differential Cascode Voltage Switch logic (DCVSL) using XOR-XNOR.







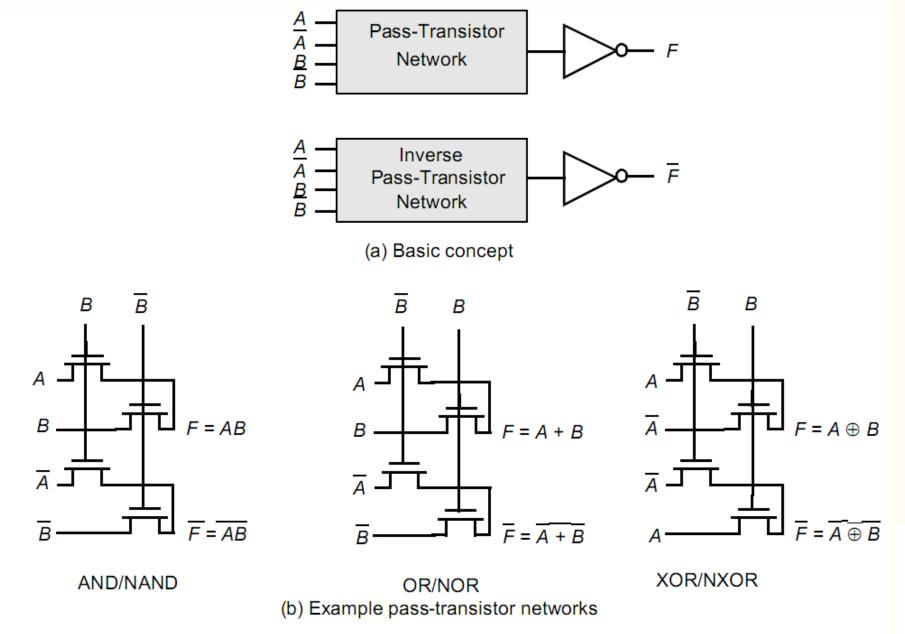
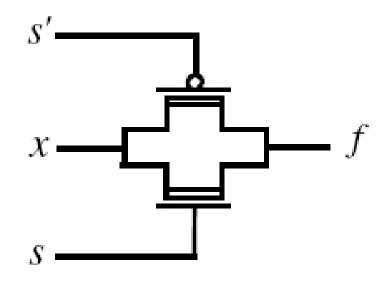


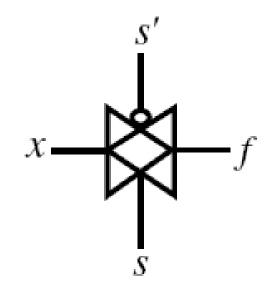
Figure 6.37 Complementary passytransister logic (CPL).



Transmission Logic Circuit

Graphical Symbol

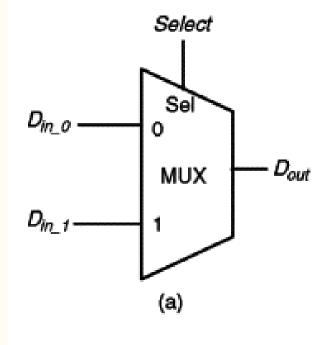


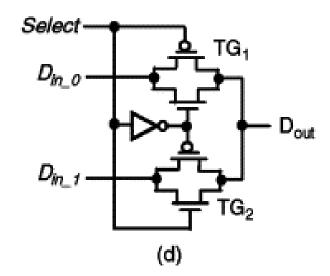




CMOS transmission gate (TG)

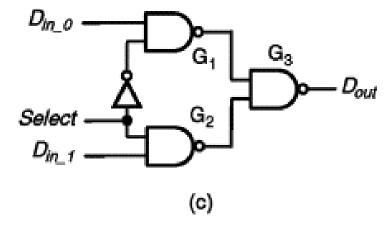


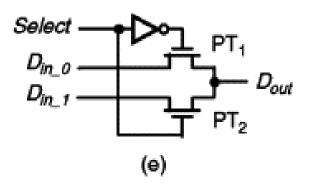




0 <i>D_{in_0}</i>	Select	D _{out}
	0	D _{in_0}
1 D _{in_1}	1	D _{in_1}

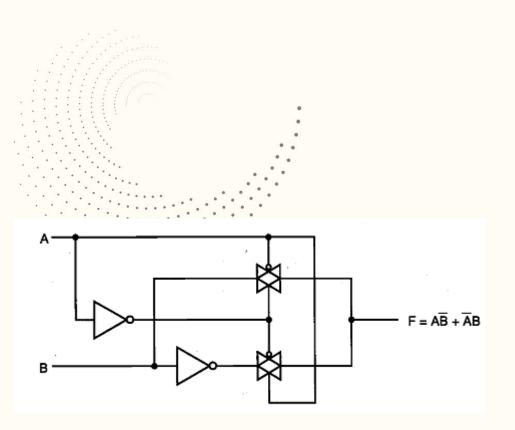
(b)

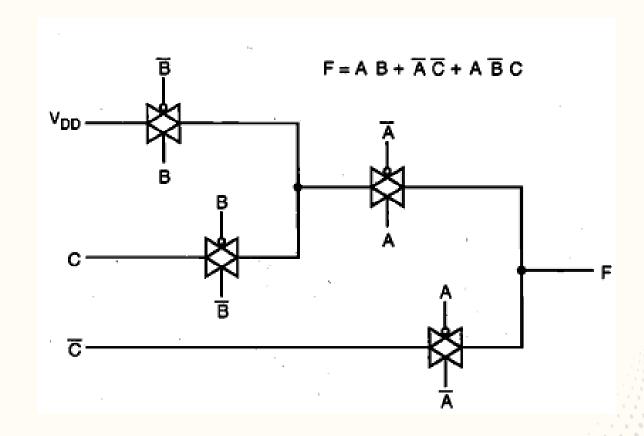














Construct CMOS complex logic circuit for given Boolean function $Y = (\overline{D + E + A})(B + C)$ and find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that (W/L)p = 15 for all pMOS transistors and (W/L)n = 10 for all nMOS transistors.

