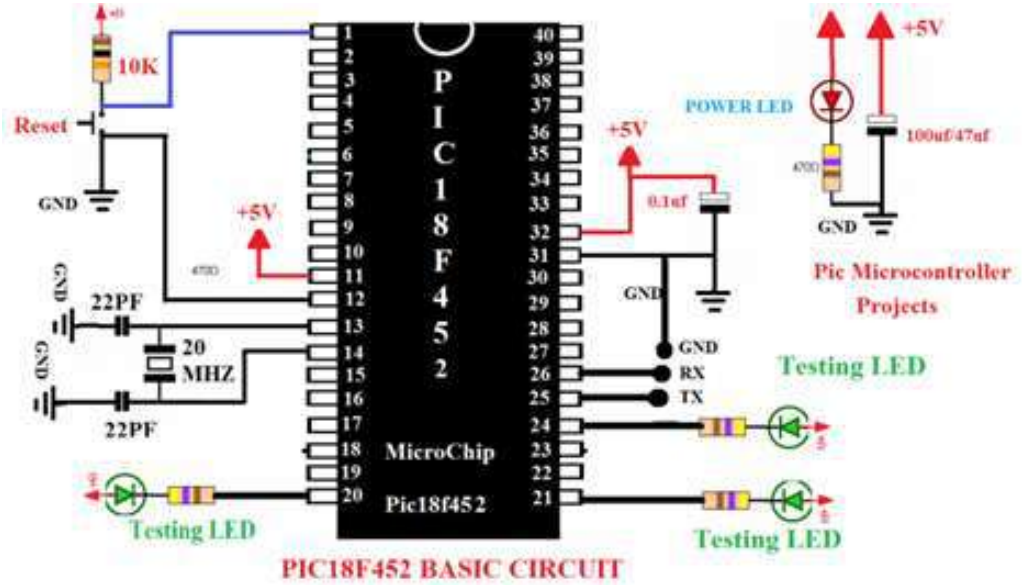
PIC (Peripheral Interface Controller) **Microcontrollers**



PIC18F452 BASIC CIRCUIT

PIC Microcontroller

- PIC microcontroller was developed in the year 1993 by microchip technology.
- The term PIC stands for Peripheral Interface Controller. Initially this was developed for supporting PDP(programmed data processor) computers to control its peripheral devices, and therefore, named as a peripheral interface device.

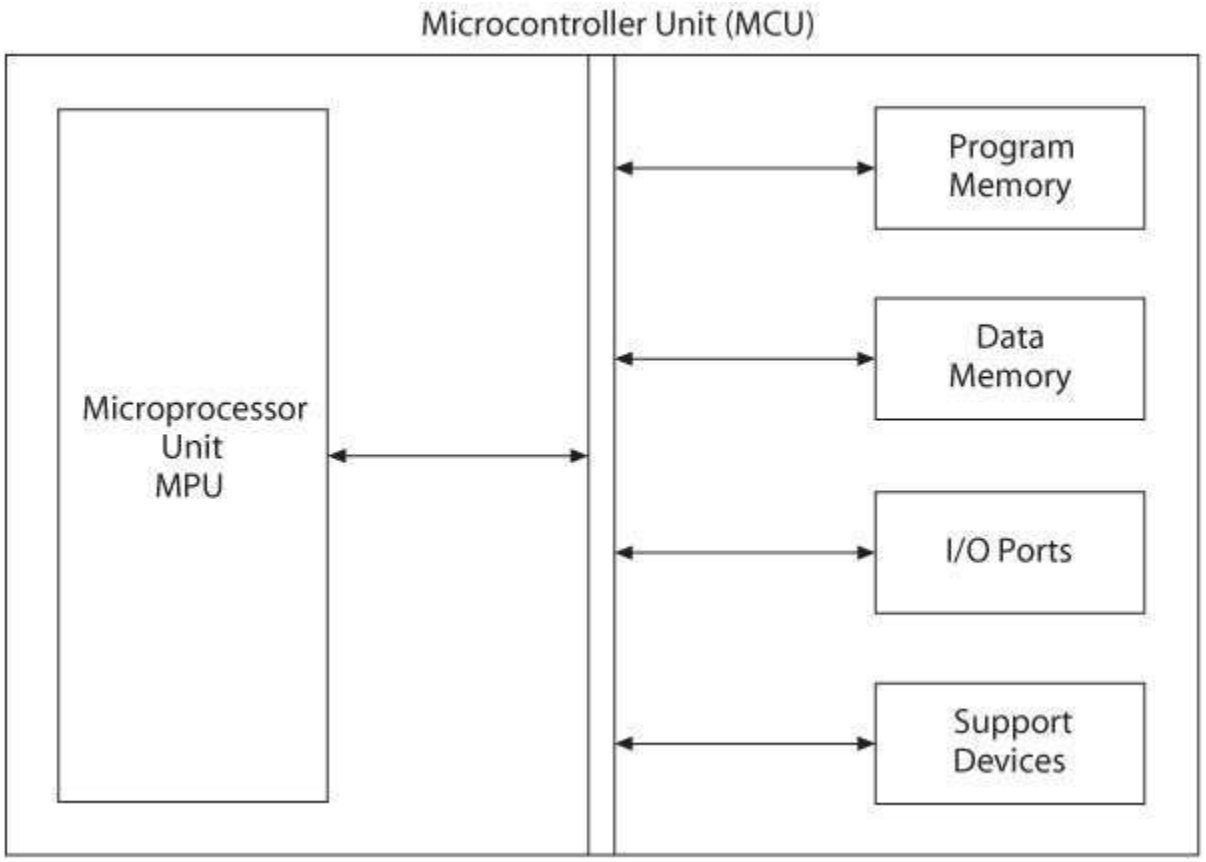
Features of the PIC18 microcontroller

- - 8-bit CPU
- - 2 MB program memory space
- - 256 bytes to 1KB of data EEPROM
- - Up to 3968 bytes of on-chip SRAM
- - 4 KB to 128KB flash program memory
- - Sophisticated timer functions that include: input capture, output compare,
- PWM, real-time interrupt, and watchdog timer
- - Serial communication interfaces: SCI, SPI, I2C, and CAN
- - Background debug mode (BDM)
- - 10-bit A/D converter
- - Memory protection capability
- - Instruction pipelining
- - Operates at up to 40 MHz crystal oscillator

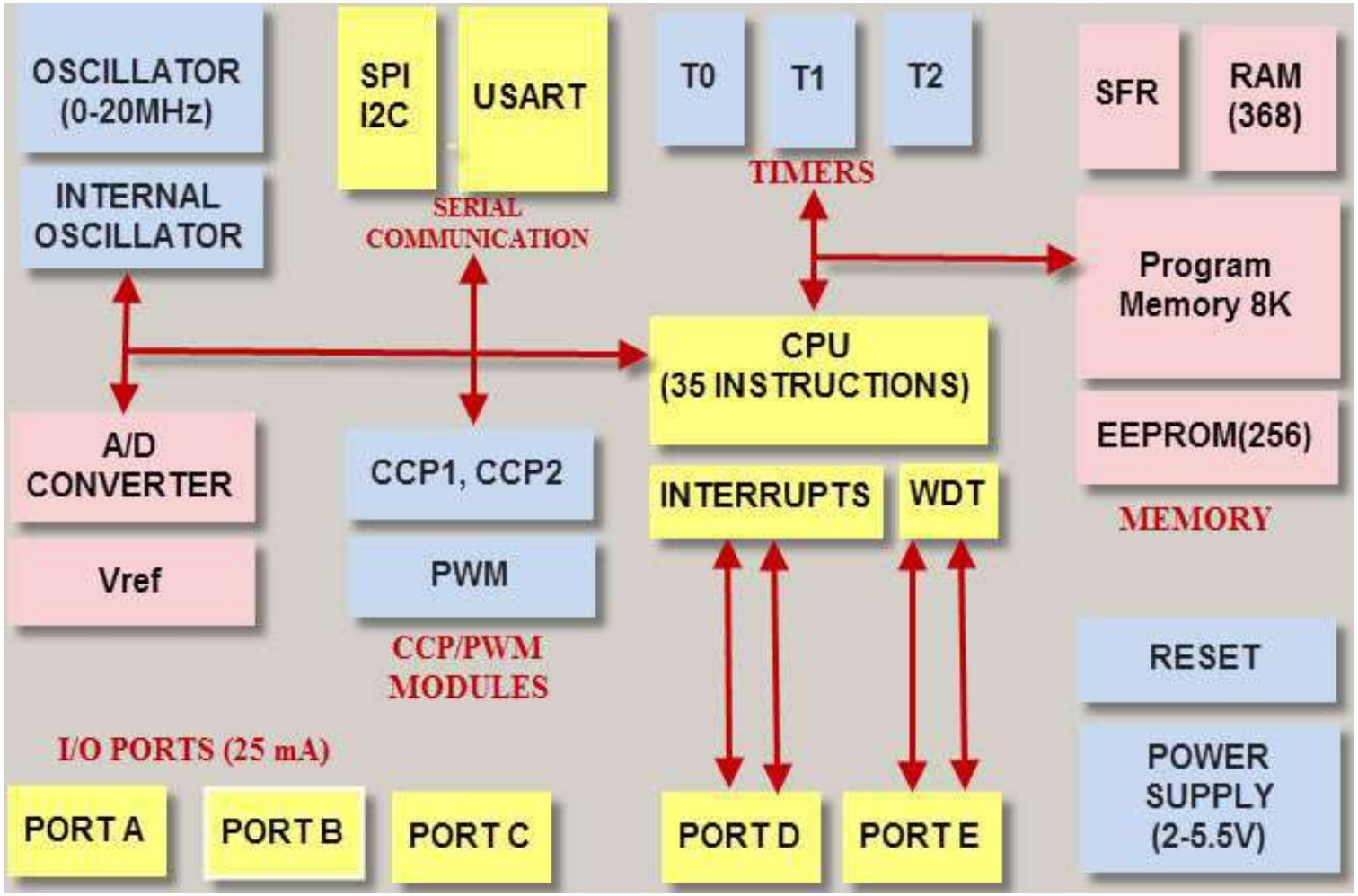
Architecture of PIC18F Microcontrollers

- Microcontroller Unit (MCU)
  - Microprocessor unit (MPU)
  - Harvard Architecture
    - Program memory for instructions
    - Data memory for data
  - I/O ports
  - Support devices such as timers

Microcontroller with the Harvard Architecture



Architecture of PIC Microcontroller



Microprocessor Unit

- Includes Arithmetic Logic Unit (ALU), Registers, and Control Unit
  - Arithmetic Logic Unit (ALU)
    - Instruction decoder
      - 16-bit instructions
    - Status register that stores flags
      - 5-bits
    - WREG – working register
      - 8-bit accumulator

Microprocessor Unit

- Registers
  - Program Counter (PC)
    - 21-bit register that holds the Program Memory address
  - Bank Select Register (BSR)
    - 4-bit register used in direct addressing the Data Memory
  - File Select Registers (FSRs)
    - 12-bit registers used as memory pointers in indirect addressing Data Memory
- Control unit
  - Provides timing and control signals
    - Read and Write operations

PIC18F - Address Buses

- Address bus
  - 21-bit address bus for Program Memory
    - Addressing capacity: 2 MB
  - 12-bit address bus for Data Memory
    - Addressing capacity: 4 KB

Data Bus and Control Signals

- Data bus
  - 16-bit instruction/data bus for Program Memory
  - 8-bit data bus for Data Memory
- Control signals
  - Read and Write

The PIC18 Memory Organization

- Data Memory and Program Memory are separated
- - Separation of data memory and program memory makes possible the
- simultaneous access of data and instruction.
- - Data memory are used as general-purpose registers or special function registers
- - On-chip Data EEPROM are provided in some PIC18 MCUs

PIC18F452/4520 Memory

- Program Memory: 32 K
  - Address range: 000000 to $007FFF_H$
- Data Memory: 4 K
  - Address range: 000 to FFF_H
- Data EEPROM
  - Not part of the data memory space
  - Addressed through special function registers

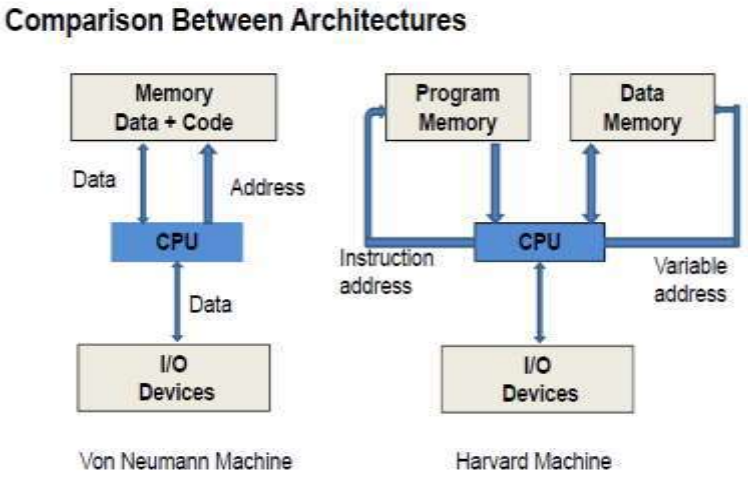
PIC MICROCONTROLLER IN DETAIL

SESSION INTRODUCTION

PIC (Peripheral Interface Controller) Microcontrollers

- As we know, a microcontroller is a combination of processor, memory and peripherals in a single chip. In a similar way PIC(stands for ”Peripheral Interface Controller”), It was created to assist PDP(Pre-programmed Data Processor) computers in controlling their peripheral devices, hence the name Peripheral Interface Controller. PIC microcontroller architecture consists of RAM, ROM, CPU, timers, counters and supports the protocols such as SPI, CAN, and UART for interfacing with other peripherals.
- At present PIC microcontrollers are extensively used for industrial purpose due to low power consumption, high performance ability and easy of availability of its supporting hardware and software tools like compilers, debuggers and simulators.
- It is a RISC (Reduced Instruction Set Computer) design. Only thirty seven instructions to remember. Like many micros the PIC is a Harvard not a von-Neumann machine.This is simpler and faster. Separate program bus and data bus. It can be different widths.

A brief look on Von-Neumann vs Harvard Architecture



PIC family have HARVARD architecture and RISC Sets

Harvard architecture is a newer concept than von-Neumann's. It rose out of the need to speed up the work of a microcontroller.

- In Harvard architecture, Data Access and Address Access are separate. Thus a greater flow of data is possible through the central processing unit. PIC16F877 uses 14 bits for instructions which allows for all instructions to be one word instructions.

Advantages of Harvard model

- An add operation of the form a:=b+c must fetch 2 operands from memory and write 1 operand to memory. In addition it is likely to have to fetch 3 instructions from memory.
- With a single memory this will take 6 cycles.
- With 2 memories, we can fetch the instructions in parallel with the data and do it in 3 cycles.
- We have different word lengths for instructions and data . 8 bit data and perhaps 12 bit instructions.

SESSION INTRODUCTION

Selection Criteria for Micro-controller

- Speed
- Capacity of memory RAM/ROM
- Number of I/O pins, Timer/Counter
- Power Consumption. Availability of tools Added feature like ADC/DAC/CCP.
- Bus like support CAN SPI I2C USB, Watch dog timer, data EEPROM

SESSION INTRODUCTION

Classification of PIC Microcontrollers

PIC Microcontroller are divided into 4 large families. Each family has a variety of components that provide built-in special features:

(1)The first family, PIC10 (10FXXX) - is called Low End.

- The PIC10FXXX devices from Microchip Technology are low-cost, high-performance, 8-bit, fully static, Flash-based CMOS microcontrollers.
- They employ a RISC architecture with only 33 single-word/ single-cycle instructions.
- The 12-bit wide instructions are highly symmetrical. The easy-to-use and easy to remember instruction set reduces development time significantly. The PIC10FXXX devices contain an 8-bit ALU and working register.

(2) The second family, PIC12 (PIC12FXXX)– is called Mid-Range.

- The PIC12FXXX most popular among these starter their way in this field.
- Mid-Range devices feature 14-bit program word architecture and are available in 8 to 64-pin packages that offer an operating voltage range of 1.8-5.5V.
- They have features as small package footprints, interrupt handling, an 8-level hardware stack, multiple A/D channels and EEPROM data memory. Mid-range devices offer a wide range of package options and a wide range of peripheral integration.
- These devices feature various serial analog and digital peripherals, such as: SPI, I2C™, USART, LCD and A/D converters.

SESSION INTRODUCTION

Classification of PIC Microcontrollers….Continue

(3) The third family is PIC16(16FXXX)

- With six variants ranging from 3.5K-14 Kbytes of Flash memory, up to 256 bytes of RAM and a mix of peripherals including EUSART, CCP and onboard analog comparators.
- These devices are well suited for designers with applications that need more code space or I/O than 14-pin variants supply.
- It can increase system performance and code efficiency by employing hardware motor control and communications capability.

(4) The fourth family is PIC 17/18(18FXXX)

- The PIC18 family utilizes a 16-bit program word architecture and incorporates an advanced RISC architecture with 32 level-deep stack, 8x8 hardware multiplier, and multiple internal and external interrupts.
- With the highest performance in Microchip's 8-bit portfolio, the PIC18 family provides up to 16 MIPS and linear memory.
- PIC18 is the most popular architecture for new 8-bit designs where customers want to program in C language.

SESSION INTRODUCTION

A Comparison between Traditional Microcontroller, PIC-16FXXX and PIC18FXXX

Traditional Microcontroller	PIC-16FXXX	PIC18FXXX
Complex Instruction Set Computer (CISC):Used in: 80X86, 8051, 68HC11, etc.	The instruction set for these MCU is also limited. Follow Havard-architecture.	77 instructions.PIC16 source code compatible.
Many instructions (usually > 100)	The interrupt structure is primitive, all interrupt sources sharing the same interrupt vector.	PIC18 series of microcontrollers for use in high-pin count,high-density, and complex applications.
Many, many addressing modes.	Do not provide direct support for advanced peripheral Interfaces such as USB, CAN bus and interfacing is not easy.	PIC18F devices provide flash program memory in sizes from 8 to 128Kbytes and data memory from 256 to 4Kbytes
Usually takes more than 1 internal clock cycle to execute	The instruction set for these MCU is also limited. Follow Harvard-architecture.	Operating at a range of2.0 to 5.0 volts, at speeds from DC to 40MHz.
Follow von-Neumann's architecture	There are no multiplication or division instructions, and branching is rather simple, being a combination of skip and goto instructions.	The PIC18F MCU offer cost efficient that uses a real-time OS(RTOS) and require a complex communication protocol stack such as TCP/IP, CAN, USB, or ZigBee.

SESSION INTRODUCTION

A Comparison between Traditional Microcontroller, PIC-16FXXX and

Comparison of 8051 and PIC18 Family

Features	8051/52	PIC18xxx
Program ROM (maximum space)	64K	2M
Data RAM (maximum space)	256bytes	4K
Timers	3	4
I/O Pins	32	33
Serial Port	1	1
ADC	Not Available	Available

PIC18FXX2 microcontrollers

Table 1 gives the characteristics of some of the popular devices in the PIC18F family. This chapter offers a detailed study of the PIC18FXX2 microcontrollers. The architectures of most of the other microcontrollers in the PIC18F family are similar.

Feature	PIC18F242	PIC18F252	PIC18F442	PIC18F452
Program memory (Bytes)	16K	32K	16K	32K
Data memory (Bytes)	768	1536	768	1536
EEPROM (Bytes)	256	256	256	256
I/O Ports	A,B,C	A,B,C	A,B,C,D,E	A,B,C,D,E
Timers	4	4	4	4
Interrupt sources	17	17	18	18
Capture/compare/PWM	2	2	2	2
Serial communication	MSSP USART	MSSP USART	MSSP USART	MSSP USART
A/D converter (10-bit)	5 channels	5 channels	8 channels	8 channels
Low-voltage detect	yes	yes	yes	yes
Brown-out reset	yes	yes	yes	yes
Packages	28-pin DIP 28-pin SOIC	28-pin DIP 28-pin SOIC	40-pin DIP 44-pin PLCC 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin TQFP

Feature and Functioning of PIC-18F452 Microcontroller

Description of PIC18F452 8-bit PIC Microcontroller

- The PIC18F452-I/P is a high-performance Enhanced Flash Microcontroller with 8 channels of 10-bit Analogue-to-digital (A/D) converter. The PIC18F452 features a C compiler friendly development environment, 256 bytes of EEPROM. It is 8-bit processor with a 40-pin DIP package that can operate at speeds from DC to 40MHz. It is Low power, high speed CMOS FLASH technology, Fully Static and RISC Design and has a Harvard based architecture which can work on Wide Operating Voltage Range (2.0V to 5.5V)

The functions that make this device unique in terms of functionality and ease of use include:

- Wide operating voltage range (2.0V-5.5V)
- Multiplexed Master Clear with pull-up/input pin
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Power-Saving Sleep mode
- C compiler optimized architecture
- Industrial and Extended Temperature range
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Power-on Reset (POR)
- In-Circuit Debug (ICD) via two pins
- Brown-out Reset (BOR) with software control option
- Watchdog Timer (WDT)

Features and specification of PIC18F4520

Features are very important for any device that makes it unique from its counterparts

Features and specification of PIC18F4520							
No. of Pins	40	RAM	4KB	External Oscillator	up to 40 MHz	Comparators	2
CPU	8-Bit PIC	EEPROM	256 Bytes	Timer (4)	16-Bit Timer (3) 8-Bit Timer (1)	Master Synchronous Serial Port (MSSP) module	1
Operating Voltage	2 to 5.5 V	ADC Number of Channels	10-Bit 13	USART Protocol	1	Capture/Compare/PWM	16bit/16bit/10bit
Program Memory	2MB	I/O Ports (5) I/O Pins	A,B,C,D,E 36	I2C Protocol	Yes	Power Saving Sleep Mode	Yes
Program Memory (Instructions)	16384	Packages	40-pin	SPI Protocol	Yes	Selectable Oscillator Option	Yes
Oscillator Start-up Timer	Yes	Watchdog Timer	Yes	Brown-out Reset	Yes	Operating High-current sink/source Each pin	25mA

Features and specification of PIC18F4520

Features are very important for any device that makes it unique from its counterparts.

The basic features of PIC18F-series microcontrollers are:

- It is 8-bit processor with a 40-pin DIP package that can operate at speeds from DC to 40MHz.
- It is Low power, high speed CMOS FLASH technology, Fully Static and RISC Design and has a Harvard based architecture which can work on Wide Operating Voltage Range (2.0V to 5.5V)
- **PIN and PORTS**: It has total 40 pins. Out of these 40 pins, 34 pins can be used as input output pins. It has five(5)I/O PORTS which are A,B,C,D,E, A(7)-B,C,D(8),E(3): Total=34 I/P output lines.

a. Port A consists of seven pins named as RA0-RA6
b. Port B consists of eight pins named as RB0-RA7
c. Port C consists of eight pins named as RC0-RC7
d. Port D consists of eight pins named as RD0-RD7
e. Port E consists of three pins named as RE0-RE2
f. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. If a pin is used as any other function then it may not be used as a general purpose I/O pin. Here we will just restrict with the input output features of ports.

Features and specification of PIC18F4520

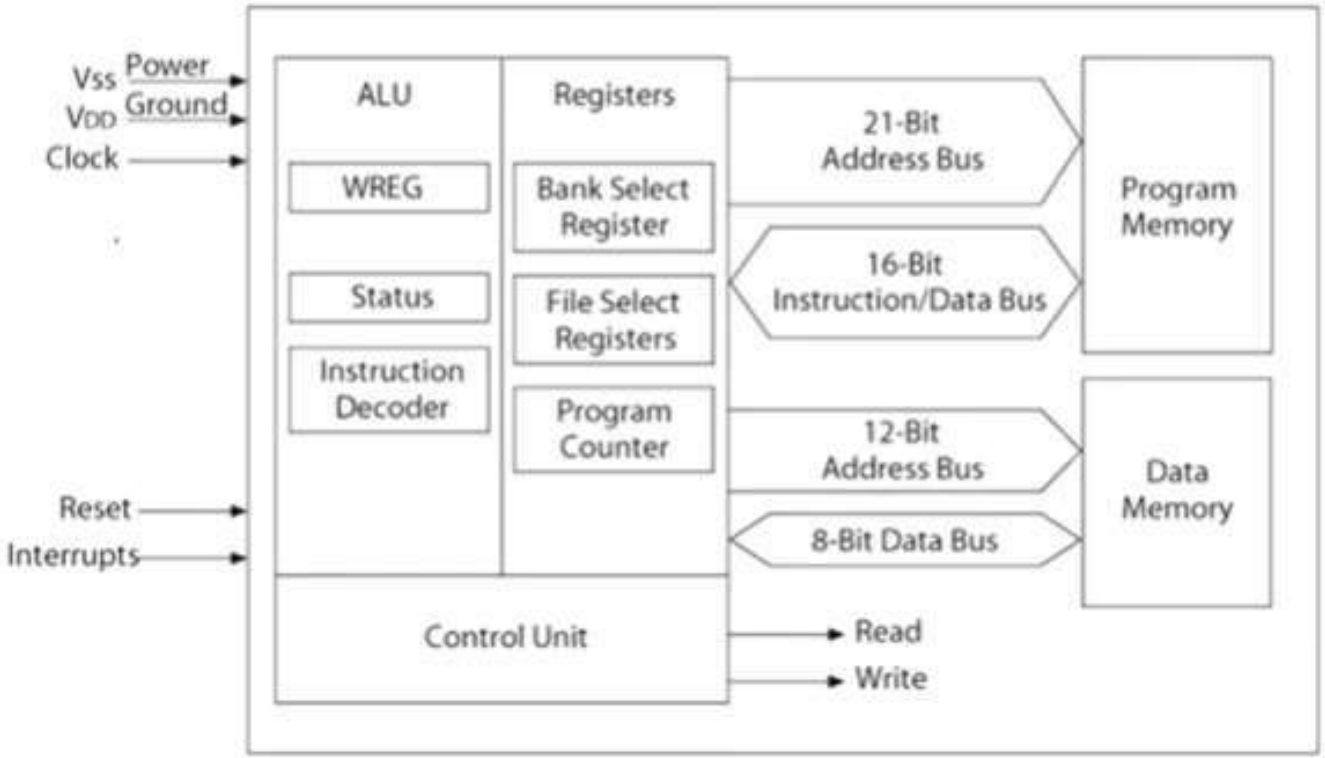
- **REGISTERS**: Each port has three registers for its operation. These registers are
  - TRIS register (data direction register)
  - PORT register (reads the levels on the pins of the device)
  - LAT register (output latch)
- It has 77 instructions sets
- **TIMERS/Counters:** It has total 4-timers.PIC18F4520 comes with three 16-bit and one 8-bit timer that can be used as a timer as well as a counter. All three timers contain internal and external clock select capability. The timer mode mainly increments the instruction cycle while the counter mode is used to increment the rising and falling edge of the pin.

Features and specification of PIC18F4520

- **Highlights on size of instruction, data path, memory capacity.**

a. It uses 16 bit wide instruction and 8-bit wide data path,
b. It uses the program memory and data memory to store the instruction and data separately.
c. It uses 21 address line to access the Program memory/Instruction. The capacity of program memory is 2MB ROM(21 Address line)
d. The size of dada memory is 4KB . It is also called data RAM. It uses 12 address line to access the data memory.
e. It has 32KB of flash RAM
f. It has 256bytes of data EPROM for storing critical information.

MPU and Memory



Features and specification of PIC18F4520

Highlights on size of Data Buses and address buses.

a. 21 –bit-address bus for program memory with addressing capacity 2MB,
b. 12 –bit-address bus for Data memory with addressing capacity 4kb
c. PIC18F-Data Buses
d. 16 –bit-instruction/data bus for program memory
e. 8 –bit-data bus for Data memory
f. High performance RISK CPU
g. Three external interrupts pins

Features and specification of PIC18F4520

Highlights on capacity and functioning of Data Memory and Program Memory.

Data Memory(RAM)

- There is 12 address buses is to locate the data memory in PIC microcontroller.
- Data memory also called as RAM.
- The size of RAM is 2^12=4kb.
- This RAM stores the data temporally in its register.
- The whole RAM is classified in to two banks.
- Each bank carry 256 byte of memory and there is 16 such bank is available.
- The lower bank reserved for SFR(Special function register) while upper is for GPR(General Purpose register)

Features and specification of PIC18F4520

Program Memory

- Program memory: A memory that contain the program which is written by the user and loaded on it.
- The PIC18F452 have 16 bits of program memory register that can be electrically erased and reprogrammed several times.
- PIC 18F452 have 21 bit address bus to access the program memory.
- The memory capacity of PIC controller is 2MB.
- It consists of Program counter and Stack memory
- A program counter (PC) is a **processor register that holds the memory address of the next instruction to be executed by the computer**. The PC is usually incremented after fetching an instruction, but can be changed by control transfer instructions like branches, calls, and returns. The PC may revert to a specific value when the computer restarts or is reset,
- The stack pointer SP, holds the address of the stack top. The stack is a sequence of RAM memory locations defined by the programmer. The stack is used to save the content of registers during the execution of a program. The stack pointer is also a register that is used to point into memory. The memory this register points to is a special area called the stack. The stack is an area of memory used to hold data that will be retrieved soon. The stack is usually accessed in a Last In First Out (LIFO) fashion. The stack is a segment of memory that stores temporary variables created by a function. In stack, variables are declared, stored and initialized during runtime.

Feature functioning of PIC18F4520

This PIC model is capable of performing many functions similar to other controllers in the PIC community. Following are the main functions of PIC18F4520.

(a) Timer:-PIC18F4520 comes with three 16-bit and one 8-bit timer that can be used as a timer as well as a counter. All three timers contain internal and external clock select capability. The timer mode mainly increments the instruction cycle while the counter mode is used to increment the rising and falling edge of the pin.

(b)Brown out Reset(BOR):-The BOR is a very useful function that allows this controller to reset once the Vdd (voltage supply) drops below a brownout threshold voltage. The multiple voltage ranges are used and provided to protect the chip once the power drops at the voltage supply line. The Power Up Timer must be kept enabled, in order to put the delay in returning the device from a BOR function. The BOR mode can be configured both ways i.e. through BOREN settings in a register as well through programming.

(c) In circuit Serial Programing:-In-**circuit serial programming** (ICSP), also called In-system **programming** (ISP), is a feature added to this device that makes it enable to be programmed in the required system after installation, setting it free from programming the device before making it

Feature functioning of PIC18F4520

(d)USART module

This controller version comes with USART module, that stands for Universal Synchronous and Asynchronous Receiver and Transmitter, and is mainly used for setting up the serial communication with external devices. There are two parts of this module called TX and RX where former is known as transmitting component that is used for transmitting serial data while later is known as receiving component, used for receiving the serial data across the attached devices.an output.

(e)Watch Dog Timer:

PIC18F4520 contains a built-in watchdog timer that brings the controller in reset position if the program hangs up during compilation or gets stuck in the infinite loop. It is worth mentioning here, this timer must be reset to the initial value after every 3 instructions in order to avoid it going to zero value in normal conditions. The watchdog timer is more or less a countdown timer that starts from 1000 and ultimately goes down to zero.

Functioning of PIC18F4520

(f)Power on Reset

Power On Reset function is very helpful and resets the controller and starts it from scratch when Vdd raises above a certain threshold value. This function is very useful to prevent the device from malfunctioning.

(g)Power Managed mode

•The power managed modes are mainly divided into three main categories called:

•**Run modes**

•**Sleep mode**

•**Idle modes**

•These categories help in identifying the areas of the device that are clocked at a specific speed. The Idle and Run modes can operate in any of three clock sources named primary, secondary, and internal oscillator block while Sleep mode is not involved in any clock source. The switching feature is added in the power managed modes that use the Timer1 oscillator as a replacement of a primary oscillator. All clocks will be cleared and stopped working in the Sleep mode.

Functioning of PIC18F4520

(h)Master Clear Reset Mode

The MCLR pin is used for calling the external reset for the chip. The reset is triggered by keeping this pin at a LOW value and is not dependent on the internal resets. The noise filter is added in the MCLR executing process that helps in detecting and removing the small pulses. The MCLRE configuration bit can also be used to disable MCLR input.

(i)PLL Circuit:- The PLL circuit is new to the PIC18F series and provides the option of multiplying up the oscillator frequency to speed up the overall operation.

(j) In-Circuit Debugger

The in-circuit debugger is useful during program development and can be used to return diagnostic data, including the register values, as the microcontroller is executing a program

Architecture of PIC Microcontroller

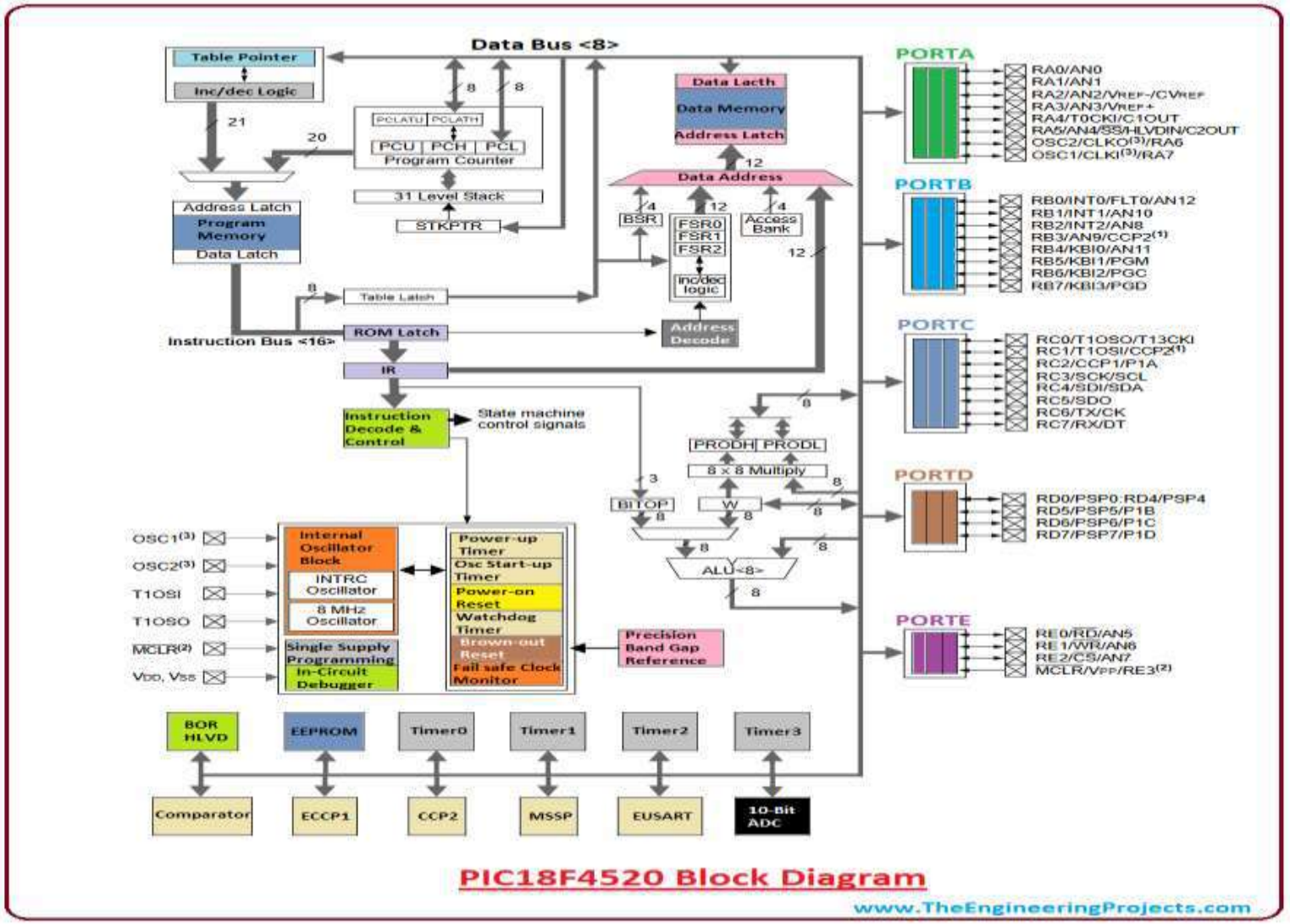
Components of Architecture of PIC Microcontroller

PIC Microcontroller architecture is based on Harvard architecture and supports RISC architecture (Reduced Instruction Set Computer). Memory organization (ram, rom, stack), CPU, timers, counter, ADC, DAC, serial communication, CCP module, and I/O ports are all part of the PIC microcontroller architecture. For communicating with additional peripherals, the PIC microcontroller supports protocols such as CAN, SPI, and UART.

•The PIC microcontroller architecture comprises of following components:

1. CPU
2. I/O ports
3. Memory organization,
4. A/D converter
5. Timers/counters
6. Interrupts
7. Serial communication
8. Oscillator
9. CCP module

Architecture of PIC Microcontroller



PIC18F4520 Block Diagram

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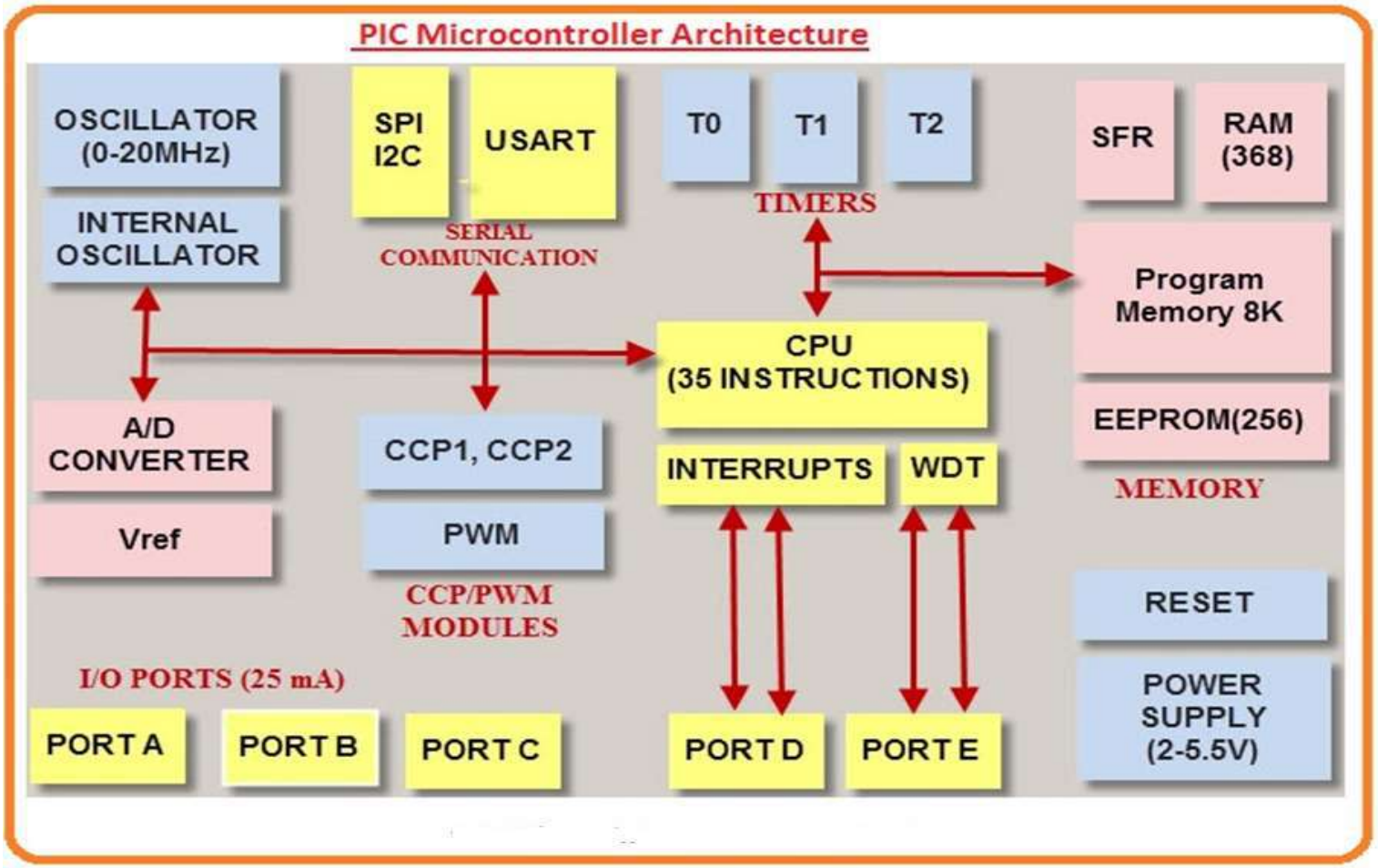
Architecture of PIC Microcontroller in a Precise way



Components of Architecture of PIC Microcontroller

1.CPU (Central Processing Unit)

It is not different from other microcontrollers CPU and the PIC microcontroller CPU consists of the ALU (Arithmetic logic unit), CU(Control Unit), MU(Memory Unit) and accumulator. Arithmetic logic unit is mainly used for arithmetic operations and to take logical decisions. Memory is used for storing the instructions after processing. To control the internal and external peripherals, control unit is used which are connected to the CPU and the accumulator is used for storing the results and further process.

The CPU is at the centre of the diagram and consists of an 8-bit ALU, an 8-bit working accumulator register (WREG), and an 8 X8 hardware multiplier. The higher byte and the lower byte of a multiplication are stored in two 8-bit registers called PRODH and PRODL respectively.

There are three register inside the CPU: (a) WREG (b) PRODH (c) PRODL.

2. I/O ports (Input/Output Ports)

•The series of PIC18 consists of five ports such as Port A, Port B, Port C, Port D & Port E.

•Port A is 7-bit port that is used as input or output port based on the status of TRISA (Tradoc Intelligence Support Activity) register.

•Port B is an 8- bit port that can be used as both input and output port.

•Port C is an 8-bit and the input of output operation is decided by the status of the TRISC register.

•Port D is an 8-bit port acts as a slave port for connection to the microprocessor BUS.

•Port E is a 3-bit port which serves the additional function of the control signals to the analog to digital converter.

Components of Architecture of PIC Microcontroller

3. Memory organization

The memory of the module is useful for storing a number of instruction which are divided into three major types:

a. Program Memory or ROM

b. Data EEPROM

c. Data RAM.

d. Flash Memory

e. Stack

(a) Program Memory :The Program memory, also known as ROM memory or Non-Volatile memory, stores the running program permanently. It doesn't depend on the power supply i.e. stores the program in the absence of the main power supply. The ROM memory is about 32K and is made with FLASH Technology.

(b) Data EEPROM :This memory permits variables to be stored as a result of burning a programme. During regular functioning, it is readable and writable (over the full VDD range). The register file does not directly map this memory. The SFRs are used to address it in a roundabout way. This memory is

Components of Architecture of PIC Microcontroller

(c)Data memory RAM.

- RAM memory, also known as volatile memory, stores the program temporarily and removes the stored program once the power supply is removed.
- It is classified into two main parts called **General-purpose registers (GPR) and Special-function registers (SFR)** :

(i) General-purpose registers (GPR): These registers don't have any special function,- CPU can easily access the data in the registers.

(ii) Special-function registers (SFR) : These registers are used for special purposes and they cannot be used as normal registers. Their function is set at the time of manufacturing. They perform the function assigned to them and user cannot change the function of SFR. Three important SFRs for programming are:

- STATUS register: It changes the bank
- PORT registers: It assigns logic values 0 or 1 to the ports
- TRIS registers: It is a data direction register for input and output

- This memory is volatile in nature as it stores the program temporarily and is power dependent i.e. once the power supply is turned off the instructions stored in the RAM will be removed.
- The RAM memory registers are the data holding places that can hold instruction, storage address, and any kind of data ranging from an individual character to bit sequence.
- The data memory can be employed as static RAM where each register comes with a 12-bit address. This memory is comprised of a total 16 banks and each bank contains a memory space of around 256 bytes..

Components of Architecture of PIC Microcontroller

(d)Flash Memory: Flash memory is also programmable read only memory (PROM) in which we can read, write and erase the program thousands of times. Generally, the PIC microcontroller uses this type of ROM.

(e)Stack: When an interrupt occurs, first the PIC microcontroller has to execute the interrupt and the existing process address. Then that is being executed is stored in the stack. After completing the execution of the interrupt, the microcontroller calls the process with the help of address, which is stored in the stack and get executes the process.

4.A/D converter: The main intention of this analog to digital converter is to convert analog voltage values to digital voltage values. A/D module of PIC microcontroller consists of 5 inputs for 28 pin devices and 8 inputs for 40 pin devices. The operation of the analog to digital converter is controlled by ADCON0 and ADCON1 special registers. The upper bits of the converter are stored in register ADRESH and lower bits of the converter are stored in register ADRESL. For this operation, it requires 5V of an analog reference voltage.

Components of Architecture of PIC Microcontroller

5.Timers/ Counters

PIC microcontroller has four timer/counters wherein the one 8-bit timer and the remaining timers have the choice to select 8 or 16-bit mode. Timers are used for generating accuracy actions, for example, creating specific time delays between two operations.

6.Interrupts

PIC microcontroller consists of 20 internal interrupts and three external interrupt sources which are associated with different peripherals like ADC, USART, Timers, and so on.

7. Serial Communication

Serial communication is the method of transferring data one bit at a time sequentially over a communication channel. There are three protocols of serial communication: USART, SPI,I2C.

•USART: The name USART stands for Universal synchronous and Asynchronous Receiver and Transmitter which is a serial communication for two protocols. It is used for transmitting and receiving the data bit by bit over a single wire with respect to clock pulses. The PIC microcontroller has two pins TXD and RXD. These pins are used for transmitting and receiving the data serially.

Components of Architecture of PIC Microcontroller

•**SPI Protocol:** The term SPI stands for Serial Peripheral Interface. This protocol is used to send data between PIC microcontroller and other peripherals such as SD cards, sensors and shift registers. PIC microcontroller support three wire SPI communications between two devices on a common clock source. The data rate of SPI protocol is more than that of the USART.

•**I2C Protocol:** The term I2C stands for Inter Integrated Circuit , and it is a serial protocol which is used to connect low speed devices such as EEPROMS, microcontrollers, A/D converters, etc. PIC microcontroller support two wire Interface or I2C communication between two devices which can work as both Master and Slave device.

8.Oscillators

Oscillators are used for timing generation. Pic microcontroller consist of external oscillators like RC oscillators or crystal oscillators. Where the crystal oscillator is connected between the two oscillator pins. The value of the capacitor is connected to every pin that decides the mode of the operation of the oscillator. The modes are crystal mode, high-speed mode and the low-power mode. In case of RC oscillators, the value of the resistor & capacitor determine the clock frequency and the range of clock frequency is 30KHz to 4MHz.

Components of Architecture of PIC Microcontroller

9.CCP module

The name CCP module stands for capture/compare/PWM where it works in three modes such as capture mode, compare mode and PWM mode.

•**Capture Mode:** Capture mode captures the time of arrival of a signal, or in other words, when the CCP pin goes high, it captures the value of the Timer1. When a signal is received, time is captured, or we can say that when the CCP pin is high, the value of the Timer1 is captured.

•**Compare Mode:** Compare mode acts as an analog comparator. When the timer1 value reaches a certain reference value, then it generates an output. It functions like an analogue comparator, which means that when the value of timer 1 hits a certain threshold, it generates an output signal.

•**PWM Mode:** PWM mode provides pulse width modulated output with a 10-bit resolution and programmable duty cycle.

Components of Architecture of PIC Microcontroller

(10)USART module

This controller version comes with USART module, that stands for Universal Synchronous and Asynchronous Receiver and Transmitter, and is mainly used for setting up the serial communication with external devices. There are two parts of this module called TX and RX where former is known as transmitting component that is used for transmitting serial data while later is known as receiving component, used for receiving the serial data across the attached devices.an output.

(11)Watch Dog Timer:

PIC18F4520 contains a built-in watchdog timer that brings the controller in reset position if the program hangs up during compilation or gets stuck in the infinite loop. It is worth mentioning here, this timer must be reset to the initial value after every 3 instructions in order to avoid it going to zero value in normal conditions. The watchdog timer is more or less a countdown timer that starts from 1000 and ultimately goes down to zero.

Components of Architecture of PIC Microcontroller

(12)Power on Reset

Power On Reset function is very helpful and resets the controller and starts it from scratch when Vdd raises above a certain threshold value. This function is very useful to prevent the device from malfunctioning.

(13)Power Managed mode

•The power managed modes are mainly divided into three main categories called:

•**Run modes**

•**Sleep mode**

•**Idle modes**

•These categories help in identifying the areas of the device that are clocked at a specific speed. The Idle and Run modes can operate in any of three clock sources named primary, secondary, and internal oscillator block while Sleep mode is not involved in any clock source. The switching feature is added in the power managed modes that use the Timer1 oscillator as a replacement of a primary oscillator. All clocks will be cleared and stopped working in the Sleep mode.

(14)Master Clear Reset Mode

The MCLR pin is used for calling the external reset for the chip. The reset is triggered by keeping this pin at a LOW value and is not dependent on the internal resets. The noise filter is added in the MCLR executing process that helps in detecting and removing the small pulses. The MCLRE configuration bit can also be used to disable MCLR input.

Features and specification of PIC18F4520

Program Memory

- Program memory: A memory that contain the program which is written by the user and loaded on it.
- The PIC18F452 have 16 bits of program memory register that can be electrically erased and reprogrammed several times.
- PIC 18F452 have 21 bit address bus to access the program memory.
- The memory capacity of PIC controller is 2MB.
- It consists of Program counter and Stack memory
- A program counter (PC) is a **processor register that holds the memory address of the next instruction to be executed by the computer**. The PC is usually incremented after fetching an instruction, but can be changed by control transfer instructions like branches, calls, and returns. The PC may revert to a specific value when the computer restarts or is reset,
- The stack pointer SP, holds the address of the stack top. The stack is a sequence of RAM memory locations defined by the programmer. The stack is used to save the content of registers during the execution of a program. The stack pointer is also a register that is used to point into memory. The memory this register points to is a special area called the stack. The stack is an area of memory used to hold data that will be retrieved soon. The stack is usually accessed in a Last In First Out (LIFO) fashion. The stack is a segment of memory that stores temporary variables created by a function. In stack, variables are declared, stored and initialized during runtime.

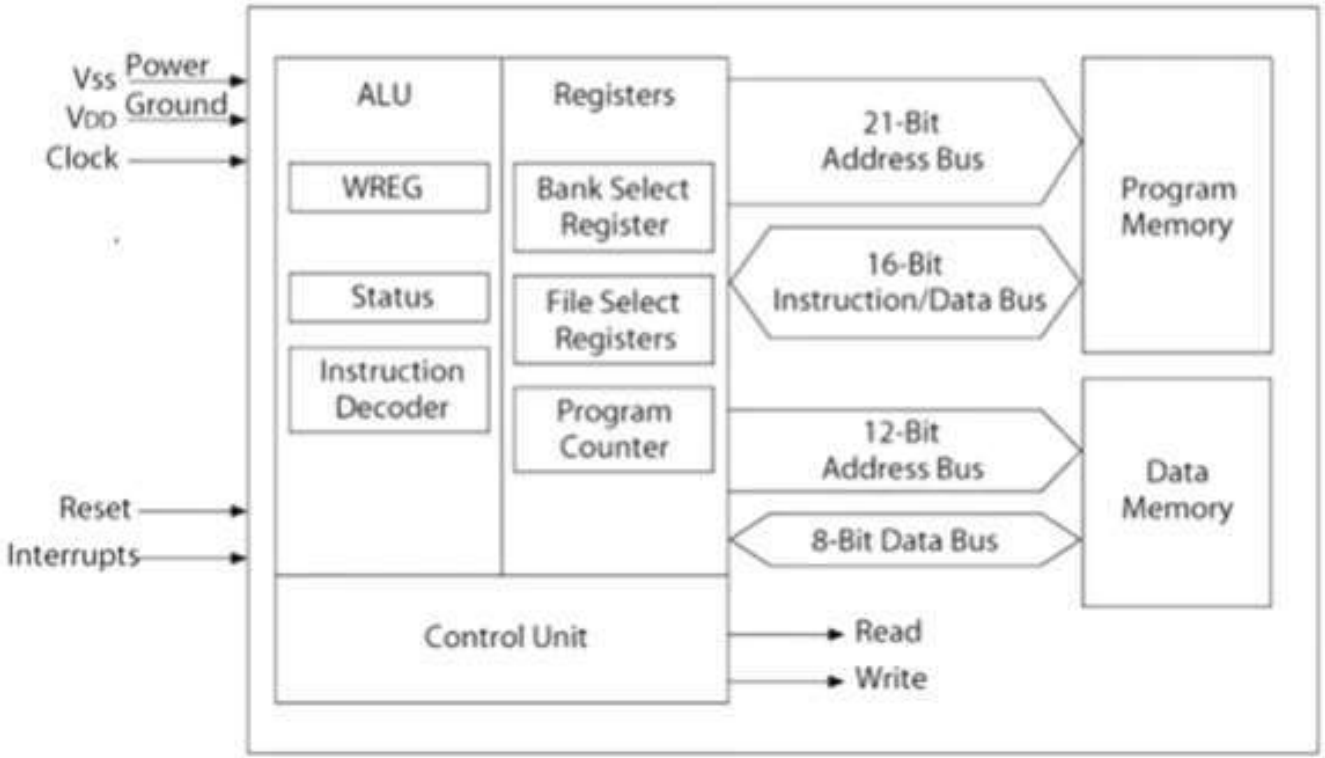
Components of Architecture of PIC Microcontroller

Program Memory Organization

The program memory map is shown in Figure.

- All PIC18F devices have a 21-bit program counter and hence are capable of addressing 2Mbytes of memory space.
- Accessing a non-existent memory location (8000H to 1FFFFFH) will cause a read of all 0s. The reset vector, where the program starts after a reset, is at address 0000.
- Addresses 0008H and 0018H are reserved for the vectors of high-priority and low-priority interrupts respectively, and interrupt service routines must be written to start at one of these locations.
- The PIC18F microcontroller has a 31-entry stack that is used to hold the return addresses for subroutine calls and interrupt processing.

MPU and Memory



Components of Architecture of PIC Microcontroller

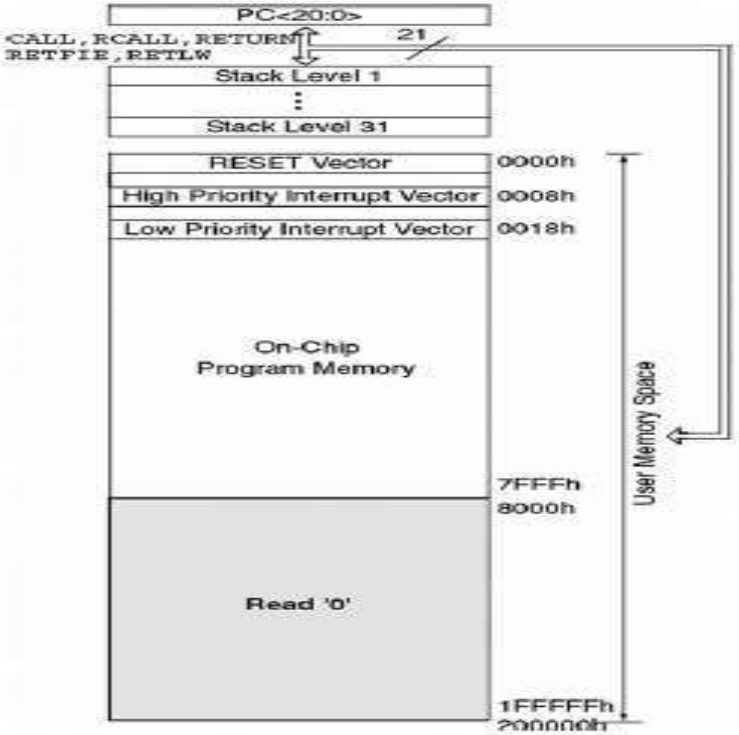


Figure 1 :Program Memory Organization

Components of Architecture of PIC Microcontroller

- The stack is not part of the program or the data memory space. The stack is controlled by a 5-bit stack pointer which is initialized to 00000 after a reset. During a subroutine call (or interrupt) the stack pointer is first incremented, and the memory location it points to is written with the contents of the program counter. During the return from a subroutine call (or interrupt), the memory location the stack pointer has pointed to is decremented.
- Program memory is addressed in bytes, and instructions are stored as two bytes or four bytes in program memory. The least significant byte of an instruction word is always stored in an even address of the program memory.
- An instruction cycle consists of four cycles: A fetch cycle begins with the program counter incrementing in Q1. In the execution cycle, the fetched instruction is latched into the instruction register in cycle Q1. This instruction is decoded and executed during cycles Q2, Q3, and Q4. A data memory location is read during the Q2 cycle and written during the Q4 cycle.

Components of Architecture of PIC Microcontroller

Data Memory Organization

- The data memory map of the PIC18F452 microcontroller is shown in Figure below.
- The data memory address bus is 12 bits with the capability to address up to 4Mbytes.
- The memory in general consists of sixteen banks, each of 256 bytes, where only 6 banks are used.
- The PIC18F452 has 1536 bytes of data memory (6 banks _ 256 bytes each) occupying the lower end of the data memory.
- Bank switching happens automatically when a high-level language compiler is used, and thus the user need not worry about selecting memory banks during programming.
- The special function register (SFR) occupies the upper half of the top memory bank..

  SFR contains registers which control operations such as peripheral devices, timers/ counters, A/D converter,

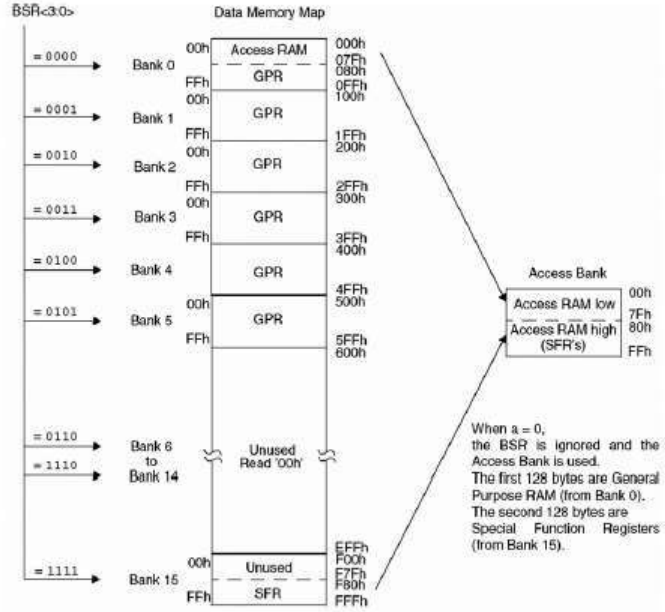
  interrupts, and USART.

Features and specification of PIC18F4520

Highlights on capacity and functioning of Data Memory.

Data Memory(RAM)

- There is 12 address buses is to locate the data memory in PIC microcontroller.
- Data memory also called as RAM.
- The size of RAM is 2^12=4kb.
- This RAM stores the data temporally in its register.
- The whole RAM is classified in to two banks.
- Each bank carry 256 byte of memory and there is 16 such bank is available.
- The lower bank reserved for SFR(Special function register) while upper is for GPR(General Purpose register)


BSR<3:0>
Data Memory Map
= 0000
Bank 0
= 0001
Bank 1
= 0010
Bank 2
= 0011
Bank 3
= 0100
Bank 4
= 0101
Bank 5
= 0110
= 1110
Bank 6
to
Bank 14
= 1111
Bank 15
00h
Access RAM
FFh
GPR
00h
GPR
FFh
00h
GPR
FFh
00h
GPR
FFh
GPR
00h
GPR
FFh
Unused
Read '00h'
00h
Unused
FFh
SFR
000h
07Fh
080h
0FFh
100h
1FFh
200h
2FFh
300h
3FFh
400h
4FFh
500h
5FFh
600h
EFFh
F00h
F7Fh
F80h
FFFh
Access Bank
Access RAM low
Access RAM high
(SFR's)
00h
7Fh
80h
FFh
When a = 0,
the BSR is ignored and the
Access Bank is used.
The first 128 bytes are General
Purpose RAM (from Bank 0).
The second 128 bytes are
Special Function Registers
(from Bank 15).

Components of Architecture of PIC Microcontroller

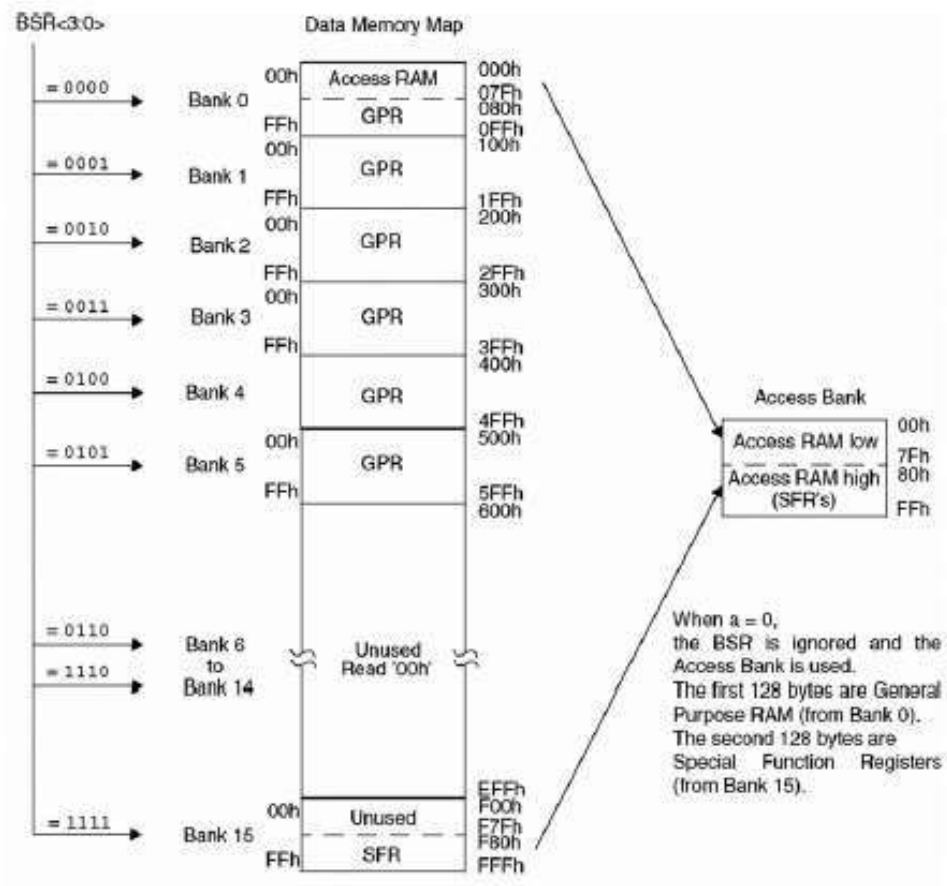


Figure 2 Data Memory Organization

▪ Advantages/Disadvantages of PIC Microcontroller:

- **ADVANTAGES OF PIC MICROCONTROLLER**

➢ PIC microcontrollers are reliable, and the percentage of PIC microcontrollers that are defective is relatively low. Because to its RISC design, the PIC microcontroller has an extremely quick performance.

➢ It is a RISC (Reduced Instruction Set Computer) design. Only thirty seven instructions to remember.

➢ It is low cost, high clock speed

➢ Because of its efficient coding, the PIC can run with significantly less programme memory than its larger competitors.

➢ When comparing to other microcontrollers, power consumption is very less and programming is also very easy.

➢ Interfacing of an analog device is easy without any extra circuitry

- **DISADVANTAGES OF PIC MICROCONTROLLER**

➢ Because of the RISC architecture, the software is somewhat long (35 instructions)

➢ One single accumulator is present and program memory is not accessible

SUMMARY

As seen, the PIC micro-controller has higher speed, more amount of RAM and ROM, larger number of I/O pins than traditional micro-controller(8051). Moreover, it has additional features such as ADC/DAC/CCP, bus support like,CAN,SPI,I2C,USB,Watch Dog Timer, Timer modes, Data EPROM that makes it ideal for manufacturing equipment, data acquisition, power conditioning and environmental monitoring.

It is a RISC (Reduced Instruction Set Computer) design. Only thirty seven instructions to remember. Like many micros the PIC is a Harvard not a von-Neumann machine. This is simpler and faster. It has separate program bus and data.

The PIC microcontroller architecture comprises of following components: CPU ,I/O ports ,Memory organization, A/D converter, Timers/counters, Interrupts, Serial communication, Oscillator ,CCP module. The functions that make this device unique in terms of functionality and ease of use include: Wide operating voltage range (2.0V-5.5V),Multiplexed Master Clear with pull-up/input pin, In-Circuit Serial Programming (ICSP) via two pins, Power-Saving Sleep mode C compiler optimized architecture, Industrial and Extended Temperature range, Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)Power-on Reset (POR),In-Circuit Debug (ICD) via two pins, Brown-out Reset (BOR) with software control option, Watchdog Timer (WDT)

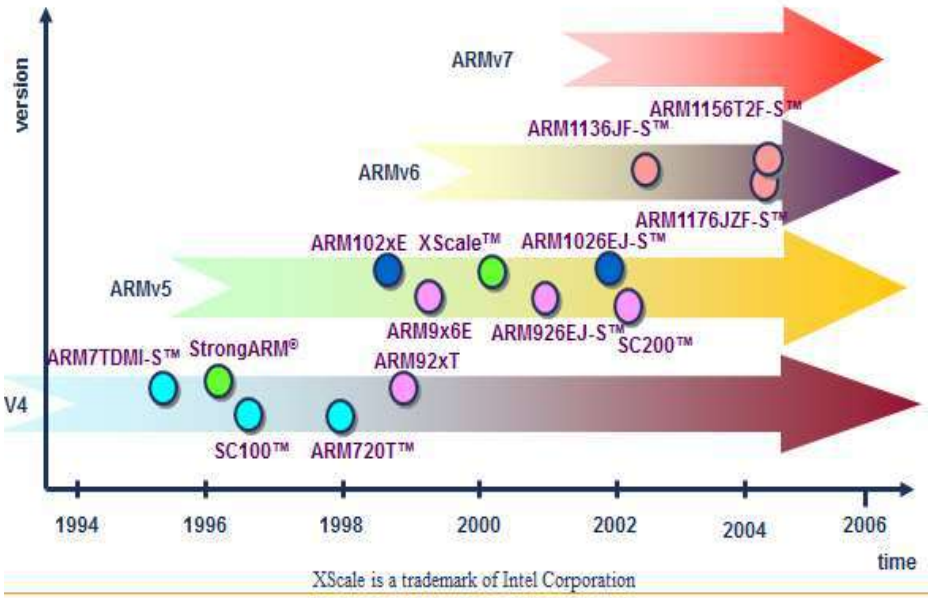
- ARM MICROCONTROLLER

What is ARM?

- Advanced RISC Machine
- First RISC microprocessor for commercial use
- Market-leader for low-power and cost-sensitive embedded applications

The History of ARM

- Developed at Acorn Computers Limited, of Cambridge, England , between 1983 and 1985
- Problems with CISC:
    - Slower memory parts
    - Clock cycles per instruction



Used in:

- Handheld devices
- High end applications involving complex computation
- Robotics
- Automation system
- Consumer electronics

Fundamentals of ARM :

- Load/store architecture
- An orthogonal instruction set.
- Mostly single-cycle execution.
- Enhanced power-saving design.
- 64 and 32-bit execution states for scalable high performance.
- Hardware virtualization support.

Features of ARM :

- High performance, low power, small in size (ideal for embedded sys)
- Large Register File, Small instruction set, Load-Store instructions
- Fixed length instructions, Conditional execution of instructions
- High code density, most instructions executable in single cycle
- 32-bit in-line barrel shifter, built-in circuit for hardware debugging
- DSP enhanced instructions, Jazelle (Java byte code extn. 3rd state)

ARM Nomenclature

A R M {x}{ y}{ z} T D M I E J F S (Example: ARM7-TDMI-S)

ARM	Advanced RISC Machine
x	Series
y	MMU (No. of Memory Management units present)
z	Cache Memory (in terms of KB)
T	Thumb instructions Support
D	Debugger (Debugging via JTAG interface)
M	Multiplier
I	In-Circuit Emulator (ICE) macrocell
E	Enhanced Instructions for DSP related applications
J	Jazelle instructions support for JAVA Codes execution
F	Floating-point unit
S	Synthesizable version

Eg. ARM7TDMI
ARM926EJ-S
ARM1136J(F)-S

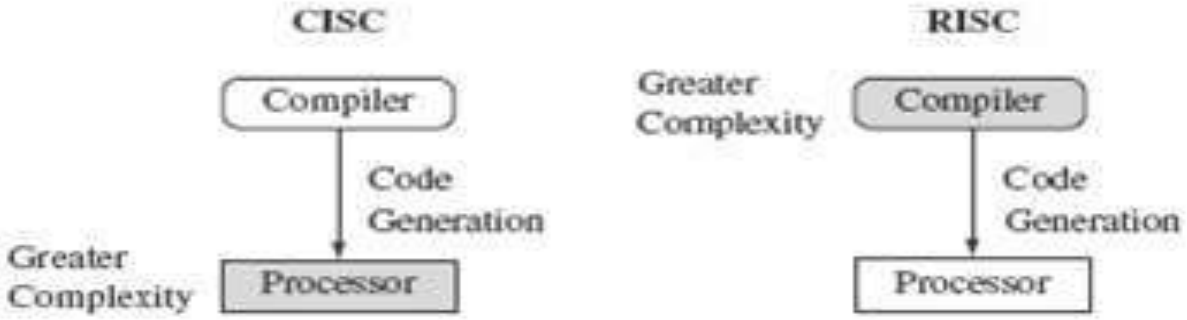
ARM & RISC DESIGN PHILOSOPHY

RISC Processors:

- It is a design philosophy aimed at delivering simple but powerful instruction set that executes within a single cycle at high clock speed.

- CISC and RISC differ in complexities of their instruction sets where CISC is more complex than RISC.

- The smaller instruction set allows a designer to implement a hardwired control unit which runs at a higher clock rate than its equivalent micro sequenced control unit.



RISC	CISC
Simple instruction taking one cycle.	Complex instruction may take one or more clock cycles.
Large register file	Few registers to store data.
Fewer instructions to access memory.	More instructions to access memory
Few addressing modes.	More addressing modes
Instruction Decoder is simple. Hardwired logic is used for the decoder.	The instruction decoder is complex. A decoder using ROM which consists microcode.
Supports pipelining. i.e. overlapping of fetch, decode, execute takes place.	Does not support pipelining.
Fixed instruction size.	Variable instruction size.
Core takes less chip area so more space for cache, MMU.	More chip area is taken by core CPU.
Complexity in software. Compiler design is difficult	Complexity in Hardware. Emphasis is on hardware
Higher clock rates. So faster.	Lower clock rates. So, comparatively slower.
Cache memory is present.	Cache memory is absent or unified cache is present

RISC Philosophy (Four major Rules)

1. Instructions:Less no of instruction classes to provide simple operations that can execute in a single cycle, each instruction is a fixed length to allow the pipeline to fetch future instructions before decoding the current instruction. (Unlike CISC)

2. Pipelines:The processing of instructions is broken down into smaller units that can be executed in parallel by pipelines, instructions can be decoded in one pipeline stage.

3. Registers:RISC machines have a large general-purpose register set & any register can contain either data or an address.

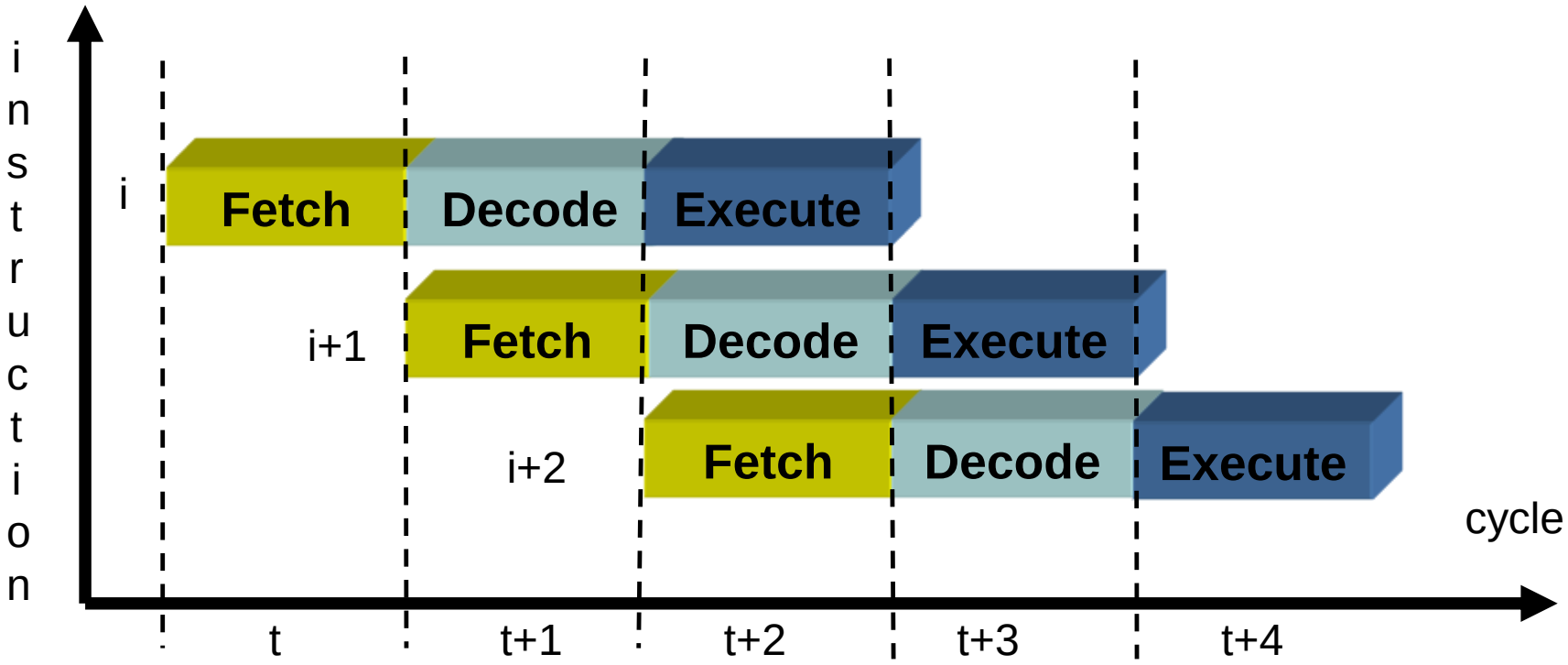
4. Load-Store Architecture: Processor operates on data held in registers. Separate load and store instructions: transfer data between the register bank and external memory. Because memory accesses are costly.

Pipeline Organization

- Increases speed – most instructions executed in single cycle
- Versions:
  - 3-stage (ARM7TDMI and earlier)
  - 5-stage (ARMS, ARM9TDMI)
  - 6-stage (ARM10TDMI)

Pipeline Organization

- 3-stage pipeline: Fetch – Decode - Execute
- Three-cycle latency, one instruction per cycle throughput

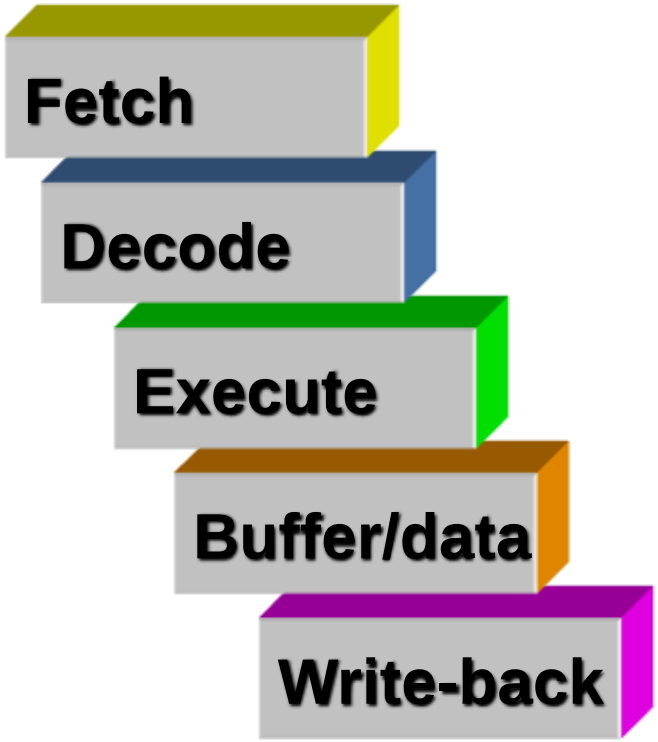


Pipeline Organization

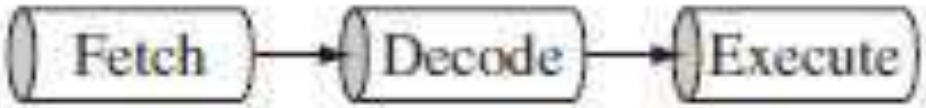
5-stage pipeline:

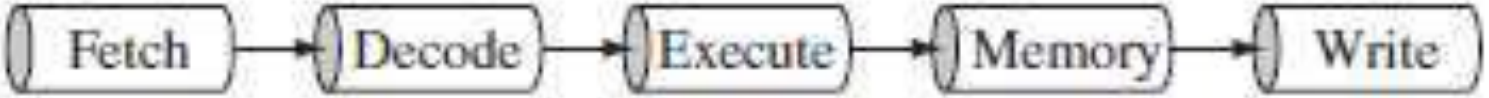
- Reduces work per cycle => allows higher clock frequency
- Separates data and instruction memory => reduction of CPI (average number of clock Cycles Per Instruction)

- Stages:



Pipeline Organization





ARM7 FUNDAMENTALS

1. All ARM instructions are 32-bit long & stored word aligned.
2. ARM processor like all RISC processors is a Load Store architecture, Von-Neuman Architecture (same program + data memory).
3. ARM has two special instructions types for transferring data in & data out of processor.
    1. Load Instruction = Copy data from memory to registers in the core.
        (Registers in the processor core <----Memory)
    2. Store Instruction = Copy data from registers to memory
        1. (Registers in processor core ----> Memory)
4. There are no data processing instructions that are directly manipulate data in memory (Hence Data processing is carried out only in registers).
5. ARM core is a 32-bit bit processor most instructions treat the registers ad holding signed or unsigned 32-bit value.
6. Data Types

Word – 32-bit, Halfword – 16-bit, Byte – 8-bit

ARM7 Features:

- 3 stage Pipeline (Fetch, Decode, Execute)
- Operating frequency: 80 MHz
- Power Consumption: 0.06 mW/MHz.
- MIPS is 0.97
- Available in Von-Neumann Architecture.
- Supports both 16- & 32-bit instruction set.

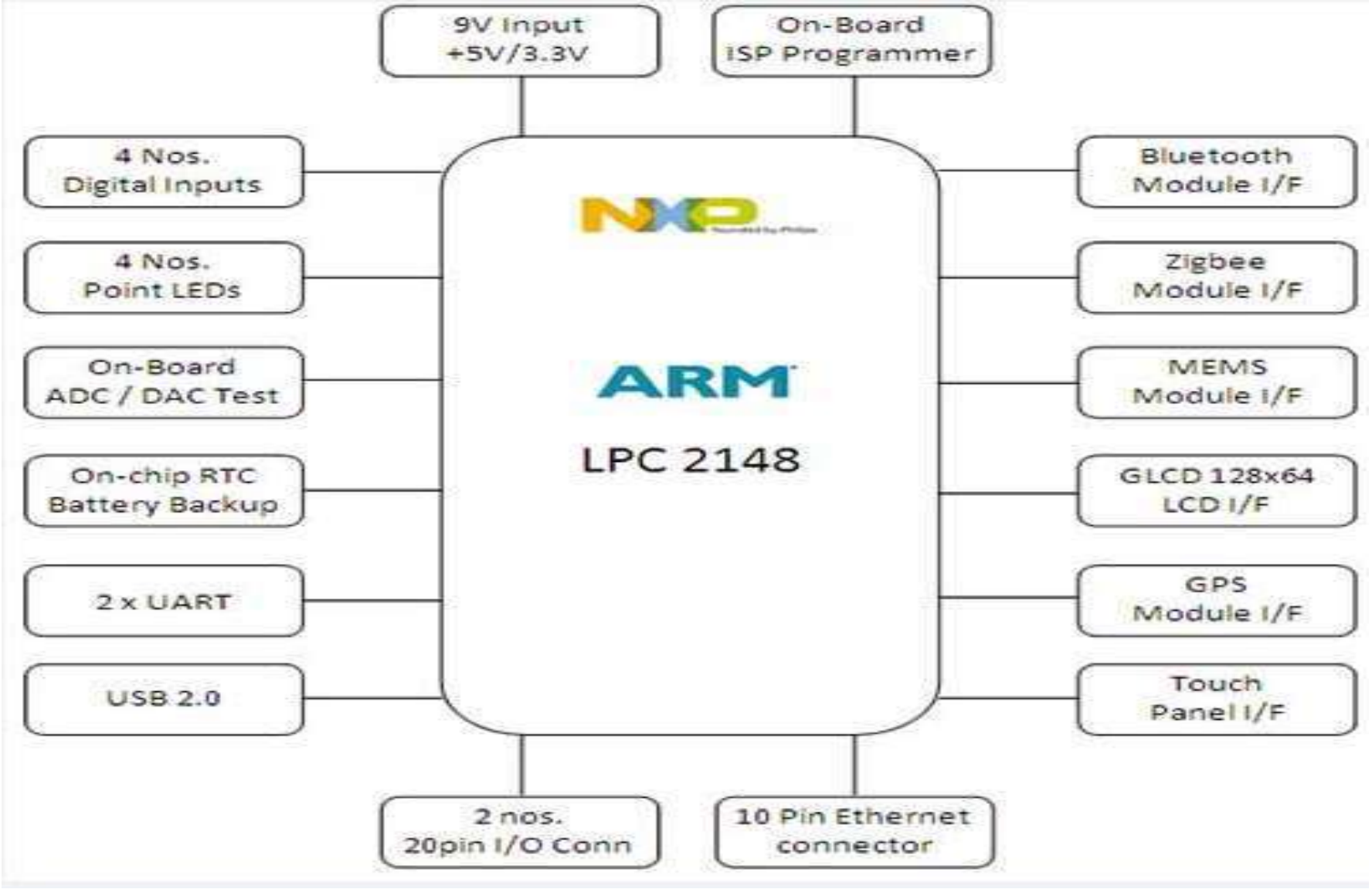
ARM Architecture

- Typical RISC architecture:
  - Large uniform register file
  - Load/store architecture
  - Simple addressing modes
  - Uniform and fixed-length instruction fields
- Enhancements:
  - Each instruction controls the ALU and shifter
  - Auto-increment and auto-decrement addressing modes
  - Multiple Load/Store
  - Conditional execution

ARM Architecture

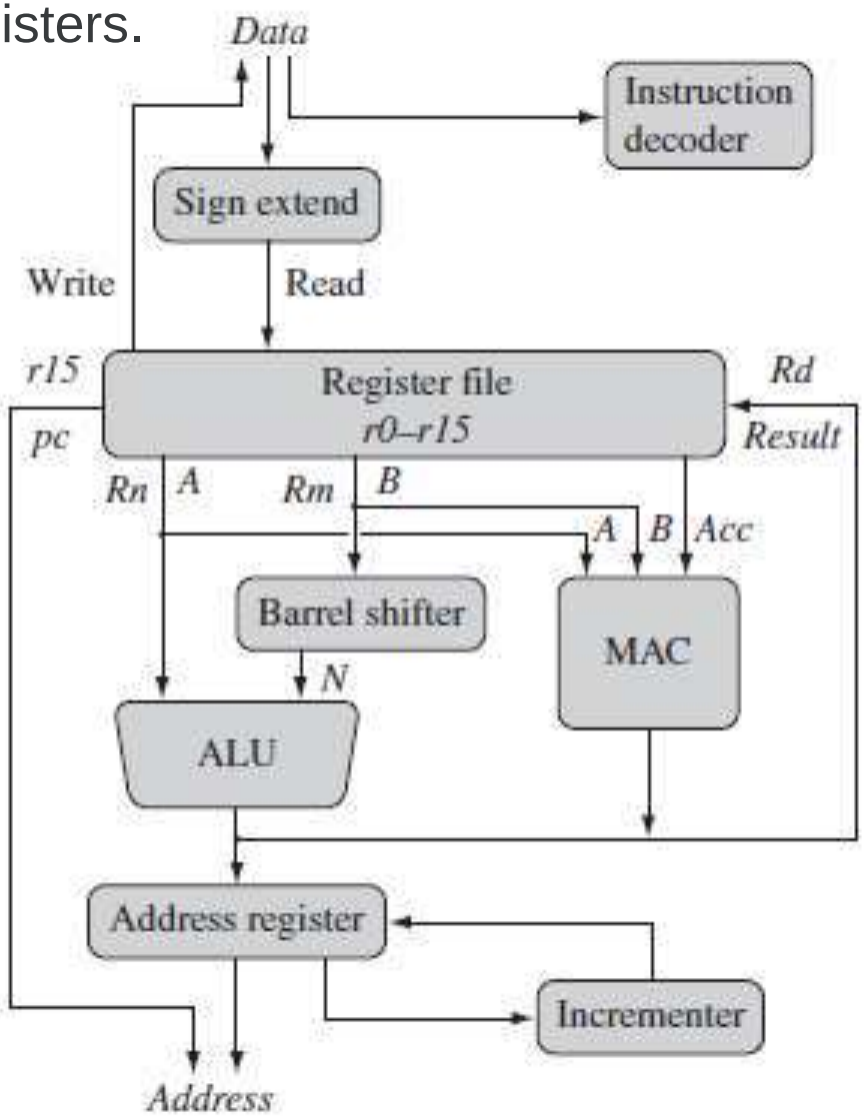
- Current low-end ARM core for applications like digital mobile phones
- TDMI
  - **T**: Thumb, 16-bit instruction set
  - **D**: on-chip Debug support, enabling the processor to halt in response to a debug request
  - **M**: enhanced Multiplier, yield a full 64-bit result, high performance
  - **I**: Embedded ICE hardware
- Von Neumann architecture
- 3-stage pipeline

ARM architecture



Date Flow Model

When an instruction is decoded inside the ARM core and how a particular instruction is executed by interacting with the internal registers file and then send result out of the registers.



Data Sizes and Instruction Sets

- The ARM is a 32-bit architecture.
- When used in relation to the ARM:
  - **Byte** means 8 bits
  - **Half word** means 16 bits (two bytes)
  - **Word** means 32 bits (four bytes)
- Most ARM's implement two instruction sets
  - 32-bit ARM Instruction Set
  - 16-bit Thumb Instruction Set
- Jazelle cores can also execute Java byte code

ARM Registers

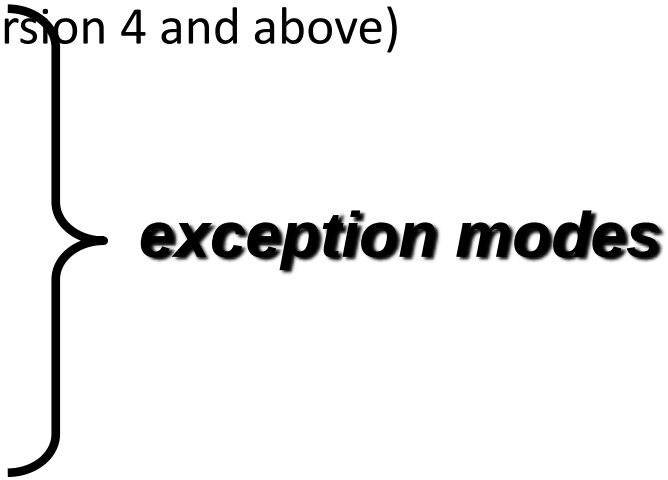
- 31 general-purpose 32-bit registers
- Others speed up the exception process
- 16 Data registers (R0-R15) & one status register (CPSR)
- R0 to R13 are orthogonal general-purpose register.
- Orthogonal means, any instruction that you can apply to ro can equally be applied to any of the other register.

  Eg. ADD ro, r1, r2

  ADD r5, r6, r7
- R13 (stack pointer) and stores the top of the stack in the current processor mode.
- R14(LR) Link Register where the core puts the return address on executing a subroutine.
- R15(PC) Program counter stores the address of next instruction to be executed.
- In ARM state all ARM instruction are 32-bits wide.
- In Thumb state all instructions are 16-bit wide.

Operating Modes

- Seven operating modes:
  - User (Non-Privileged): Only allows read access to the control field in CPSR
  - Privileged: Allow full read and write access of CPSR
    - System (version 4 and above)
    - FIQ
    - IRQ
    - Abort
    - Undefined
    - Supervisor



Operating Modes

User mode

- Normal program execution mode
- System resources unavailable
- Mode changed by exception only

Exception mode

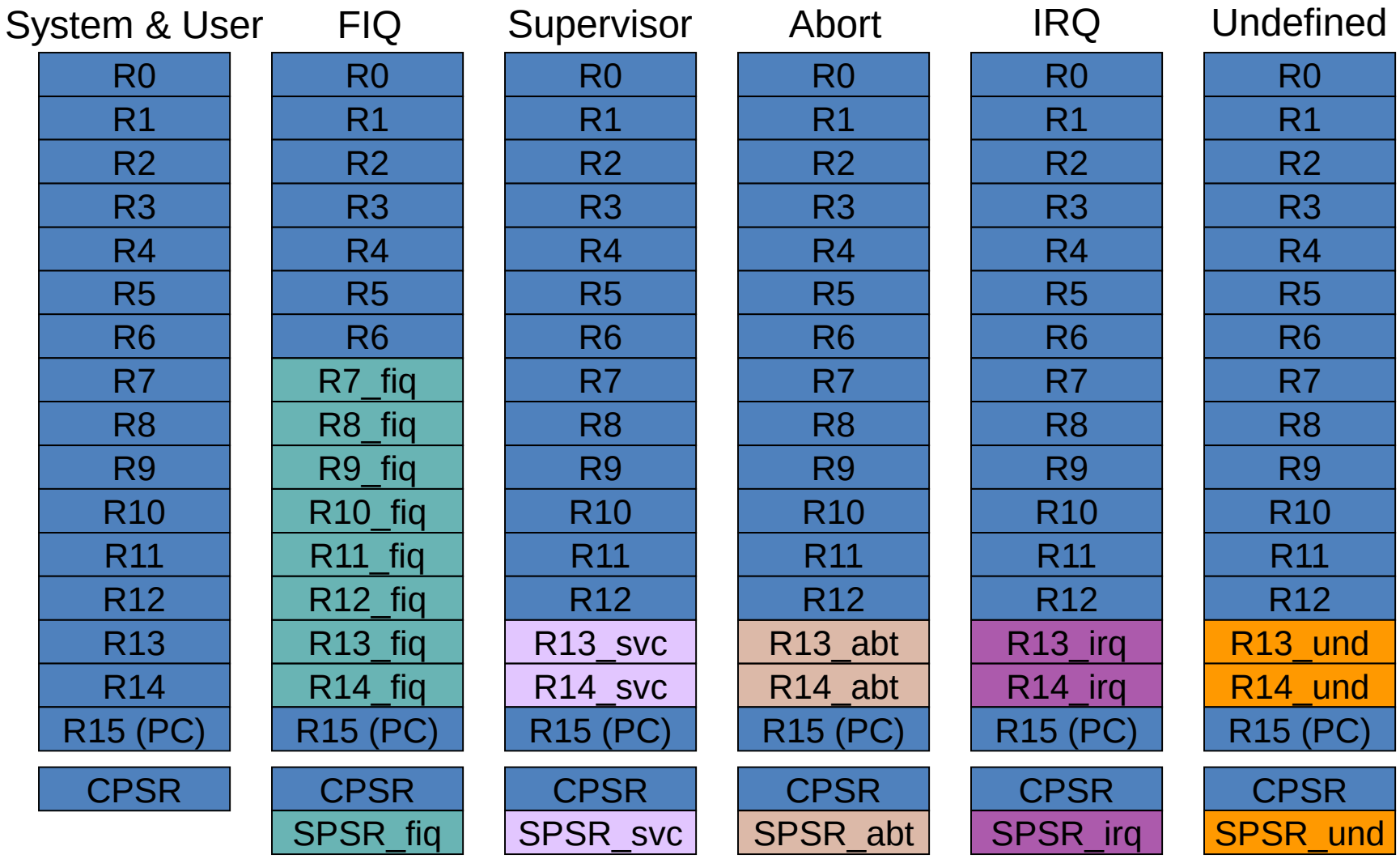
- Entered upon exception
- Full access to system resources
- Mode changed freely

Processor Modes

The ARM has seven basic operating modes:

- **User** : unprivileged mode under which most tasks run
- **FIQ** : entered when a high priority (fast) interrupt is raised
- **IRQ** : entered when a low priority (normal) interrupt is raised
- **Supervisor** : entered on reset and when a Software Interrupt instruction is executed
- **Abort** : used to handle memory access violations
- **Undef** : used to handle undefined instructions
- **System** : privileged mode using the same registers as user mode

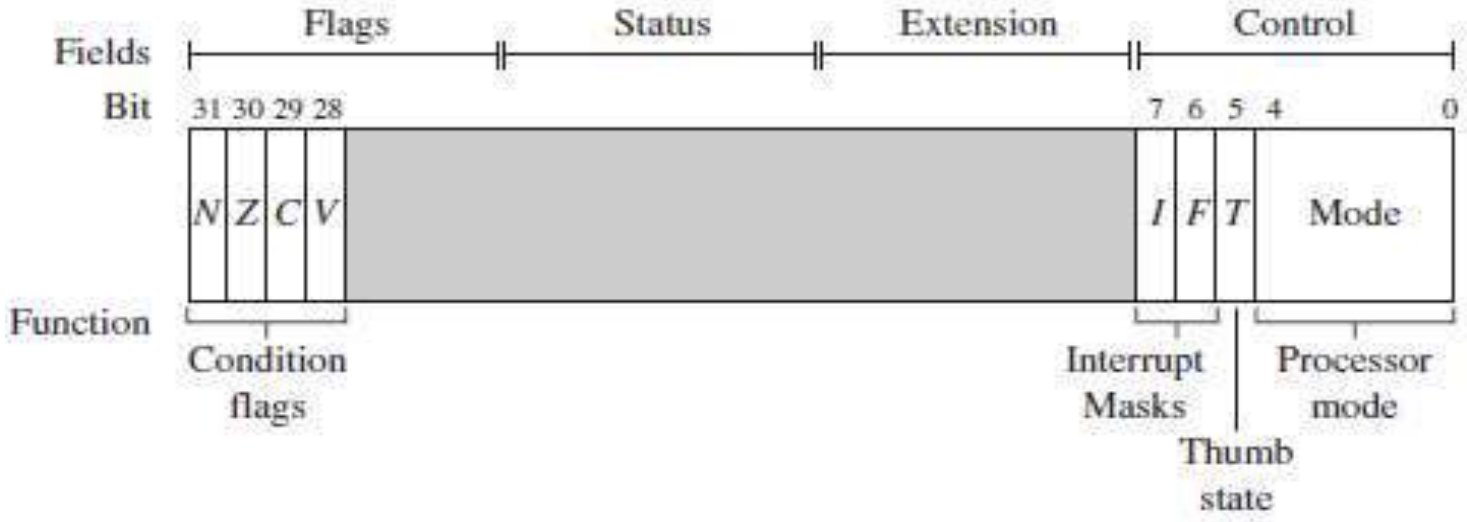
ARM7 Programmer's Model or Register Model



- In total 17(Visible)+20(Banked Rrgisters)=37
- The active registers available in the user mode are shown below.
- This is protected mode which is normally used while executing applications.
- 16 Data registers & one status register
- r0 to r13 are **orthogonal general purpose register.**
- Orthogonal means, any instruction that you can apply to ro can equally be applied to any of the other register.
  - Eg. ADD ro, r1, r2
  - ADD r5, r6, r7
- **R13 (stack pointer)** and stores the top of the stack in the current processor mode.
- **R14(LR) Link Register** where the core puts the return address on executing a subroutine.
- **R15(PC) Program counter** stores the address of next instruction to be executed.
- In ARM state all ARM instruction are 32-bits wide.
- In Thumb state all instructions are 16-bit wide.
- In ARM state Instruction have to be four byte aligned in the memory. Which implies that the bottom two bits of the PC are always zero(Memory location 1000H,1004,1008H).

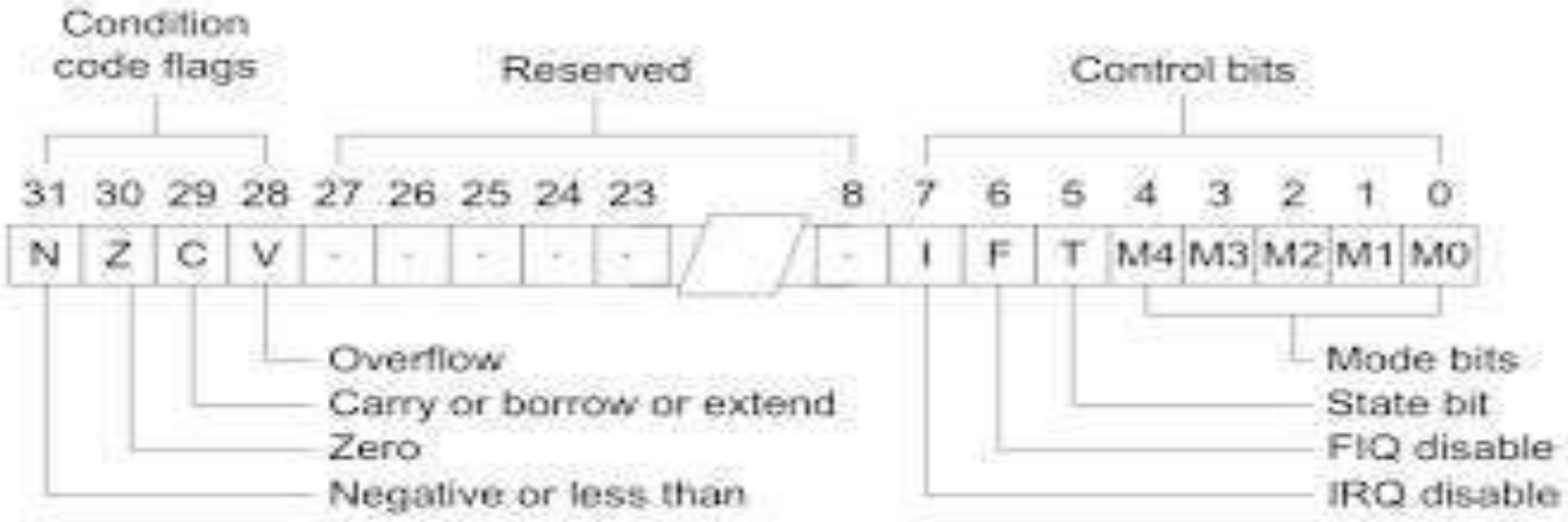
CPSR
CURRENT PROCESSOR STATUS REGISTER

•ARM core uses CPSR to monitor & control internal operations.



•CPSR fields is divided in to four fields,
each 8-bits wide: flags, status, extension, and control.

•In some ARM processor cores have extra bits allocated J bit (available only on Jazelle enabled processing which execute 8-bit instructions).



Flag bit	Sets when
N- Negative	In case of signed no. operations If result MSB=1 ;Indicates the result of operation is NEGATIVE
Z- Zero	The result of operation is zero
C- Carry	The result causes an unsigned carry(carry out of MSB)
V-Overflow	The result causes a signed overflow
Q- Saturation	The result causes an overflow or saturation
I- Interrupt request Disable	If set interrupt request channel is disabled
F- Fast interrupt request Disable	If set fast interrupt request channel is disabled
J- Jazelle instruction set	If set processor will execute Jazelle instructions
T-Thumb instruction set	If set processor will execute Thumb Instruction set

PROCESSOR MODES

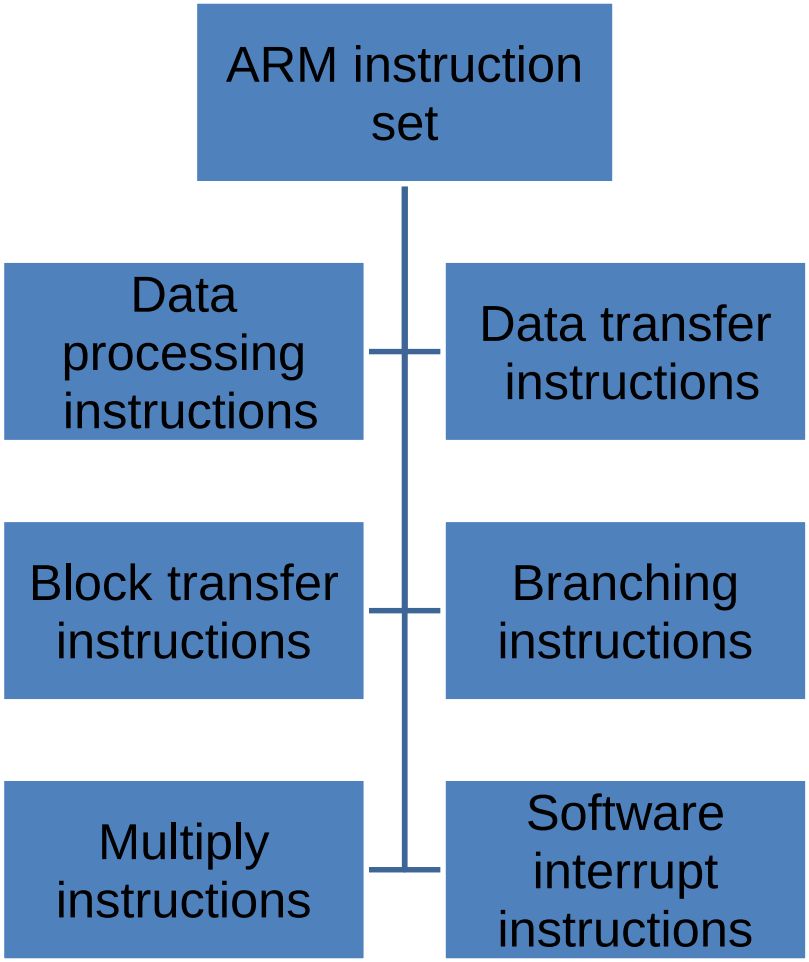
Mode	Abbreviation	Privileged	Mode[4:0]
Abort	abt	yes	10111
Fast interrupt request	fiq	yes	10001
Interrupt request	irq	yes	10010
Supervisor	svc	yes	10011
System	sys	yes	11111
Undefined	und	yes	11011
User	usr	no	10000

Exceptions

Exception	Mode	Priority	IV Address
Reset	Supervisor	1	0x00000000
Undefined instruction	Undefined	6	0x00000004
Software interrupt	Supervisor	6	0x00000008
Pre fetch Abort	Abort	5	0x0000000C
Data Abort	Abort	2	0x00000010
Interrupt	IRQ	4	0x00000018
Fast interrupt	FIQ	3	0x0000001C

Exception types, sorted by Interrupt Vector addresses

ARM Instruction Set



ARM vs THUMB MODE

ARM and Thumb instruction set features.

	ARM (*cpsr* $T = 0$)	Thumb (*cpsr* $T = 1$)
Instruction size	32-bit	16-bit
Core instructions	58	30
Conditional execution[a]	most	only branch instructions
Data processing instructions	access to barrel shifter and ALU	separate barrel shifter and ALU instructions
Program status register	read-write in privileged mode	no direct access
Register usage	15 general-purpose registers +*pc*	8 general-purpose registers +7 high registers +*pc*

Advanced Microcontroller Bus Architecture

- The ARM **Advanced Microcontroller Bus Architecture** (**AMBA**) is an open-standard, on-chip interconnect specification for the connection and management of functional blocks in System-On-Chip(SoC) designs.
- It facilitates development of multi-processor designs with large numbers of controllers and peripherals with a bus architecture.
- AMBA is widely used on a range of ASIC and SoC parts including applications processors used in modern portable mobile devices like smartphones. AMBA is a registered trademark of ARM Ltd.

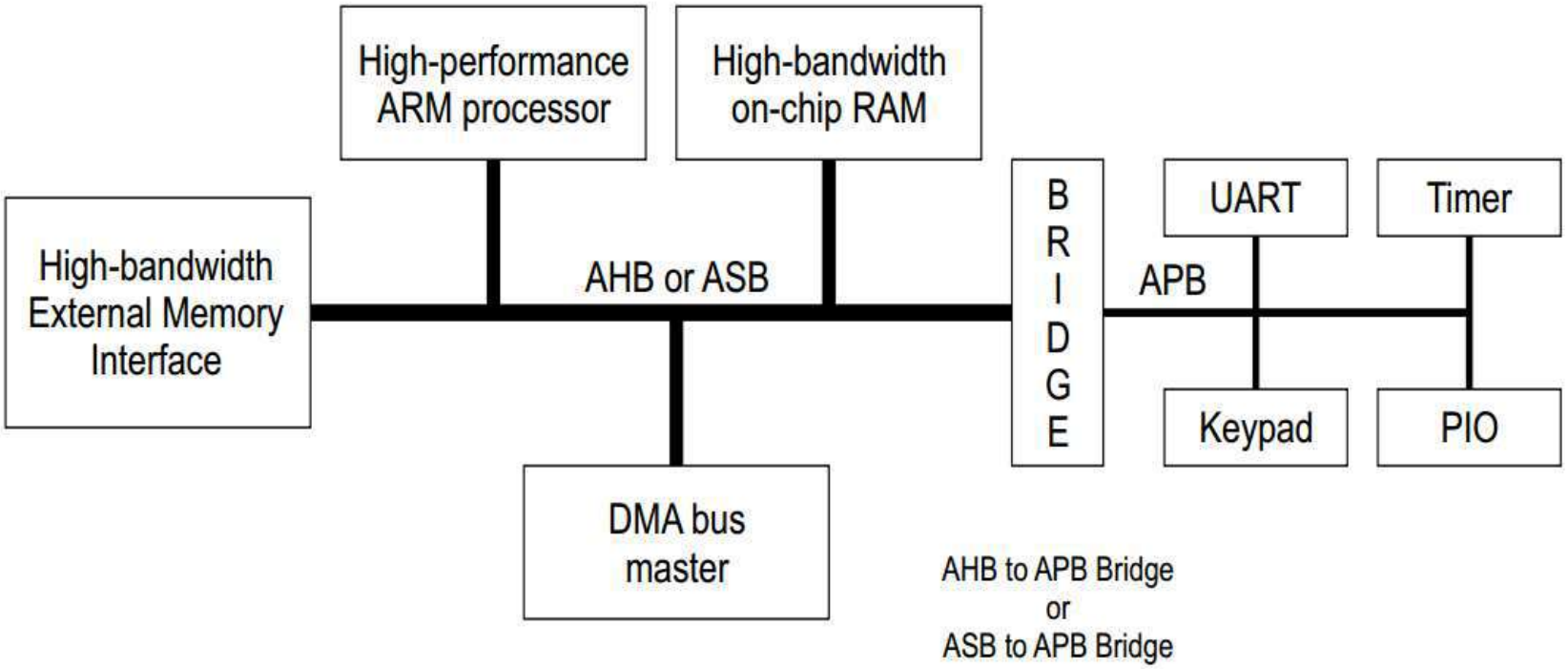
Advanced Microcontroller Bus Architecture

- AMBA was introduced by ARM in 1996. The first AMBA buses were Advanced System Bus (ASB) and Advanced Peripheral Bus (APB).
- In its second version, AMBA 2 in 1999, ARM added AMBA High-performance Bus (AHB) that is a single clock-edge protocol.
- In 2003, ARM introduced the third generation, AMBA 3, including Advanced Extensible Interface (AXI) to reach even higher performance interconnect and the Advanced Trace Bus (ATB) as part of the Core Sight on-chip debug and trace solution.

Advanced Microcontroller Bus Architecture

- In 2010 the AMBA 4 specifications were introduced starting with AMBA 4 AXI4, then in 2011 extending system wide coherency with AMBA 4 ACE.
- In 2013 the AMBA 5 CHI (Coherent Hub Interface) specification was introduced, with a re-designed high-speed transport layer and features designed to reduce congestion.

AMBA BUS


High-performance ARM processor
High-bandwidth on-chip RAM
High-bandwidth External Memory Interface
AHB or ASB
B R I D G E
APB
UART
Timer
Keypad
PIO
DMA bus master
AHB to APB Bridge
or
ASB to APB Bridge

AMBA BUS

- AMBA is a bus standard devised by ARM with aim to support efficient on-chip communications among ARM processor cores.
- AMBA is one of the leading on-chip busing systems used in high performance SoC design.
- AMBA is hierarchically organized into two bus - segments and peripheral bus, mutually connected via bridge that buffers data and operations between them.

AMBA BUS


CHI
Coherent Hub Interface
CHI is a credited coherency protocol, layered architecture for scalability
CHI
ACE
AXI coherency Extensions
ACE is superset of AXI – brings system-wide coherency across multicore clusters
ACE +Lite
ACE5 +Lite
AXI
Advanced eXtensible Interface
AXI supports separate A/D phases, bursts, multiple outstanding addresses, OoO responses
AXI3
AXI4 +Lite, +Stream
AXI5
AHB
Adv. High-performance Bus
AHB supports 64/128 bit, multi-master. AHB-Lite for single masters
AHB
AHB +Lite
AHB5 +Lite
APB
Advanced Peripheral Bus
System bus for low b/w peripherals
APB2
APB3
APB4