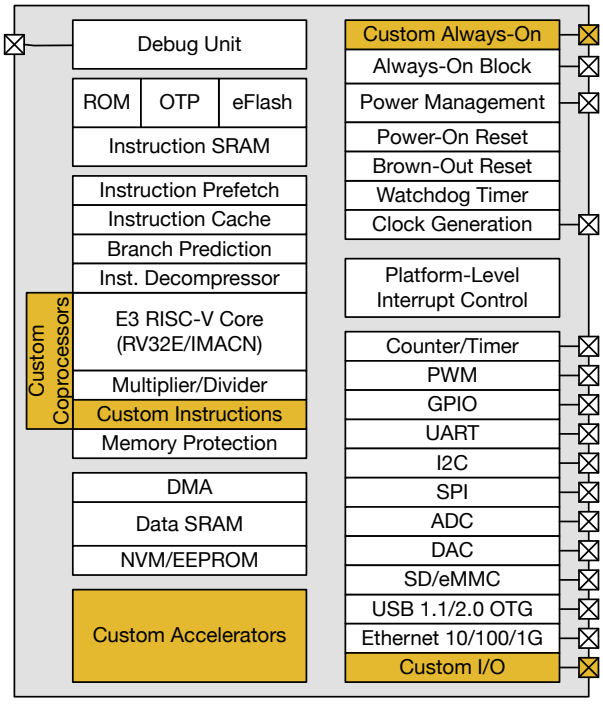
SiFive Freedom E300 Platform

Introduction

The E300 platform is the first member of SiFive's Freedom Everywhere family of customizable RISC-V SoCs. By combining a highly configurable base platform with customer-specific hardware extensions, the Freedom Everywhere family provides low-NRE and rapid time-to-market solutions for performance, cost, and power-sensitive embedded and IoT markets.

Each E300 SoC includes a SiFive E3 RISC-V Core Complex with integrated instruction and data memories, a platform-level interrupt controller, on-chip debug unit, and an extensive selection of peripheral devices. All aspects of the base E300 platform can be flexibly configured. In addition, the platform can be readily extended with customer-specific instruction-set extensions, custom coprocessors, custom accelerators, custom I/O, and custom always-on blocks. The resulting application-specific E300 SoC is optimized for manufacture in a TSMC 180nm process, and delivered as packaged tested parts by SiFive.



Configurable E3 RISC-V Core Complex

The configurable E3 RISC-V Core Complex provides a high-performance single-issue in-order 32-bit execution pipeline, with a peak sustained execution rate of one instruction per clock cycle.

The E3 Core Complex can optionally implement prefetch buffers, and/or an instruction cache to accelerate instruction fetch. A range of static and dynamic branch prediction schemes are available and can be configured to trade off predictability, area, energy, and performance.

Supported RISC-V base ISA variants include RV32E (16 user registers) and RV32I (32 user registers). The RISC-V ISA standard C extension reduces code size and dynamic energy consumption while increasing performance by adding additional 16-bit compressed instruction encodings. The RISC-V ISA standard M extension adds hardware multiply and divide instructions, with a range of performance options including a fully pipelined multiply unit.

To support rich embedded application software functionality on top of a small secure trusted code base, the E3 Core Complex can optionally support the RISC-V N extension, with user mode, user-level interrupts, and physical memory protection.

The E3 Core Complex can be extended with new custom instructions that operate on the existing user registers, or with custom coprocessors containing new registers and new instructions.

All SiFive E3 Core Complexes are guaranteed to be compatible with all applicable RISC-V standards.

Custom Accelerators

Custom autonomous accelerators can be added to provide application-specific processing. The custom accelerators can directly access on-chip memories and peripheral devices, and can generate and receive interrupts from the platform-level interrupt controller.

On-Chip Memory

The on-chip memory system can be flexibly configured to include ROM, OTP, eFLASH, NVM/EEPROM, and/or

SRAM of various sizes.

Peripheral Devices

Peripheral devices can be selected from a large catalog of standard components, including counter/timers, watchdogs, PWM, GPIO, UART, I2C, SPI, ADC, DAC, SD/eMMC, USB 1.1/2.0 OTG, and 10/100/1000 Ethernet. A central autonomous DMA engine can be added to reduce processor overhead in servicing I/O transfers to and from data memory. Third-party peripheral IP can be attached via industry-standard SoC buses or TileLink.

Interrupt Controller

The configurable platform-level interrupt controller supports a large number of inputs and programmable priority levels, and with the addition of the N extension can also support nested interrupt handling for fast interrupt response.

Always-On Block and Power Management

E300 SoCs can be configured with active power management to reduce leakage current in sleep mode. The Always-On Block (AON) supports low-power sleep with wakeup from an internal real-time clock interrupt or external I/O stimulus, or custom always-on circuitry.

Debug Support

Each E300 system includes extensive platform-level debug facilities including hardware breakpoints, watchpoints, and single-step execution accessed via an industry-standard JTAG interface and supported by a full set of open-source debug tools. All components in the system, including the processor, accelerators, memories, peripheral devices, and interrupt controller, can be controlled and monitored over the debug port.

Software Tools

SiFive provides a full open-source RISC-V embedded software development toolchain for E300 SoCs, including modern C and C++ compilers with soft-floating-point support, standard libraries, assemblers, linkers, and the FreeRTOS real-time operating system, together with debug tools to drive the on-chip debug hardware.

E300 FPGA Development Board

E300 FPGA boards with preconfigured designs are available to support development of software and hardware for the E300 platform. Developers can register at `dev.sifive.com`.

Further Information

On request, SiFive can provide additional information on further customization options including compute accelerators, multiprocessor support, hardware floating-point, external memory interfaces, and available packaging technologies.

Proprietary Notice

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