PARUL UNIVERSITY - Faculty of Engineering and Technology

Department of Computer Science & Engineering

SYLLABUS FOR 4th Sem BTech PROGRAMME

Computer Organization & Architecture (203105253)

Type of Course: BTech

Prerequisite: Digital Electronics, Basic Understanding of Computer System.

Rationale: This course is concerned with the structure and behaviour of the various functional modules of Computer and how they interact to provide the processing needs of the user. This course also helps to understand basic instruction formats and parallel processing. It will help to develop their understanding about the organization of computer parts.

Teaching and Examination Scheme:

Teaching Scheme			Credit	Examination Scheme					Total
				External		Internal			
Lect Hrs/	Tut Hrs/	Lab Hrs/		T	P	T	CE	P	
3	0	0	3	60	-	20	20	-	100

Lect - Lecture, **Tut** - Tutorial, **Lab** - Lab, **T** - Theory, **P** - Practical, **CE** - CE, **T** - Theory, **P** - Practical

Contents:

Sr.	Topic	Weightage	Teaching Hrs.
1	**FUNCTIONAL BLOCKS OF A COMPUTER:**: CPU, memory, input-output subsystems, control unit. Instruction set architecture of a CPU–registers, instruction execution cycle, RTL Interpretation of instructions, addressing modes, instruction set. Case study – instruction set of some common CPUs	15%	7
2	**DATA REPRESENTATION**: Signed number representation, fixed and floating point representations, Character representation. Computer arithmetic – integer addition and Subtraction, ripple carry adder, carry look-ahead adder, etc. multiplication – shift-and add, Booth multiplier, carry save multiplier, et c. Division restoring and non-restoring techniques, floating point arithmetic.	20%	9

3	**INTRODUCTION TO X86 ARCHITECTURE:**: **CPU CONTROL UNIT DESIGN:** hardwired and micro-programmed design approaches, Case study – design of a simple hypothetical CPU. **MEMORY SYSTEM DESIGN:** Semiconductor memory technologies, memory organization.	15%	7
4	**PERIPHERAL DEVICES AND THEIR CHARACTERISTICS:**: Input-output subsystems, I/O device interface, I/O transfers–program controlled, interrupt driven and DMA, privileged and non-privileged instructions, software interrupts and exceptions. Programs and processes–role of interrupts in process state transitions, I/O device interfaces – SCII, USB	15%	7
5	**PIPELINING::**: Basic concepts of pipelining, throughput and speedup, pipeline hazards. **PARALLEL PROCESSORS:** Introduction to parallel processors, Concurrent access to memory and cache coherency.	15%	7
6	**MEMORY ORGANIZATION:**: Memory organization: Memory interleaving, concept of hierarchical memory organization, cache memory, cache size vs. block size, mapping functions, replacement algorithms,write policies	20%	9

***Continuous Evaluation:**

It consists of Assignments/Seminars/Presentations/Quizzes/Surprise Tests (Summative/MCQ) etc.

Reference Books:

1. Computer Organization and Design: The Hardware/Software Interface
   David A. Patterson and John L. Hennessy, Elsevier; 5th Edition
2. Computer Organization and Embedded Systems
   CarlHamacher; McGraw Hill Higher Education.; 6th Edition
3. Computer Architecture and Organization
   John Hayes; McGraw-Hill
4. Computer Organization and Architecture: Designing for Performance
   William Stallings; Pearson Education; 10th Edition
5. Computer System Design and Architecture
   Vincent P. Heuring and Harry F. Jordan; Pearson Education; 2nd Edit ion

Course Outcome:

After Learning the course the students shall be able to:

1. Draw the functional block diagram of a single bus architectureofacomputeranddescribethefunctionofthe instruction execution cycle, RTL interpretation ofinstructions, addressing modes, instruction set.

2. Write assembly language program for specified microprocessor for computing16 bit multiplication, division and I/O device interface (ADC, Control circuit, serialport communication).

3. Write a flowchart for Concurrent access to memory and cache coherency in ParallelProcessors and describe the process.

4. Given a CPU organization and instruction, design a memory module and analyze its operation by inter facing wit h t he CPU.
5. Given a CPU organization, assess its performance, and apply design techniques to enhance performance using pipelining, parallelism and RISC methodology