CS & IT

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Computer Organization & Architecture

Instruction & Addressing Modes

DPP: 1

Q1 Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. How many memory locations are required to store each instruction in the memory?

Q2 Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. If a program has 500 instructions, which is stored in the memory then the amount of memory required to store the entire program is _____ bytes?

Q3 The word addressable memory of a computer has 256K words of 32-bit each. The computer has an instruction format with four fields; an operation code field, a mode field to specify one of 8 addressing modes, a register address field to specify one of the 64 processor registers and a memory address field.
The bits for each field required in instruction format if the instruction is stored exactly in one word in memory?
(A) Opcode: 5, Addressing mode: 3, Register: 6, Memory address: 20
(B) Opcode: 3, Addressing mode: 3, Register: 6, Memory address: 20
(C) Opcode: 5, Addressing mode: 3, Register: 6, Memory address: 18
(D) Opcode: 3, Addressing mode: 3, Register: 6, Memory address: 18

Q4 A digital computer has a memory unit with 32-bits per word. The instruction set consists of 240 different operations. All the instructions have an operation code part (opcode) and an address part (allowed for only 1 address). Each instruction is stored in one word of memory. The maximum allowable size of memory (word addressable) is _____Mbytes?

Q5 Consider a system which supports 2-address and 1-address instructions. The system uses 16 bits instructions and 5-bits addresses. If there are total 32 2-address instructions then maximum how many 1-address instructions can be formulated?

Q6 Consider a system which supports 3-address, 2-address and 1 -address instructions. It has 32-bit instructions with 8-bits addresses. If there are 254 3-address instructions and 1024 1-address instructions, then maximum how many 2-address instructions can be formulated?

Q7 Consider a system which supports 2-address and 1-address instructions. The system has 18 bits instructions. If there are 7 2-address instructions and 1152 1-address instructions, then the maximum size of memory supported by system is _____bytes?

Q8 Consider a system which supports 2-address, 1-address and 0-address instructions. The system

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has 'i' bits instructions and 'a' bits addresses. If there are 'x' 2-address instructions and 'y' 1-address instructions then which of the following is correct for maximum number of 0-address instructions supported by system?

(A) $2^i - 2^a x - y$

(B) $2^i - 2^{2a} x - y$

(C) $2^i - 2^{2a} x - y2^a$

(D) $2^i - 2^a x - y2^a$

Q9 Consider there are 4 types of instructions in system:

Type 1: One opcode and 2 registers

Type 2: One opcode and 1 register

Type 3: One opcode and 1 memory address

Type 4: One opcode, 1 register and 1 memory address

Number of registers in CPU = 128

Maximum instruction length: 32bits (Variable length instructions supported)

Total Instructions: Type-1: 15, Type-2: 20, Type-3: 12, Type-4: 14

Maximum memory address size = _____ bits

Q10 Consider a register-based architecture system which can support maximum 2-address instructions. For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?

```
t1 = X + Y
t2 = Z * 2
t3 = t2 + A
t4 = t3 – t1
t5 = t4 + t3
```

Note: X, Y, A and Z are memory operands; and consider first operand as destination operand and there is no any optimization done by compiler.

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Answer Key

Q1	2
Q2	4000
Q3	(C)
Q4	64~64
Q5	1024~1024
Q6	508~508
Q7	128~128
Q8	(C)
Q9	19~19
Q10	3

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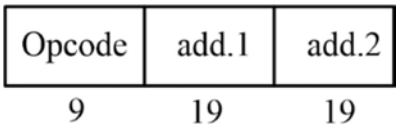
Hints & Solutions

Q1 Text Solution:

Number of words in memory = 2MB/4B = 512K = 2^{19}, hence memory address size = 19-bits

Instruction format will be like:



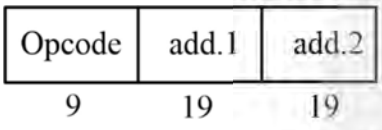
Instruction length = 9 + 19 + 19 = 47 bits

To store 47 bits, 2 addresses in memory required. Because in memory as given in question at one address one word of 4bytes (32 bits) only can be stored.

Q2 Text Solution:

Number of words in memory = 2MB/4B = 512K = 2^{19}, hence memory address size = 19-bits

Instruction format will be like:



Instruction length = 9 + 19 + 19 = 47 bits

To store 47 bits, 2 addresses in memory required. Because in memory as given in question at one address one word of 4bytes (32 bits) only can be stored.

To store 500 instructions, 500 × 2 = 1000 locations are required. Hence 1000 × 4Bytes = 4000 bytes space is needed in memory.

Q3 Text Solution:

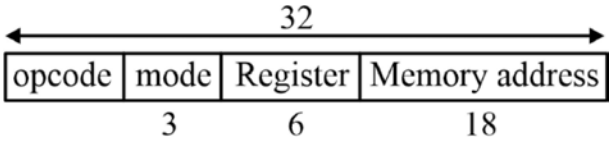
Number of words in memory = 256k= 2^{18}, hence address size = 18 bits

Number of registers = 64, hence register field has 6 bits

Number of modes = 8, hence bits for modes = 3 bits

Instruction is stored on exactly 1 word in memory. Hence instruction length = 32 bits

Instruction format will be as follows:



Bits in opcode = 32 – (3+6+18) = 5 bits

Q4 Text Solution:

Number of distinct instructions supported = 240, hence number of bits in opcode = 8 bits

Instruction is stored on exactly 1 word in memory. Hence instruction length = 32 bits

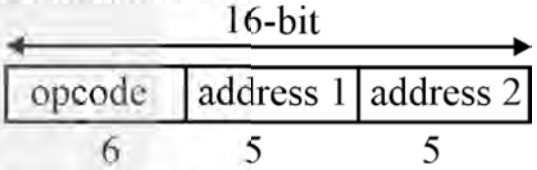
Number of bits for address = 32 – 8 = 24 bits

Number of addresses in memory = 2^{24}

Size of memory = 2^{24} * 32 bits = 2^{24} * 4 bytes = 2^{26} bytes = 64 Mbytes

Q5 Text Solution:

2-address instruction format:

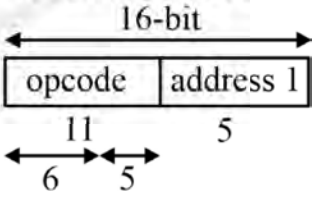


Max number of opcode combinations = 2^6 = 64

Used opcodes = 32

Unused = 64 – 32 = 32

1-address instruction format



Maximum number of 1-address instructions = 32 × 2^5 = 1024

Q6 Text Solution:

Assume there are x 2-address instructions used.

3-address instruction format:

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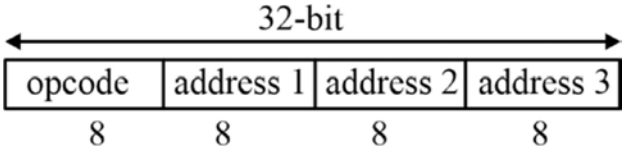
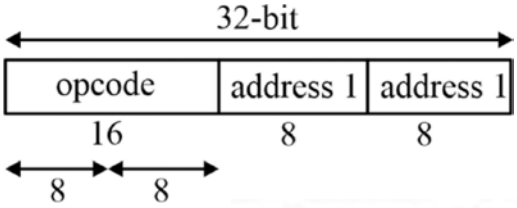


Maximum 3 address instructions = 2^8 = 256

Used 3 address instructions = 254

Unused opcodes = 265-254 = 2

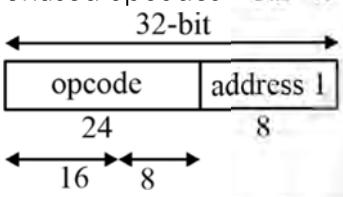
2-address instruction format:



Maximum 2 address instructions = 2^*2^8 = 512

Used 2 address instructions = x

Unused opcodes = 512– x



1-address instruction format:

Maximum 1 address instructions = (512 – x) × 2^8

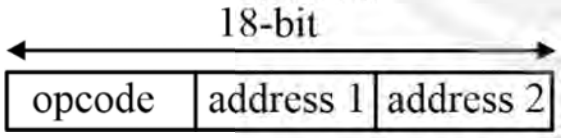
Given 1-address instructions = 1024,

Hence (512 – x) ×2^8 = 1024

x = 508

Q7 Text Solution:

2-address instruction format:



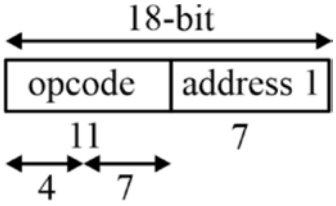
As given number of 2 address instructions = 7, hence opcode must have atleast 3 bits, but if we use 3 bits opcode then for both the addresses 15-bits are remaining, and 15-bits can't be distributed in 2 equal parts. Hence we will start with opcode as 4-bits, so that each address can have 7-bits equally.

Maximum 2 address instructions = 2^4 = 16

Used 2 address instructions = 7

Unused opcodes = 16 – 7 = 9

1-address instruction format:



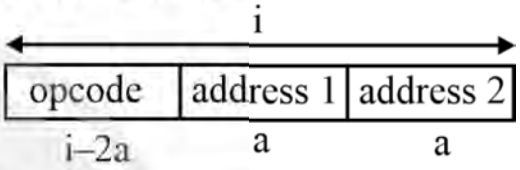
Maximum 1 address instructions = 9 × 2^7 = 1152, which is matching with given data question.

Hence memory address length is 7-bits.

Memory size = 2^7 bytes =128 bytes

Q8 Text Solution:

2-address instruction format:

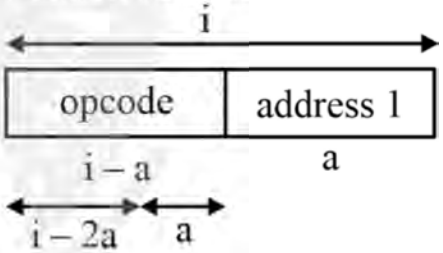


Maximum 2 address instructions = 2^{i-2a}

Used 2 address instructions = x

Unused opcodes = (2^{i-2a}) – x

1-address instruction format:



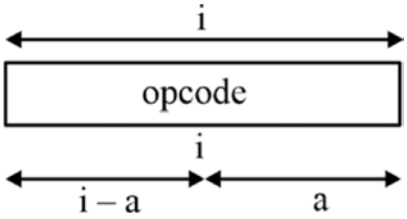
Maximum 1 address instructions = $(2^{i-2a} - x) \times 2^a$

= $2^{i-a} - x2^a$

Used 1 address instructions = y

Unused opcodes = $2^{i-a} - 2x^a - y$

0-address instruction format:



Maximum 0 address instructions = = $(2^{i-a} - x2^a - y) \times 2^a$

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$= 2^i - x2^{2a} - y2^a$

Q9 Text Solution:

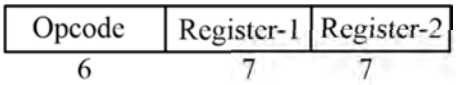
Number of registers = 128, hence register field in instruction will have 7 bits

As given in question that the variable length instructions are supported, hence for all types of instructions, opcode size will be fixed.

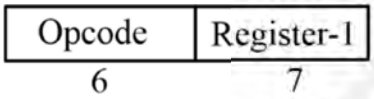
Total number of instructions = 15 + 20 + 12 + 14 = 61, hence opcode will have 6 bits

Type 1 Instruction format

Instruction length of type 1 = 6+7+7=20 bits

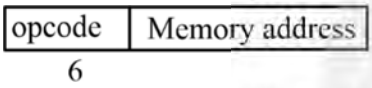


Type 2 Instruction format



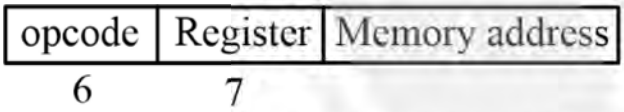
Instruction length of type 2 = 6+7=13 bits

Type 3 Instruction format



Here memory address is not known.

Type 4 Instruction format



Here also memory address is not known. If assuming type 3 uses maximum size instruction of 32-bits, then memory address size will be = 32 – 6 =26 bits.

But 26-bits memory address will make type 4 instruction size = 6 + 7 + 26 = 39 bits which is larger than given maximum instruction size of 32 bits. Hence Type 4 should use maximum instruction size of 32 bits and memory address will be length = 32 – (7+6) = 19 bits.

Based on it type 3 instruction length will be = 6 + 19 = 25 bits

Q10 Text Solution:

Following will be instructions generated for the given basic block:

R1 ← X

R2 ← Y

R1 ← R1 + R2

R2 ← Z

R2 ← R2 * 2

R3 ←A

R2 ← R2 + R3

R3 ← R2

R3 ← R3 – R1

R3 ← R3 + R2

Total number of registers needed = 3