CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Cache Organization

Lecture No.- 07

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Recap of Previous Lecture

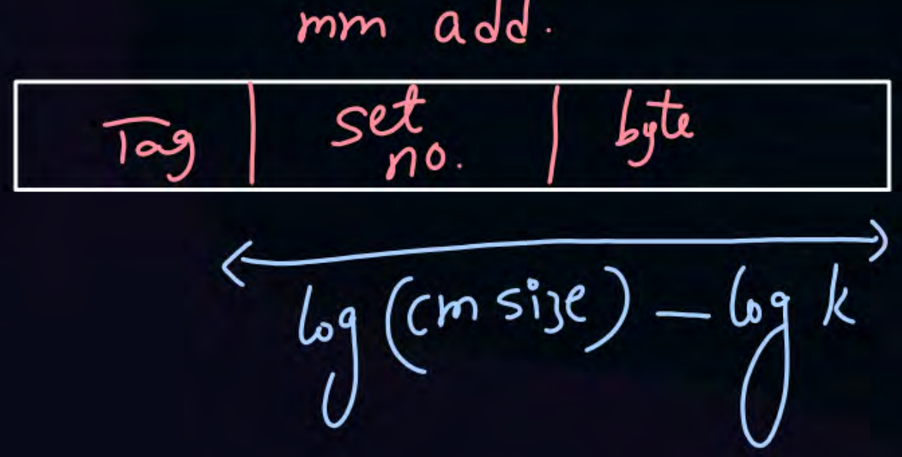
Topic Direct Mapping

Topic Set Associative Mapping

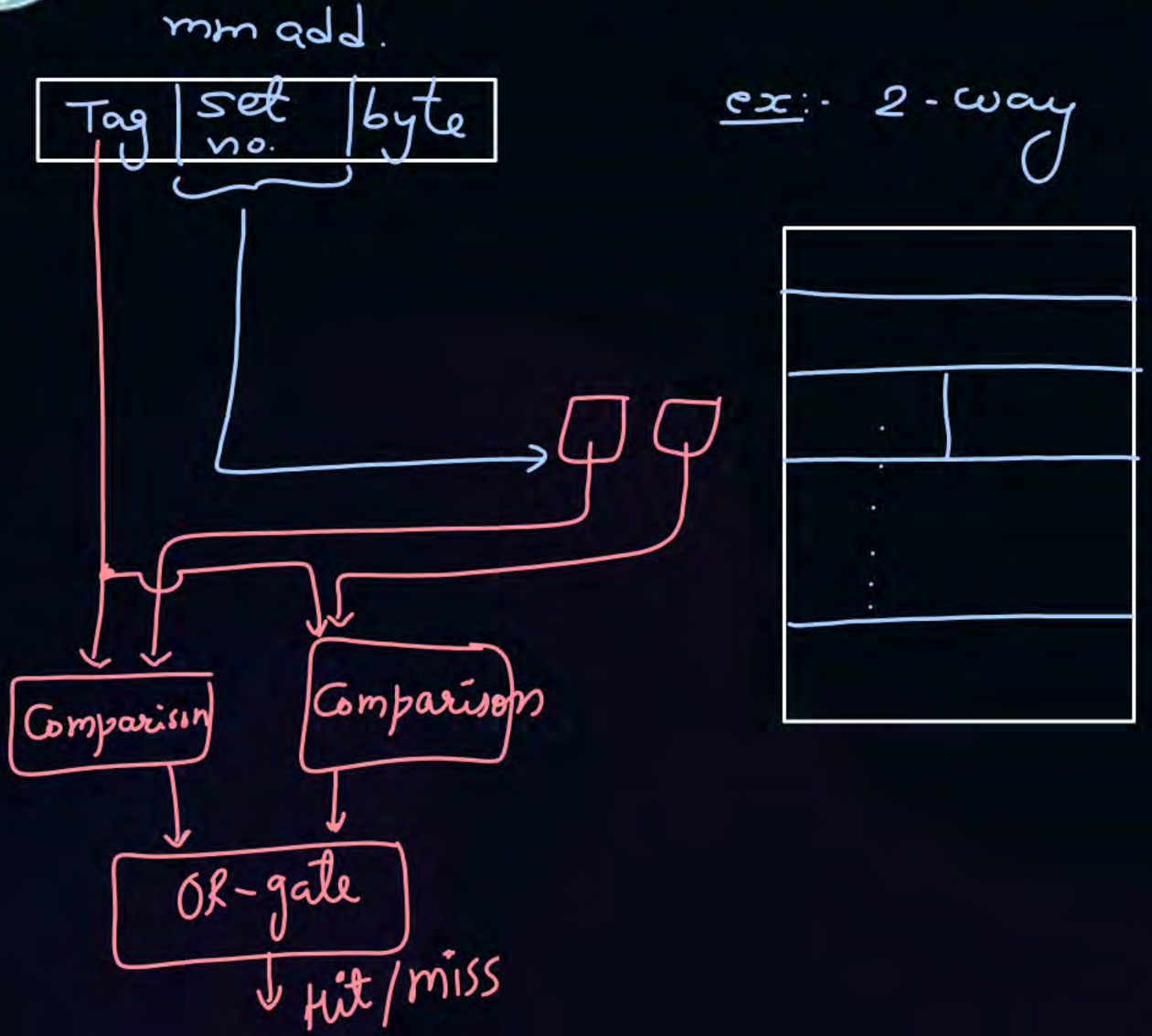
Topics to be Covered

Topic Fully Associative Mapping

Topic Set Associative Mapping

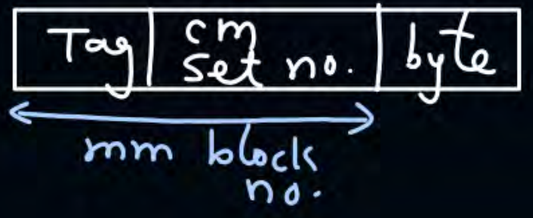


Topic : Checking Hit/Miss in Set Associative Mapping



Topic : Calculating CM Set Number from MM Address

If mm add. given in binary ⇒



Convert

—"— in hexadecimal

If mm add. given in decimal ⇒

mm block no. = ⌊mm add. / block size⌋

byte = mm add. % block size

Tag = ⌊mm block no. / no. of sets in cm⌋

cm set no. = mm block no. % no. of sets in cm

[MCQ]

$\rightarrow 2^{24}$ B $\Rightarrow$ mm add. = 24 bits

#Q. A computer system with a word length of 32 bits has a 16 MB byte- addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four physical addresses represented in hexadecimal notation.

A1 = 0x42C8A4 — 11 00 1000 $\Rightarrow$ set no. $(8)_{10}$

A2 = 0x546888 — 01 10 1000 $\Rightarrow$ set no. $(40)_{10}$

A3 = 0x6A289C — 00 10 1000 $\Rightarrow$ set no. $(40)_{10}$

A4 = 0x5E4880 — 01 00 1000 $\Rightarrow$ set no. $(8)_{10}$

Which one of the following is TRUE?

mm add. — 24

Tag	set	byte
10	6	8

$\log 2^{16} - \log 4$

$= 16 - 2$

14

A ✗ A1 and A4 are mapped to different cache sets.

C ✓ A2 and A3 are mapped to the same cache set.

A ✗ A3 and A4 are mapped to the same cache set.

C ✗ A1 and A3 are mapped to the same cache set.

Topic : Fully Associative Mapping

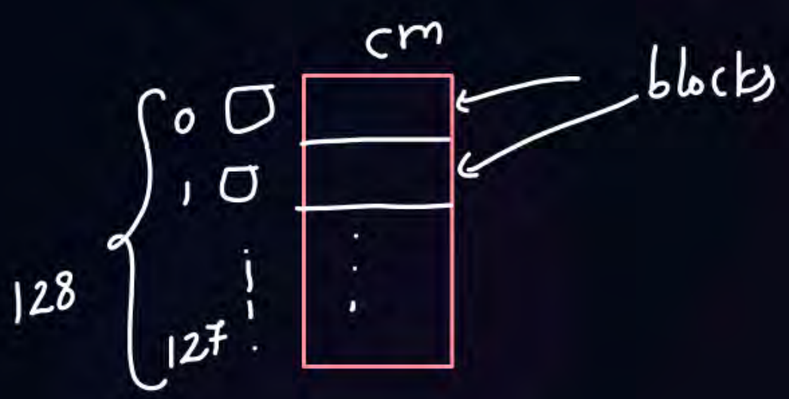
Ex:-

Direct:-

no. of blocks in cm = $2^7 = 128$

mm add.

Tag	cm block	byte
y	7	x

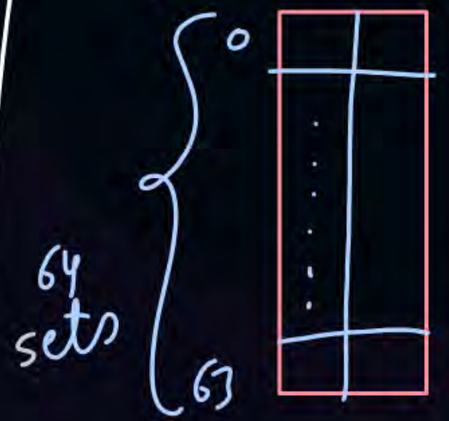


2-way :-

no. of sets = $\frac{128}{2} = 64$

mm add.

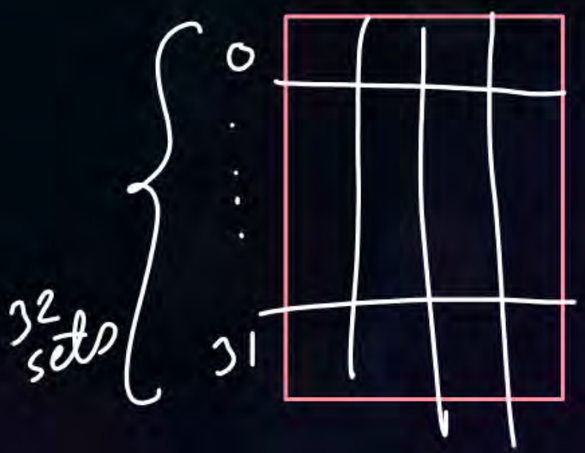
Tag	cm set no.	byte
y+1	6	x



4-way :-

no. of sets = $\frac{128}{4} = 32$

Tag	set	byte
y+2	5	x



Topic : Fully Associative Mapping

max possible associativity → fully associative mapping

⇒

all cm blocks are organized under single set!

$\log_2 1 = 0$

⇒ Index is zero here.

Tag directory size = no. of blocks in cache * (Tag + extra bits)

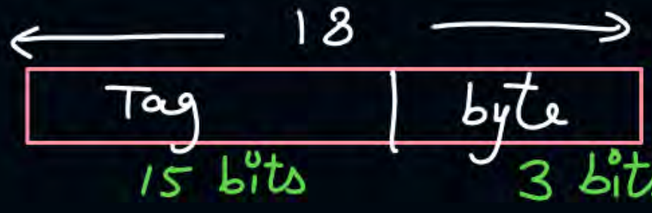
---

ex:- cm size = 1kB

block size = 8 bytes = 2^3

mm add. = 18 bits

fully associative



Tag directory size = 2^7 * 15 bits

no. of blocks in cm = $\frac{1kB}{8B}$

$= \frac{2^{10}}{2^3} = 2^7$

Question

Cache Size = 16MB

MM address = 40 bits

Block size = 64 bytes $= 2^6$ B

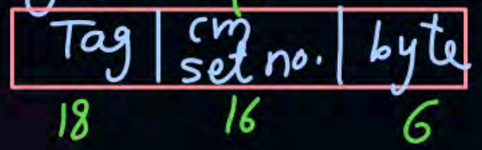
$$\text{no. of blocks in cm} = \frac{16\text{MB}}{64\text{B}} = \frac{2^{24}}{2^6} = 2^{18}$$

$$\text{no. of sets in cm} = \frac{2^{18}}{4} = 2^{16}$$

Calculate index, tag, tag directory size for direct, 4-way set associative and fully associative mappings?

Direct

4-way :-



Fully :-

	Direct	4-way set ass.	fully
Index	18 bits	16 bits	0
Tag	16 bits	18 bits	34 bits
Tag directory	$2^{18} * 16$ bits	$2^{18} * 18$ bits	$2^{18} * 34$ bits

Topic : Cache Mappings

	Index	Tag
Minimum	Fully ass.	Direct
Maximum	Direct mapping	fully

and tag directory size

Ques) Consider a fully associative cache with no. of block is cache 2^{12}. The main mem. contains 2^{24} no. of blocks. The tag directory size required in cache ?

Soln

> for fully ass. mapping mm block no. itself is Tag.

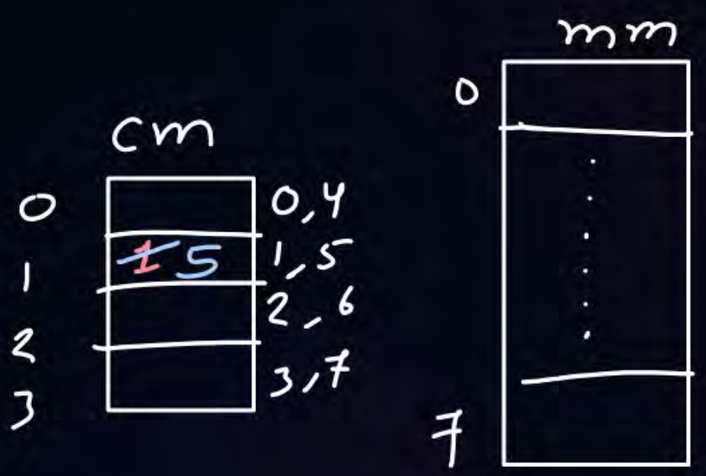
Tag directory size = $2^{12} * 24$ bits

Topic : Block Replacement

Direct mapping :-

cm ⇒ 4 blocks

mm ⇒ 8 blocks



CPU Req :-

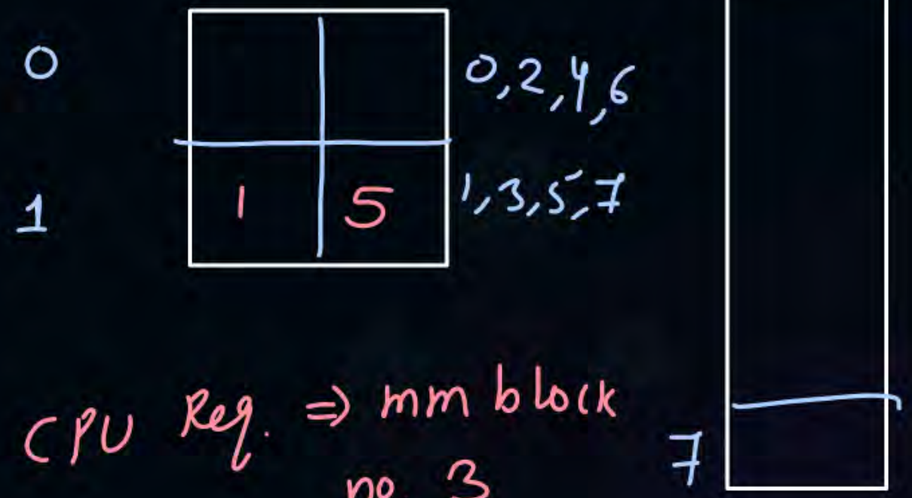
mm block no.

1, 5

↓ ↘

miss miss but it replaces block 1

2-way set associative :-



CPU Req. ⇒ mm block no. 3

⇓

need a replacement policy.

Direct mapping ⇒ no any replacement policy needed

set ass. & fully ass. ⇒ Replacement policy needed

Replacement policy :-

LRU (Least Recently Used) is implemented.

⇓

Replace block which has not been used since longest period of time.

[MCQ]

#Q. Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is:

8, 12, 0, 12, 8

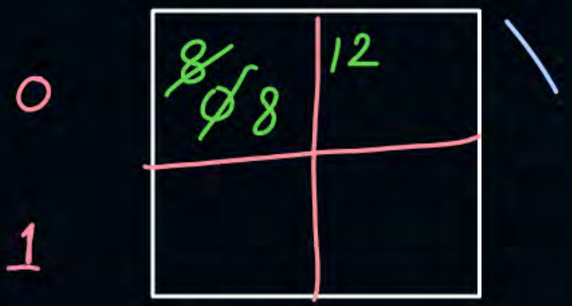
miss miss miss miss

no. of sets = $\frac{4}{2} = 2$

8 % 2 = 0

12 % 2 = 0

0 % 2 = 0



A 2

B 3

C 4

D 5

[MCQ]

#Q. Consider a Direct Mapped Cache with 8 cache blocks (numbered 0-7). If the memory block requests are in the following order

3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24.

Which of the following memory blocks will not be in the cache at the end of the sequence?

A 3

B ✓ 18

C 20

D 30

cm block no.
= (mm block no.) % no. of blocks in cm

3 % 8 ⇒ 3
5 % 8 ⇒ 5

[MCQ]

H.W.

#Q. Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 block and the request for memory blocks is in the following order:

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155

Which one of the following memory block will not be in cache if LRU replacement policy is used?

A 3

B 8

C 129

D 216

[MCQ]

H.W.

#Q. Consider a fully associative cache with 8 cache blocks (numbered 0–7) and the following sequence of memory block requests:

4,3,25,8,19,6,25,8,16,35,45,22,8,3,16,25,7

If LRU replacement policy is used, which cache block will have memory block 7?

A 4

B 5

C 6

D 7

2 mins Summary

Topic Set Associative Mapping

Topic Fully Associative Mapping

Happy Learning

THANK - YOU