Batch: English

Subject : Digital Electronics

DPP-05

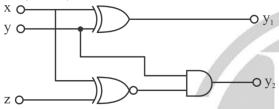
Chapter: Combinational Circuit

Topic: HS, FS, Serial Adder

[MCQ]



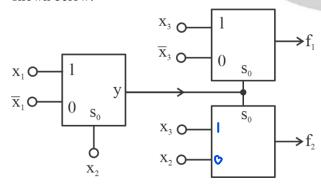
1. The circuit shown below, is a controlled half adder/half subtractor. The inputs to half adder/half subtractor are x and y while z is a control. The outputs are y₁ and y₂.



- (a) Half adder for z = 0
- (b) Half subtractor for z = 1
- (c) Half adder for z = 1 and half subtractor for z = 0
- (d) Half adder regardless of whether z = 0 or z = 1 due to design defect.

Statement for question 2 & 3.

Three multiplexer of size 2×1 , are interconnected as shown below:



[MCQ]



- **2.** The function f_1 and f_2 are
 - (a) $f_1 = (x_1 \oplus x_2)x_3$ and $f_2 = x_1\overline{x}_2 + x_1\overline{x}_3 + x_2x_3$
 - (b) $f_1 = x_1 \oplus x_2 \oplus x_3$ and $f_2 = \overline{x_1}x_2 + \overline{x_1}x_3 + x_2x_3$
 - (c) $f_1 = \overline{(x_1 \oplus x_2 \oplus x_3)}$ and $f_2 = x_1 x_2 + x_1 x_3 + x_2 x_3$
 - (d) $f_1 = x_1(x_2 \oplus x_3)$ and $f_2 = x_1x_2 + x_1x_3 + \overline{x_2}$

[MCQ]

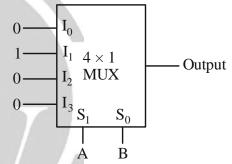


- **3.** What is this circuit?
 - (a) Full adder
- (b) Full subtractor
- (c) Magnitude comparator (d) Priority encoder

[MCQ]



4. The output of the following circuit diagram represents



- (a) Borrow of half subtractor
- (b) Carry of Half Adder
- (c) Sum of half adder
- (d) None of them

[MCQ]



5. The design of a combinational logic circuit with three inputs x, y, z and three outputs A, B, C is attempted. The constraint is that designer has only HA, HS, FA and FS units only in his inventory.

When the binary input is 0, 1, 2 or 3 the binary output is same as input and when binary input is 4, 5, 6 or 7 the binary output is 2 less than binary input. What completes the design?

- (a) One FA and one HS
- (b) One HA and one HS
- (c) One HA only
- (d) One FA only

[NAT]



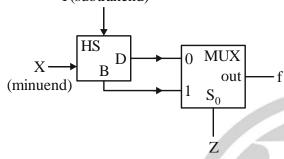
6. A serial adder is operating with a clock frequency of 10 MHz. The time required to sum 1011011 and 10110 is _____ (in μsec)

[MCQ]



A half subtractor (HS) and 2 × 1 MUX are interconnected as demonstrated below. What is NOT correct about this circuit?

Y(subtrahend)



- (a) For Z = 0, f = 1 indicates that the minuend and the subtrahend bits are different.
- (b) For Z = 0, f = 0 indicates that minuend and subtrahend bits are same, that is, X = Y = 0 or X = Y = 1.
- (c) For Z = 1, f = 1 indicates that X < Y.
- (d) For Z = 1, f = 0 indicates that subtrahend bit is definitely 0.

[MCQ]



- **%.** What does minuend and subtrahend denotes in a subtractor?
 - (a) Their corresponding bits of input
 - (b) Its output
 - (c) Its input
 - (d) Borrow bits

[MCQ]



- **9.** What is the expression for difference, borrow of full subtractor circuit
 - (a) Diff = $A \oplus B \oplus C$, Borrow = $\overline{A}C + (A \odot B)C$
 - (b) Diff = $A \oplus B \oplus C$, Borrow = $\overline{A}B + (\overline{A \oplus B}) \cdot C$
 - (c) Diff = $A \odot B \odot C$, Borrow = $\overline{A}B + (\overline{A \odot B})C$
 - (d) Diff = $A \odot B \odot C$, Borrow = $\overline{A}C + (A \odot B)C$

[MCQ]



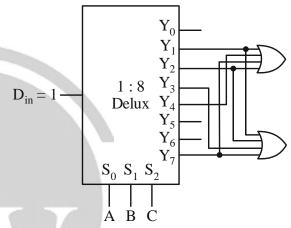
19. A D flip-flop is used in a 4-bit serial adder, why?

- (a) It is used to invert the input of the full adder
- (b) It is used to store the output of the full adder
- (c) It is used to store the carry output of the full adder
- (d) It is used to store the sum output of the full adder

[MCQ]



11. The circuit shown in the given figure represents a/an:

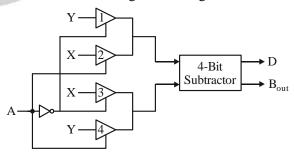


- (a) decoder
- (b) equality detector
- (c) full adder
- (d) full subtractor

[MCQ]



12. Consider the following circuit diagram



A 4-bit subtractor, four 4-bit three-state buffers (with bus input and output), and one inverter is used to subtract two numbers (Y - X), X = 0101 and Y = 0010 If A = 0, then D and B_{out} are respectively

- (a) 0011 and 0
- (b) 1101 and 0
- (c) 0011 and 1
- (d) 1101 and 1

Answer Key

1. (c)

2. (b)

3. (b)

4. (a)

5. (c)

6. (0.7)

7 (d)

8. (c)

9. (b)

10. (c)

11. (d)

12. (d)





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