

CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Cache Organization

Lecture No.- 06

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Recap of Previous Lecture



Topic

Cache Mapping

Topic

Direct Mapping

Topic

Tag & Index

Topics to be Covered



Topic

Direct Mapping

Topic

Set Associative Mapping

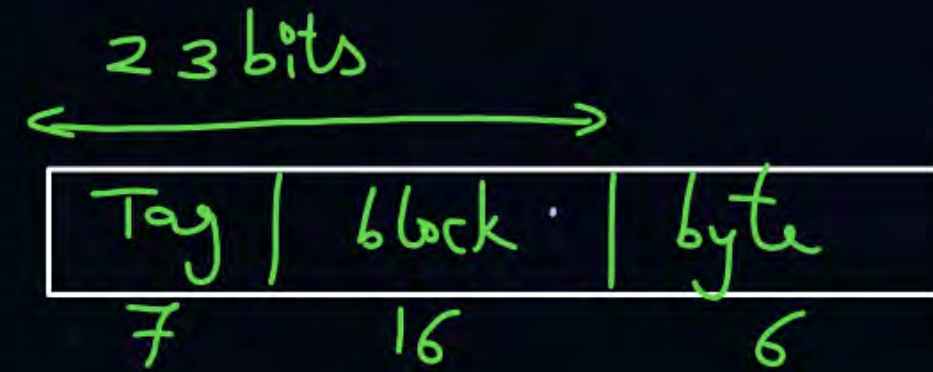
Topic

Fully Associative Mapping

[NAT]



mm add.
mm block no. | offset



#Q. Blocks in Main memory = 2^{23}
Blocks in Cache memory = 2^{16}
Block Size: 64 Bytes = $2^6 B$
Direct Mapping

$$\text{mm size} = 2^{23} * 2^6 B = 2^{29} B$$

↓
mm add = 29 bits

No. of bits required for Byte Offset = ? 6 bits

No of bits required for main memory address = ? 29 bits

Index-bits = ? 16

Tag-bits = ? 7

Size of Tag Directory = ? $2^{16} * 7$ bits

#Q.

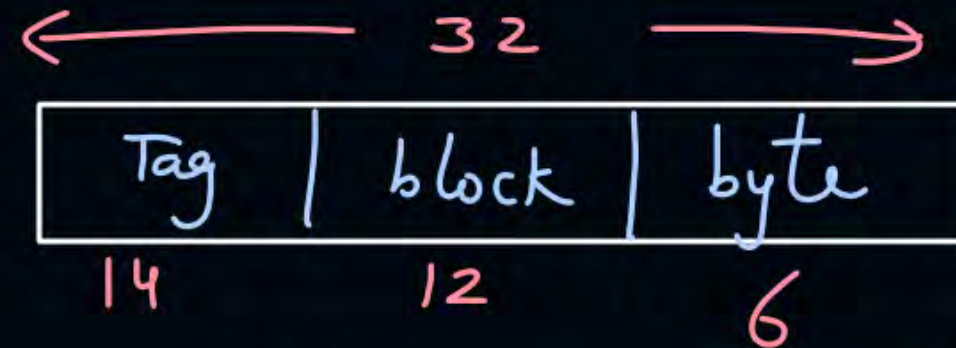
→ 1 word = 4 Bytes
 32-bit architecture CPU

Main Memory Size = 4GB = 2^{32} B \Rightarrow add. = 32 bits

Cache Size = 256KB = 2^{18} B

Block Size = 16 Words = $16 * 4 = 64$ B

Direct Mapping



← $\log 2^{18} = 18$ bits →

No. of bits required for Byte Offset = ? 6

No of bits required for main memory address = ? 32

No of bits required for main memory block no. = ? 26 bits

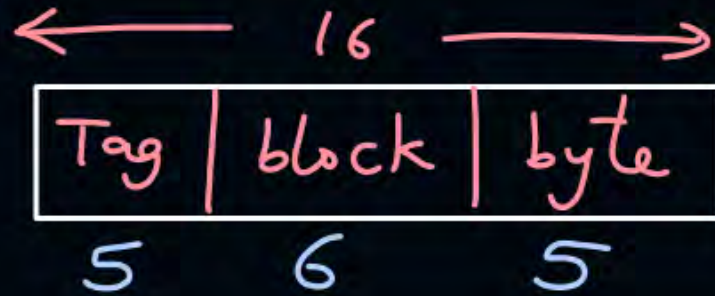
Index-bits = ? 12 bits

Tag-bits = ? 14 bits

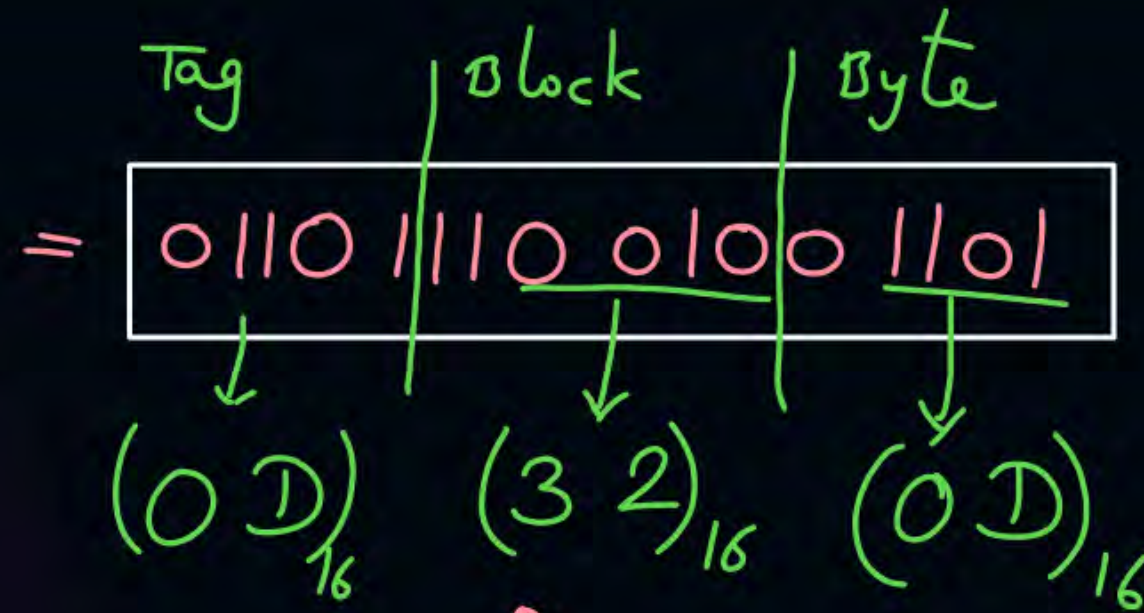
Size of Tag Directory = ? $2^{12} * 14$ bits



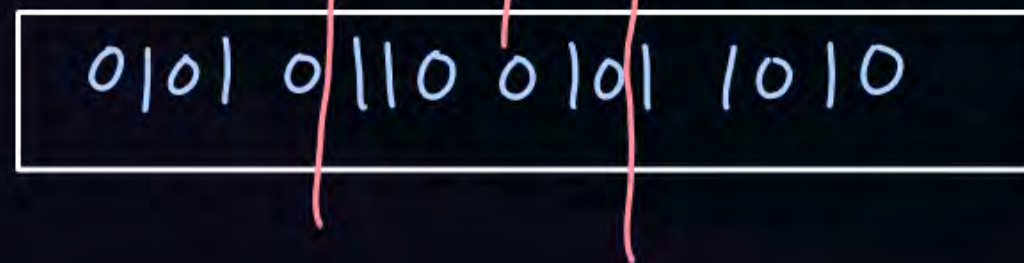
Topic : Calculating CM Block Number from MM Address



$$\text{mm add.} = (6E4D)_{16}$$



$$\text{mm add.} = (565A)_{16} \Rightarrow$$



both addresses
map to same
cm block.

If mem add. given in decimal:-

$$\text{Binary} \Rightarrow (10101)_2 = (21)_{10}$$

y	x
101	01

3 bits 2 bits

$$x = 2^2 = 4$$

$$x = 21 \% 4 = 1$$

$$y = \lfloor 21 / 4 \rfloor = 5$$

$$(101)_2 \Rightarrow (5)_{10}$$

$$(01)_2 = (1)_{10}$$

mm add.

mm block no.	byte no.
	3

$$\text{block size} = 8 \text{ bytes} = 2^3 \Rightarrow \text{byte no} = 3 \text{ bits}$$

$$\text{byte no.} = (\text{mm add.}) \% \text{ block size}$$

$$\text{mm block no.} = \left\lfloor (\text{mm add.}) / \text{block size} \right\rfloor$$

mm block no.		byte
Tag	cm block no.	byte

$$\text{cm block no.} = (\text{mm block no.}) \% \text{ no. of blocks in cache}$$

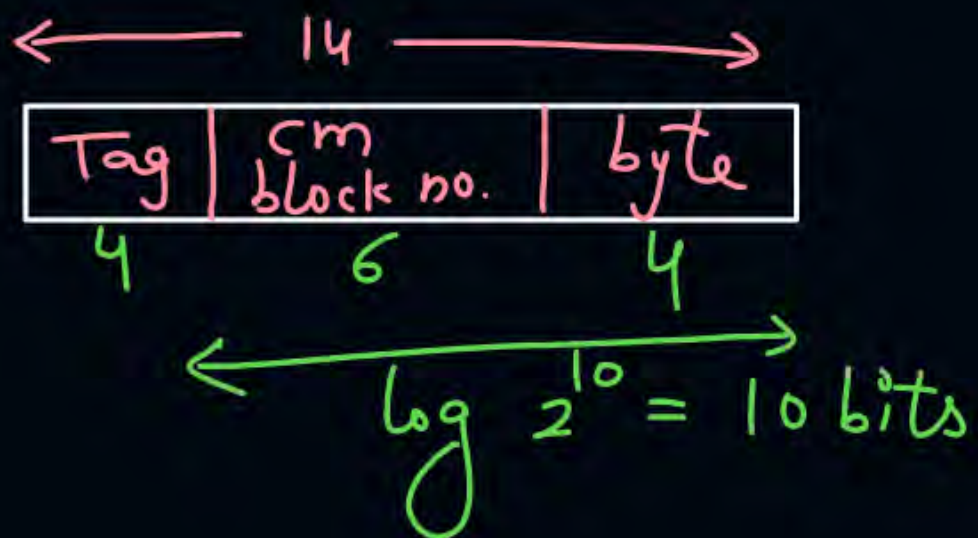
$$\text{Tag} = \left\lfloor (\text{mm block no.}) / \text{no. of blocks in cache} \right\rfloor$$

ex:- block size = 16 bytes

cm size = 1KB

mm add = 14 bits

Direct mapping



no. of blocks in cache = $2^6 = 64$

add. = $(5623)_{10}$

\Rightarrow

$$\text{mm block no} = \left\lfloor \frac{5623}{16} \right\rfloor = 351$$

$$\text{byte no.} = 5623 \% 16 = 7$$

$$\text{cm block no.} = 351 \% 64 = 31$$

$$\text{Tag} = \left\lfloor 351 / 64 \right\rfloor = 5$$

mm block no.	byte
351	7



Topic : Checking Hit/Miss in Direct Mapped Cache

mem add.



Tags cache

☐ 0

☐ 1

☐ 2

⋮



Blocks

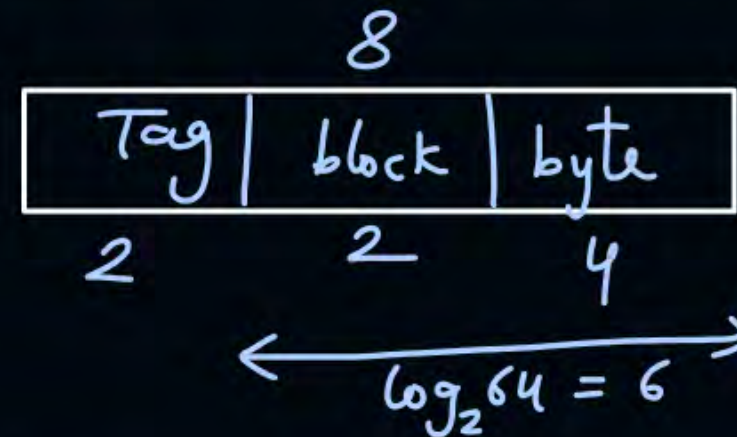
Comparison

Hit/miss

#Q. Consider a 64 bytes direct mapped cache with a block size of 16 bytes. Main memory size is 256 bytes. Currently in the cache, the blocks are having tags as follows:

	Block	Tag
0	00	10
1	01	01
2	10	11
3	11	01

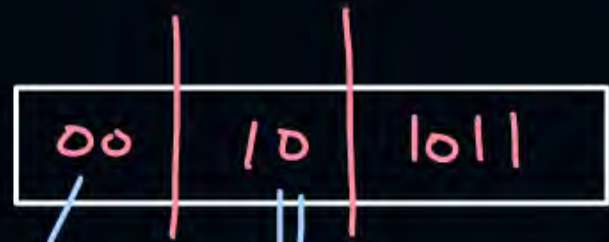
mm add. = 8 bits



Identify the correct statement with respect to the availability of the main memory data into cache?

- a) Main memory byte number 243 present in cache
- ✓ b) Main memory byte number 143 present in cache
- c) Main memory byte number 43 present in cache
- ✓ d) Main memory byte number 119 present in cache

c) $(43)_{10} = (00101011)_2$



cm block no = 10

gots cache at block 10
 & check tag there = 11

Tag = 00 } not matching

miss

(c) mm blockno = $\left\lfloor \frac{43}{16} \right\rfloor = 2$

cm block no. = $2 \% 4 = 2$

Tag = $\left\lfloor 2 / 4 \right\rfloor = 0$

check at cm block no.
 2 tag 0 is there or not

not
 miss

a) $(243)_{10}$

mm block no = 15

cm block no = $15 \% 4 = 3$
Tag = $\lfloor 15 / 4 \rfloor = 3$ } miss

b) $(143)_{10}$

mm block no = $\lfloor 143 / 16 \rfloor = 8$

cm block no = $8 \% 4 = 0$
Tag = $8 / 4 = 2$ } hit

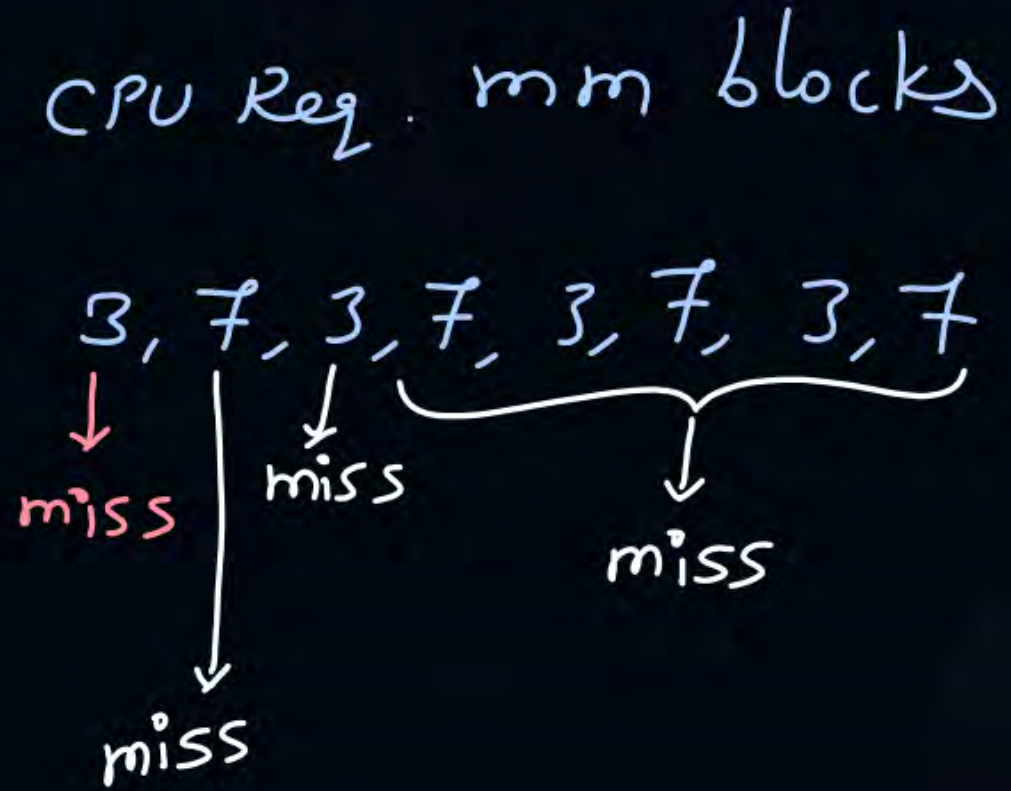
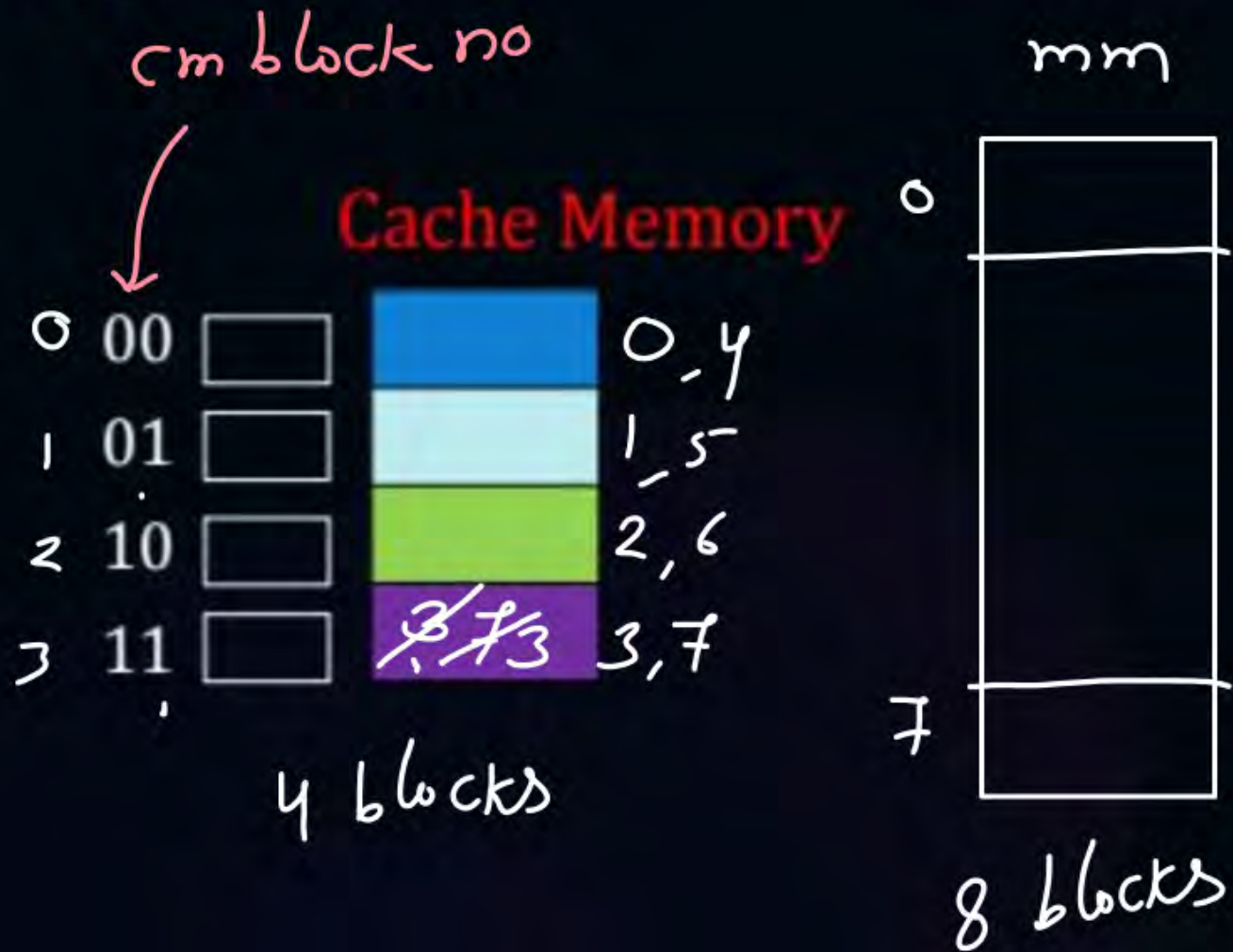
d) $(119)_{10}$

mm block no = $\lfloor \frac{119}{16} \rfloor = 7$

cm block no = $7 \% 4 = 3$
Tag = $7 / 4 = 1$ } hit



Topic : Problem With Direct Mapping





Topic : Set Associative Mapping

2-way set associative

Tag			
0	<input type="checkbox"/>	<input type="checkbox"/>	0, 2, 4, 6
1	<input type="checkbox"/>	<input type="checkbox"/>	1, 3, 5, 7

cm set no.
(Index)



CPU Reg. mm block no.

3, 7, 3, 7, 3, 7, 3, 7

miss miss Hit Hit

Direct mm block no.

Tag	cm block no.
1	2

2-way mm block no.

Tag	Set no.
2	1

if cache \Rightarrow 16 blocks
2-way set ass.

0		
<u>1</u>		
7		

$$\text{no. of sets in cm} = \frac{\text{no. of blocks in cm}}{\text{associativity}}$$

$$\text{no. of bits for cm set no.} = \log_2(\text{no. of sets in cache})$$

$$\text{cm block no.} = (\text{mm block no.}) \% \text{ no. of sets in cache}$$



Topic : Set Associative Mapping

mm add.

mm block no.		byte no.
Tag	cm set no.	byte no.

Index

for each block Tag infoⁿ is maintained.

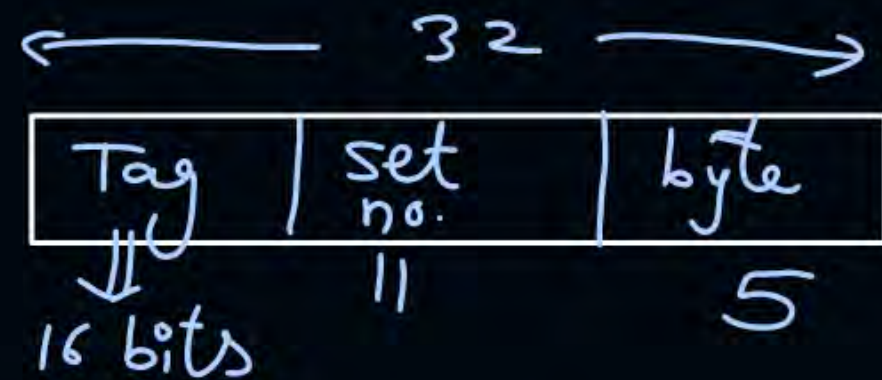
Tag directory size

$$= \text{no. of blocks in cache} * (\text{Tag} + \text{extra bits})$$

Ques) mm add = 32 bits
cm size = 128 kbytes
2-way set associative
block size = 32 bytes = 2^5 B

$$\text{no. of blocks in cm} = \frac{128 \text{ kB}}{32 \text{ B}} = \frac{2^{17}}{2^5} = 2^{12}$$

$$\text{no. of sets in cm} = \frac{2^{12}}{2} = 2^{11} \Rightarrow \text{set no} = 11 \text{ bits}$$



Tag directory size
 $= 2^{12} \times 16 \text{ bits}$

#Q. A computer has a 512Kbyte, 4-way set associative, write back data cache with block size of 16 Bytes. The processor sends 34 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit

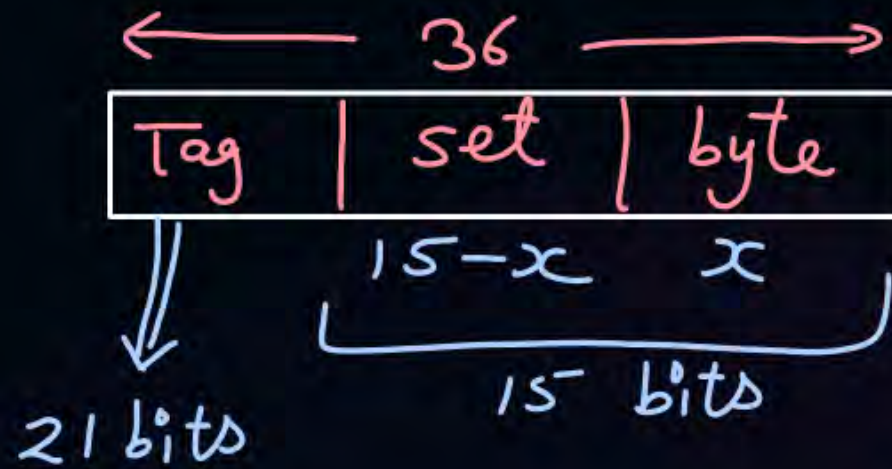
1. The number of bits in the tag field of an address is 17 bits
2. The size of the cache tag directory is $= 2^{15} * (17 + 2 + 1 + 1) \text{ bits} = 2^{15} * 21 \text{ bits}$

34		
Tag	Set	byte
17	13	4

$$\text{no. of blocks in cm} = \frac{512 \text{ KB}}{16 \text{ B}} = \frac{2^{19}}{2^4} = 2^{15}$$

$$\text{no. of sets in cm} = \frac{2^{15}}{4} = 2^{13} \Rightarrow \text{set no} = 13 \text{ bits}$$

#Q. The width of the physical address on a machine is 36 bits. The width of the tag field in a 256 KB 8-way set associative cache is 21 bits?



assume block size = 2^x bytes \Rightarrow byte no. = x bits

$$\text{no. of blocks in cache} = \frac{256 \text{ KB}}{2^x \text{ B}} = 2^{18-x}$$

$$\log_2(\text{cm size}) - \log_2 k$$

$$\log_2 2^{18} - \log_2 8 = 15 \text{ bits}$$

k-way set associativity

$$\text{no. of sets in cache} = \frac{2^{18-x}}{8} = \frac{2^{18-x}}{2^3} = 2^{15-x}$$

\Downarrow

set no. = $(15-x)$ bits



2 mins Summary



Topic

Direct Mapping

Topic

Set Associative Mapping

Topic

Fully Associative Mapping



Happy Learning

THANK - YOU