CS & IT ENGINEERING

Computer Organization Architecture

Basic Of COA

DPP- 01 Discussion Notes

By- Devvrat sir

[MCQ]

#Q. In a microprocessor, the register which holds address of the next instruction to be fetched?

Ans [B]

A Accumulator

B Program Counter

C Stack Pointer

D Instruction Register

PC (Program Counter) ⇒ It contains the address of ins⑤ which is going to be executed next.

[MCQ]

#Q. The following register holds the instruction before it goes for decode?

A Data Register

B Accumulator

C Address Register

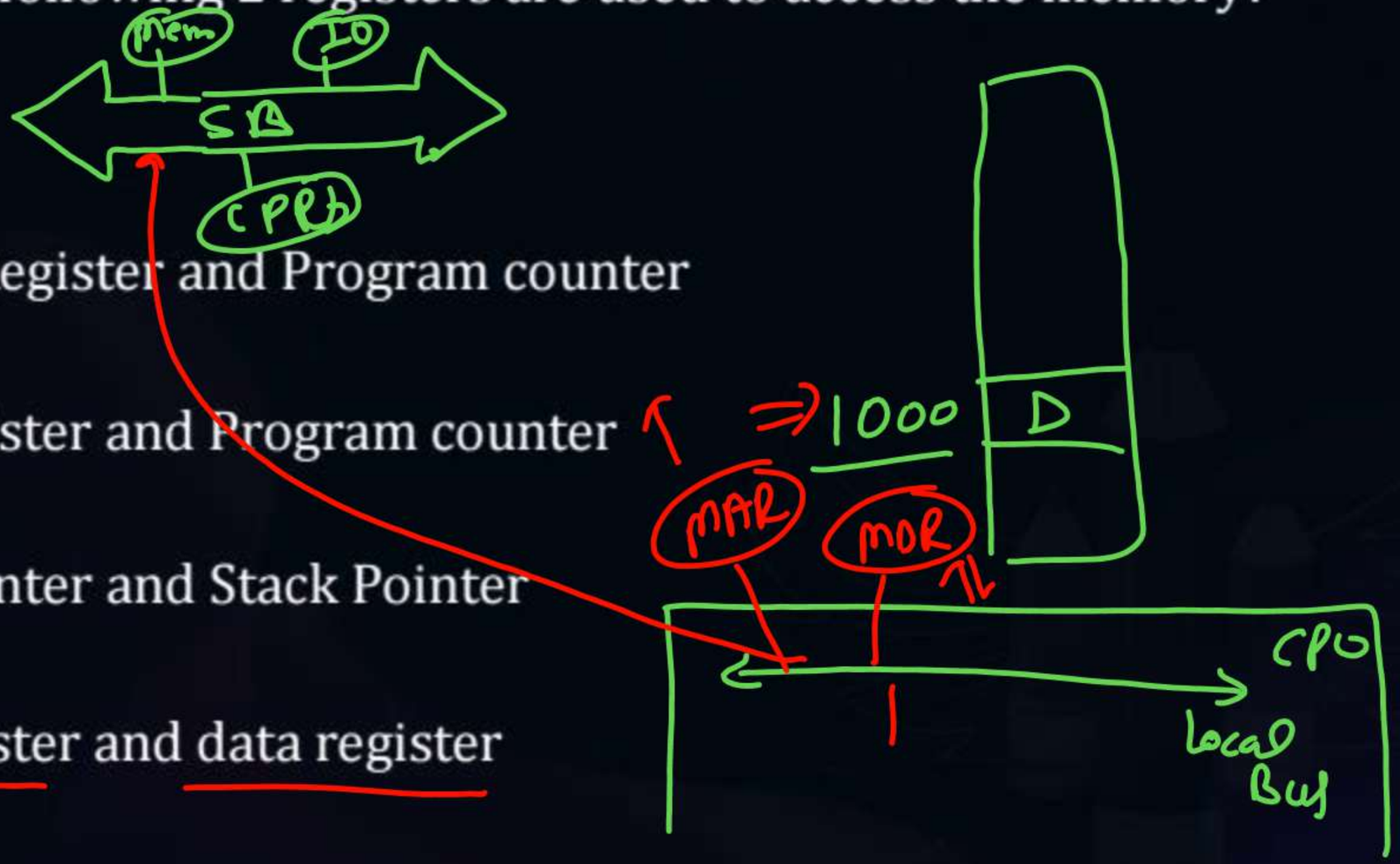
D Instruction Register

IR – Hold the opcode

[MCQ]

#Q. Which of the following 2 registers are used to access the memory?

Ans [D]



A Instruction Register and Program counter

B Address Register and Program counter

C Program counter and Stack Pointer

D Address register and data register

[MSQ]

Ans [B, C]

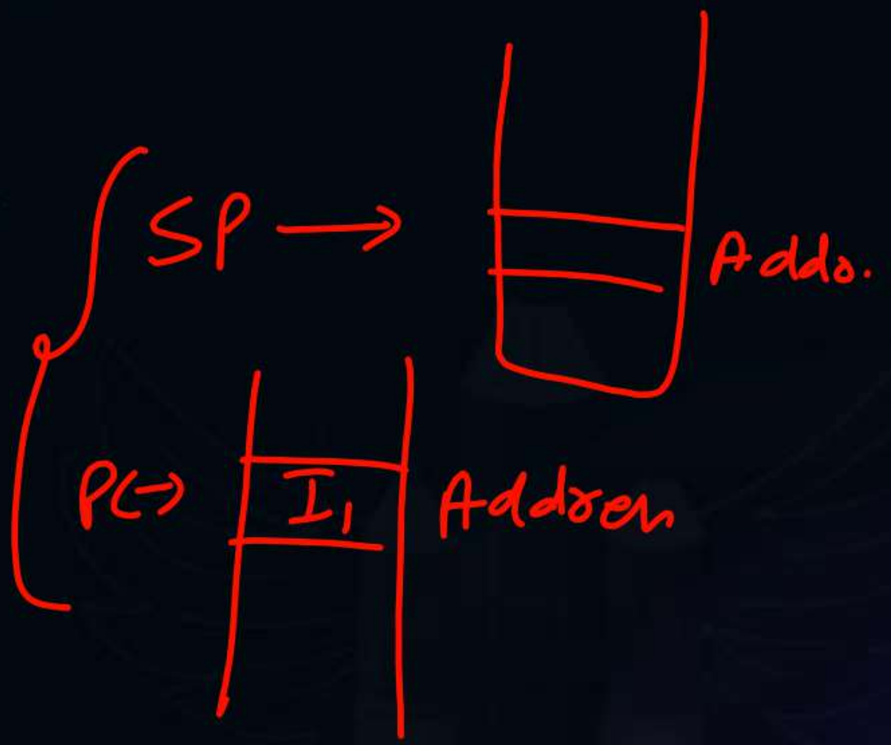
#Q. In a CPU which of the following pair of registers should have same capacity of storage?

A. Instruction Register and Program counter

B. Address Register and Program counter

C. Program counter and Stack Pointer

D. Address register and Data register



[MCQ]

Ans[C]

#Q. Which is not a CPU architecture?

A. Single Accumulator architecture

B. General Register architecture

C. Base Register architecture

D. Stack architecture

CPU Arch. are.

1. Single Acc. Arch.
2. Stack Arch.
3. General Reg. Arch.

[MCQ]

Ans[A]

#Q. Which of the following is included in the architecture of computer?

1.Addressing Modes, Design of CPU

2.Instruction Set, Data Format

3.Secondary Memory, Operating System

A 1 and 2

B 2 and 3

C 1 and 3

D 1, 2 and 3

Archi. of Computer

① Addressing modes Supported

② Detailed CPU Design

③ Instruction set.

④ Data format

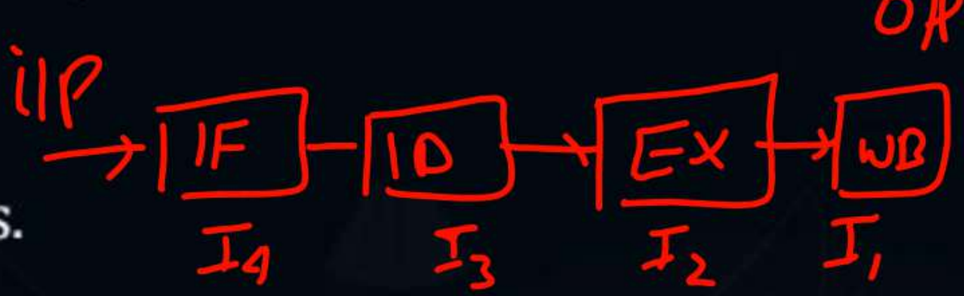
[MCQ]

Ans [C]

#Q. Consider the following statements:

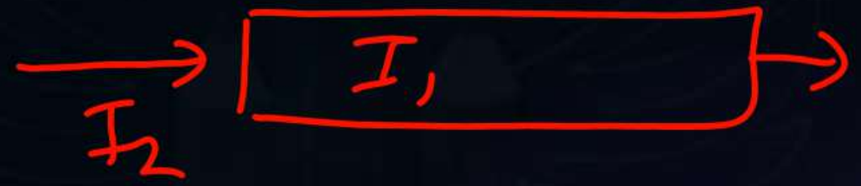
1. A computer will have a multiply instruction
2. Multiply instruction will be implemented by a special division unit

Which of the following is correct?



A ✗ Both 1 and 2 are not architectural design issues.

B Both 1 and 2 are not organizational issues.



C ✓ 1 is an architectural design issue while 2 is an organizational issue.

D ✗ 1 is an organizational issue while 2 is an architectural design issue.

[MCQ]

Ans [C]

#Q. A CPU has 24-bits instruction. A program starts at address 600 (in decimal). Which of the following is a legal program counter value?

A 700

B 800

C 900

D 950

Instruction size
= 24 bit
= $\frac{24}{8}$ Bytes
= 3 Bytes.

[MCQ]

Ans [C]

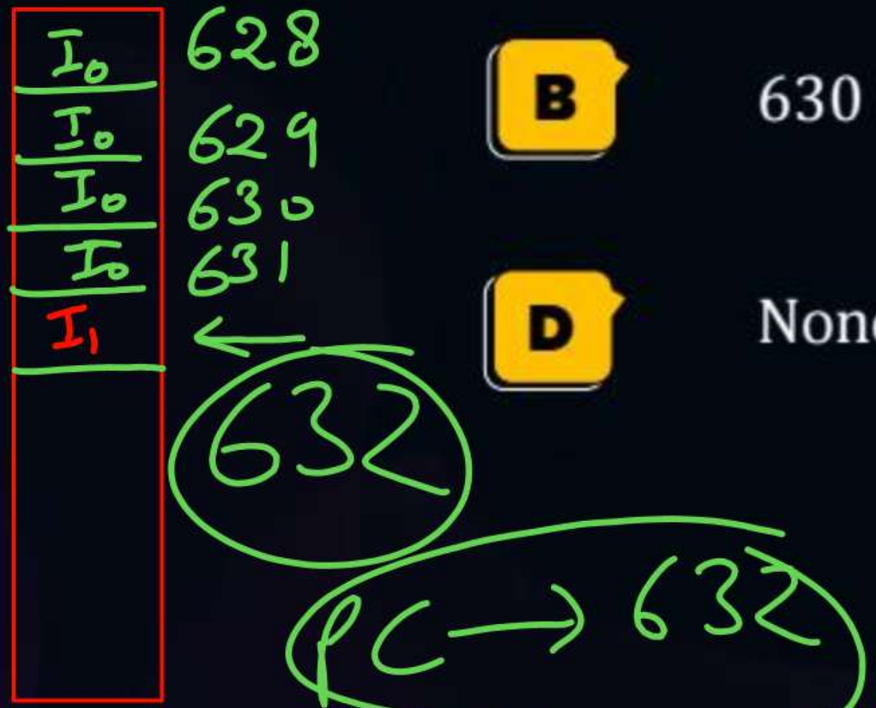
#Q. Consider a computer which has 2-word instructions. 1 word size is 2 bytes. In main memory an instruction is stored at location 628 (decimal). The decimal value of PC when this instruction will be execution in CPU?

A 628

B 630

C 632

D None



Inst Size = 2 word
1 word = 2B
Inst Size = 2x2 B
= 4B

[NAT]

Ans [42]

#Q. Consider the following program segment. Here R1, R2 and R3 are the general-purpose register. Assume that the content of memory location 3000 is 50 and location 2000 is 25. Content of register R2 is 12. All numbers are in decimal. After the execution of this program the value of memory location 2000 is?

Instructions	Operations
MOV R1, #15	R1 ← #15
MOV (2000), R1	M[2000] ← R1
ADD R2, (2000)	R2 ← R2 + M[2000]
MOV(3000), R2	M[3000] ← R2
MOV R3, R1	R3 ← R1
ADD R3, (3000)	R3 ← R3 + M[3000]
MOV (2000), R3	M[2000]← R3
HALT	Stop

R2 [~~12~~ 29] $12 + 15 = 27$

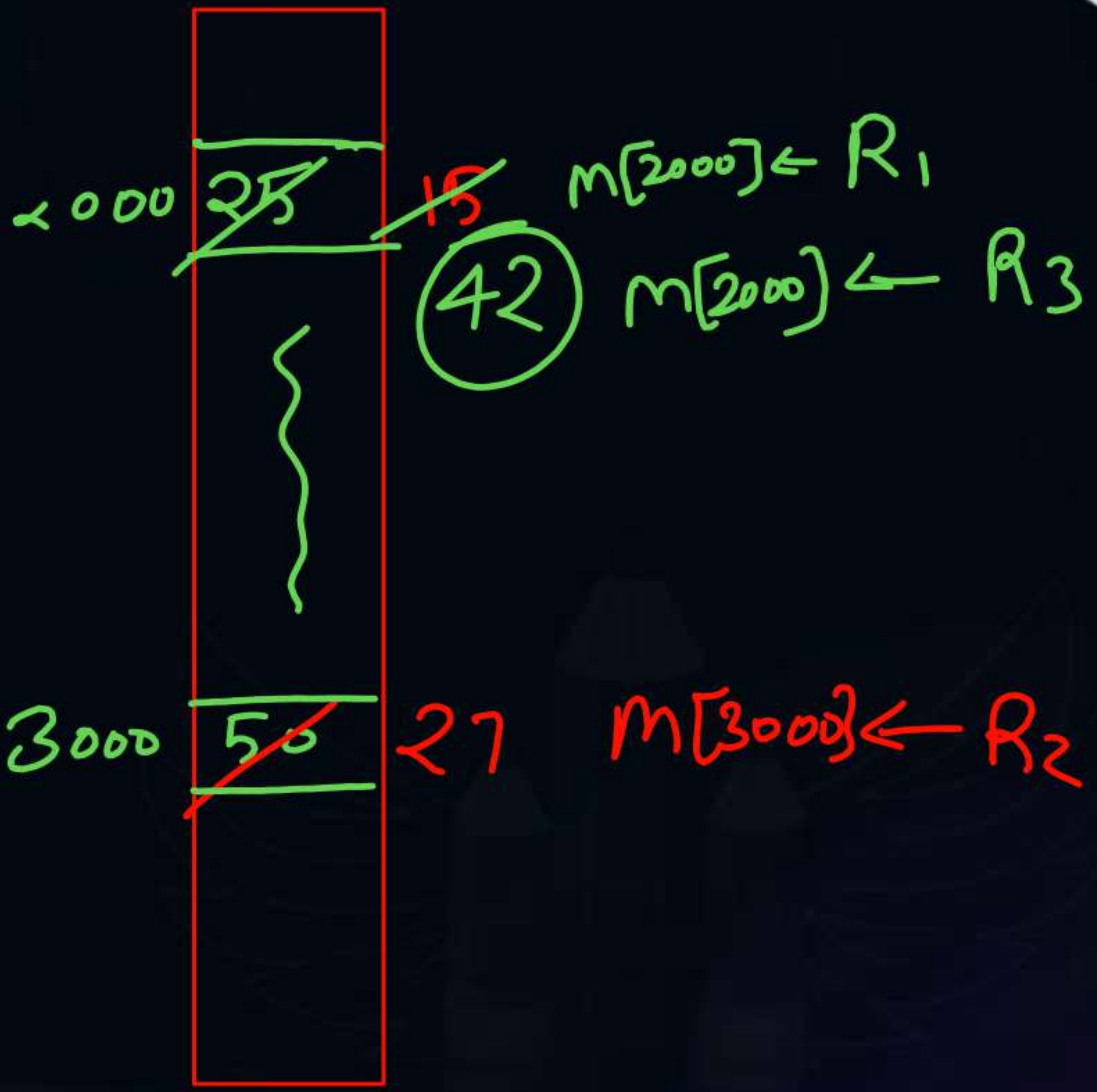
R1 [15] $R_1 \leftarrow \#15$

R_3 [17] $R_3 \leftarrow R_1$

$R_3 \leftarrow R_3 + M[3000]$

$= 15 + 27$

$= 42$



[NAT]

#Q. Consider the following program segment. Here R1 and R2 are the general-purpose register. Assume that the content of memory location 3000 is 27 and location 2000 is 13. Content of register R2 is 10. All numbers are in decimal. After the execution of this program the value of R2 is?

	Instructions	Operations
	MOV R1, #7	R1 ← #7
X:	DEC R1	R1 ← R1 – 1
	JNZ Y	Jump to Y on Non-Zero
	ADD R2, (3000)	R2← R2 + M[3000]
	JMP Z	Jump to Z
Y:	ADD R2, (2000)	R2 ← R2 + M[2000]
	JMP X	Jump to X
Z:	HALT	Stop

R2 10 → 115

10+13=23

23+13=36

36+13=49

49+13=62

62+13=75

75+13=88

R1 7 → 6 → 5 → 4 → 3 → 2 → 1 → 0

$R_2 \leftarrow R_2 + M[3000]$

115 ← 88+27

THANK - YOU