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CS&IT

Computer Organization and Architecture

DPP: 1

CPU & Control Unit

Q1 Consider a CPU with clock rate of 200MHz. If the CPU has average CPI of 5 then average instruction execution time is _____nanoseconds?

Q2 A CPU runs on 500MHz clock rate and is executing a program which consists 1000 instructions. If the measured average CPI (Cycles per instructions) for the program is 6 then total time required to run the program on CPU is _____microseconds?

Q3 A CPU runs on x MHz clock rate and is executing a program which consists 200 instructions. If the measured average CPI (Cycles per instructions) for the program is 4 and total time required to run the program on CPU is 4 microseconds, then the value of x is _____?

Q4 A CPU is used for executing n instructions. For executing these n instruction CPU has taken 6 cycles per instruction on average. The CPU operates on 2GHz clock rate. The CPU takes total of 0.75 microseconds to execute these n instructions. Later the same CPU used for executing 2n number of instructions and for executing 2n instructions its CPI (Cycles per Instruction) has been reduced to 5. Total time required by CPU to execute 2n instructions is _____ microseconds (correct up to 2 decimal places)?

Q5 Consider a microprogrammed control unit which has to support 64 number of instructions. For each instruction execution, control unit generates a sequence of 32 control words. Each microinstruction contains 3 fields: 137 control signals to support horizontal control unit, a MUX select field to select one of 16 inputs, and a next address field. The size of control memory needed is _____ Kbites?

Q6 Design of a vertical microprogrammed control unit requires to generate 40 signals. Out of the first 34 those only 3 signals can be active at a time. And for remaining 6, anyone can be active anytime. The microinstruction of the control unit stores control signal information along with 3-bit mux select and 10-bits address field. The size of control memory required is _____Kbits?

Q7 Consider a processor with byte-addressable memory. Assume that all registers, including program counter (PC) and Program Status Word (PSW), are size of four bytes. A stack in the main memory is implemented from memory location 500 and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is 660. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
- Store the value of PSW register in the stack
- Load the starting address of the subroutine in PC

The content of PC just before the fetch of a CALL instruction is 1600. Immediately after the fetch of CALL instruction value of PC will be _____?

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Answer Key

Q1	25
Q2	12
Q3	200
Q4	1.25
Q5	75
Q6	37
Q7	1604

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Hints & Solutions

Q1 Text Solution:

Average instruction execution time is = CPI × cycle time

= 5 × (1/200MHz)

$= \frac{5\times1}{200}\mu\,\text{sec.}$

$= \frac{5\times1000}{200}n\,\text{sec.}$

= 25 nsec.

Q2 Text Solution:

Program Execution time = number of instructions × CPI × Cycle time

$= 1000 \times 6 \times 1\frac{1}{500\text{MHz}}$

$= 12\mu\,\text{sec.}$

Q3 Text Solution:

Program Execution time = number of instructions × CPI × Cycle time

$4\ \mu\text{sec} = 200\ \times 4 \times \frac{1}{\text{clock rate}}$

$\text{clock rate} = \frac{200}{4\mu\text{sec.}} \times 4$

= 200 MHz

Q4 Text Solution:

Program Execution time = number of instructions × CPI × Cycle time

$0.75\ \mu\text{sec.} = \text{n} \times 6 \times \frac{1}{2\text{GHz}}$

$n = \frac{0.75\times\mu\text{ sec.}\times2\text{GHz}}{6}$

n = 250

Now for 2n = 2×250 = 500 instructions, given that CPI is 5 and now calculating execution time

Program Execution time = number of instructions × CPI × Cycle time

$= 500 \times 5 \times \frac{1}{2\text{GHz}}$

= 1250 nsec.

$= 1.25\mu\,\text{sec.}$

Q5 Text Solution:

Total number of control words needed in memory = 64 × 32 = 512

Hence for 512 control words, memory will need 9 bits address.

There are 137 signals for horizontal control unit hence 137 bits are needed for control signals.

There are 16 inputs in MUX hence 4 bits are needed for MUX select.

Microinstruction format will be as follows:

control signals	MUX select	Address
137		4

9

Complete size of microinstruction = 137 + 4 + 9

= 150 bits

Memory size needed = 2^9 × 150 bits

= 2^9 × 2 × 75 bits

= 75 Kbits

Q6 Text Solution:

First 34 signals will be in first 3 groups with all 34 signals in each group to make active any combination of signals. And rest 6 signals will be stored in horizontal manner.

For each group of 34 signals, in encoded manner 6 bits are used per group in vertical microprogrammed control unit.

The microinstruction format will be as follows:

Group 1	Group 2	Group 3	6 Signals	MUX Select	Address
6	6	6			
6	3	10			

Microinstruction size = 6 + 6 + 6 + 6 + 3 + 10

= 37 bits

Control memory size = 2^{10} × 37 bits

= 37 Kbits

Q7 Text Solution:

Call instruction size = 2 words

= 2×2

= 4 bytes.

In byte addressable memory 4 bytes will be stored on 4 memory locations.

Before fetch of CALL instruction value of PC is 1600, which means the address of CALL

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instruction is 1600.

Once the CALL instruction is fetched the PC value will be incremented by 4, hence

Immediately after the fetch of CALL instruction value of PC will be = 1600 + 4

=

1604