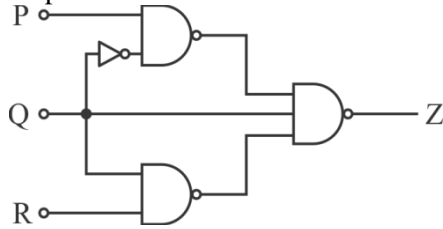


Subject : Digital Logic

Chapter : Logic Gate

DPP-02

1. For a 3-input logic circuit shown below, the output Z can be expressed as

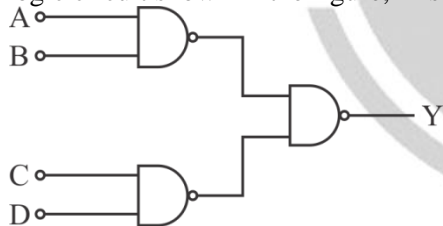


- (a) $Q + \bar{R}$ (b) $P\bar{Q} + R$
 (c) $\bar{Q} + R$ (d) $P + \bar{Q} + R$

2. The complete set of only those Logic Gates designated as Universal Gates is

- (a) NOT, OR and AND Gates
 (b) XNOR, NOR and NAND Gates
 (c) NOR and NAND Gates
 (d) XOR, NOR and NAND Gates

3. In the logic circuit shown in the figure, Y is given by



- (a) $Y = ABCD$
 (b) $Y = (A + B)(C + D)$
 (c) $Y = A + B + C + D$
 (d) $Y = AB + CD$

4. $F = AB + CD + E$ will be implemented with how many minimum number NAND gates?

- (a) Three (b) Four
 (c) Five (d) Six

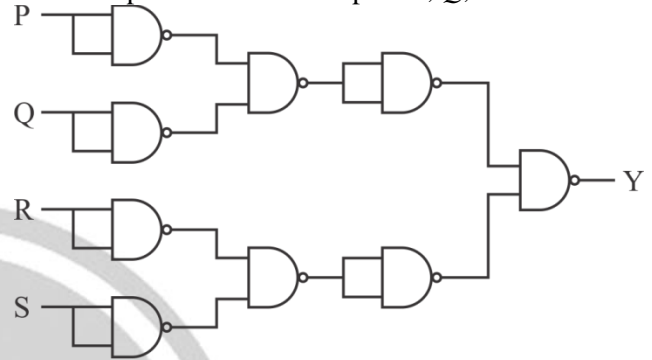
5. The minimum number of NAND gates required to reduce the expression $((A + B)C)D$ is

- (a) 6 (b) 5
 (c) 8 (d) 4

6. In a two-input NAND gate, if both inputs are shorted, it will behave like a _____ gate.

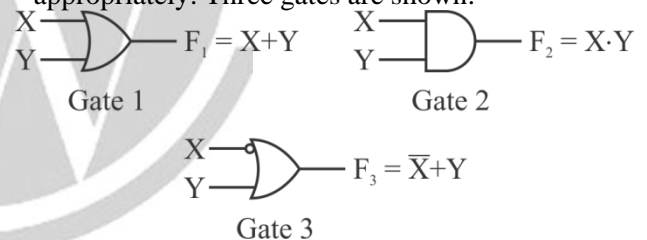
- (a) Buffer (b) AND
 (c) NOT (d) EX-OR

7. For the circuit shown in figure the Boolean expression for the output Y in terms of inputs P, Q, R and S is



- (a) $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$ (b) $P + Q + R + S$
 (c) $(\bar{P} + \bar{Q}) + (\bar{R} + \bar{S})$ (d) $(P + Q)(R + S)$

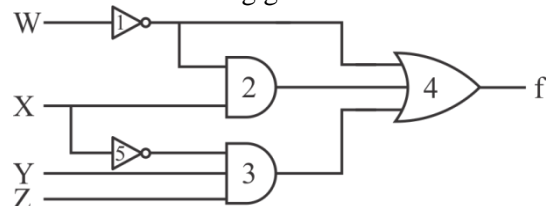
8. A universal logic gate can implement any Boolean function by connecting sufficient number of them appropriately. Three gates are shown:



Which one of the following statements is TRUE ?

- (a) Gate 1 is a universal gate.
 (b) Gate 2 is a universal gate.
 (c) Gate 3 is a universal gate
 (d) None of the shown is a universal gate.

9. Consider the following gate network:



Which one of the following gates is redundant?

- (a) Gate No. 1 (b) Gate No. 2
 (c) Gate No. 3 (d) Gate No. 4

10. The minimum of NAND gates required to implement $A + A B C$ is equal to

- (a) 0 (b) 1
 (c) 4 (d) 7

Answer Key

1. (c)
2. (c)
3. (d)
4. (d)
5. (b)

6. (c)
7. (b)
8. (c)
9. (b)
10. (a)



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