# CS & IT

## Computer Organization & Architecture

DPP: 2

## Instruction & Addressing Modes

**Q1** A relative branch mode type instruction is stored in memory starting from address 240. The branch is made to an address 140. What should be the value of relative address field of the instruction, if each instruction is stored on 2 memory locations?
Note: All numbers are in decimal

**Q2** Consider the following:
1. Operation code
2. Source operand reference
3. Result operand reference
4. Next instruction reference

Which of the above are typical elements of machine instructions?
(A) 1, 2 and 3 only
(B) 1, 2 and 4 only
(C) 3 and 4 only
(D) 1, 2, 3 and 4

**Q3** Which addressing mode helps to access table data in memory efficiently?
(A) Indirect mode
(B) Immediate mode
(C) Auto-increment or Auto-decrement mode
(D) Index mode

**Q4** An addressing mode in which the location of the data is contained within the mnemonic, is known as?
(A) Immediate addressing mode
(B) Implied addressing mode
(C) Register addressing mode
(D) Direct addressing mode

**Q5** The addressing modes used for source operand in the following instructions are respectively?
R1 ← #5
R1 ← M[5000]
R1 ← M[R2]
(A) Implied, direct, register
(B) Implied, direct, register indirect
(C) Immediate, direct, register indirect
(D) Immediate, direct, register

**Q6** Consider a PC-relative mode type branch instruction which takes branch on address 720 in memory. The instruction has offset value 160. What is the starting address of this instruction in memory, if each instruction is stored in memory on 4 locations?
Note: All numbers are in decimal

**Q7** Consider the system in which in fetch cycle complete instruction is fetched. Which of the following addressing modes do(es) not require memory access for operand after fetch cycle?
(A) Register Mode
(B) Register Indirect Mode
(C) Indirect Mode
(D) Indexed Mode

# Answer Key

| | |
|---|---|
| Q1 | -102~-102 |
| Q2 | (A) |
| Q3 | (C) |
| Q4 | (B) |
| Q5 | (C) |
| Q6 | 556 |
| Q7 | (A) |

# Hints & Solutions

**Q1 Text Solution:**

PC value when the given address is in execution = 240 + 2 = 242

Target address given = 140

In PC relative mode target address = PC value + relative address

140 = 242 + relative address

Relative address = 140 – 242 = –102

**Q2 Text Solution:**

With in an instruction operation code (opcode), source and destination operand references are specified in general. But next instruction reference is not because for that CPU maintains a register program counter (PC).

**Q3 Text Solution:**

To access table data (contiguous data) efficiently Auto-increment or Auto-decrement mode are used because using single instruction of these modes, entire table can be accessed without changing the instruction.

**Q4 Text Solution:**

Mnemonic means the character short form of opcodes, like for addition ADD, for subtraction SUB etc. So the addressing mode in which operand is specified within opcode itself is implied mode.

**Q5 Text Solution:**

R1 ← #5, in this instruction source value 5 is mentioned in instruction, hence it is immediate mode

R1 ← M[5000], in this instruction source value is taken from memory and memory address 5000 is mentioned in instruction hence it is direct mode

R1 ← M[R2], in this instruction source value is taken from memory and memory address is given indirectly in register R2, hence it is register indirect mode.

**Q6 Text Solution:**

In PC relative mode target address = PC value + relative address

720 = PC + 160

PC = 720 – 160

PC = 560

PC value will be the address of next instruction when the current instruction is in execution, and current instruction is stored in memory on 4 locations, hence starting address of current instruction = 560 – 4 = 556

**Q7 Text Solution:**

In register mode operand is present in CPU register, hence memory access is not required for operand.

In register indirect mode the register will provide memory address where the operand is stored, hence memory access is required.

In Indirect mode the operand is taken from memory only.

In indexed mode the address of operand is obtained by adding base address in index register value but operand is obtained from memory only.