CS & IT ENGINEERING

Computer Organization Architecture

Memory Organization

DPP 01 Discussion Notes

By-Dr.Astha Singh

[MCQ]

#Q. The memory cycle time of a memory is 500nsec. The maximum rate with which the memory can be accessed?

Note: Consider memory as byte addressable.

A 500 Bytes / Sec

B 2000 Bytes / Sec

C 2 Mbytes / Sec

D 2 GBytes / Sec

In 500 nano second 1 data accessed from memory = 1 byte

In 1 second ——— 1 byte / 500 ns = 0.002 byte

⇒ 2 Mega

[NAT]

#Q. The address bus width of a memory of size 4096×8 bits is ___ bits?

12

No. of cells in Memory = 4096 = 2^{12}

address size for Memory = 12 bits

[NAT]

#Q. Consider a byte addressable memory which has 0.2GBPS writing rate. The memory access time is 5 nanoseconds?

for 0.2 GB —— 1 seconds

1 byte data time Taken = 1/0.2

= 5 nano seconds

[NAT]

#Q. Consider a word addressable memory of total capacity of 4GB. The memory is accessed using a minimum of 29 bits address bus. The word size per address in this memory is ___ bytes?

$4\,GB = 2^{29} / \text{Word Size}$

$= 4\,G \times 2^{29}$

$= 2^{32} / 2^{29}$ bytes

$= 2^3$ bytes

$\Rightarrow$ 8 bytes

[MCQ]

#Q. Consider a memory with maximum size of X bytes. Memory is word addressable with word size of W bytes. The size of the address bus of the processor is at least ____ bits?

No of cell in Memory = Total capacity / word size = X/W

Address size of Memory $\log_2(X/W)$

A $\log_2(X/W)$

B $2^{(X/W)}$

C X/W

D $\log_2(X)$

[MCQ]

#Q. A DRAM chip of 64M×16 bits has 128K rows of cells with y cells in each row. If DRAM takes x-ns for 1 refresh then total refresh time of the DRAM is ____ Microseconds, if $x = 2 * \log_2 y$?

A 1200

B 2304

C 3202

D 5444

→

No. of Row cell * 1 Refresh time.

128K X 18

= 2304

[NAT]

#Q. A 32-bits wide main memory unit with a capacity of 16GB is built using 128M×8-bits RAM chips. If there are x-horizontal arrangements of chips are there, with y number of chips in each horizontal arrangement then the value of 10x+y is?

→ 16 GB / 4 bytes = 4G

memory → 4G × 4 bytes

chip capacity = 128 M × 8 = 128 × 1 bytes

No. of chip required = Total capacity / 1 chip

(4G × 4) / 128M × 1

=

10x + y = 10 × 32 + 4

= 324

THANK - YOU