CS & IT ENGINEERING

Computer Organization Architecture

Instruction and Addressing Modes

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DPP 02 Discussion Notes

[NAT]

#Q. A relative branch mode type instruction is stored in memory starting from address 240. The branch is made to an address 140. What should be the value of relative address field of the instruction, if each instruction is stored on 2 memory locations? -102

Note: All numbers are in decimal

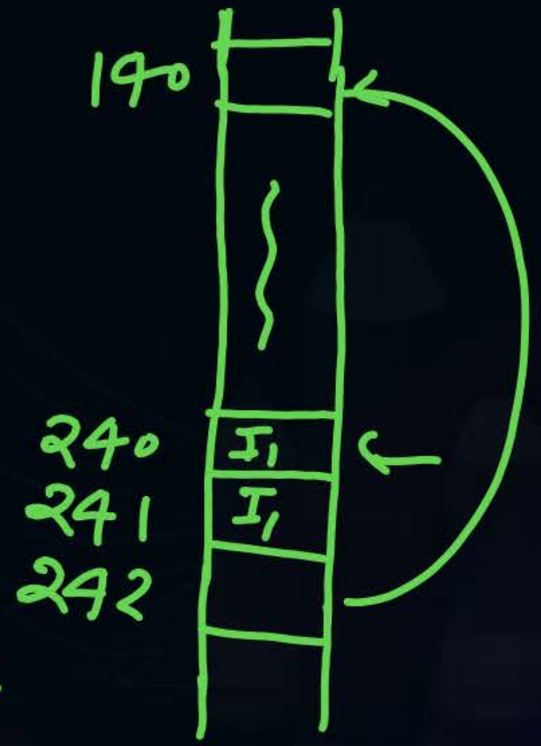
EA = PC + relative Addr. field

140 = 242 + rAf

rAf = 140 - 242

= -102

PC → 242



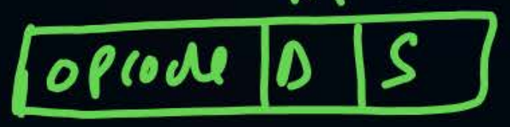
[MCQ]

Ans [A]

MUL, ADD, DIV

#Q. Consider the following:

1. Operation code (opcode)
2. Source operand reference
3. Result operand reference
4. Next instruction reference (PC) Program counter



$R_1 + R_2$

$m[x] \leftarrow m[x] + m[y]$

Which of the above are typical elements of machine instructions?

A. 1, 2 and 3 only

B. 1, 2 and 4 only

C. 3 and 4 only

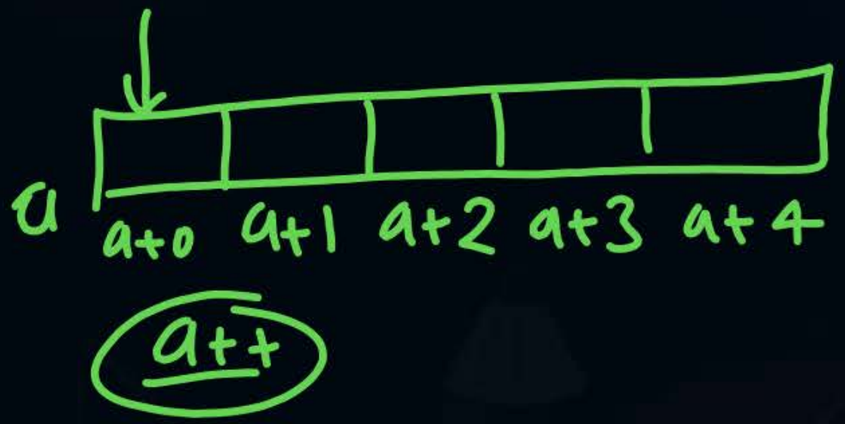
D. 1, 2, 3 and 4

[MCQ]

Ans[c]

#Q. Which addressing mode helps to access table data in memory efficiently?

array



A Indirect mode

B Immediate mode

C Auto-increment or Auto-decrement mode

D Index mode

[MCQ]

Ans [B]

$R_1 \leftarrow \#1$

#Q. An addressing mode in which the location of the data is contained within the mnemonic, is known as?

↳ used in computer to define or specify a computing funtion.

A Immediate addressing mode

B Implied addressing mode

C Register addressing mode

D Direct addressing mode

Used in computing to provide user with a means to quickly access function.

[MCQ]

Ans [C]

#Q. The addressing modes used for source operand in the following instructions are respectively?

R1 ← #5 Immediate

R1 ← M[5000] Direct Memory Acces

R1 ← M[R2]

A Implied, direct, register

B Implied, direct, register indirect

C Immediate, direct, register indirect

D Immediate, direct, register

[NAT]

556

#Q. Consider a PC-relative mode type branch instruction which takes branch on address 720 in memory. The instruction has offset value 160. What is the starting address of this instruction in memory, if each instruction is stored in memory on 4 locations?

Note: All numbers are in decimal

(A) 560 ✗
(B) 556 ✓
(C) 557
(D) 558
(E) 559 ✗

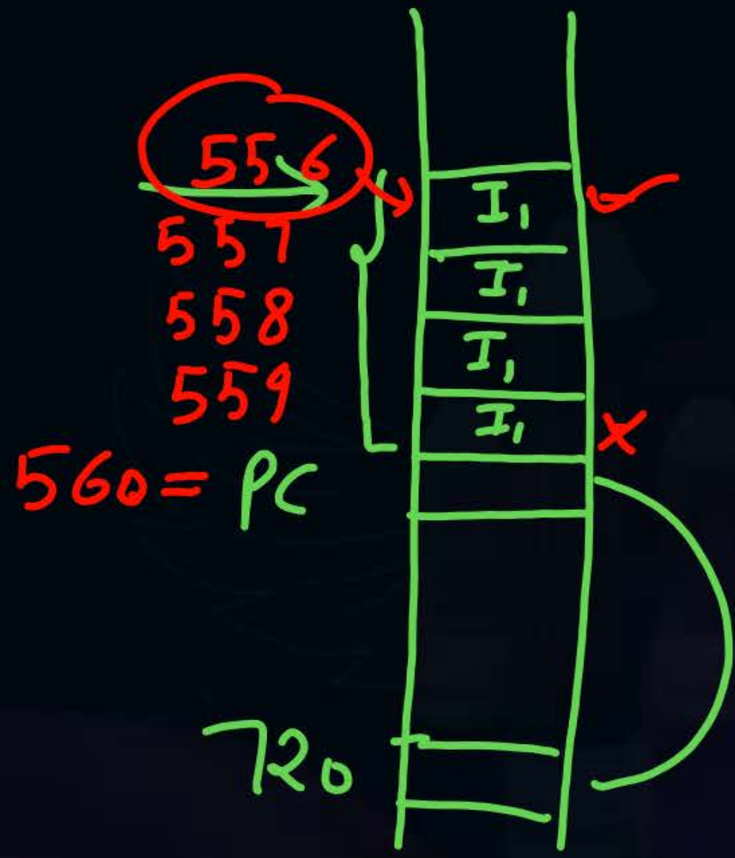
offset value = 160

EA = PC + offset

720 = PC + 160

PC = 720 − 160

= 560



[MCQ]

Ans A[A]

#Q. Consider the system in which in fetch cycle complete instruction is fetched. Which of the following addressing modes do(es) not require memory access for operand after fetch cycle?

A Register Mode

B Register Indirect Mode

C Indirect Mode

D Indexed Mode

M[[2000]]

$R_1 \leftarrow M[R_2]$

R_2 2000

THANK - YOU