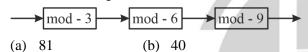
## Branch: CS & IT

## **Batch: English**

## Subject : Digital Logic Chapter : Sequential Circuits

**DPP-03** 

- 1. If Mod-60 counter is cascaded with Mod 40 counter, then it will becomes,
  - (a) Mod 100 counter
  - (b) Mod 2400 counter
  - (c) Mod 20 counter
  - (d) Mod 140 counter
- **1.** The maximum decimal count of 7-bit asynchronous counter is \_\_\_\_\_.
- **3.** The modulus of given block is,



- (c) 144
- (d) 162
- **4.** If input frequency of clock is 10 KHz then output frequency of counter will be \_\_\_\_\_ KHz [Assume mod of counter is 5]

- 5. For given block, the value of  $f_0$  is \_\_\_\_\_Hz.  $f_i = 500$ Hz  $\longrightarrow$  mod - 4  $\longrightarrow$  mod - 10  $\longrightarrow$   $f_0$
- **6.** Symmetric square wave of time period 100 μsec can be obtained from square wave of time period 10 μsec by using a
  - (a) divide by -5 circuit
  - (b) divide by -2 circuit
  - (c) divide by -5 followed by a divide by 2 circuit
  - (d) None of these
- 7. How many flip flops are required to construct Mod–31 counter?
  - (a) 4
- (b) 3
- (c) 2
- (d) 5

## **Answer Key**

- 1. (b)
- 2. (127)
- 3. (d)
- 4. (2)

- 5. (12.5)
- 6. (c)
- 7. (d)





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