CS & IT ENGINEERING

DIGITAL LOGIC
Sequential Circuit

Lecture No. 11

By- CHANDAN SIR

Recap of Previous Lecture

Sequential Circuit

Asynchronous Counter-

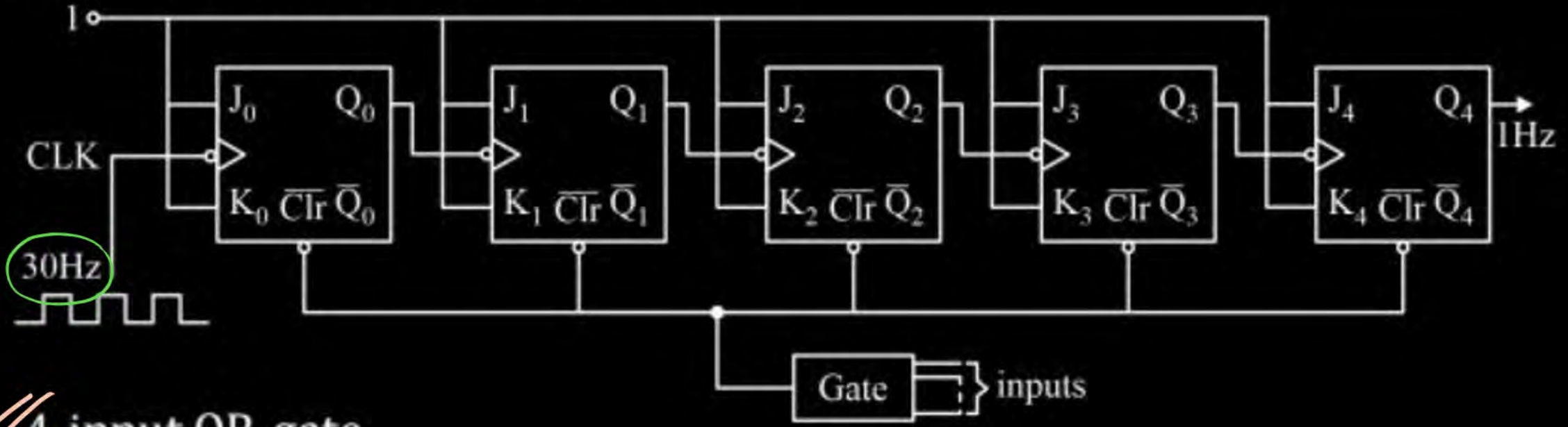
Topics to be Covered

Sequential Circuit

- Questions Practice

(MCQ)

#Q. Consider the following counter as shown below is needed to divide the 30 Hz line frequency down to 1 Hz. $\overline{Q}$ output is used in input of gate. Required logic gate for this counter is,



A 4-input OR-gate

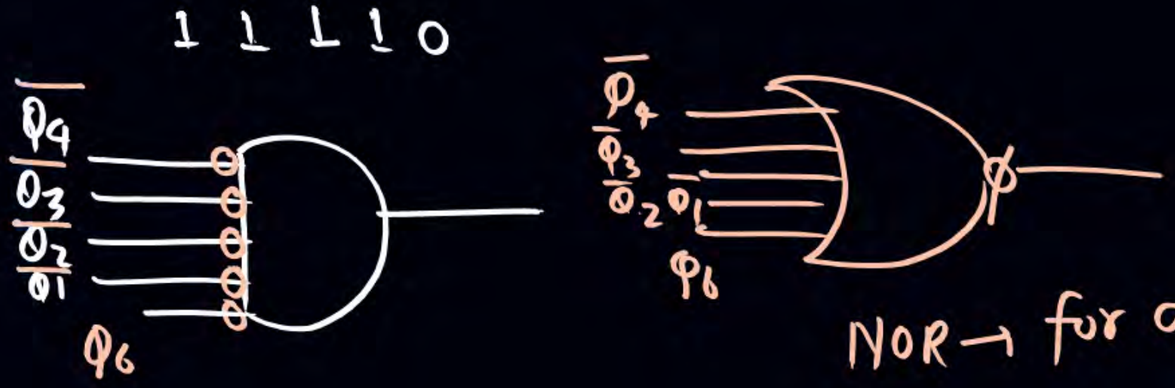
B 3-input NAND-gate

C 4-input NAND-gate

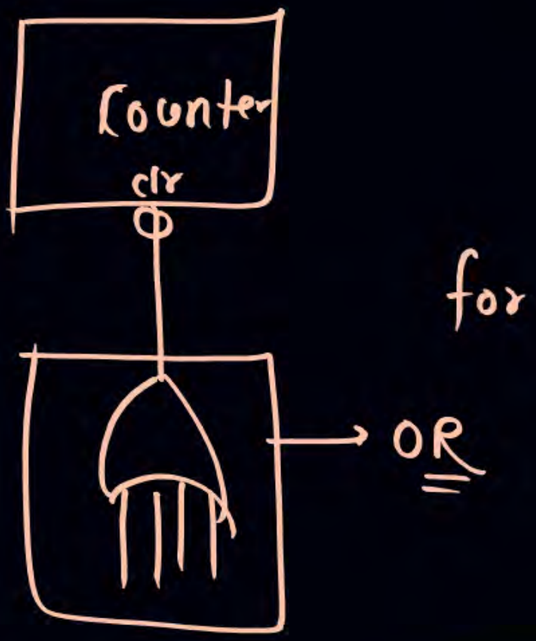
D 4-input NOR-gate

$$f_{out} = \frac{f_{in}}{M}$$

$$M = \frac{f_{in}}{f_{out}} = \frac{30Hz}{1Hz} = 30$$



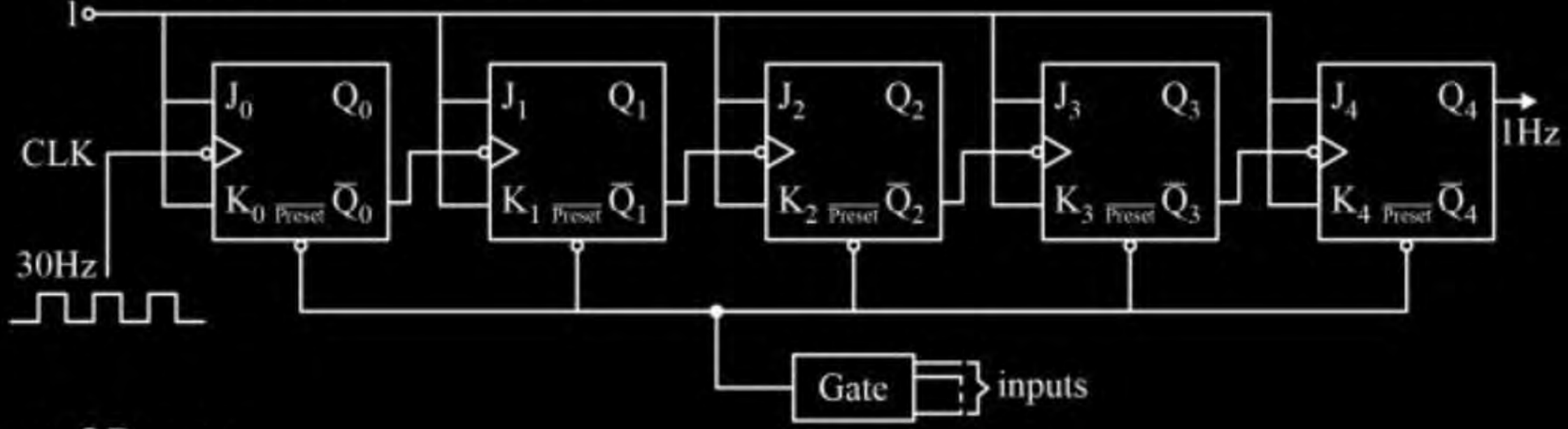
NOR → for active high



for active Low

(MCQ)

#Q. Consider the following counter as shown below is needed to divide the 30 Hz line frequency down to 1 Hz. Q output is used in input of gate. Required logic gate for this counter is



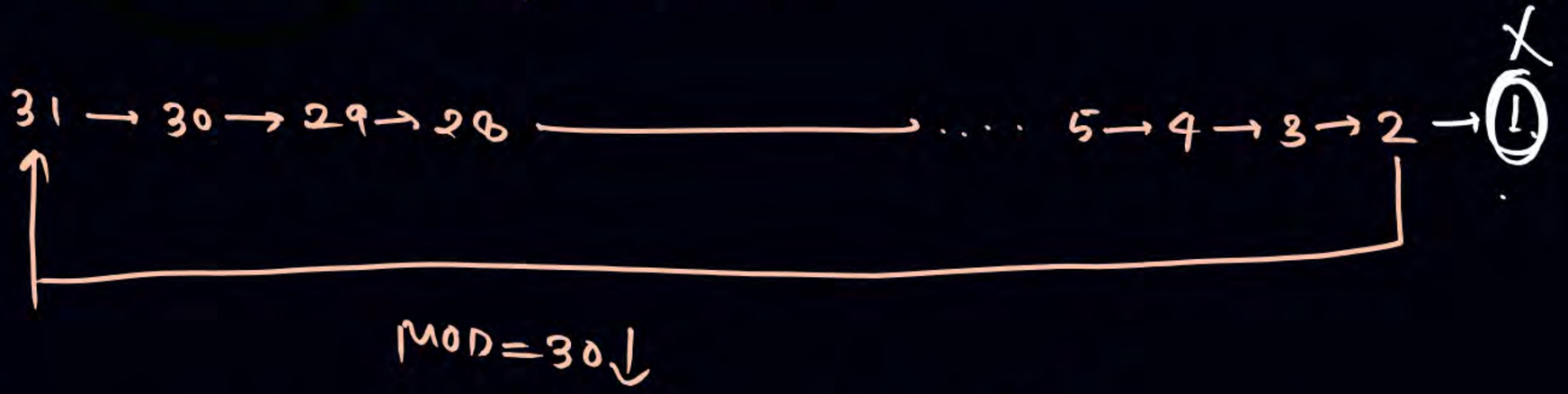
A 3-input OR-gate

B 3-input NOR-gate

C 4input NAND-gate

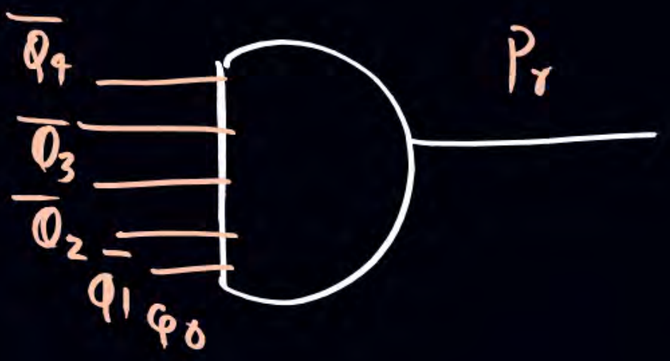
D 4-input OR gate

MOD-30 Down Ripple counter

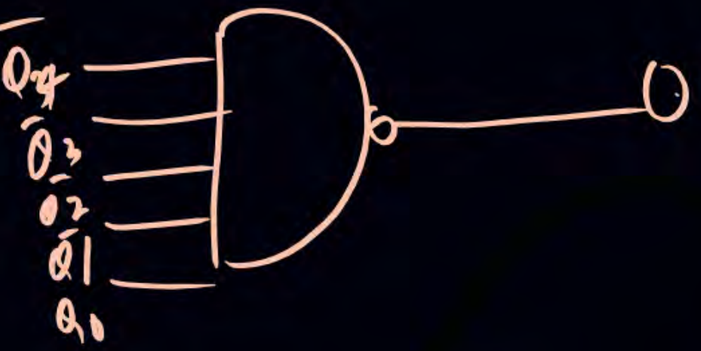


Active High

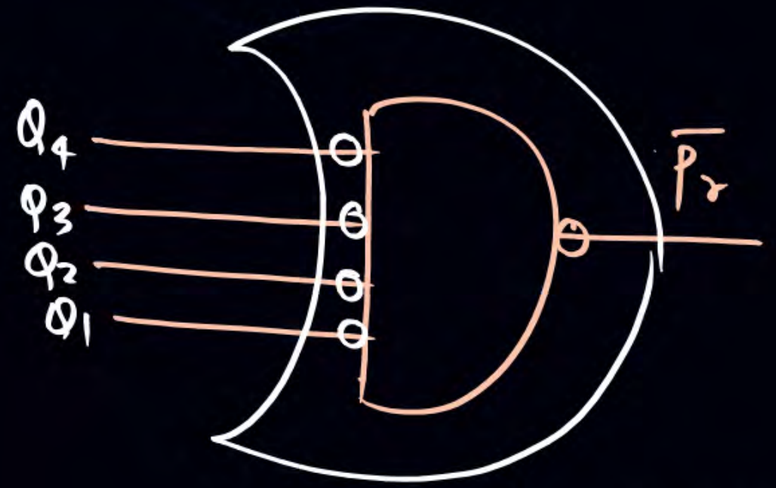
$P_r = 0000\perp$



Active Low



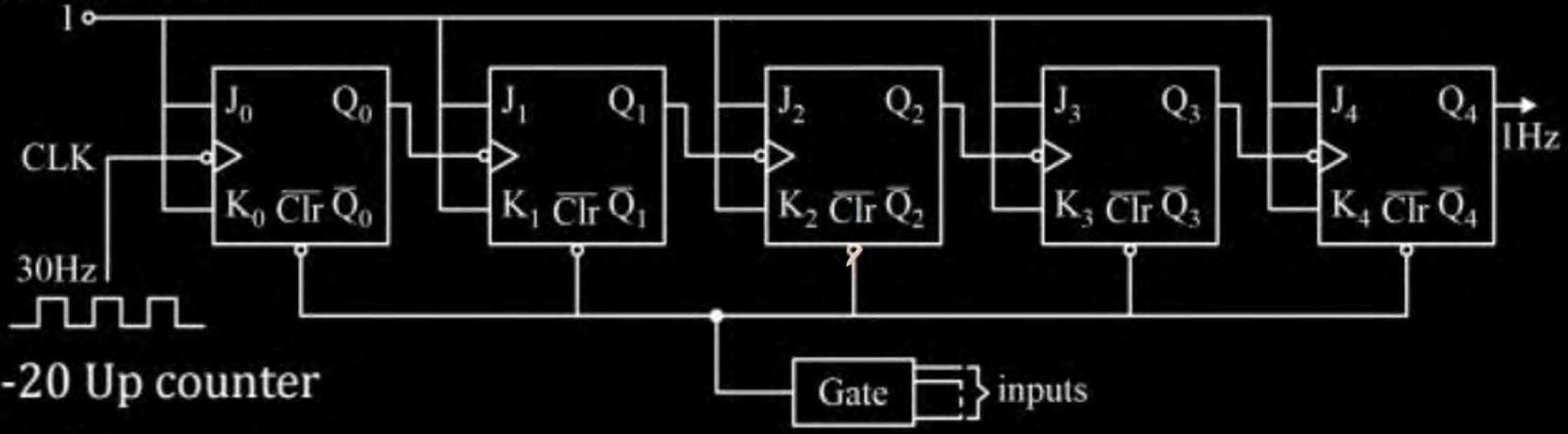
Active Low



Bubbled NAND = OR

(MCQ)

#Q. Counter circuit as shown in figure given below, if all the FFs outputs(Q) are connected as the inputs of the NAND-gate with Q_3, Q_1 and Q_0 HIGH and rest are LOW. $\overline{Clr}$ pin is synchronous with clock, then the ripple counter works as



A mod-20 Up counter

B mod-11 Up counter

C mod-11 Down counter

D mod-12 Up counter

$clr = \overline{Q_4}\, Q_3\, \overline{Q_2}\, Q_1\, Q_0$

$= 0\ 1\ 0\ 1\ 1$ → 11

Asynchronous clear

0 → 10

MOD-11 UP

→ State at which Reset/Preset occure do nt count.

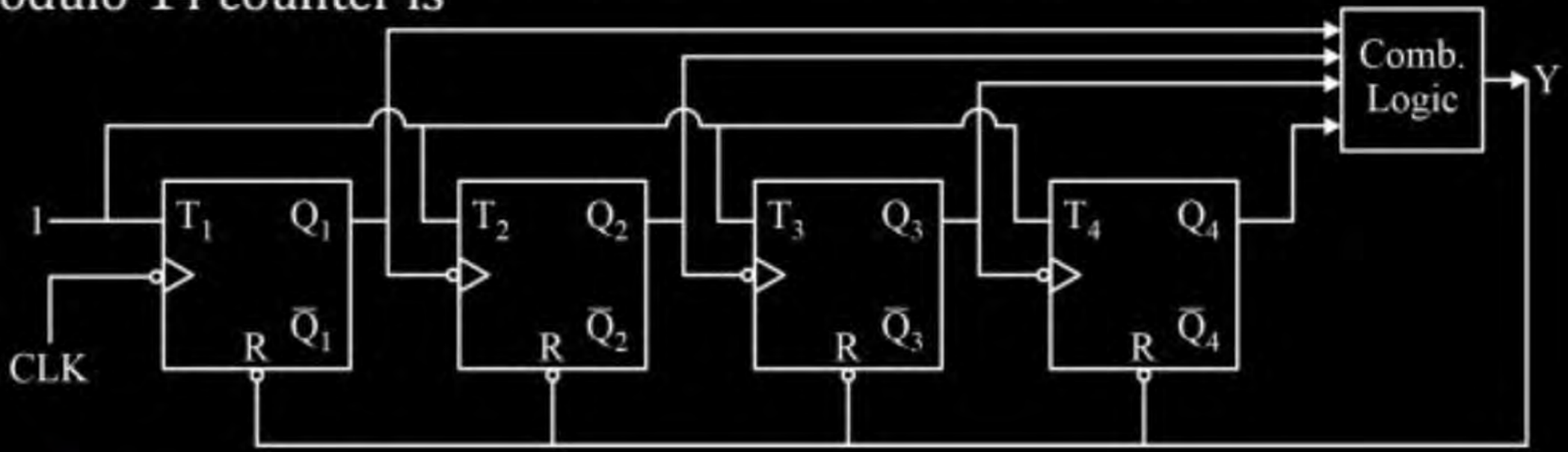
Synchronous Reset/Preset

→ State at which Reset/Preset occure we have to count.

0 → 11 → MOD-12 UP

(MCQ)

#Q. The counter shown in figure is built with 4-toggled FFs. The FFs can be set asynchronous clear when R = 0. The logic required to realize a modulo-14 counter is



A $Y = \overline{Q}_4 + \overline{Q}_3 + \overline{Q}_2 + Q_1$

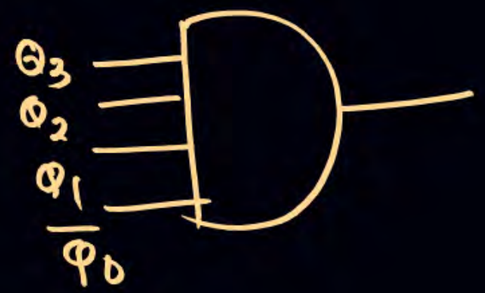
B $Y = Q_4\, Q_3\, Q_2\, \overline{Q}_1$

C $Y = Q_4 + Q_3 + Q_2 + \overline{Q}_1$

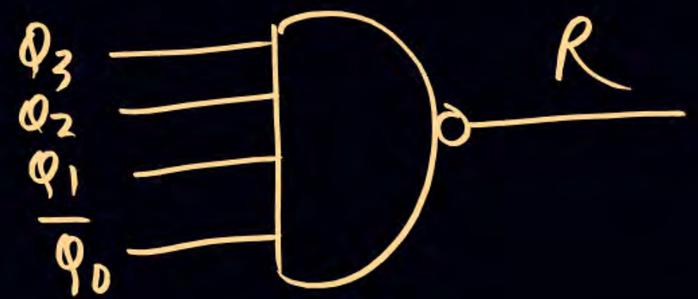
D $Y = \overline{Q}_4\, \overline{Q}_3\, \overline{Q}_2\, Q_1$

MOD-14 UP

Clr = 1 1 1 0



Active high

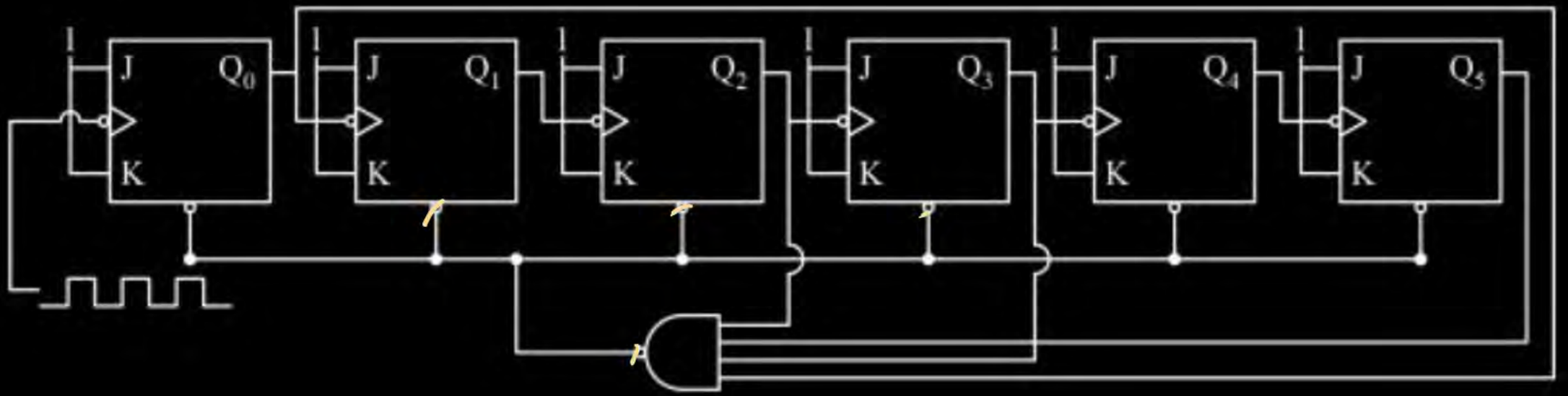


$$R = \overline{Q_3 \cdot Q_2 \cdot Q_1 \cdot \overline{Q_0}}$$

$$= \bar{Q}_3 + \bar{Q}_2 + \bar{Q}_1 + Q_0$$

(NAT)

#Q. Consider an asynchronous counter design as shown below. Assume Q_0 is the output of LSB FFs and Q_5 is the output of MSB FF and all J, K inputs are logically at '1'. $\overline{Clr}$ pin is synchronous, the mod number 'N' for this given counter is _____.



$Clr = Q_5 \bar{Q}_4 Q_3 Q_2 \bar{Q}_1 Q_0$

$1\ 0\ 1\ 1\ 0\ 1 \longrightarrow (45)$

Asynchronous Reset

0 — 44

MOD = 45 UP

synchronous Reset

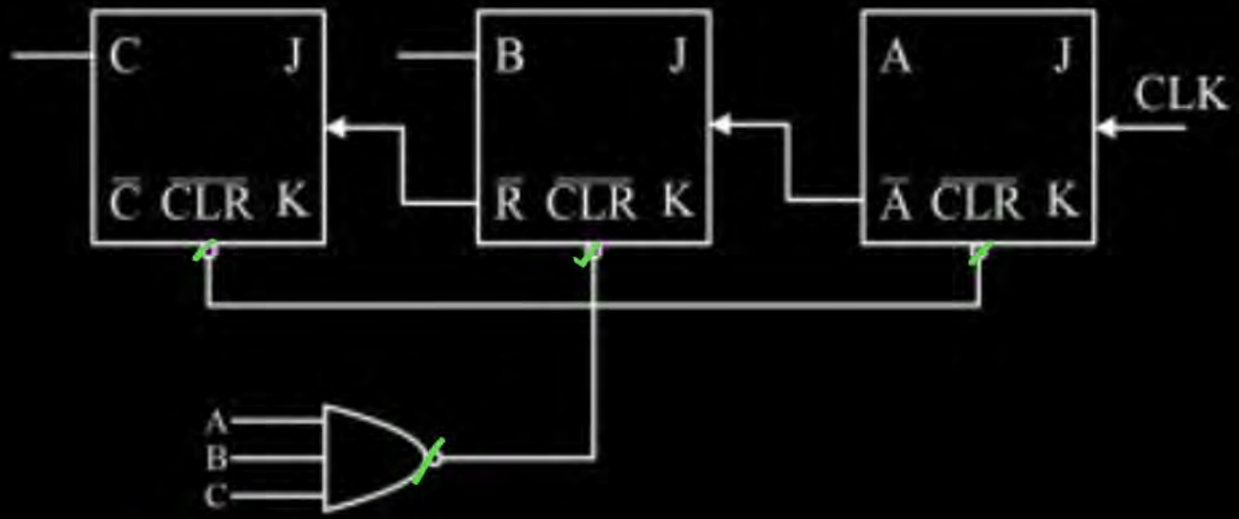
0 — 45

MOD = 46 UP

(MCQ)

#Q. Assuming all J = K = 1 in the counter shown below, find the counting sequence

UP counter



A. 000 to 111

B. 111to 000

C. 100 to 000

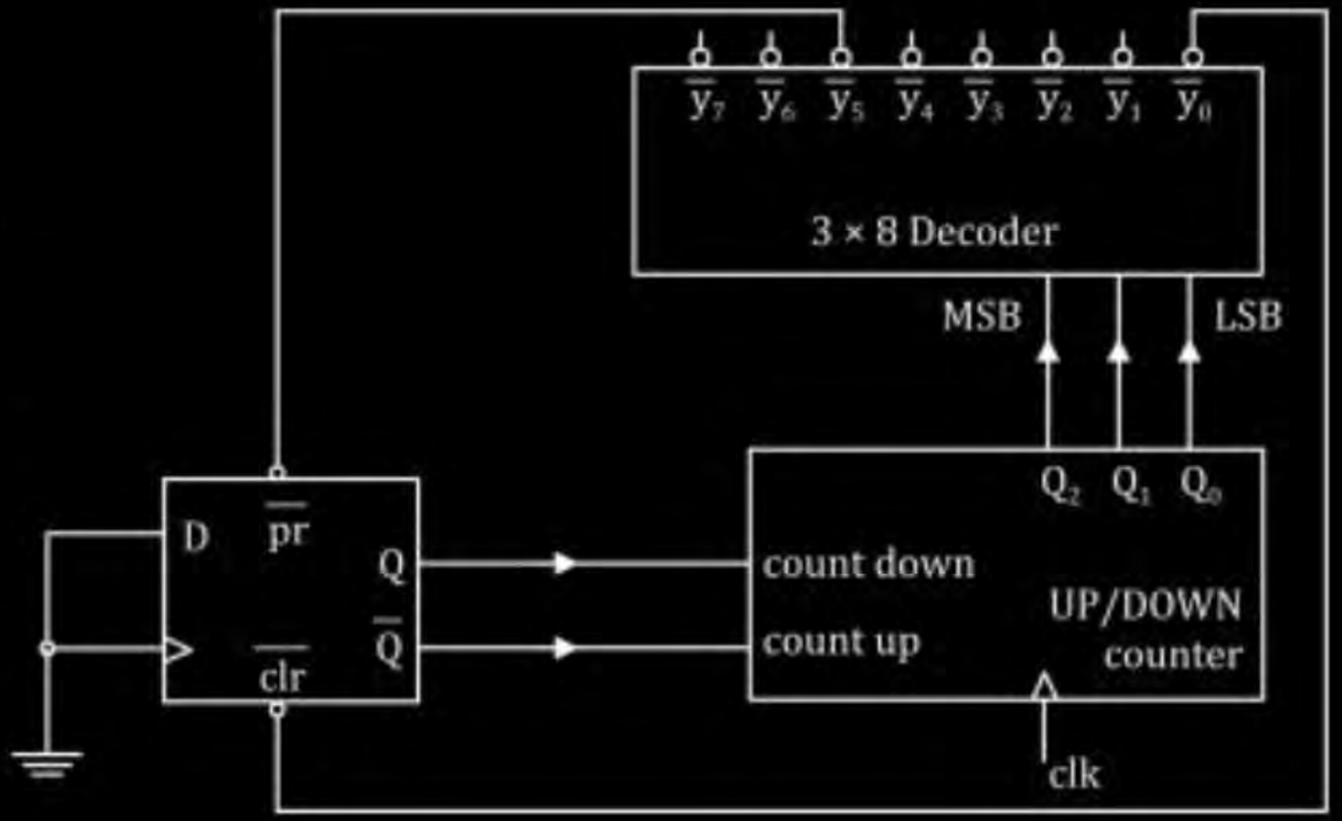
D. 000 to 110 ✓

Clr = (↓ ↓ ↓) X

000 → 110

#Q.

A flip flop with active low preset and clear, a 3×8 decoder and a up/down counter, are interconnected as shown below. Assume initially $Q_2 = Q_1 = Q_0 = 0$. The counter outputs in decimal for 12 clock pulses, will be



(A) 0, 1, 2, 3, 4, 4, 3, 2, 1, 1, 2, 3, 4

(B) 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5, 0

(C) 0, 1, 2, 3, 4, 5, 5, 4, 3, 2, 1, 0, 1

(D) 0, 1, 2, 3, 4, 5, 4, 3, 2, 1, 0, 1, 2

	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	0	0
7	0	1	1
8	0	1	0
9	0	0	1
10	0	0	0
11	0	0	1

12

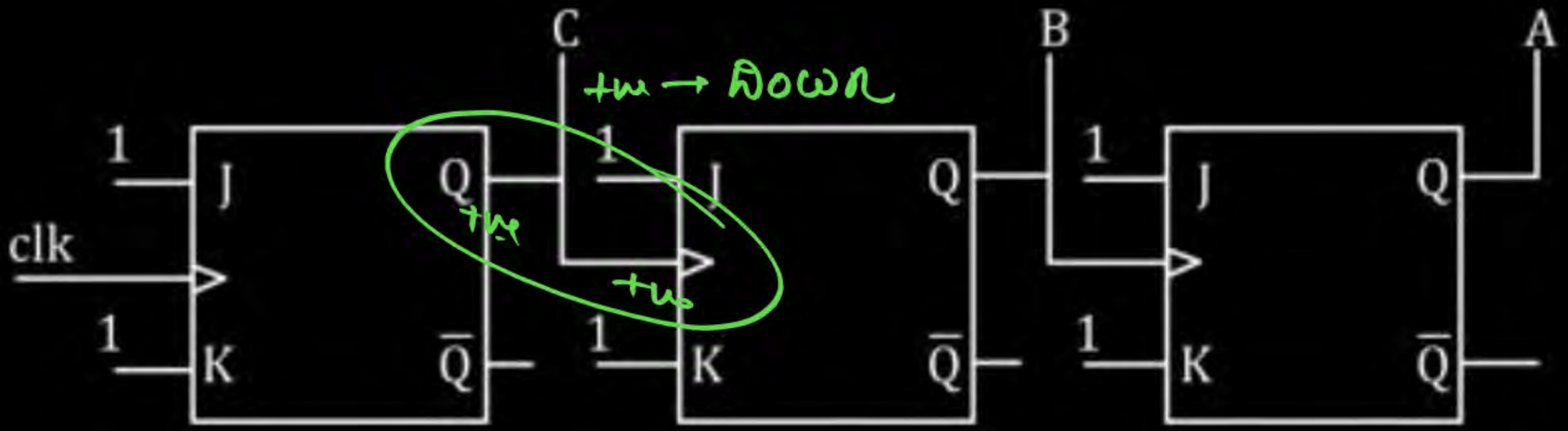
0 → 1 → 2 → 3 → 4 → 5 → 4 → 3 → 2 → 1 → 0

↓

3 ← 2 ← 1

#Q.

The circuit shown below, is a 3 -bit ripple counter with A as MSB. The flip flops in the circuit, are rising edge triggered. The counting direction is



(A) always up

(B) always down

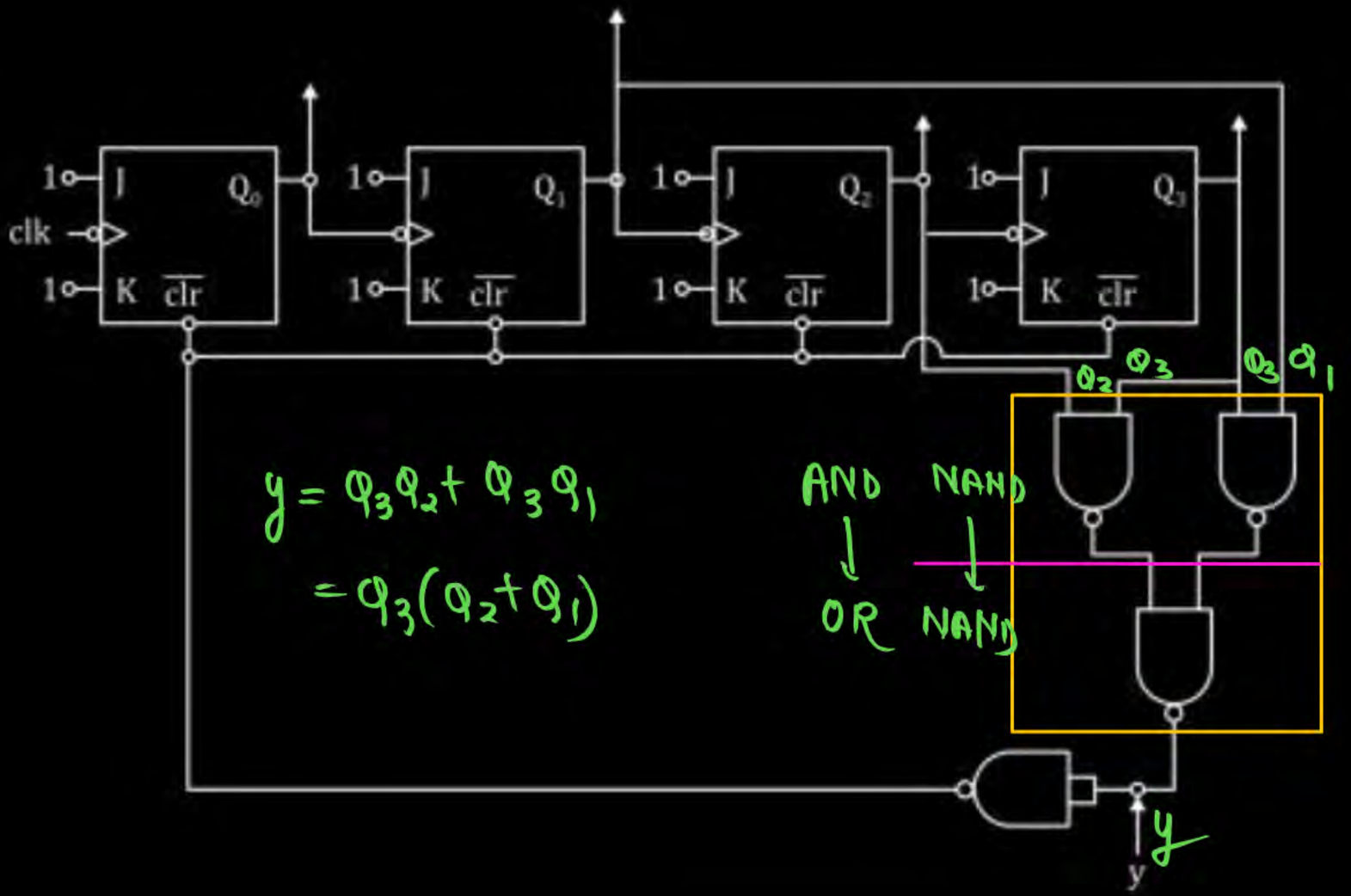
(C) up or down depending on initial state of C

(D) up or down depending on initial state of C, B and A.

#Q.

A circuit for truncated ripple counter together with a reset function labelled y, is shown below

The reset function y can be expressed as



A $y = Q_3 (Q_2 + Q_1)$

B $y = Q_3 + Q_2Q_1$

C $y = \overline{Q_3 (Q_2 + Q_1)}$

D $y = \overline{Q_3 + Q_2Q_1}$

#Q.

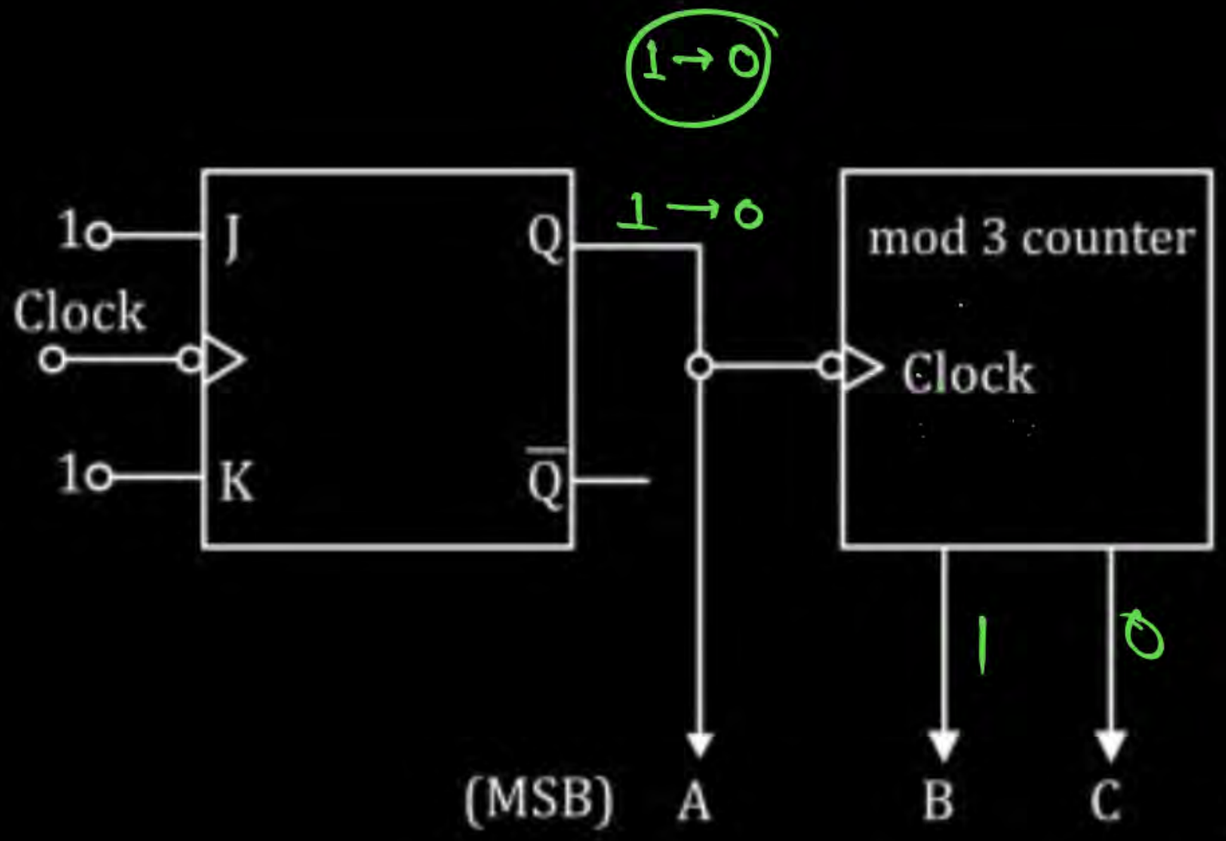
In the figure shown below, initially ABC = 000. After three clock pulses, the state ABC will be

A 110

B 011

C 001

D 101



CLK	A	B	C
0	0	0	0
1	1	0	0
2.	0	0	1
3.	1	0	1
4.	0	1	0

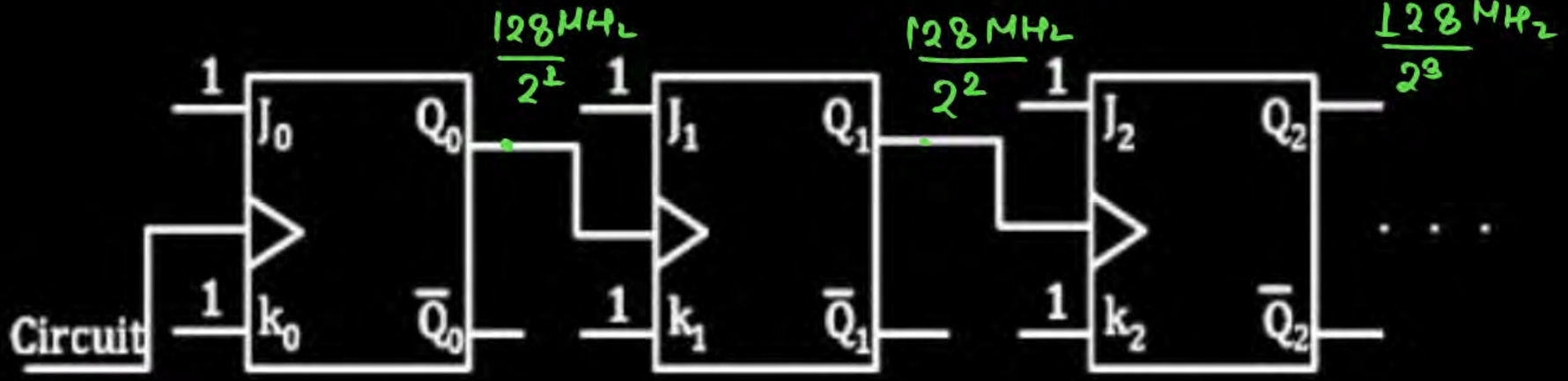
A sequential circuit is as given below has total 20 FFs connected. If input clock frequency is 128 MHz, at output of 16^{th} FF frequency of the waveform will be:

A 8 MHz

B 12.8 MHz

C 1.95 KHz.

D 4 MHz



$f_{in} = 128 MHz$

$f_{Q_{15}} = \frac{f_{in}}{2^{15}} = \frac{128 \times 10^6 Hz}{2^{15}} = \frac{128 \times 10^6}{2^9} = \frac{1000 kHz}{2^9}$

(Q_{15} → 16th FF o/p)

$= \frac{1000}{512} kHz$

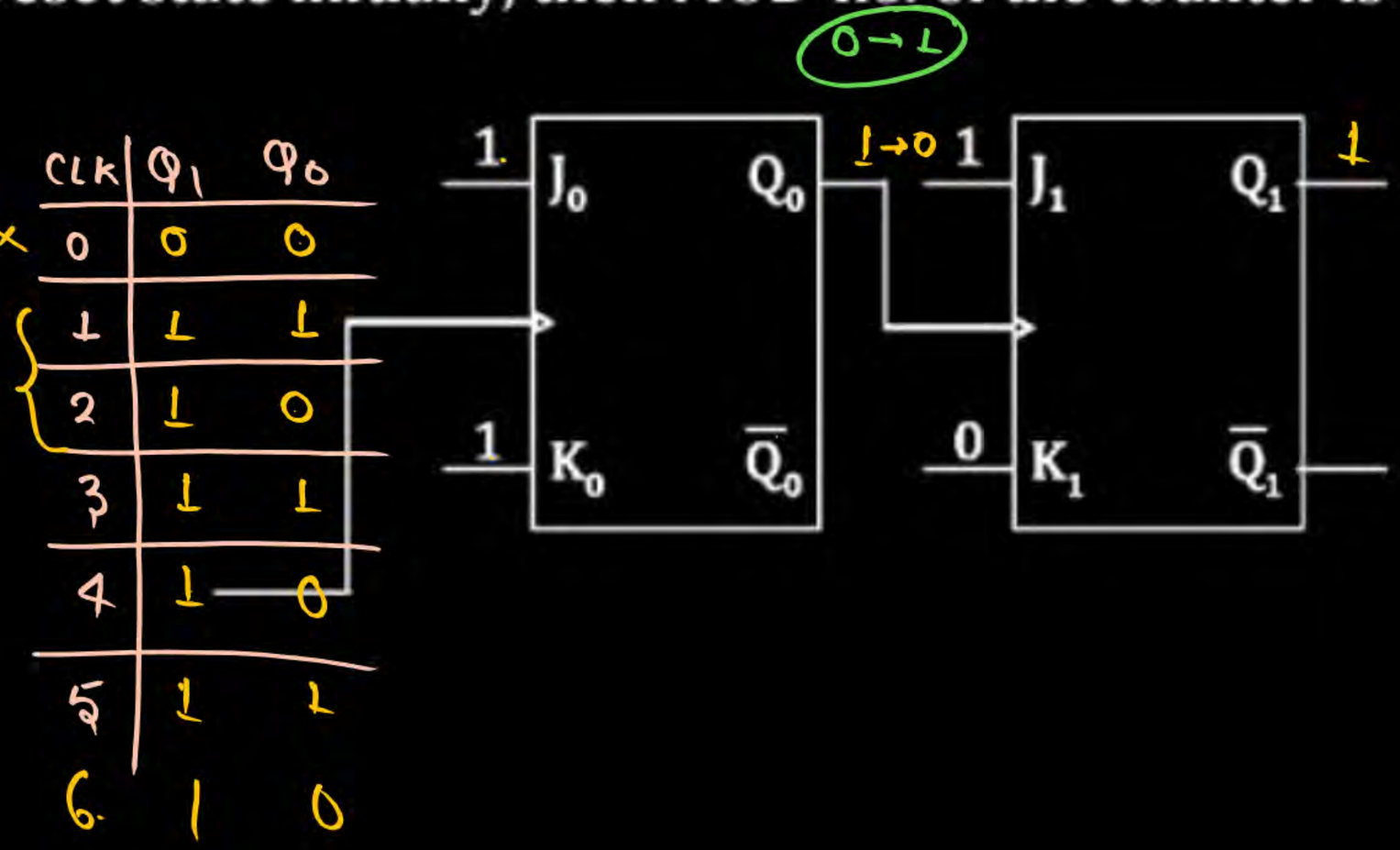
NOTE

freq → K → $10^3 = 1000$

In Binary (bit) $K = 2^{10} = 1024$

Question **(MCQ)**

A sequential circuit is as given below:
Both the FFs are at reset state initially, then MOD-no. of the counter is

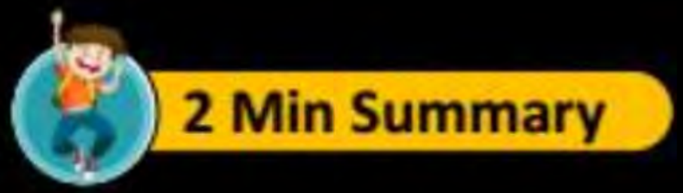


A MOD-4 counter

B MOD-3 counter

C MOD-2 counter

D None of these



Sequential Circuit

Thank You GW Soldiers!