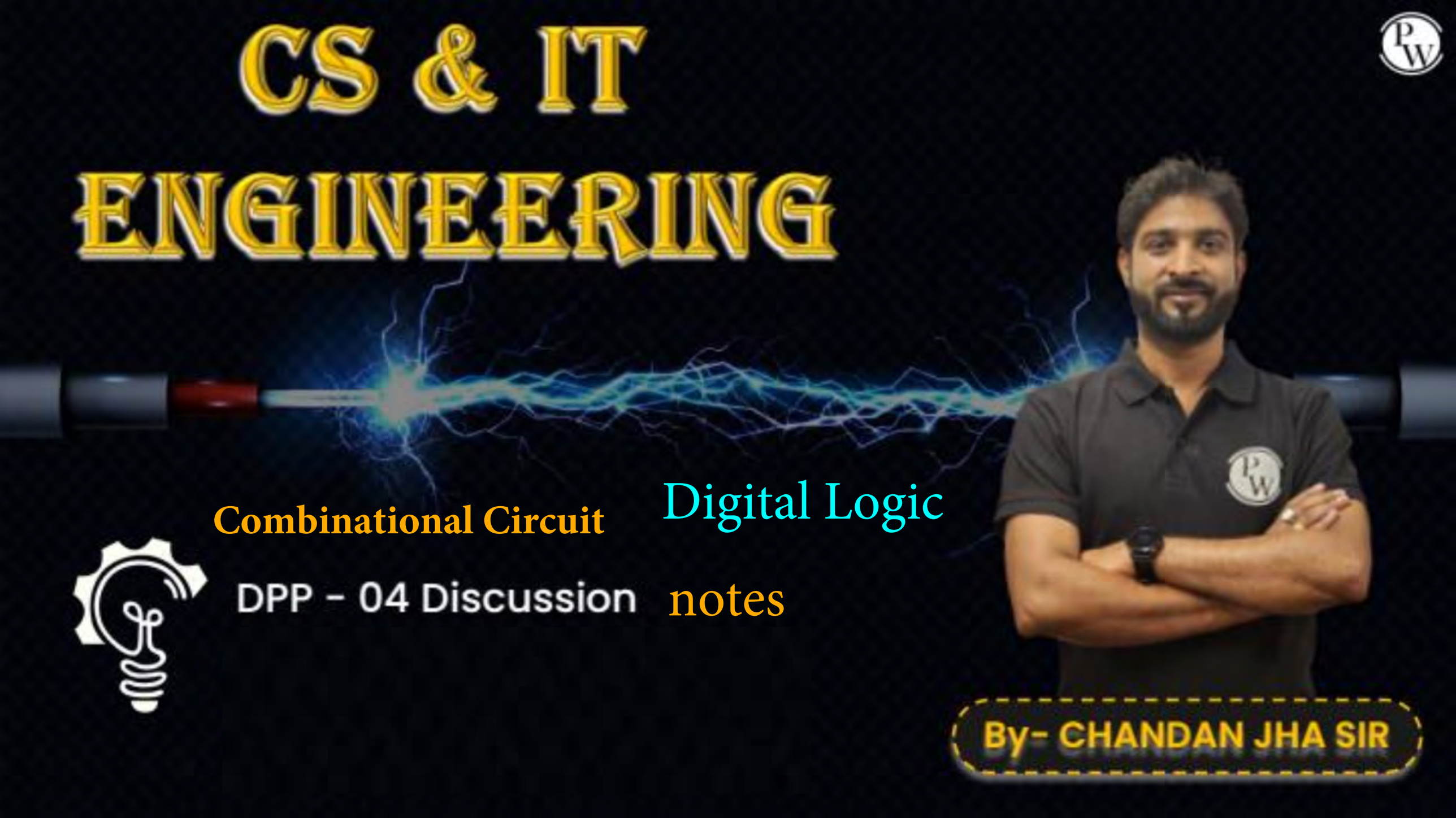
CS & IT ENGINEERING



Combinational Circuit

Digital Logic

DPP - 04 Discussion

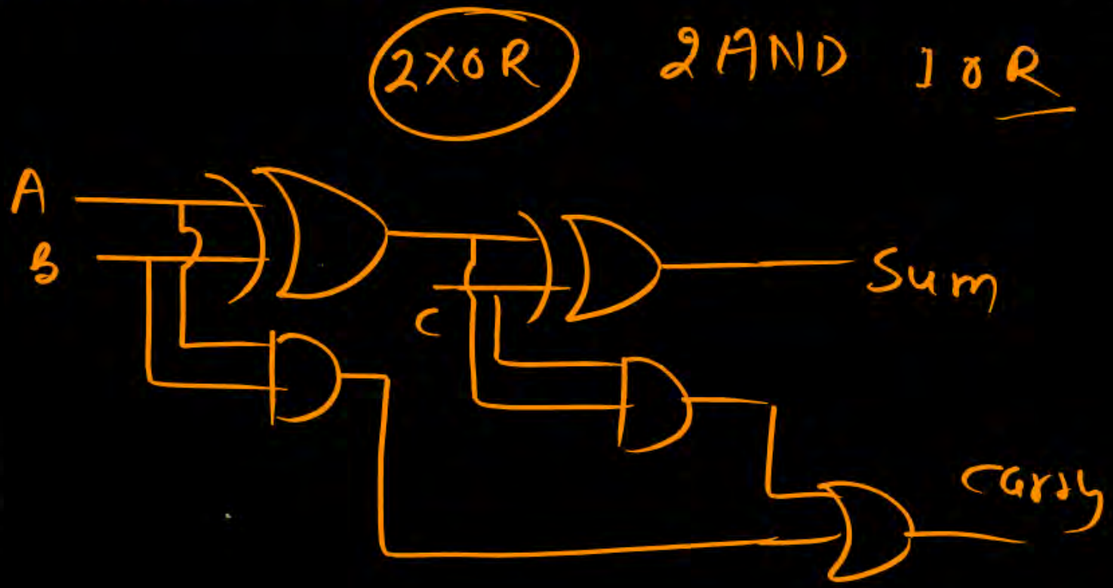
notes

By- CHANDAN JHA SIR

01 DPP Question

Question **MCQ**

What are basic gates required to implement a full adder



A 1 EX – OR gate, 1 AND gate

B 2 EX – OR gate, 1 OR gate

C 2 EX – OR gate, 2 AND gate, 1 OR gate

D 1 EX – OR gate, 2 AND gate, 2 OR gate

Question **NAT**

How many half adders are required to implement the following expressions.

$$D = \bar{A}BC + A\bar{B}C, \quad E = A \oplus B \oplus C$$

$$F = \bar{A}C + AB\bar{C} + \bar{B}C$$

$D = (\bar{A}B + A\bar{B})C$

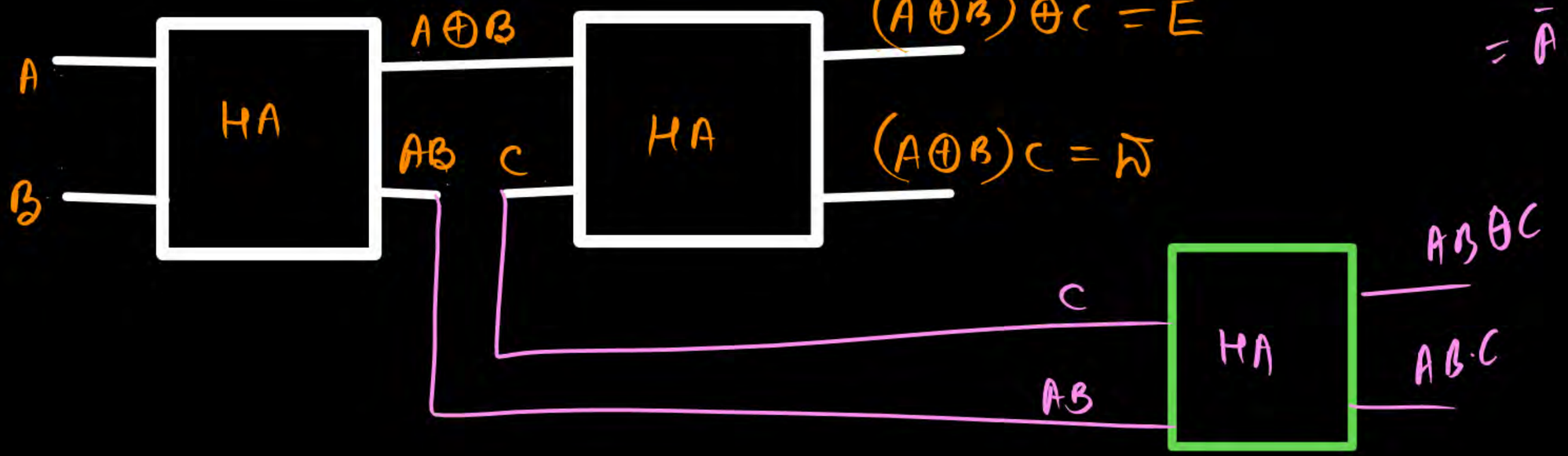
$= (A \oplus B)C$

$A \oplus B \oplus C = \bar{A}BC + AB\bar{C}$

$= (\bar{A} + \bar{B})C + AB\bar{C}$

$= \bar{A}C + \bar{B}C + AB\bar{C}$

$= F$ //



Question MCQ

★★★

The following multiplexer circuit is equivalent to _____.

A Implementation of sum equation of full adder

B Implementation of carry equation of full adder

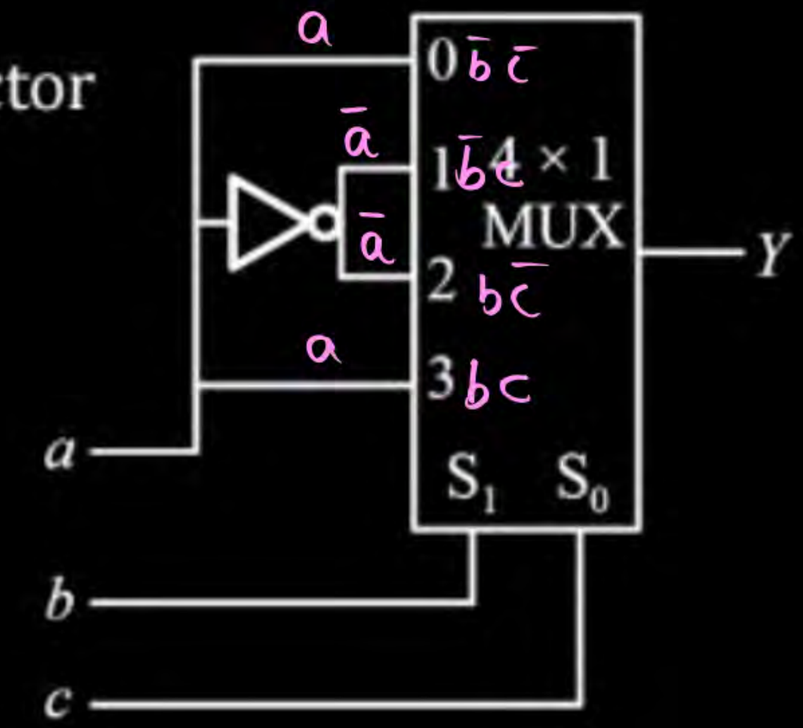
C Implementation of borrow equation of full subtractor

D All the above

$$Y = a\bar{b}\bar{c} + \bar{a}\bar{b}c + \bar{a}bc + abc$$

$$= \Sigma m(1,2,4,7) = a \oplus b \oplus c$$

sum, Diff



Question MCQ

★★☆

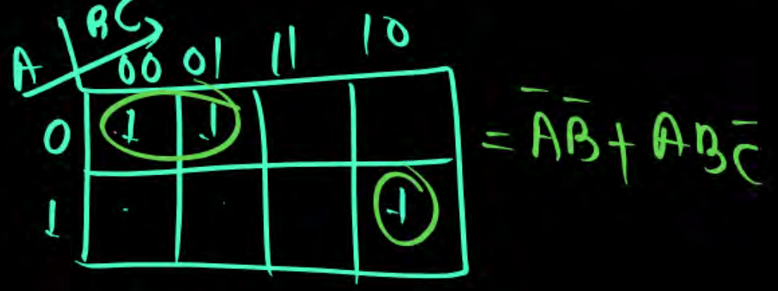
A 3 line to 8 line decoder with three inputs A, B, C and two outputs y_1 and y_2, is configured as shown below. The minimized expression of outputs will be

A $y_1 = \bar{A}\,\bar{B} + AB\bar{C};\ y_2 = \overline{A \oplus B}$

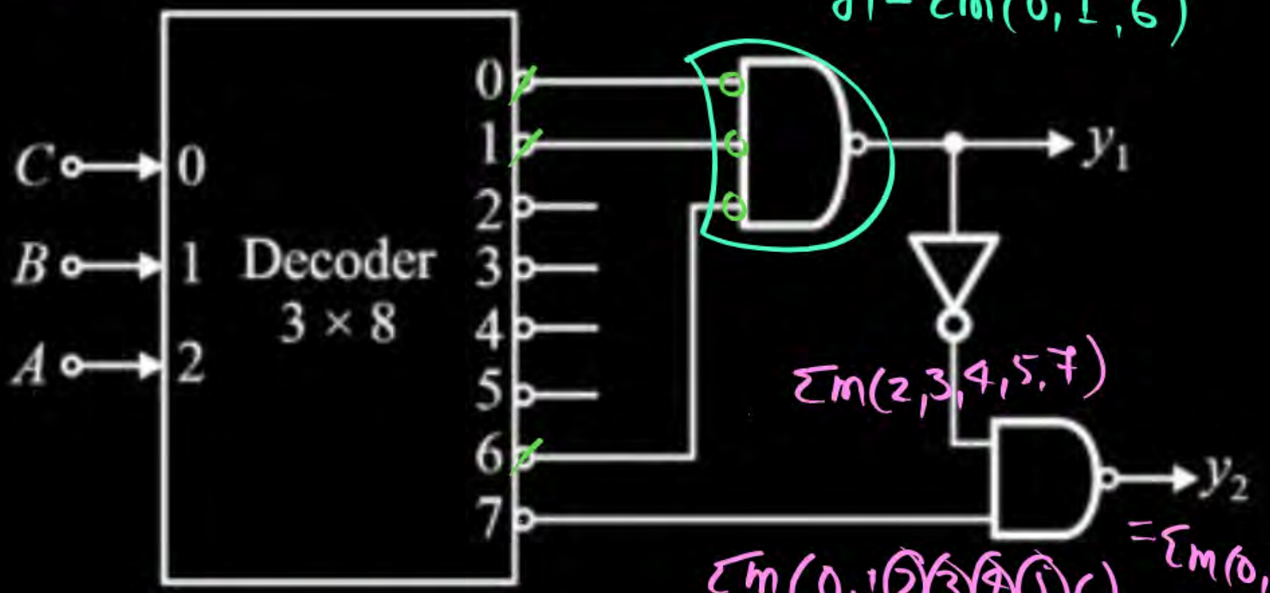
B $y_1 = AB + \bar{A}\bar{B}C;\ y_2 = A \oplus B$

C $y_1 = \bar{A}B + A\bar{C};\ y_2 = AB + AC$

D $y_1 = A\bar{B} + \bar{A}C;\ y_2 = \bar{A}B + \bar{B}C$



$= \bar{A}\bar{B} + AB\bar{C}$



$y_1 = \Sigma m(0,1,6)$

$\Sigma m(2,3,4,5,7)$

$\Sigma m(0,1,2,3,4,5,6)$

$= \Sigma m(0,1,6,7)$

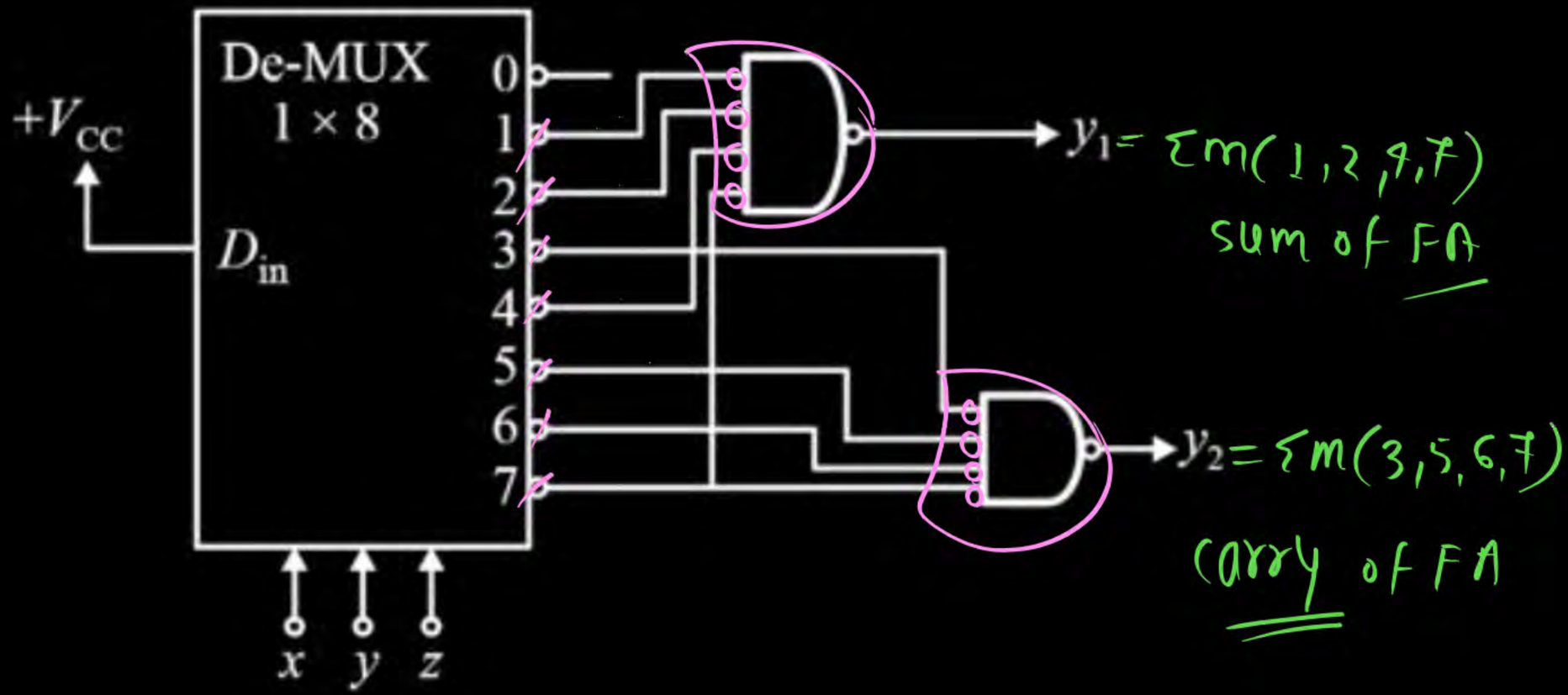
$y_2 = \Sigma m(0,1,6,7)$

$= \bar{A}\bar{B} + AB = A \odot B = \overline{A \oplus B}$

Question **MCQ**

★★★

A demultiplexer of size 1 × 8 with active low outputs, is programmed as shown below. The circuit has three inputs x, y, z and generates two outputs y_1, y_2.



What is this circuit

A Half subtractor

B Full subtractor

C Half adder

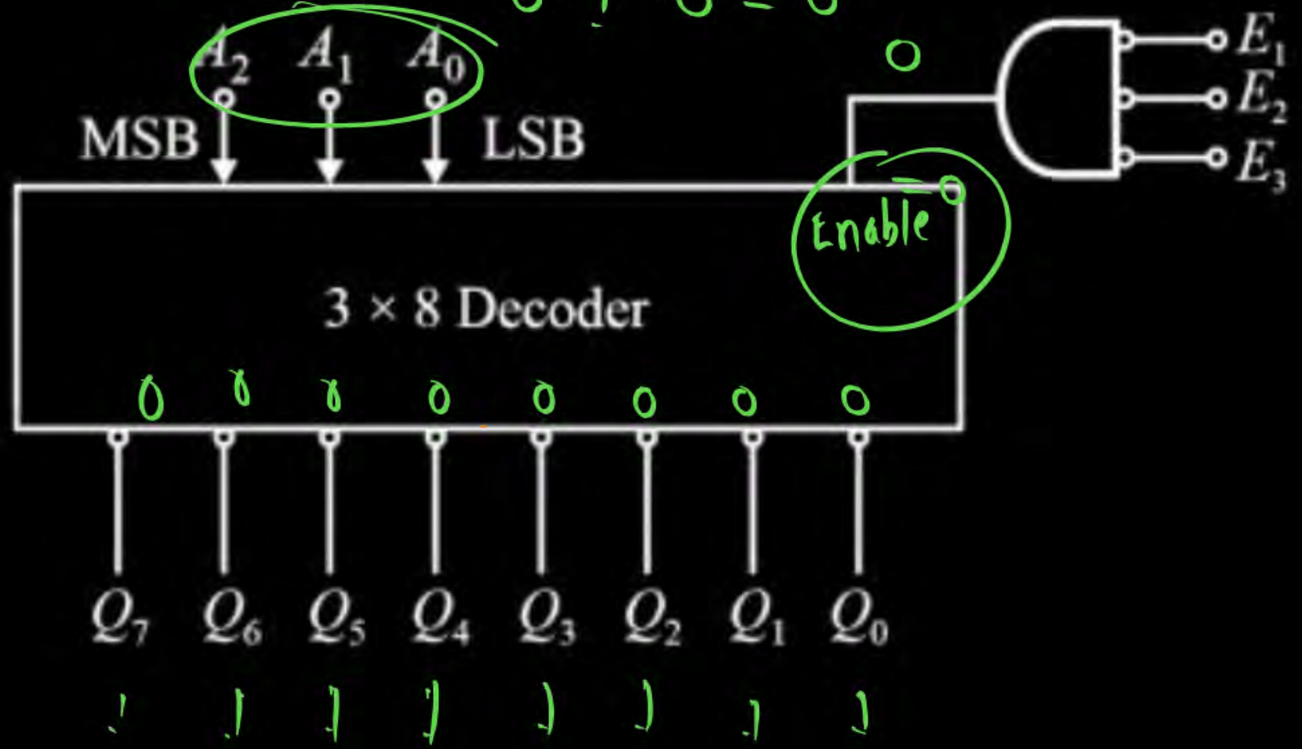
D Full adder

Question **MCQ**

The logic diagram of a 3 × 8 decoder with active low outputs is shown below. What is state of outputs Q_7, ... Q_0 for the set of inputs $E_3 = E_1 = 1$, $E_2 = 0$, $A_2 = A_1 = 1$ and $A_0 = 0$?

Enable = $\bar{E}_3\,\bar{E}_2\,\bar{E}_1$

0 1 0 = 0



A	1111	1111
B	1011	1111
C	1111	0111
D	0000	0000

Question MCQ

★★☆

A 3 line to 8 line decoder with active low outputs, is used to realize Boolean function involving three variables x, y and z(x is MSB and z is LSB) as shown below.

The minimized Boolean function f(x, y, z) in POS format, will be

$f = \Sigma m(1,3,5,6)$

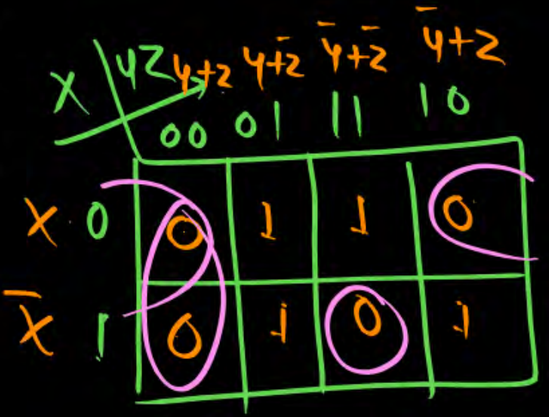
A $(\bar{x}+\bar{y}+\bar{z})(x+y+z)(x+\bar{y}+\bar{z})(\bar{x}+y+\bar{z})$

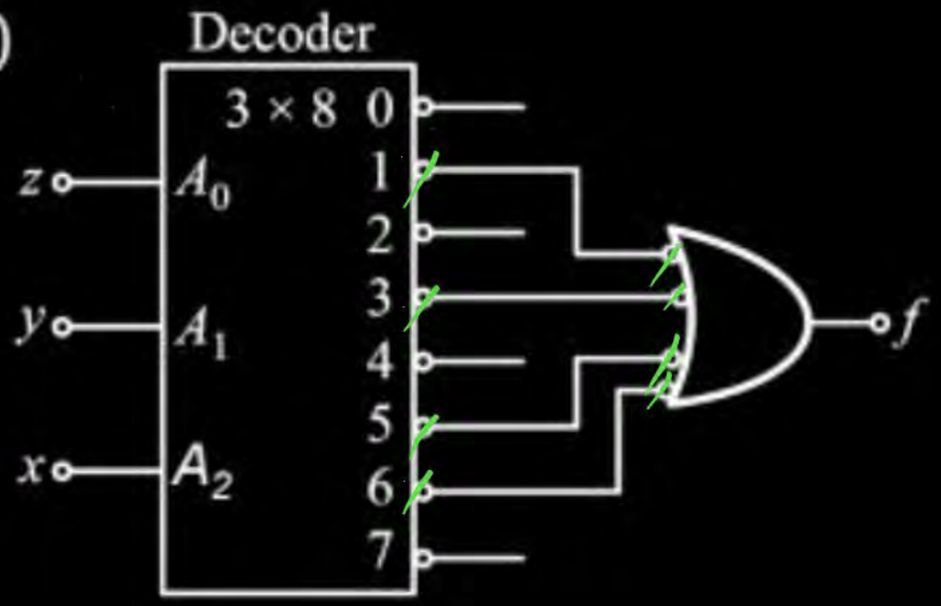
B $(\bar{x}+\bar{y}+z)(\bar{x}+y+z)(x+\bar{y}+z)(x+y+\bar{z})$

C $(x+z)(y+z)(\bar{x}+\bar{y}+\bar{z})$

D $(\bar{x}+\bar{z})(\bar{y}+\bar{z})(x+y+z)$

$(x+z)\cdot(y+z)\,(\bar{x}+\bar{y}+\bar{z})$





Question **MCQ**

★★☆

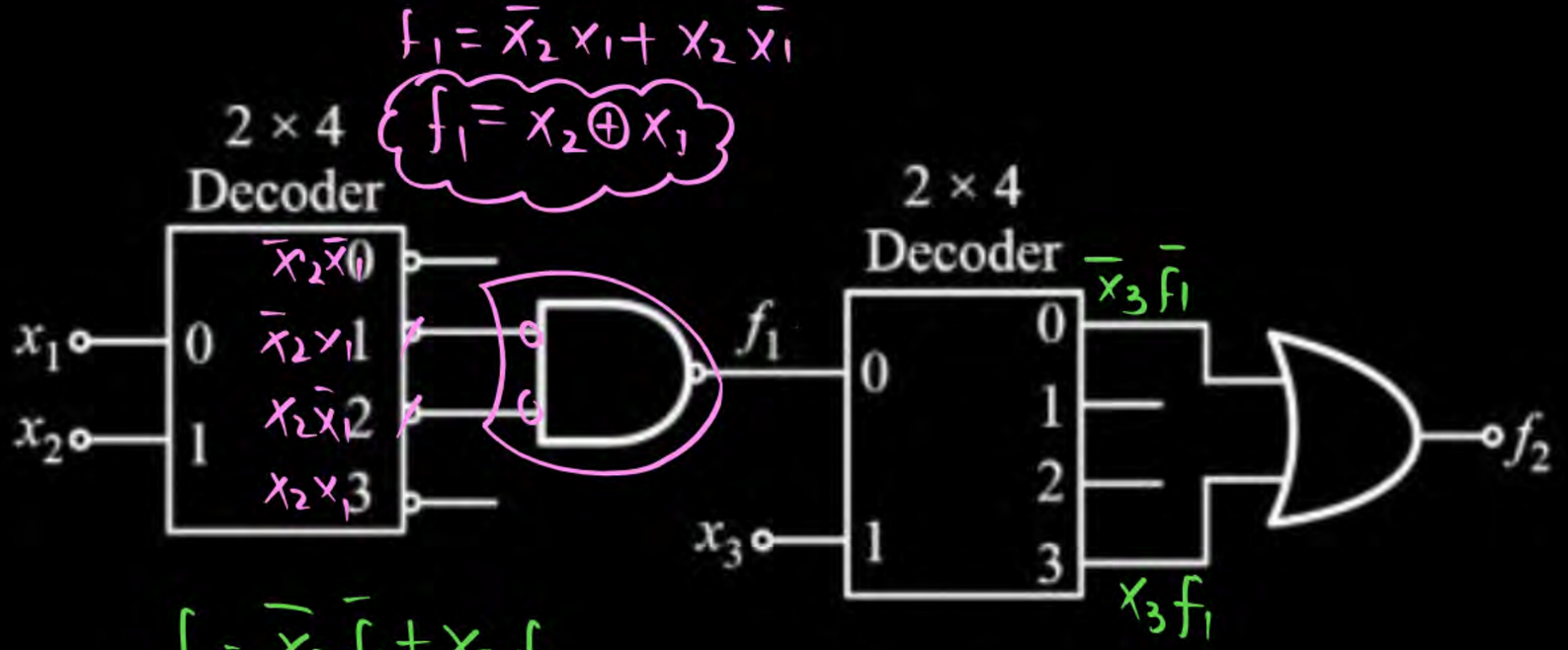
Two 2 × 4 decoders one with active low outputs and another with active high output are interconnected as shown below. The output function $f_2(x_3, x_2, x_1)$ will be

A $f_2 = (x_1 \oplus x_2) \odot x_3$

B $f_2 = (x_1 \odot x_2) \odot x_3$

C $f_2 = (x_1 \oplus x_2) \oplus x_3$

D $f_2 = (x_1 \oplus x_2) \oplus x_3$



$f_2 = \bar{x}_3 \bar{f}_1 + x_3 f_1$

$= x_3 \odot f_1 = x_3 \odot (x_2 \oplus x_1)$

Question **MCQ**

Three half adders HA_1, HA_2 and HA_3 are inter-coupled as shown below. The four output functions y_1, y_2, y_3 and y_4 are expressed in terms of inputs a, b and c. Which one of the following output expressions, is correct?

A $y_1 = (a \oplus b)c$

B $y_2 = (a \oplus b) \oplus c$

C $y_3 = ab \oplus c$

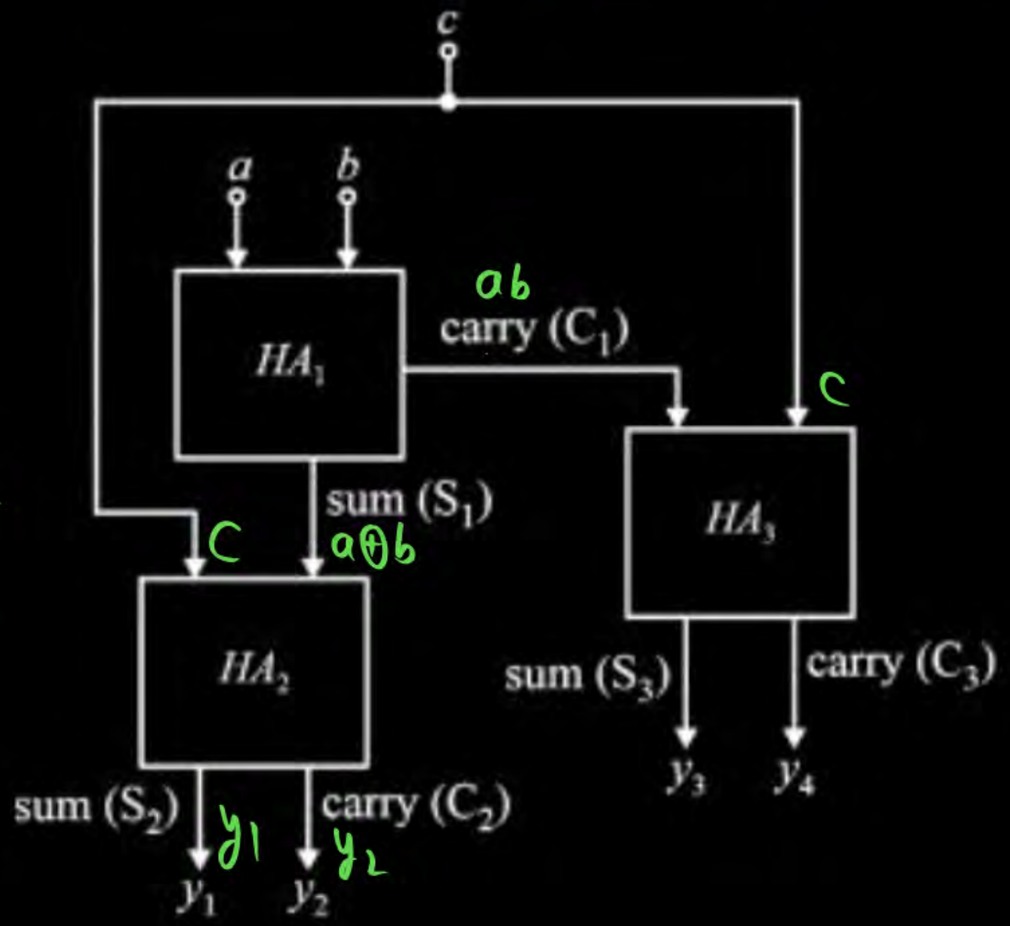
D $y_4 = a(b \oplus c)$

$y_1 = a \oplus b \oplus c$

$y_2 = (a \oplus b)\, c$

$y_3 = ab \oplus c$

$y_4 = abc$



Question **MCQ**

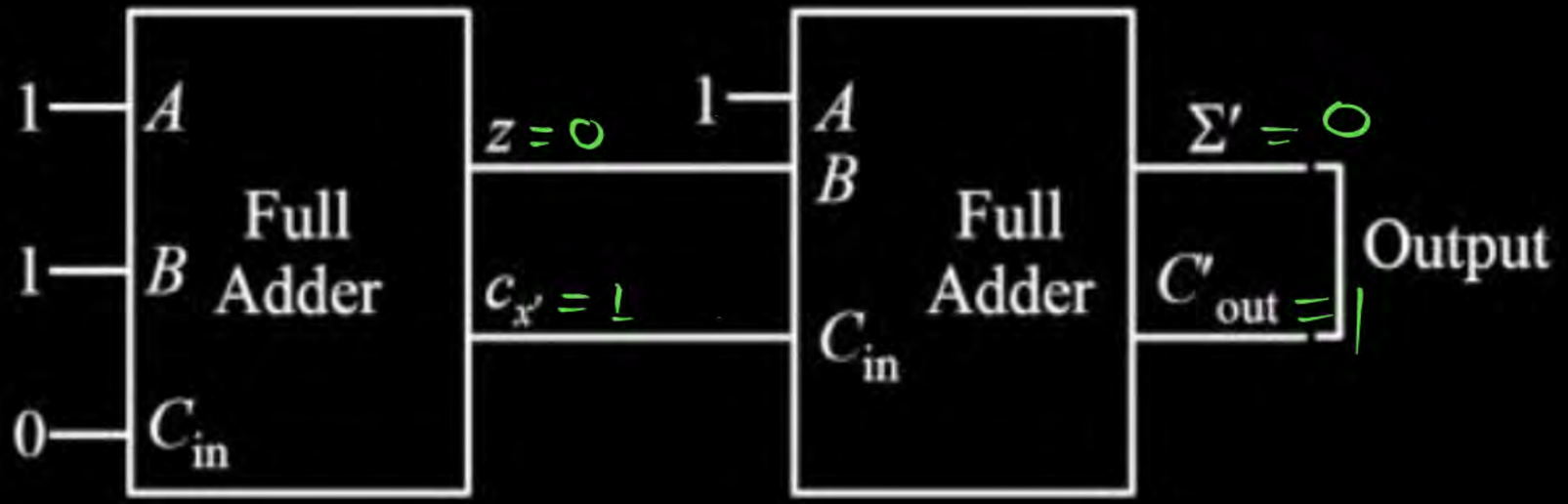
Determine the outputs for the circuit shown below.

A $\Sigma' = 1, C'_{out} = 1$

B $\Sigma' = 0, C'_{out} = 0$

C $\Sigma' = 0, C'_{out} = 1$

D $\Sigma' = 1, C'_{out} = 0$



1 + 0 + 1

Question MCQ

How many half adders, will be required to add two k bit numbers?

A $2k + 1$

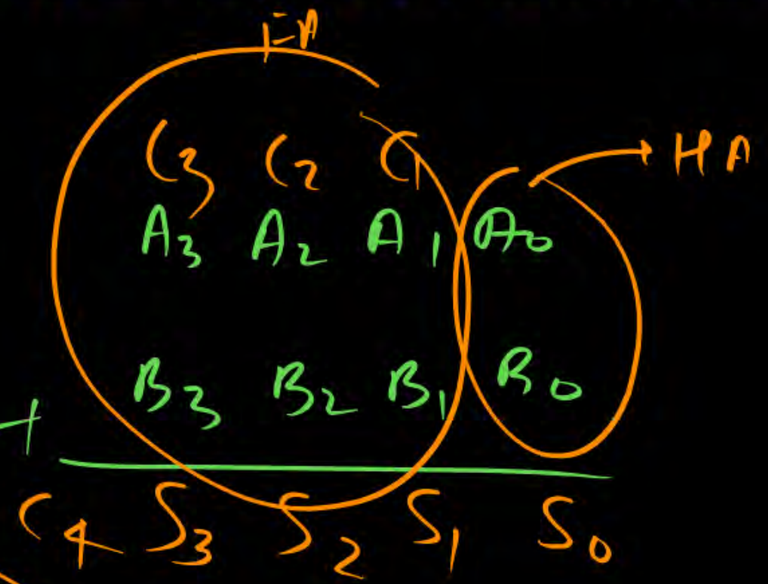
B $2k - 1$

C $2k$

D $2(k + 1)$

4 bit

3 FA + 1 HA



k bits

$(2k-1)$ HA + $(k-1)$ OR

Question NAT

★★☆

Eight 1-bit full adders are cascaded. Each 1-bit full adder generates carry out bit in 10 ns and sum bit in 30 ns. The number of addition performed per second, will be __1__ $\times 10^7$

$n = 8$

$T = (n-1)T_{carry} + Max\{T_{sum}, T_{carry}\}$

$= \{7 \times 10 + 30\}$ ns

$T = 100$ ns

$\frac{1}{T} = \frac{1}{100 \times} 10^9 = \frac{100 \times 10^7}{100} = 1 \times 10^7$

Thank you

GW

Soldiers !