# **Batch: English**

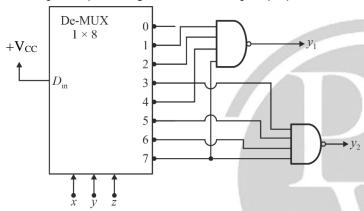
# Digital Logic Combinational Circuits

DPP-03

[MCQ]

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1. A demultiplexer of size  $1 \times 8$  with active low outputs, is programmed as shown below. The circuit has three inputs x, y, z and generates two outputs  $y_1$ ,  $y_2$ .



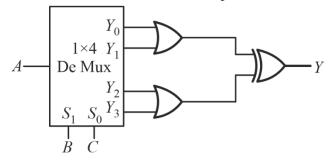
If de-multiplexer has active high output instead of active low outputs, then in order that outputs do not change

- (a) NAND gates should be replaced by NOR gates
- (b) NAND gates should be replaced by OR gates
- (c) NAND gates should be replaced by AND gates
- (d) the inputs x, y, z should be inverted

### [MCQ]

**★**★☆

2. For what values of A, B, C the output (Y) will be 0

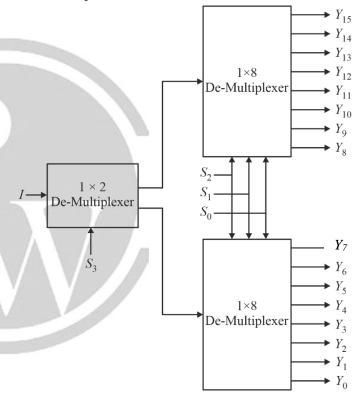


- (a) A = 1, B = 0, C = 0
- (b) A = 0, B = 1, C = 1
- (c) A = 1, B = 1, C = 0
- (d) A = 1, B = 1, C = 1

### [MCQ]



**3.** The figure shown below is a block diagram of \_\_\_\_\_ demultiplexer?

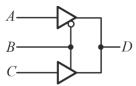


- (a) 1 to 4
- (b) 1 to 8
- (c) 1 to 16
- (d) None of the above

## [MCQ]



4. Identify the circuit shown below?



- (a) Bidirectional buffer
- (b) De-multiplexer
- (c) Multiplexer
- (d) Encoder

### [NAT]



**5.** How many inputs will a decimal to BCD encoder have?\_\_\_\_\_

# [MCQ]



- **6.** Which one of the following de multiplexer requires only five select lines?
  - (a)  $1 \times 2$  de Mux
  - (b)  $1 \times 4$  De Mux
  - (c)  $1 \times 8$  De Mux
  - (d)  $1 \times 32$  De Mux

### [NAT]



7. What is the minimum number of  $1 \times 4$  De Mux required to implement  $1 \times 2^{10}$  De Mux.\_\_\_\_

## [MCQ]



8. To implement a 1 : 128 De-Mux we require *M* number of 1 : 8 De-mux and N numbers of 1 : 2 De-mux.

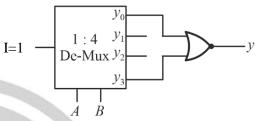
Then which of the following is correct

- (a) (M-N)/2 = 9
- (b) M + N = M
- (c) M/N = M
- (d) (M+N)/2=9

## [MCQ]



**9.** Consider a circuit as shown below:



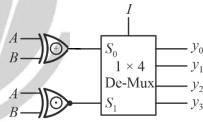
Output y is

- (a) A + B
- (b)  $\overline{A \cdot B}$
- (c)  $A \oplus B$
- (d) A  $\odot$  B

### [MCQ]



10. Consider a combinational circuit as shown below.



For any sequence A, B which of the output pins  $(y_0 \text{ to } y_3)$  can be active

- (a)  $y_0$  and  $y_3$  only
- (b)  $y_1$  and  $y_2$  only
- (c)  $y_1$  only
- (d) all pins can be active

# **Answer Key**

- 1. (b)
- **2. (b)**
- 3. (c)
- 4. (c)
- **5.** (10)
- 6. (d)
- 7. (341)
- 8. (c)
- 9. (c)
- **10.** (b)





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