CS & IT ENGINEERING

Computer Organization Architecture

Cache Organization

DPP- 02 Discussion Notes

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[MCQ]

#Q. Consider a 512KB direct mapped cache with block size of 32 bytes. The main memory address is of 34-bits. The size of index and tag in bits are?

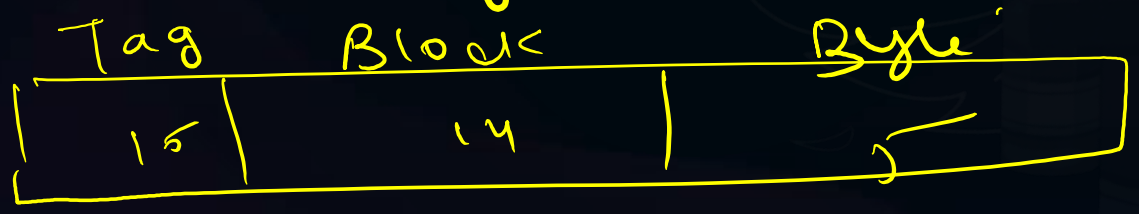
A 15, 14

B 14, 15

C 19, 14

D 14, 19

34 bit Main memory address is divide.



Block size = 32 bytes = 2^5 bytes

no. of 5 bits

No. of block in Cache = 512 KB / 32 KB

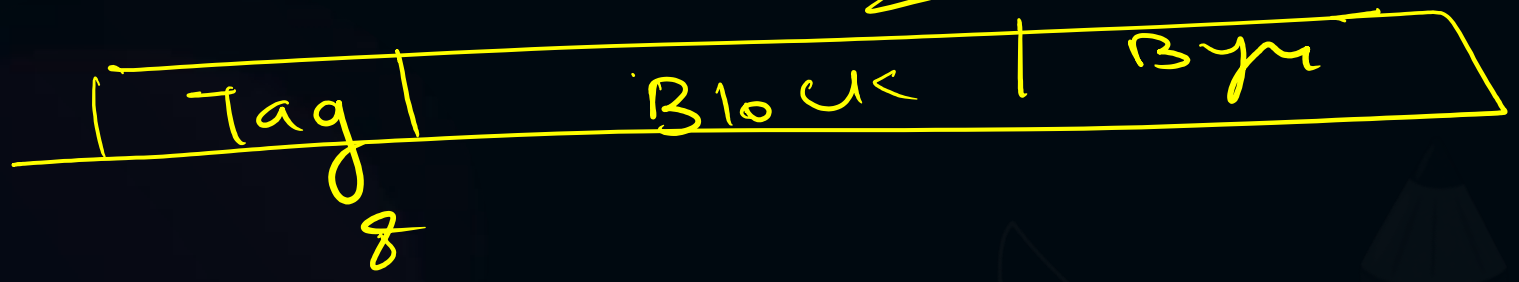
= 16K = 2^{14}

Tag bits ⇒ 34 − (14 + 5)

= 15 bits

[NAT]

#Q. Consider a direct mapped cache of size 256MB. Cache controller maintains 8-bits tag for each block in cache. The maximum size of main memory (byte addressable) supported in the system is 64 GB?



$= \log(\text{Cache Size}) = \log 256\,\text{MB}$

$= 28$ bits

enter Main Memory address

$8 + 28 = 36$ bits

Main Memory size $= 2^{36}$

$=$ 64 GB

[NAT]

#Q. The size of memory required at cache controller to store metadata is 2KBytes. The metadata includes tag bits, 1 modified bit and 1 valid bit. The cache contains 1K blocks of 16bytes each and organized as direct mapped. The size of main memory is___ Mbytes?

No. of block in Cache = 1K

$= 2^{10}$

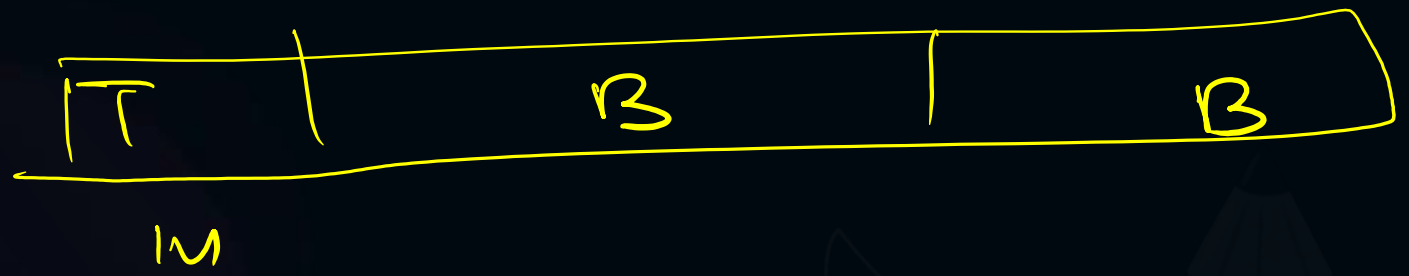
Block Size = 16 bytes $= 2^4$

14 + 10 + 4 = 28 bit

$2^{28} = 256$ MB

[NAT]

#Q. Consider a direct mapped cache of size 256KB. The CPU generates x- bit addresses. The number of tag bits in main memory address are 14 bits then value of x is _____?



log 14 + 18 = 32 bit

[MCQ]

#Q. Assume a computer has 32-bit addresses. Each block stores 64 bytes. A direct-mapped cache has 512 blocks. Match the block (line) of the cache (in decimal) we look for each of the given hexadecimal addresses in the table?

A. 1A2BC012: 256, FFFF00FF: 3, 12345678: 345, C109D532: 340

B. 1A2BC012: 512, FFFF00FF: 7, 12345678: 243, C109D532: 320

C. 1A2BC012: 128, FFFF00FF: 5, 12345678: 345, C109D532: 420

D. 1A2BC012: 255, FFFF00FF: 1, 12345678: 247 , C109D532: 240

Tag	Block	Byte
17	9	6

No. of block
$= 512$
$= 2^9$
$64 = 2^6$
6 bit

$(1A2BC012_6) = 000\ 1101\ 0101\ 1011$

Block no. $(101010100)_2$

$= 2(340)_{10}$.

[NAT]

#Q. Consider a cache with 2^{13} blocks of size 32Bytes each. The CPU generates addresses of 32-bits. The cache controller stores 1 valid bit, 1 modified bit and tag-bits for each metadata entry. The cache controller has a maximum memory of 18Kbytes to store the metadata. The cache is organized as k-way set associative. Maximum value of k to utilize the cache controller memory in optimized manner is ___?

32 bytes = 2^5.

Tag directory size = No of block x (Tag bit + extra)

18 K byte = 2^{13} x (Tag + 1 + 1) bit

18 K x 8 = 2^{13} x (Tag + 1 + 1) bit

18 = tag + 2

Tag = 16

Tag bit (16)	byte (5)

Set-offset

no. of bit

32 - (16 + 5)

= 11 bit

$2^{11} = 2^{13}$

= 4

[NAT]

#Q. Consider a direct mapped write back data cache of size 2KB with the block size of 128 bytes. The cache is considered to be empty initially. The byte addressable main memory has size 1Mbytes. Further consider that there is an array A[35][20] with each element occupies 4 bytes. The base address of array is (1A300)16. The array is accessed 3 times. And between the accesses, there is no any data cache changes happen. Hit ratio (correct upto 1 decimal place) of cache for this array access is ___%?

Array size $35 \times 20 = 700$ elements

$\Rightarrow 700 \times 4$ bytes $= 2800$ bytes

$= \underline{\text{ceil}}\ (2800 \text{ bytes} / 128 \text{ bytes})$

$= 22$

Second Refence $\Rightarrow 22 - 16 = 6$ blocks

Total no. of bus $= 678 + 688 + 688$

$\Rightarrow \underline{2054}$

Hit Ratio $2054 / 2100$

$= 0.97$

$\geq 97\%$

THANK - YOU