

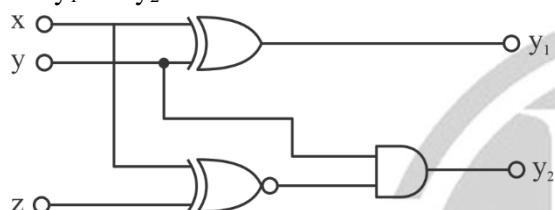
**Subject : Digital Electronics**  
**Chapter : Combinational Circuit**  
**Topic : HS, FS, Serial Adder**

DPP-05

[MCQ]

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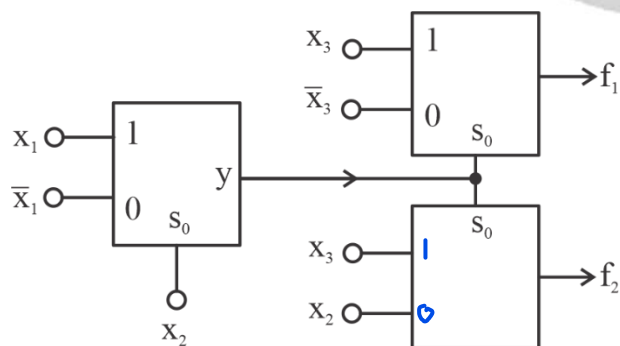
1. The circuit shown below, is a controlled half adder/ half subtractor. The inputs to half adder/ half subtractor are x and y while z is a control. The outputs are  $y_1$  and  $y_2$ .



- (a) Half adder for  $z = 0$   
 (b) Half subtractor for  $z = 1$   
 (c) Half adder for  $z = 1$  and half subtractor for  $z = 0$   
 (d) Half adder regardless of whether  $z = 0$  or  $z = 1$  due to design defect.

**Statement for question 2 & 3.**

Three multiplexer of size  $2 \times 1$ , are interconnected as shown below:



[MCQ]

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2. The function  $f_1$  and  $f_2$  are
- (a)  $f_1 = (x_1 \oplus x_2)x_3$  and  $f_2 = x_1\bar{x}_2 + x_1\bar{x}_3 + x_2x_3$   
 (b)  $f_1 = x_1 \oplus x_2 \oplus x_3$  and  $f_2 = \bar{x}_1x_2 + \bar{x}_1x_3 + x_2x_3$   
 (c)  $f_1 = \overline{(x_1 \oplus x_2 \oplus x_3)}$  and  $f_2 = x_1x_2 + x_1x_3 + x_2x_3$   
 (d)  $f_1 = x_1(x_2 \oplus x_3)$  and  $f_2 = x_1x_2 + x_1x_3 + \bar{x}_2\bar{x}_3$

[MCQ]

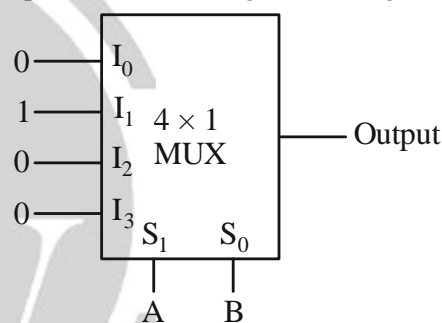
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3. What is this circuit?  
 (a) Full adder (b) Full subtractor  
 (c) Magnitude comparator (d) Priority encoder

[MCQ]

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4. The output of the following circuit diagram represents



- (a) Borrow of half subtractor  
 (b) Carry of Half Adder  
 (c) Sum of half adder  
 (d) None of them

[MCQ]

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5. The design of a combinational logic circuit with three inputs x, y, z and three outputs A, B, C is attempted. The constraint is that designer has only HA, HS, FA and FS units only in his inventory.

When the binary input is 0, 1, 2 or 3 the binary output is same as input and when binary input is 4, 5, 6 or 7 the binary output is 2 less than binary input. What completes the design?

- (a) One FA and one HS  
 (b) One HA and one HS  
 (c) One HA only  
 (d) One FA only



## Answer Key

1. (c)
2. (b)
3. (b)
4. (a)
5. (c)
6. (0.7)

7. (d)
8. (c)
9. (b)
10. (c)
11. (d)
12. (d)



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