CS & IT ENGINEERING

Digital Logic

Combinational Circuits

DPP - 05 Discussion Notes

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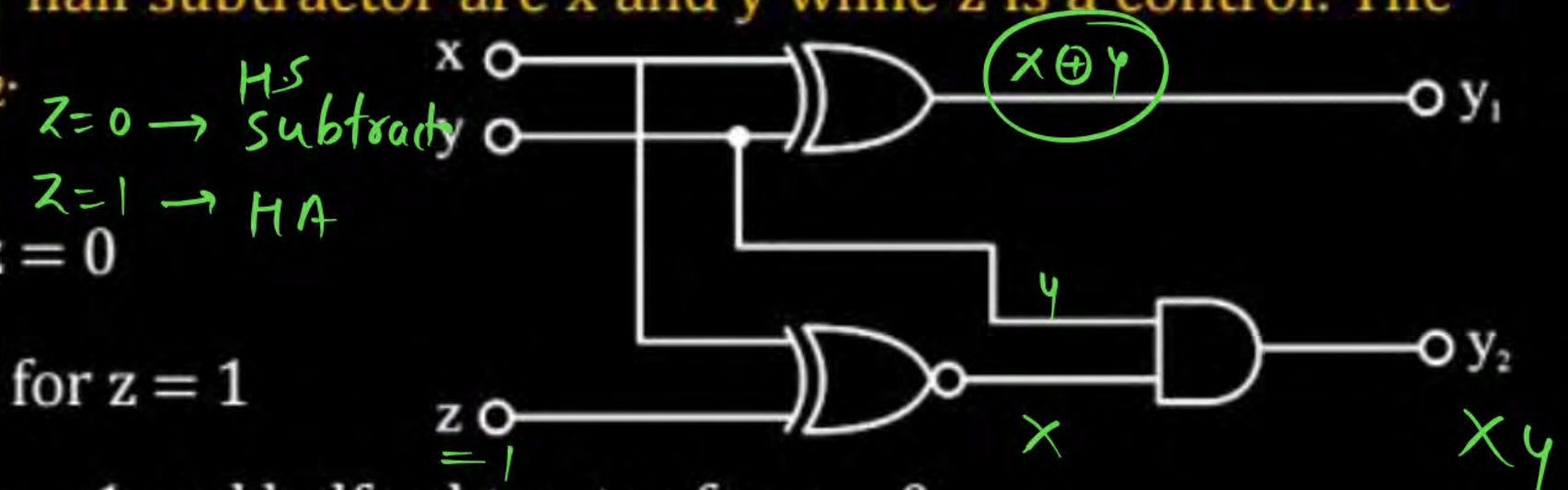
01 Question

02 Discussion

Question **MCQ**

The circuit shown below, is a controlled half adder/ half subtractor. The inputs to half adder/ half subtractor are x and y while z is a control. The outputs are y_1 and y_2.



A Half adder for $z = 0$

B Half subtractor for $z = 1$

C Half adder for $z = 1$ and half subtractor for $z = 0$

D Half adder regardless of whether $z = 0$ or $z = 1$ due to design defect.

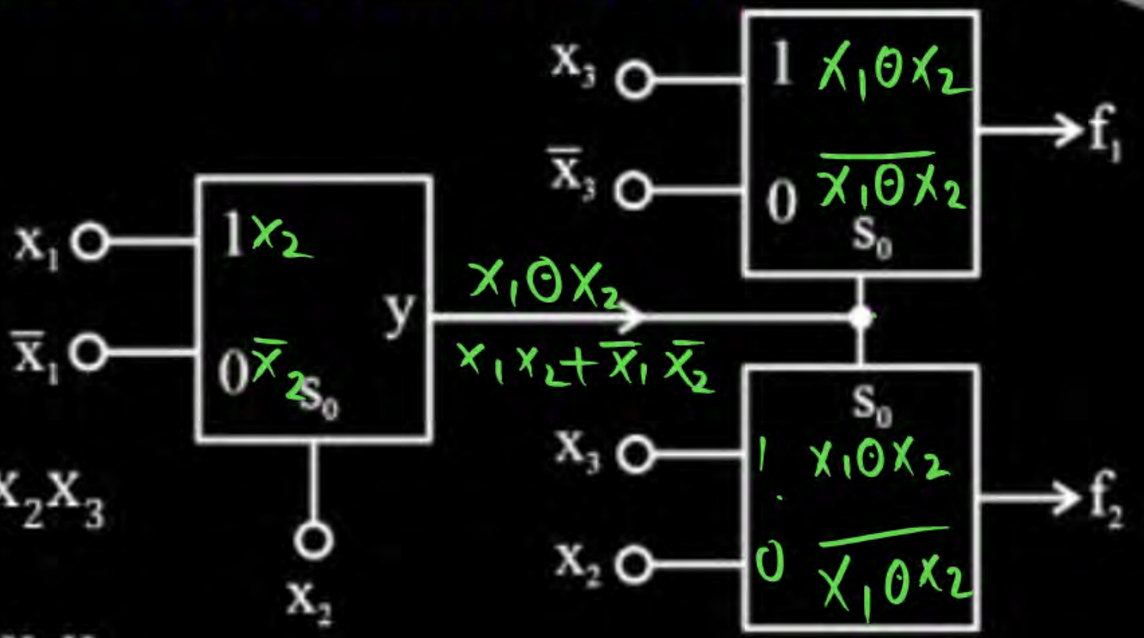
$x \oplus z = 1$ $x \oplus \bar{z} = 0$

$x \oplus 1 = z$ $x \oplus 0 = \bar{z}$

Question MCQ

★★☆

Three multiplexer of size 2×1, are interconnected as shown below:



The function f_1 and f_2 are

$f_1 = x_1 \oplus x_2 \oplus x_3$ → Difference

$f_2 = \bar{x}_1 x_2 + \bar{x}_1 x_3 + x_2 x_3$ → Borrow

A $f_1 = (x_1 \oplus x_2)x_3$ and $f_2 = x_1\bar{x}_2 + x_1\bar{x}_3 + x_2x_3$

B $f_1 = x_1 \oplus x_2 \oplus x_3$ and $f_2 = \overline{x_1}x_2 + \overline{x_1}x_3 + x_2x_3$

C $f_1 = \overline{(x_1 \oplus x_2 \oplus x_3)}$ and $f_2 = x_1x_2 + x_1x_3 + x_2x_3$

D $f_1 = x_1(x_2 \oplus x_3)$ and $f_2 = x_1x_2 + x_1x_3 + \overline{x_2}\,\overline{x_3}$

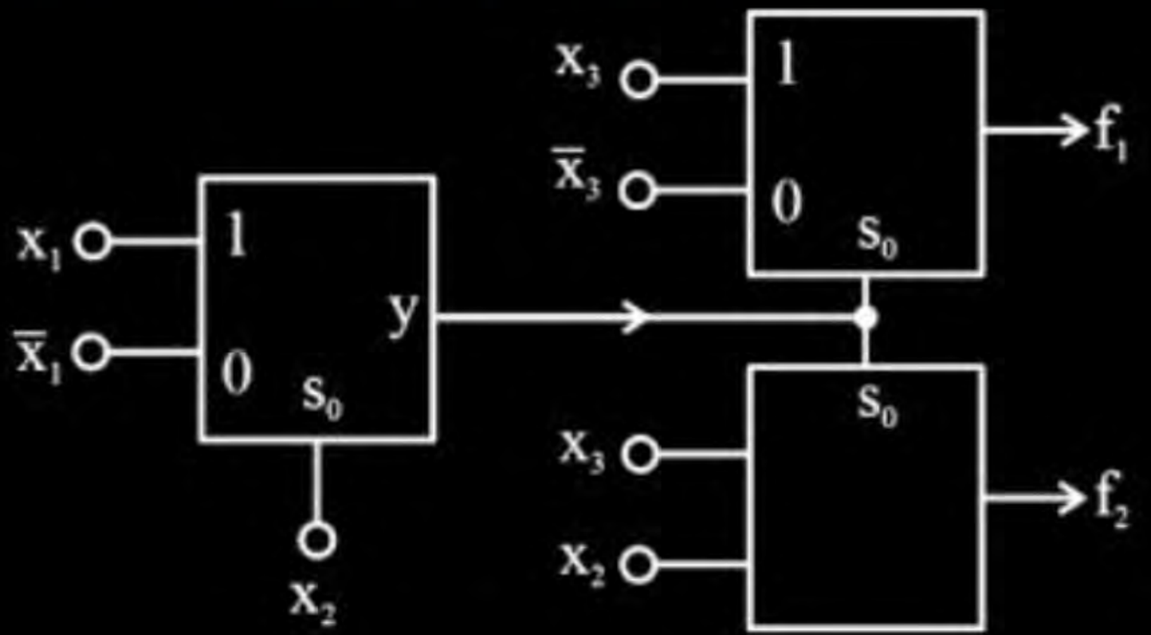
$f_1 = (x_1 \odot x_2)x_3 + \overline{x_1 \odot x_2} \cdot \bar{x}_3$

$= (x_1 \odot x_2) \odot x_3 = x_1 \oplus x_2 \oplus x_3$

Question **MCQ**

Three multiplexer of size 2×1, are interconnected as shown below:

What is this circuit?



A Full adder

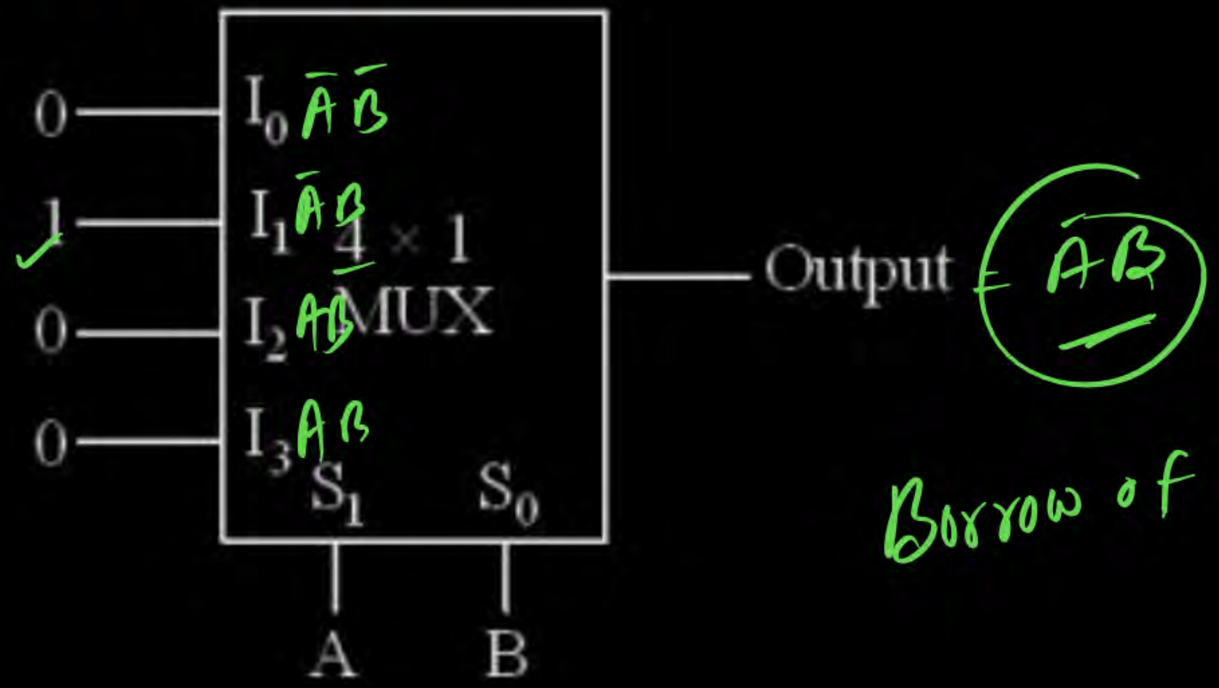
B Full subtractor

C Magnitude comparator

D Priority encoder

Question MCQ

The output of the following circuit diagram represents



Borrow of H.S.

A Borrow of half subtractor

B Carry of Half Adder

C Sum of half adder

D None of them

Question **MCQ**

★★★

The design of a combinational logic circuit with three inputs x, y, z and three outputs A, B, C is attempted. The constraint is that designer has only HA, HS, FA and FS units only in his inventory.
When the binary input is 0, 1, 2 or 3 the binary output is same as input and when binary input is 4, 5, 6 or 7 the binary output is 2 less than binary input. What completes the design?

A One FA and one HS

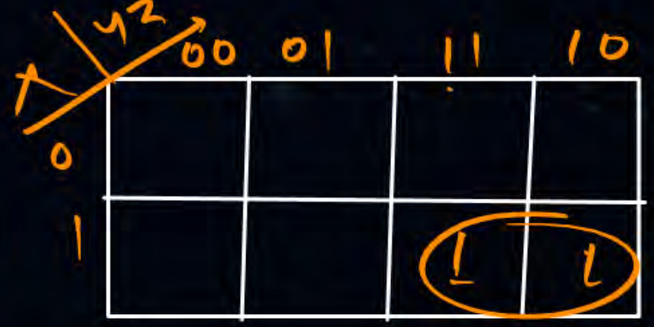
B One HA and one HS

C One HA only

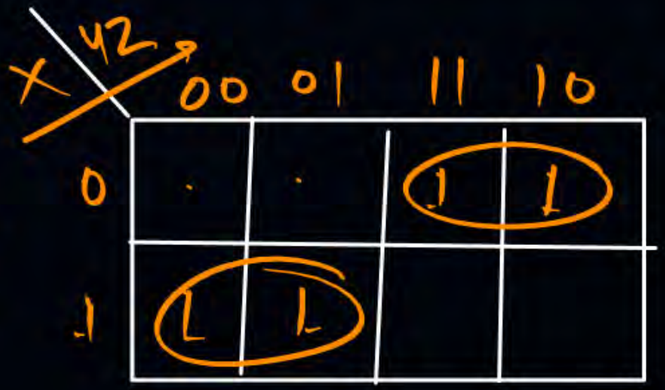
D One FA only

X	Y	Z	A	B	C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	1	0	1

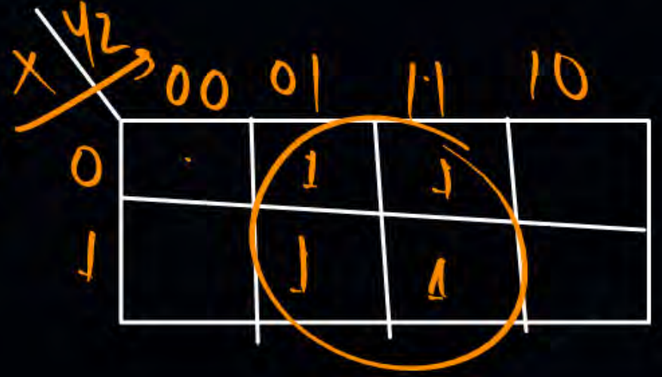
(A)



(B)



(C)



$A = XY$

(HA)

$B = \bar{X}Y + X\bar{Y} = X \oplus Y$

$C = Z$

Question NAT

A serial adder is operating with a clock frequency of 10 MHz. The time required to sum 1011011 and 10110 is 0.7 (in μsec)

$n = 7$

$$T = n \cdot T_{clk}$$

$$= 7 \times \frac{1}{f_{clk}}$$

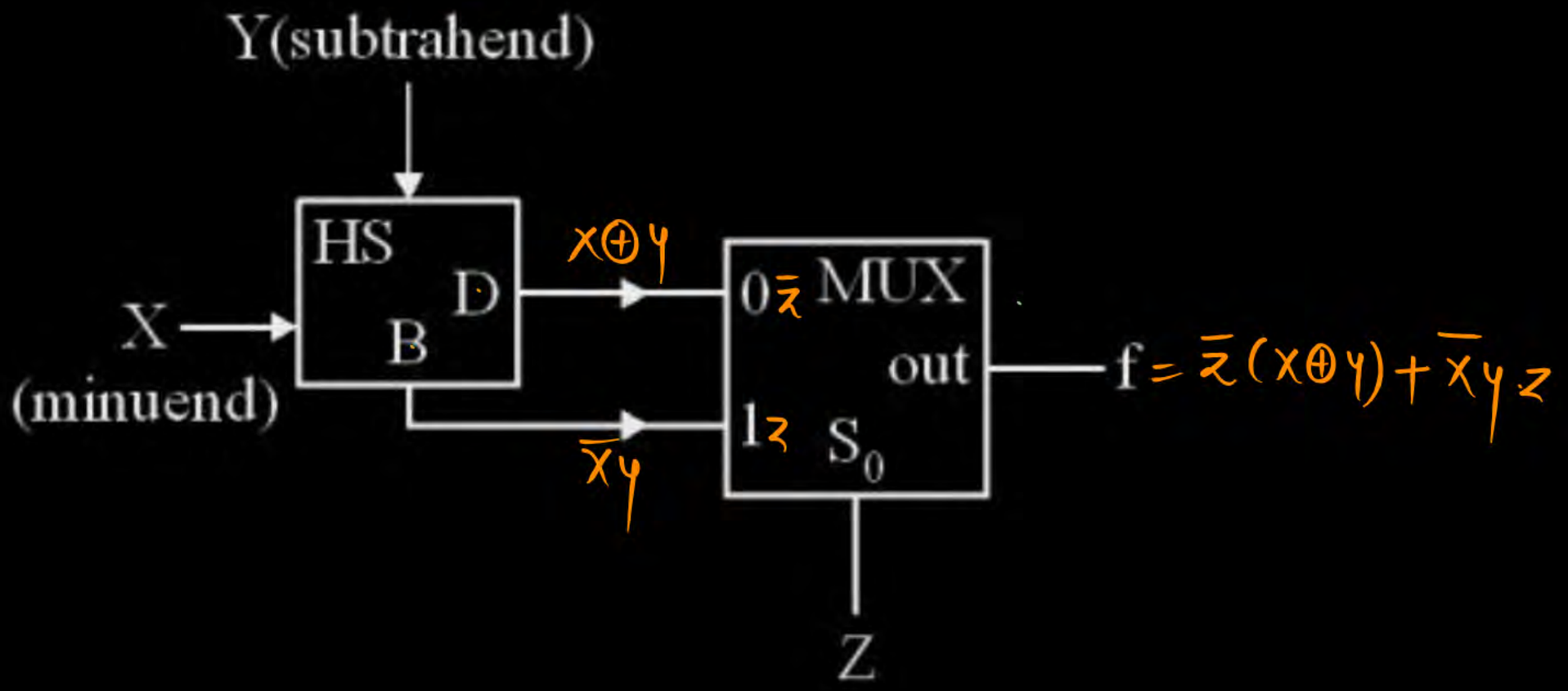
$$= 7 \times \frac{1}{10 \times 10^6}$$

$$= 0.7 \times 10^{-6} \text{ sec}$$

$$= 0.7 \mu s$$

Question **MCQ**

A half subtractor (HS) and 2 × 1 MUX are inter-connected as demonstrated below. What is NOT correct about this circuit?



Continue...

$f = (x \oplus y)\bar{z} + \bar{x}yz$ $f = x \oplus y$ $f = 1$ $x = \bar{y}$

A For Z = 0, f = 1 indicates that the minuend and the subtrahend bits are different. ✓

B For Z = 0, f = 0 indicates that minuend and subtrahend bits are same, that is, X = Y = 0 or X = Y = 1.

$f = (x \oplus y)\bar{z} + \bar{x}yz$

$f = x \oplus y$ $f = 0$ $x = y$

C For Z = 1, f = 1 indicates that X < Y.

$f = (x \oplus y)\bar{z} + \bar{x}yz = \bar{x}y \quad (x < y)$

D For Z = 1, f = 0 indicates that subtrahend bit is definitely 0.

X

$f = \bar{x}y$

Question MCQ

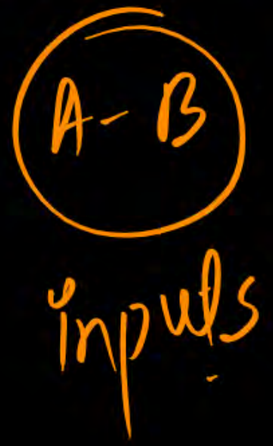
What does minuend and subtrahend denotes in a subtractor?

A Their corresponding bits of input

B Its output

C Its input

D Borrow bits



Question MCQ

What is the expression for difference, borrow of full subtractor circuit

A $\text{Diff} = A \oplus B \oplus C, \quad \text{Borrow} = \bar{A}C + (A \odot B)C$

B $\text{Diff} = A \oplus B \oplus C, \quad \text{Borrow} = \bar{A}B + \overline{(A \oplus B)} \cdot C$

C $\text{Diff} = A \odot B \odot C, \quad \text{Borrow} = \bar{A}B + \overline{(A \odot B)}\,C$

D $\text{Diff} = A \odot B \odot C, \quad \text{Borrow} = \bar{A}C + (A \odot B)C$

$D = A \oplus B \oplus C$

$B = \Sigma m(1,2,3,7)$

$= \bar{A}B + \overline{(A \oplus B)}\,C$

$= \bar{A}B + \bar{A}C + BC$

Question MCQ

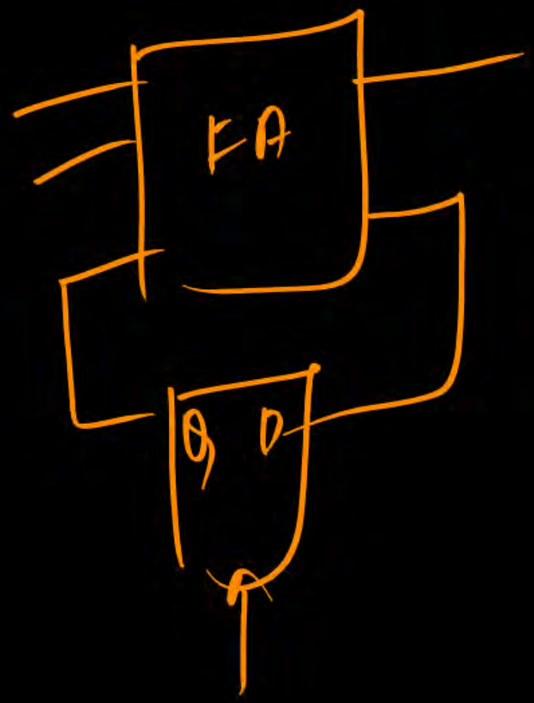
A D flip-flop is used in a 4-bit serial adder, why?

A It is used to invert the input of the full adder

B It is used to store the output of the full adder

C It is used to store the carry output of the full adder

D It is used to store the sum output of the full adder



Question MCQ

The circuit shown in the given figure represents a/an:

A decoder

B equality detector

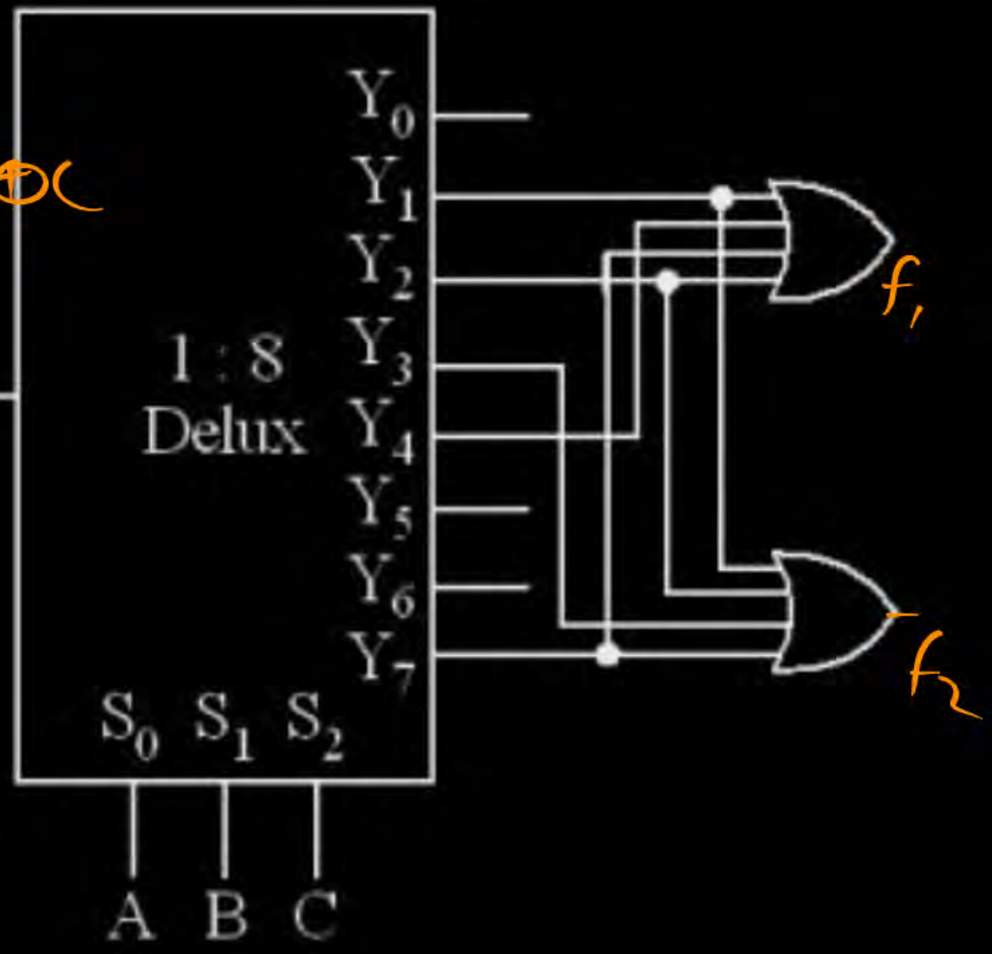
C full adder

D full subtractor

$f_1 = \Sigma m(1,2,4,7) = A \oplus B \oplus C$

$f_2 = \Sigma m(1,2,3,7)$

↳ Borrows



Question **MCQ**

Consider the following circuit diagram

A 4-bit subtractor, four 4-bit three-state buffers (with bus input and output), and one inverter is used to subtract two numbers (Y - X),

X = 0101 and Y = 0010

If A = 0, then D and B_{out} are respectively

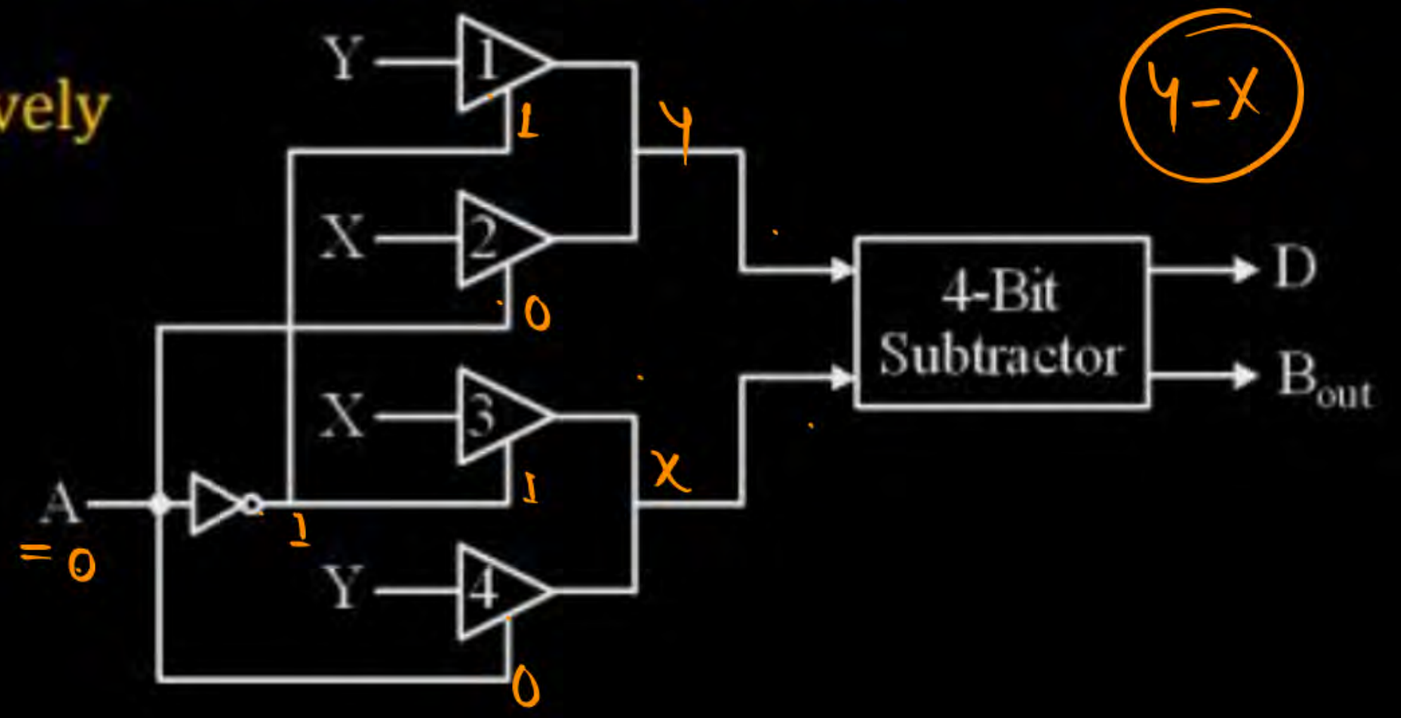
Diff Y − X

= 0010

0101

1101

(1) Borr



Y − X

- A 0011 and 0
- B 1101 and 0
- C 0011 and 1
- D 1101 and 1

Thank you

GW

Soldiers !