

CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

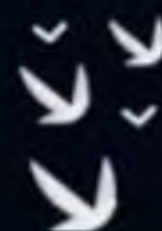
Cache Organization

Lecture No.- 03

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Recap of Previous Lecture



Topic

Cache Memory

Topic

Average Memory Access Time



Topics to be Covered



Topic

Cache Write

Topic

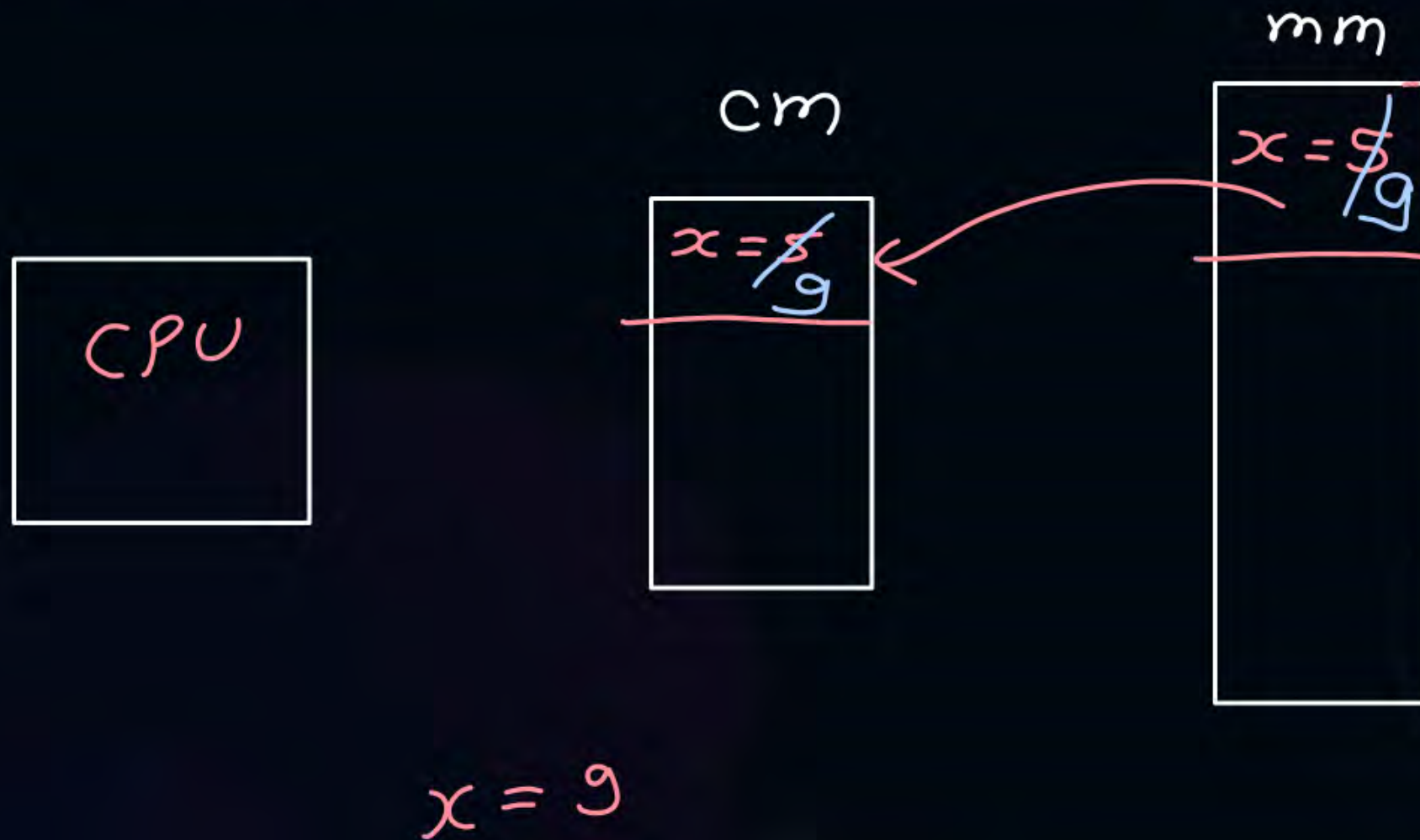
Write Through & Write Back Cache

Topic

Write Allocate vs No Write Allocate



Topic : Cache Write or Write Propagation





Topic : Cache Write or Write Propagation

1. Write Through
2. Write Back



Topic : Write Through



write in cm and mm are done simultaneously.

Advantage :-

→ consistency for values in cm & mm.

Disadvantage :-

→ Time consuming because irrespective of hit or miss in cache, for write operation mm is accessed.



Topic : Write Back

write operation performed in cm only and the cache block is written back to mm only when it is replaced.

Adv:-

→ Time saving as compared to write through

Disadv:-

→ Inconsistency for values in cm & mm.

write through:-

cm

i=1

2 3 4 5 6 7 8 9 10 11

mm

i=1

2 3 4 5 6 7 8 9 10 11

write back:-

cm

i=1

2 3 4 5 6 7 8 9 10

mm

i=10

for(i=1; i<10; i++)

{

|||

}



Topic : Write Allocate vs No Write Allocate



Write Allocate: \Rightarrow Used with write back

The block is loaded on a write miss.

No Write Allocate: \Rightarrow Used with write through

The block is modified in the main memory and not loaded into the cache.

write through with no write allocate

Read

write

Hit in cache

CPU reads
required
content from
Cache

miss in cache

CPU reads req.
content from mm
and the missed block
is copied from mm to
Cache.

If a block is replaced
from cache then no
need to write it back
in mm.

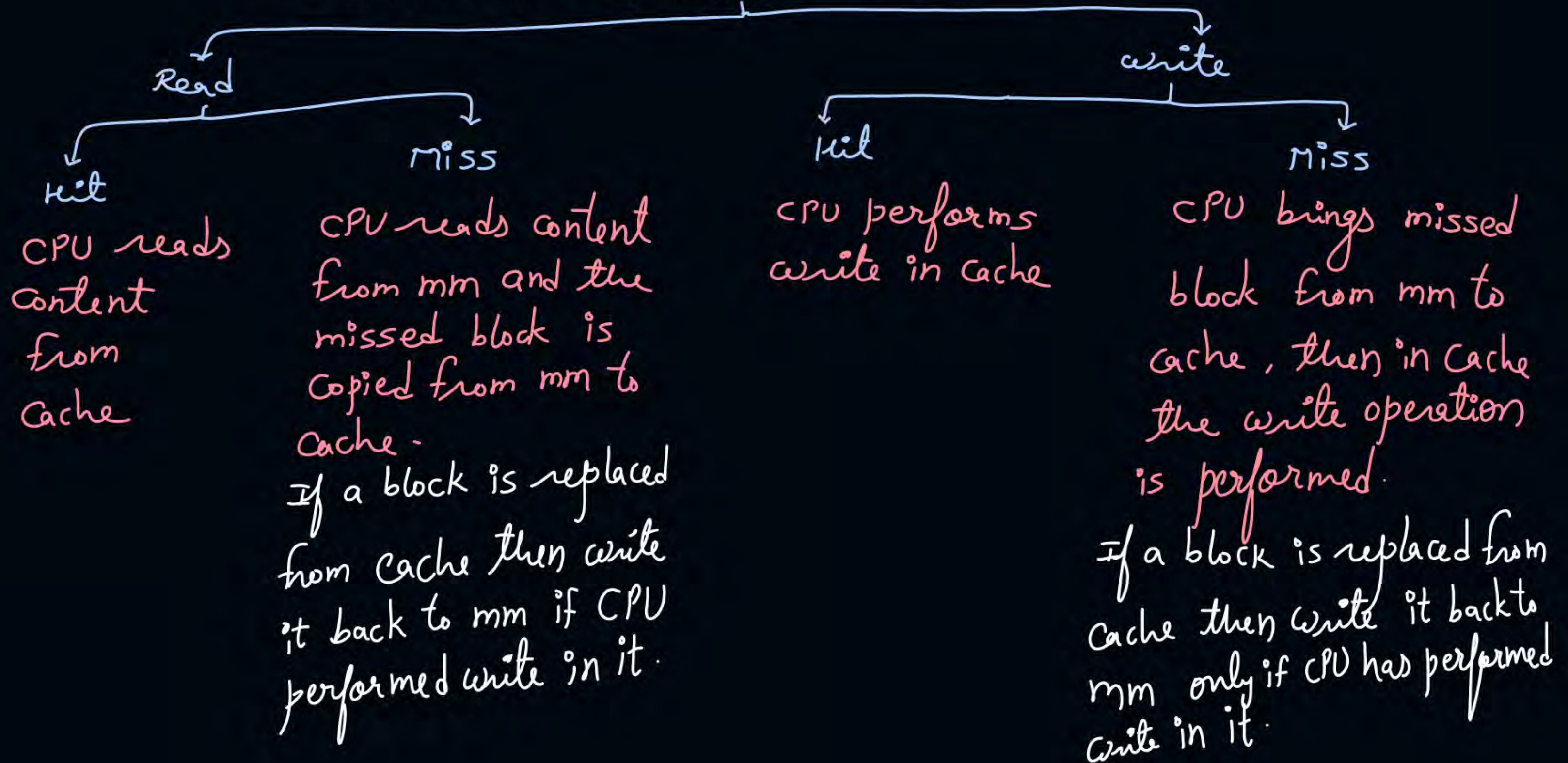
Hit

CPU performs
write in cache
and mm
simultaneously

Miss

CPU performs write
in mm and do not
bring missed block
in cache

write back with write allocate





Topic : T_{avg} in Write Through Cache \rightarrow (simultaneous access)

$$T_{avg \text{ read}} = H * t_{cm} + (1-H) (t_{mm})$$

$$T_{avg \text{ write}} = t_{mm} \quad \text{actually } \max(t_{cm}, t_{mm})$$

$$T_{avg} = \text{fraction of read operations} * T_{avg \text{ read}} + \text{fraction of write operations} * T_{avg \text{ write}}$$

Effective hit rate
of write through cache = Fraction of
read operations * hit rate



when CPU accesses
only cache

[MCQ]

$$t_{cm} = 100 \text{ ns} \quad t_{mm} = 1000 \text{ ns}$$
$$H = 90\%$$



#Q. A system has a write through cache with access time of 100ns and hit ratio of 90%. The main memory access time is 1000ns. The 70% of memory references are for read operations.

1. Average memory access time for read operations only $= 0.90 * 100 + 0.1 * 1000$
 $= 190 \text{ ns}$
2. Average memory access time for write operations only $= 1000 \text{ ns}$
3. Average memory access time for read-write operations both
 $\hookrightarrow = 0.7 * 190 + 0.3 * 1000$
 $= 433 \text{ ns}$
4. Effective Hit ratio
 $= 0.7 * 0.9 = 0.63$

#Q. Size of data sent to main memory from CPU:

1. For write hit, when a write through cache is used? \Rightarrow 1 data size
2. For write miss, when a write through cache is used? \Rightarrow 1 data size
3. For write hit, when a write back cache is used? \Rightarrow Nothing
4. For write miss, when a write back cache is used? \Rightarrow Nothing

[MCQ]



#Q. Size of data sent from main memory to cache:

only when missed block
Copied from mm to cache

1.

For write hit, when a write through cache is used?

↖ No write allocate

2.

For write miss, when a write through cache is used?

3.

For write hit, when a write back cache is used?

↖ write allocate

4.

For write miss, when a write back cache is used?

⇒ 1 block

} nothing

⇒ nothing

Tavg for write back:- (hierarchical access)

$$T_{avg \text{ read or write}} = H * t_{cm} + (1-H)(t_{cm} + t_{bt} + \text{write back time})$$

$$\text{write back time} = d * t_{bt}$$

d = fraction of modified or dirty blocks replaced from cache.

$$\text{Ans} = 3.6625 \text{ ns}$$

#Q. The memory access time is 2 nanosecond for a read operation with a hit in cache, 10 nanoseconds for a read operation with a miss in cache, 4 nanoseconds for a write operation with a hit in cache and 15 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 memory read operations and 60 memory write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is?

	Read	write
Hit	2	4
miss	10	15

$$T_{\text{avg read}} = 0.9 * 2 + 0.1 * 10 = 2.8 \text{ ns}$$

$$T_{\text{avg write}} = 0.9 * 4 + 0.1 * 15 = 5.1 \text{ ns}$$

$$\text{fraction of read} = \frac{100}{160} = 0.625$$

$$\text{fraction of write} = \frac{60}{160} = 0.375$$

$$\begin{aligned} T_{avg} &= (0.625 * 2.8) + (0.375 * 5.1) \\ &= 3.6625 \text{ ns} \end{aligned}$$

#Q. The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations; 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is?

#Q. Assume a miss rate of 2% for the instruction cache and of 4% for the data cache, a miss penalty of 100 cycles for all misses, and a frequency of 36% of loads and stores. If the CPI is 2 without memory stalls, determine how much faster the processor runs with a perfect cache that never misses.



2 mins Summary



Topic

Cache Write

Topic

Write Through & Write Back Cache

Topic

Write Allocate vs No Write Allocate



Happy Learning

THANK - YOU