CS & IT ENGINEERING

Digital Logic
Combinational circuit

DPP Solution 06

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01 Questions

02 Discussion

Q.1

A 4-bit parallel binary adder is built using four full adders. If each full adder takes 44 ns to produce the sum bit and 14 ns to produce carry bit, then the time required for addition of two 4-bit number is

A. 100 ns

B. 86 ns

C. 146 ns

D. 190 ns

$T = (n-1)T_{carry} + Max\{T_{sum}, T_{carry}\}$

$= 3 \times 14 + 44$

$= 86\,ns$

Q.2 A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using four full adders. The total propagation time of this 4-bit binary adder in microseconds is _____.

$T = (n-1)\{T_{AND} + T_{OR}\} + T_{SUM}$ → $2T_{XOR}$

$= 3 \times \{1.2 + 1.2\} + 4.8\ \mu s$

$= 3 \times 1.2\ \mu s + 4.8\ \mu s$

$= 7.2 + 4.8\ \mu s$

$= 12\ \mu s$

A. 19.2

B. 20

C. 12

D. 45

Q.3

Figure I show a 4-bits ripple carry adder realized using full adders and figure II shows the circuit of a full-adder (FA). The propagation delay of the XOR, AND and OR gates in Figure II are 20 ns, 15 ns and 10 ns respectively. Assume all the inputs to the 4-bit adder are initially reset to 0.

At t = 0, the inputs to the 4-bit adder are changed to $X_3X_2X_1X_0$ = 1100, $Y_3Y_2Y_1Y_0$ = 0100 and $Z_0 = 1$

The output of the ripple carry adder will be stable at t (in ns) = 50 ns

_____.

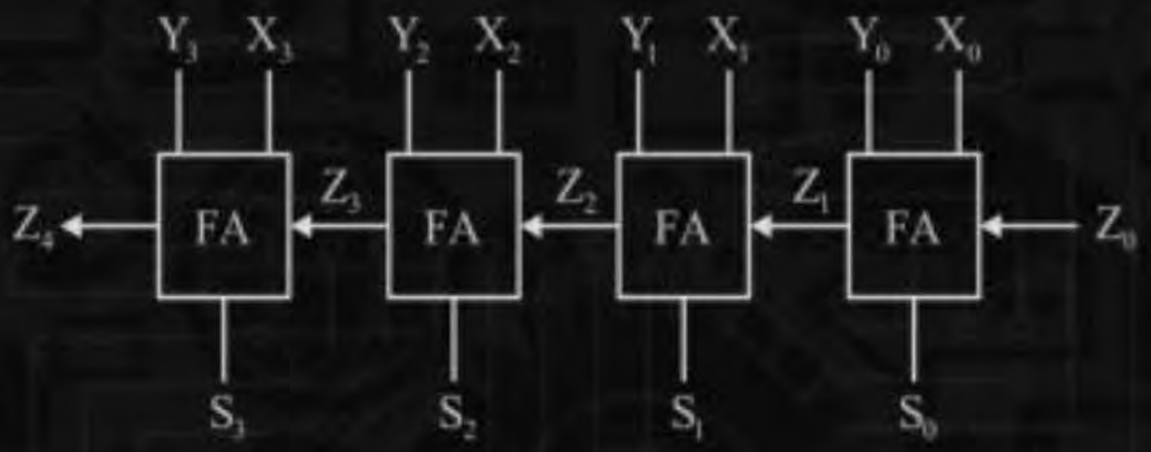


Figure-I

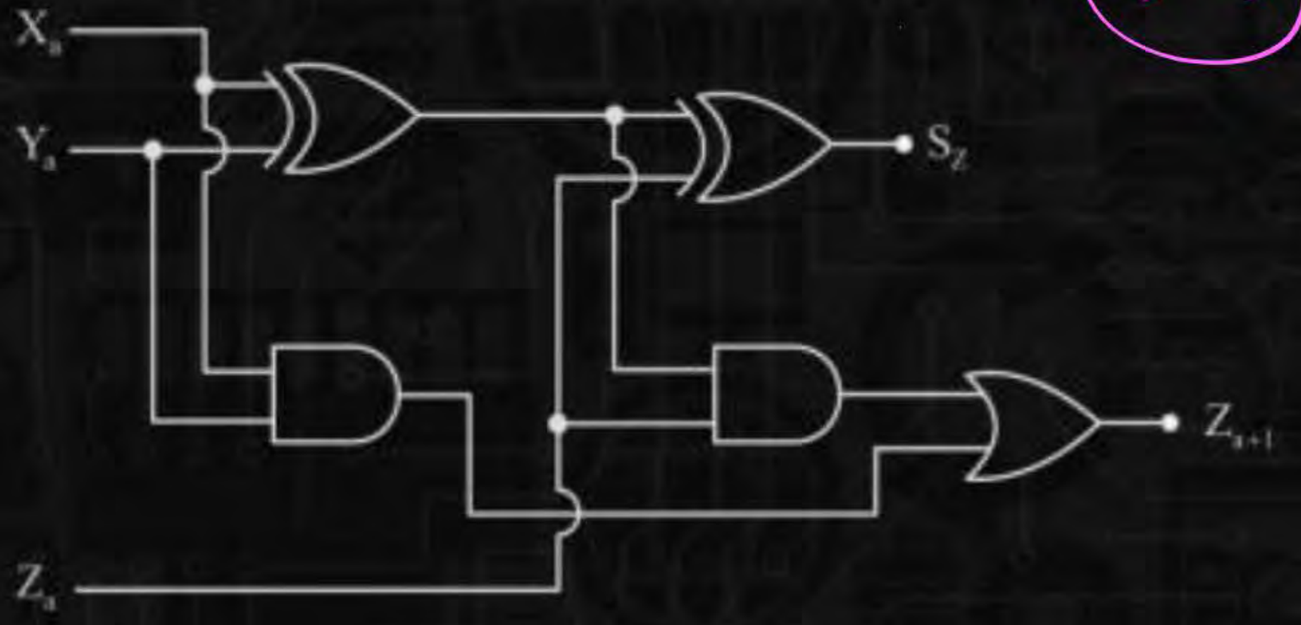
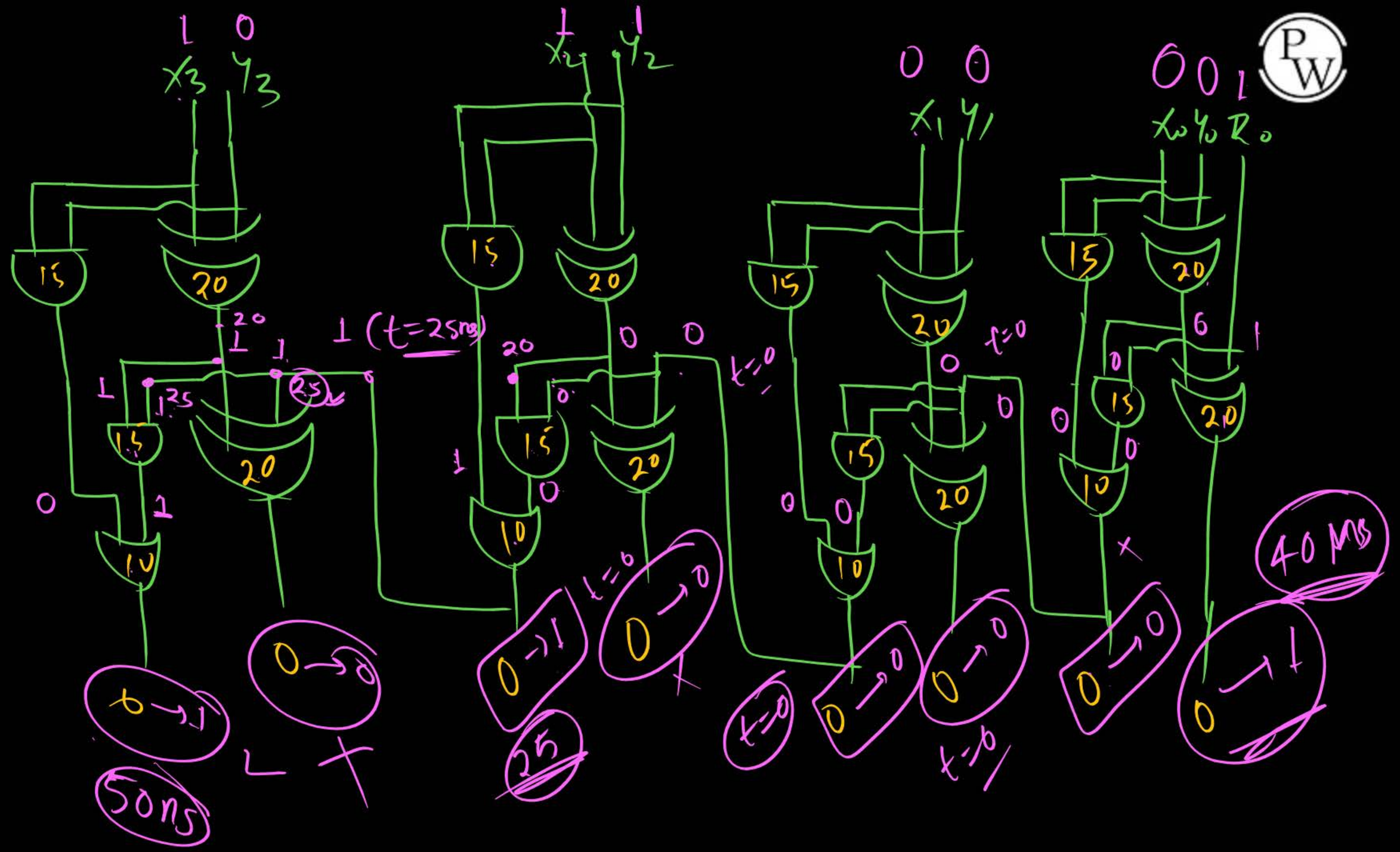


Figure-II



1 0
x_3 y_3
1 1
x_2 y_2
0 0
x_1 y_1
0 0 1
x_0 y_0 R_0
15
20
10
1 (t=25ns)
t=0
0→1
0→0
25
50ns
40 ms

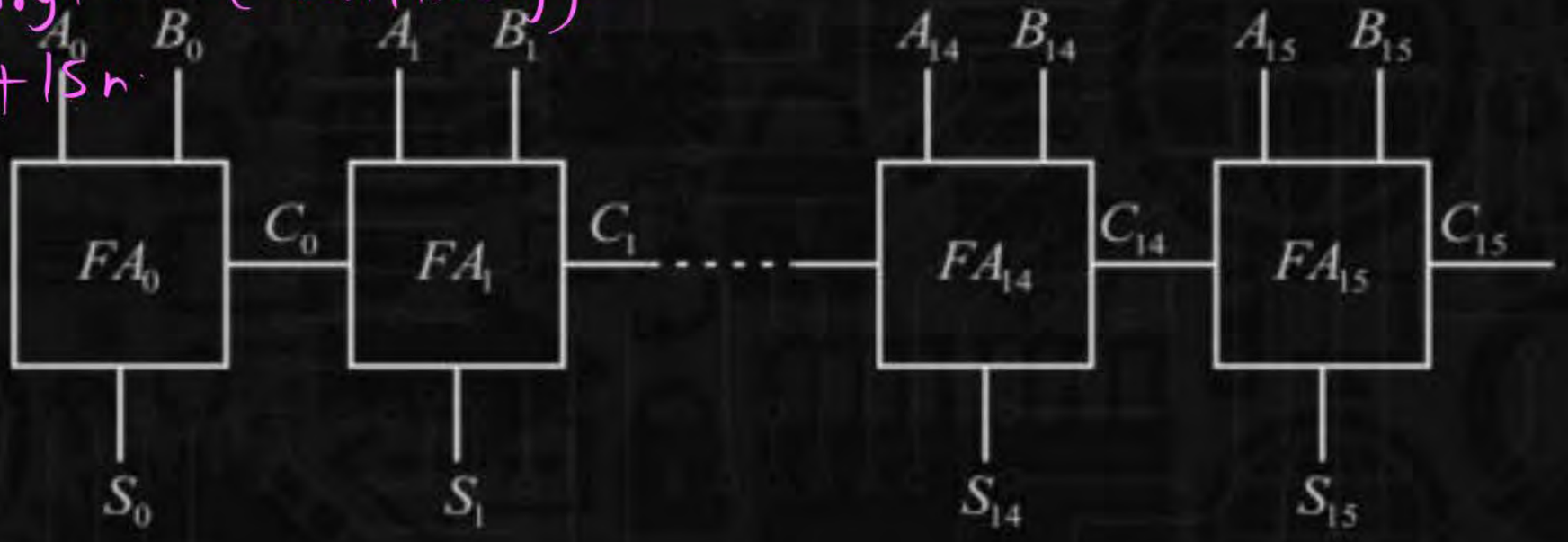
Q.4

A 16 bit ripple carry adder is realized using 16 identical full adders (FA) as shown in the figure. The carry-propagation delay of each FA is 12 ns and the sum-propagation delay of each FA is 15 ns. The worst case delay (in ns) of this 16-bit adder will be____.

$T = (n-1)T_{carry} + Max\{T_{sum}, T_{carry}\}$

$= 15 \times 12ns + 15ns$

$= 195ns$



Q.5 Eight 1-bit full adders arc cascaded. Each 1-bit full adder generates carry out bit in 10ns and sum bit in 30 ns. The number of addition performed per second, will be

A. 10^9

B. 0.5×10^7

C. 10^7

D. 0.125×10^7

$T_{sum} = 30ns$

$T_{carry} = 10ns$

$T = (n-1) T_{carry} + Max\{T_{sum}, T_{carry}\}$

$= 7 \times 10 + 30ns$

$= 100ns$

$\frac{1}{T} = \frac{10^9}{100}$ $\quad \frac{1}{s} = \frac{1000 \times 10^6}{100} = 10^7$

Q.6

A 16-bit parallel adder is designed using 16, 1-bit full adders. Each 1-bit full adder is designed using X-OR, AND and OR gates. The delay contributed by X-OR gate is 20ns while that contributed by AND/OR gate is 10ns. The number of additions per second that a 16-bit parallel adder can perform reliability, will be

A. 2.94×10^6

B. 3.125×10^6

C. 3.33×10^6

D. 4×10^6

$T = (n-1)\{T_{AND} + T_{OR}\}p + 2T_{XOR}$

$T = 15 \times \{20ns) + 40ns$

$T = 300ns + 40ns$

$T = 340ns$

$\frac{1}{T} = \frac{10^9}{340}$

$= \frac{1000 \times 10^6}{340}$

$= 2.96 \times 10^6$

Q.7 How many half adder and OR gate are needed to construct 4-bit parallel adder ?

A. 8 HA, 4 OR gate

B. 7 HA, 4 OR gate

C. 7 HA, 3 OR gate

D. 8 HA, 3 OR gate

$(2n-1)$ HA + $(n-1)$ OR

$(2\times4-1)$ HA + $(4-1)$ OR

7 HA + 3 OR

THANK YOU GW
SOLDIERS !