CS & IT ENGINEERING

Digital Logic

Sequential Circuit

DPP 04 Discussion

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01 Questions

02 Discussion

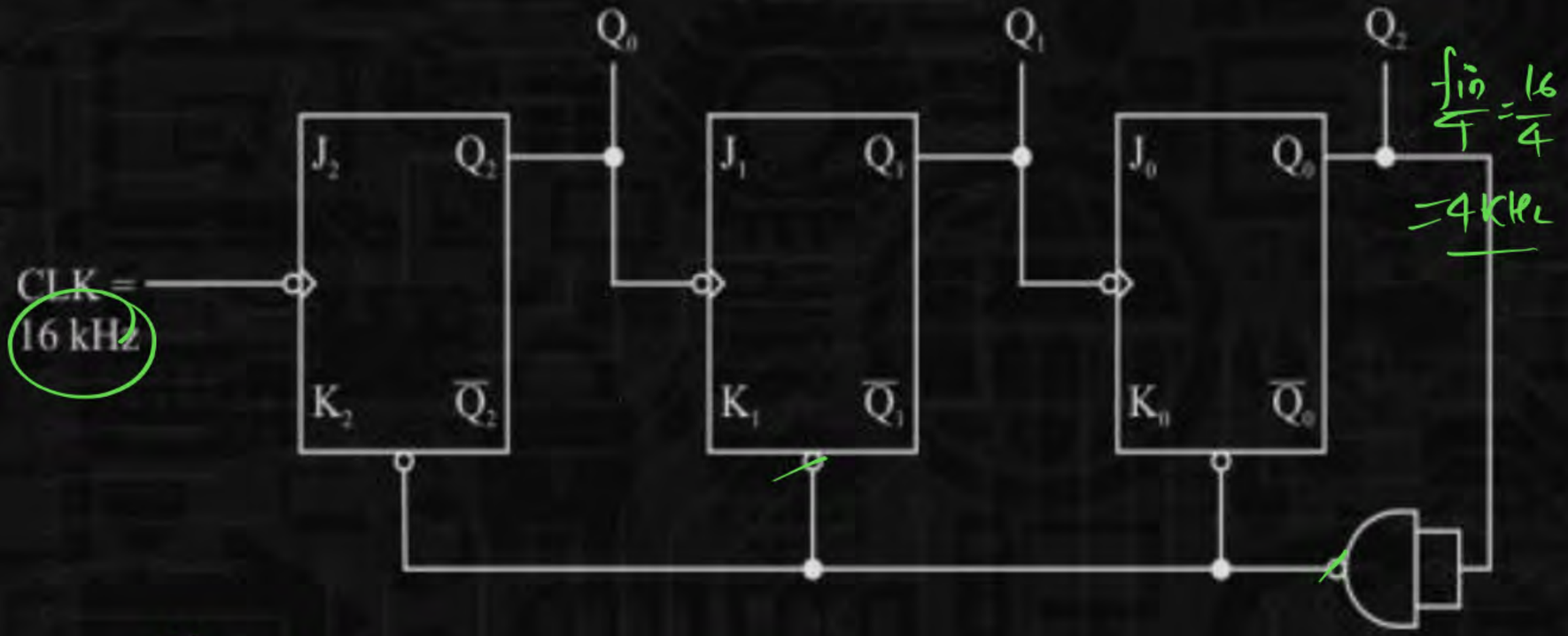
Q.1 What is the output signal frequency of the following counter if the clock signal frequency is 16 kHz? All 'J' and 'K' inputs are connected to 1.

A. 4 kHz

B. 8 kHz

C. 10 kHz

D. 16 kHz



$\frac{f_{in}}{4} = \frac{16}{4}$

$= 4\,kHz$

$Clr = Q_2 \bar{Q}_1 \bar{Q}_0$

$1\ 0\ 0 \rightarrow (4)$

MOD = 4

Q.2

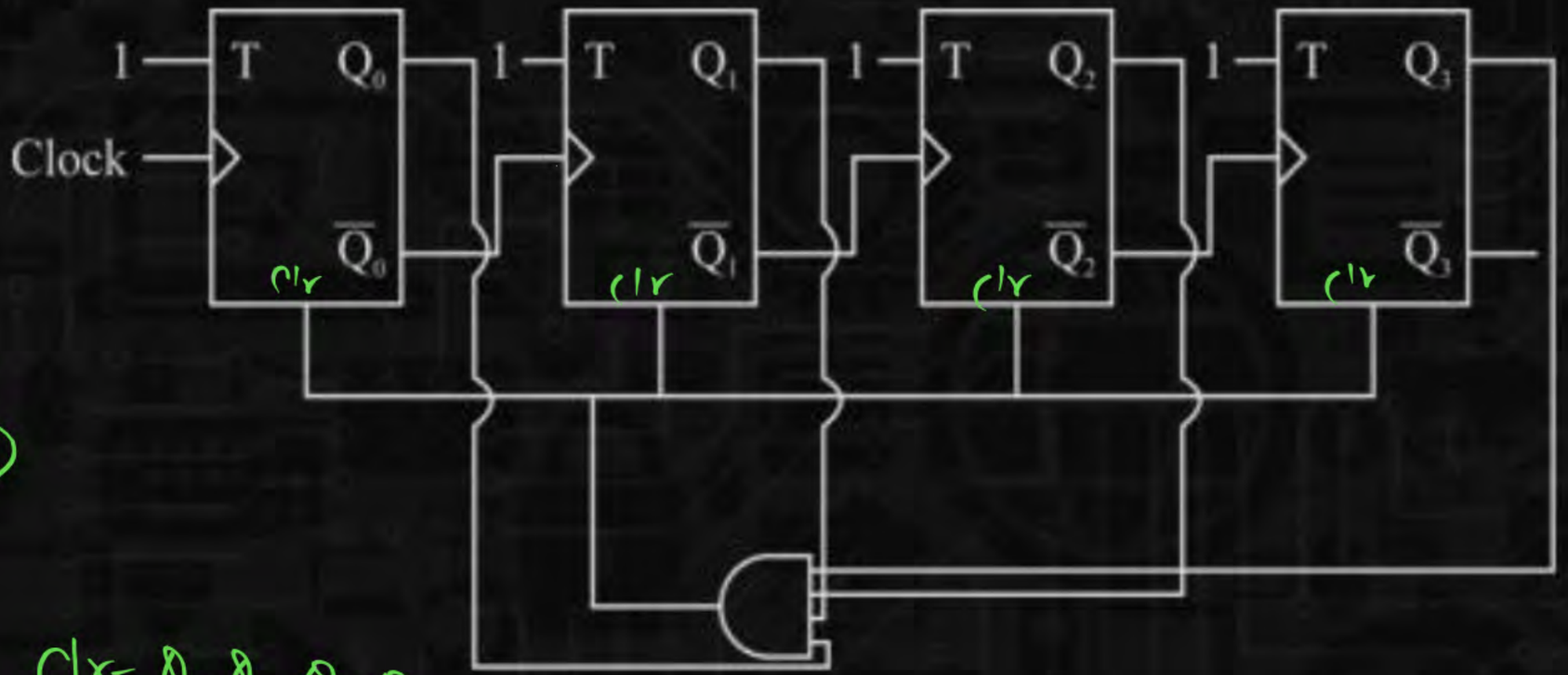
The circuit is counter of mod

A. Mod-0

B. Mod-16

C. Mod-15

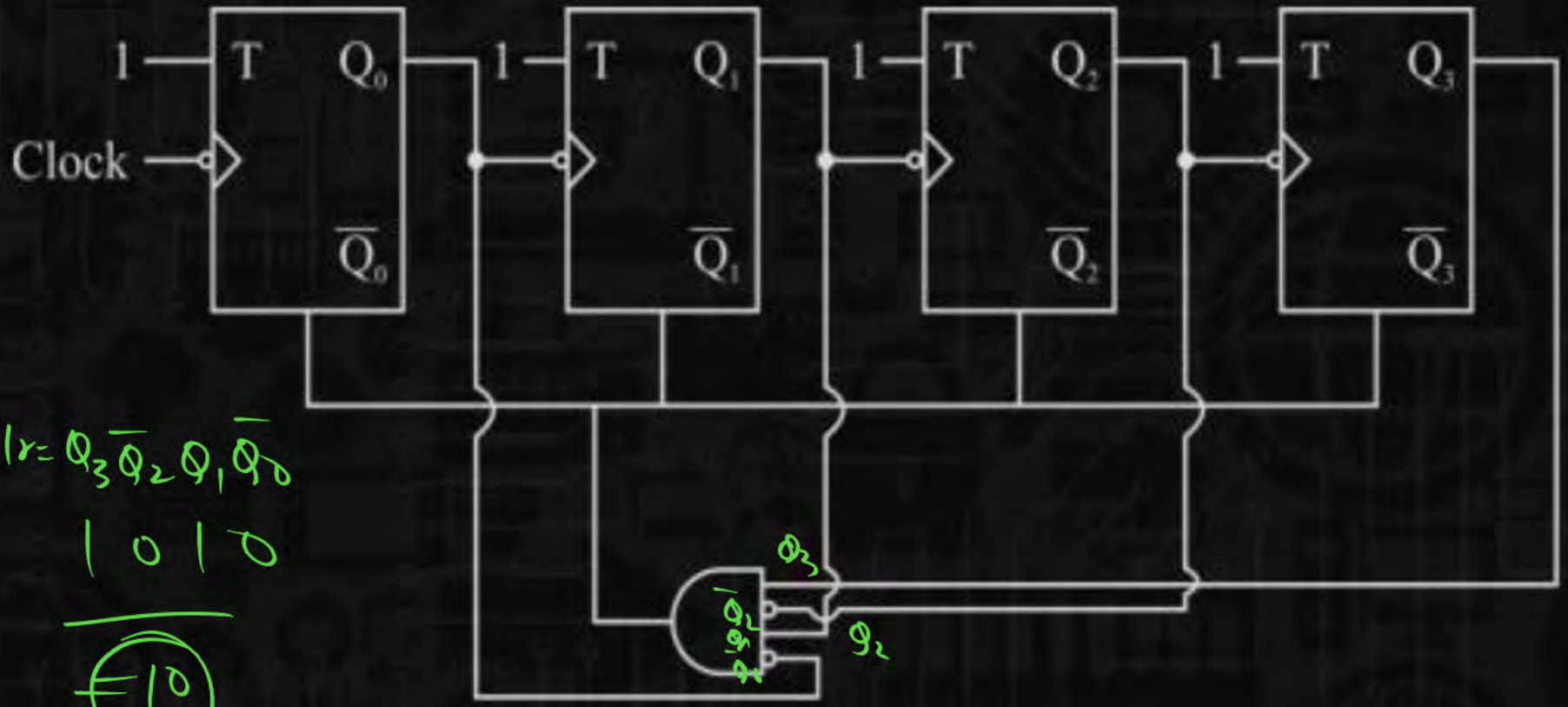
D. Mod-14



clr = $Q_3 Q_2 Q_1 Q_0$

1 1 1 1 = 15

Q.3 The circuit is a counter of mod 10



$clr = Q_3\overline{Q}_2Q_1\overline{Q}_0$

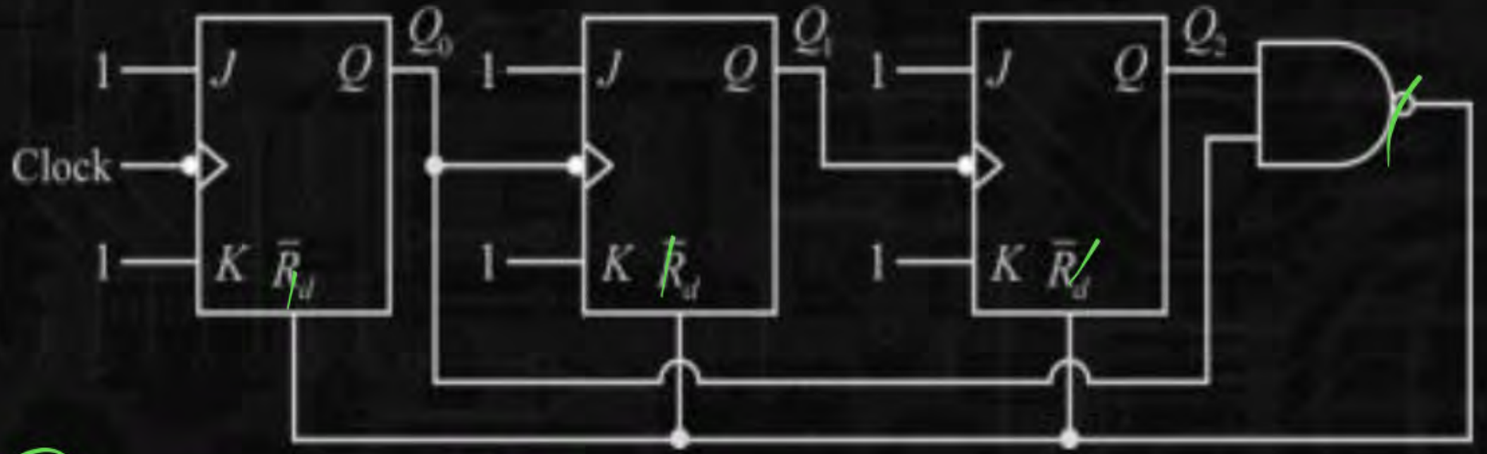
1 0 1 0

10

MOD = 10

Q.4

The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset ($\bar{R}_d$ input). The counter corresponding to this circuit is



A. a modulo-5 binary up counter.

B. a modulo-6 binary down counter.

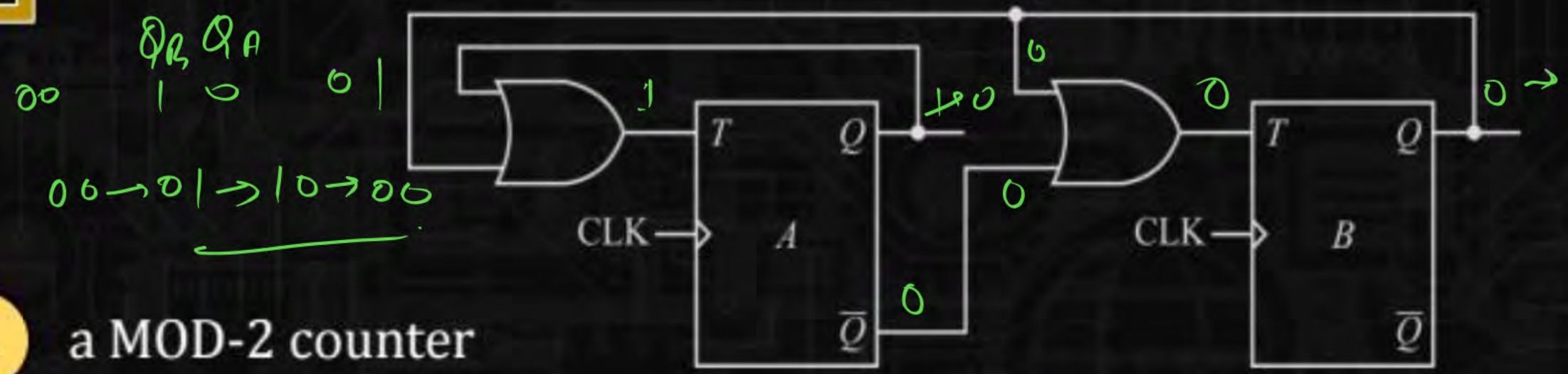
C. a modulo-5 binary down counter.

D. a modulo-6 binary up counter.

$(1)_2 = Q_2\bar{Q}_1Q_0$

$|0|_2 = (5)_{10}$

Q.5 The circuit shown in figure is



A. a MOD-2 counter

B. a MOD-3 counter

C. generate sequence 00, 10, 01, 00.....

D. generate sequence 00, 10, 00, 10, 00

CLK	Q_A	Q_B
0	0	0
1	0	1
2	1	0
3	0	0


THANK YOU GW
SOLDIERS !