Memory Management Practice Questions

Linking, Loading and Memory Allocation

1) Consider the block sizes and the process sizes as given in the table below. Perform the memory allocation using First Fit algorithm.

Block Size (KB)	Process Size(KB)
B1: 28	P1: 46
B2: 98	P2: 89
B3: 78	P3: 27
B4: 25	P4: 76
B5: 47	P5: 25

2) Consider the block sizes and the process sizes as given in the table below. Perform the memory allocation using First Fit algorithm.

Block Size (KB)	Process Size(KB)
B1: 287	P1: 461
B2: 982	P2: 891
B3: 780	P3: 279
B4: 255	P4: 763
B5: 479	P5: 259

Because blocks are of fixed size we cannot another process into these blocks because of internal fragmentation.

3) Consider the block sizes and the process sizes as given in the table below. Perform the memory allocation using Best Fit algorithm.

Block Size (KB)	Process Size(KB)
B1: 28	P1: 46
B2: 98	P2: 89
B3: 78	P3: 27
B4: 25	P4: 76
B5: 47	P5: 25

4) Consider the block sizes and the process sizes as given in the table below. Perform the memory allocation using Best Fit algorithm.

Block Size (KB)	Process Size(KB)
B1: 287	P1: 461
B2: 982	P2: 891
B3: 780	P3: 279
B4: 255	P4: 763
B5: 479	P5: 259

5) Consider the block sizes and the process sizes as given in the table below. Perform the memory allocation using Worst Fit algorithm.

Block Size (KB)	Process Size(KB)
B1: 28	P1: 46
B2: 98	P2: 89
B3: 78	P3: 27
B4: 25	P4: 76
B5: 47	

6) Consider the block sizes and the process sizes as given in the table below. Perform the memory allocation using Worst Fit algorithm.

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B1: 287	P1: 461
B2: 982	P2: 891
B3: 780	P3: 279
B4: 255	P4: 763
B5: 479	

7) Consider the following fixed partition memory information of a certain system with four processes. Block sizes{B1,B2,B3,B4} ={200,30,700,50} and process sizes{P1,P2,P3,P4} = {20,200,500,50}. Using the first fit memory allocation, calculate the total internal fragmentation.
A) 710
B) 680
C) 700
D) 690

8) Consider the following fixed partition memory information of a certain system with four processes. Block sizes{B1,B2,B3,B4} ={200,30,700,50} and process sizes{P1,P2,P3,P4} = {20,200,500,50}. Using the best fit memory allocation, calculate the total internal fragmentation.
A) 210
B) 180
C) 200
D) 190

9) Consider the following fixed partition memory information of a certain system with four processes. Block sizes{B1,B2,B3,B4} ={200,30,700,50} and process sizes{P1,P2,P3,P4} = {20,200,500,50}. Using the worst fit memory allocation, calculate the total internal fragmentation.
A) 710
B) 680
C) 700
D) 690

10) Consider the following fixed partition memory information of a certain system with four processes. Block sizes{B1,B2,B3} ={5,10,20} and process sizes{P1,P2,P3,P4} = {10,20,30}. Using the next fit memory allocation, find the block that remains unallocated.
A) B1
B) B2
C) B3
D) All blocks are allocated.

11) Which of the following are the advantages of dynamic linked libraries? **[MSQ]**

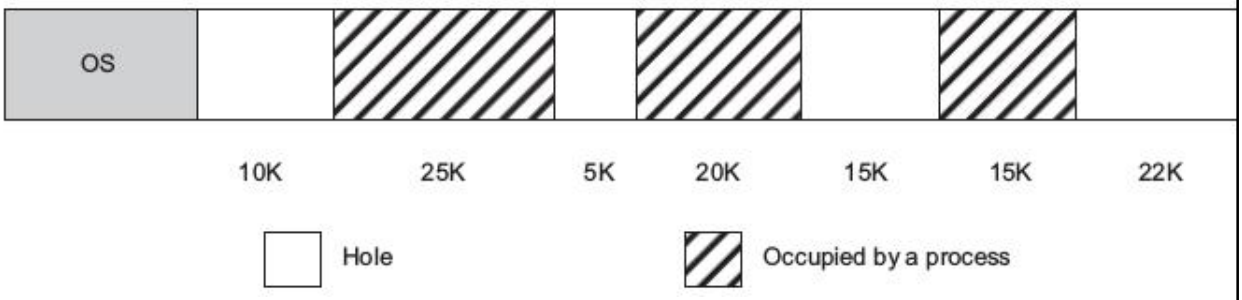
A) The executable is smaller.
B) When the library is changed, the code that references it does not usually need to be recompiled.
C) Every loaded program contains a duplicate copy of library routines. For static linking
D) Multiple programs can access the same library at the same time.

12) Consider a program X with three procedures, A, B, and C, are to be linked together into one process and loaded into memory. The length of each procedure is 600 words. The memory manager uses paging where page size is 1000 words and page tables occupy 1 page each. Assume that all procedures and all tables are in memory. The total internal fragmentation with the above allocation for program X is _____ words. **[NAT]**

13) A memory management unit performs memory mapping by converting a logical address into a physical address, with the help of _____

A) base registers
B) base and limit registers
C) limit registers
D) none

14) *Consider the memory allocation scenario as shown in figure below. Allocate memory for additional requests of 4K and 10K (in this order). The total internal fragmentation for memory allocation, using first-fit, best-fit, and worst-fit allocation methods in that order is*



A) 1K, 11K, 8K

B) 11K, 8K, 1K

C) 1K, 10K, 18K

D) 11K, 1K, 8K

Paging and Segmentation

15) Consider a machine with 1 MB physical memory and a 32 bit virtual address space. If the page size is 4 KB, the size of the page table is _____ MB. **[NAT]**

16) In a virtual memory system, size of virtual address is 32-bit, size of physical address is 30-bit, page size is 4 Kbyte and size of each page table entry is 24-bit. The main memory is byte addressable. The maximum number of bits that can be used for storing protection and other information in each page table entry is _____. **[NAT]**

17) The page size in a system is increased while keeping everything else (including the total size of main memory) the same. Which of the following is/are TRUE as a result of this increase in page size **[MSQ]**

A) Size of the page table of a process decreases.
B) Internal fragmentation of main memory increases.
C) TLB hit rate increases
D) Size of the page table of a process increases.

18) Consider a system with byte addressable memory, 32 bit logical addresses, 4KB page size and page table entries of 4 bytes each. The size of the page table in the system in is _____MB.

19) Consider a machine with 64 MB physical memory and a 32 bit virtual address space. If the page size is 4 KB, what is the size of the page table?

20) In a virtual memory system, size of virtual address is 32-bit, size of physical address is 30-bit, page size is 4 Kbyte and size of each page table entry is 32-bit. The main memory is byte addressable. The maximum number of bits that can be used for storing protection and other information in each page table entry is _____.

21) Given that virtual address space is 4 KB and page table entry size is 8 bytes. Calculate the optimal page size .

22) The virtual address space is 2^22 bytes and page size is 4KB. What is the maximum page table entry such that the entire page table fits in one page? Ans is in bytes not in bits

23) Consider a virtual address with a page size of 1KB. Two-level paging is used with equal number of entries in every page table. If the page table entry is 2 bytes long, what is the maximum size of the physical address space. ?

24) A system has a 32 bit virtual address space, and combines both segmentation and paging as shown below. The page table entry is of 4 bytes, 4 bits for the segment, 16 for the page, and 12 for the offset. The CPU issues a read for address 0xC0DEDBAD, then the page address is _____ .

SEGMENT NUMBER| PAGE NUMBER| OFFSET

A) 0x0DED
B) 0xC0DE
C) 0xDBAD
D) 0xDEDB

25) A multilevel page table is preferred in comparison to a single level page table for translating virtual address to physical address because [MSQ]
(A) it reduces the memory access time to read or write a memory location
(B) it helps to reduce the size of page table needed to implement the virtual address space of a process
(C) it is required by the translation lookaside buffer
(D) it helps to reduce the number of page faults in page replacement algorithms

26) Consider a virtual memory system with 40-bit virtual addresses, 32-bit physical addresses,

and 16 KB pages, the TLB stores 128 entries and the cache is directly mapped. Then, the total number of bits in TAG, INDEX and OFFSET are
A. 11, 7, 14
B. 19, 7, 14
C. 7, 19, 14
D. 7, 11, 14

27) Consider a 32-bit computer with page size 2KB and physical memory of 32 GB. Each virtual page has additional 8 bits for hardware control. The computer has a two-level page table. The minimum number of bits in second level page table entry is
(A) 24
(B) 32
(C) 40
(D) 16

28) Consider a process with 4 pages, numbered 0–3. The page table of the process consists of the following logical page number to physical frame number mappings: (0, 11), (1, 35), (2, 3), (3, 1). The process runs on a system with 16 bit virtual addresses and a page size of 256 bytes. The process accesses virtual address 770, which logical page number does this virtual address correspond to?
A) Page 3
B) Page 0
C) No entry found.
D) Page 1

29) Which of the following is/are TRUE ? **[MSQ]**

A) A smaller page size leads to smaller page tables
B) A smaller page size leads to more TLB misses
C) A smaller page size leads to fewer page faults
D) A smaller page size reduces paging I/O throughput

30) Which of the following is/are true about the logical address to physical address binding.**[MSQ]**
A) This binding can be done at compile time.
B) Converts symbolic addresses to relocatable addresses.
C) This binding cannot be done at run time.
D) Data used within the compiled source is offset within the object module.

31) Which of the following is/are true.**[MSQ]**

A) Dynamic loading provides better memory-space utilization .
B) Dynamic loading does not require special support from the OS.
C) Linking cannot be postponed until execution time.
D) Dynamic linking is particularly useful for libraries.

32) Which of the following is/are true.**[MSQ]**

A) Valid bit indicates that the associated page is legal.
B) Present or absent bit says whether a particular page has a frame mapped.
C) Valid/Invalid bits are part of page table entry.
D) Valid/Invalid bits are part of memory management hardware.

33) Which of the following is/are true.**[MSQ]**

A) Paging suffers from internal fragmentation.
B) Page tables are the overhead on the memory.
C) Multi level paging leads to increased memory overhead.
D) Multi level paging leads to increase in memory access time .

34) A system has a 32 bit virtual address space, and combines both segmentation and paging as shown below. The page table entry is of 4 bytes, 4 bits for the segment, 16 bits for the page, and 12 bits for the offset. The CPU issues a read for address 0xC0DEDBAD, then the page address is _____ .

SEGMENT NUMBER	PAGE NUMBER	OFFSET

A) 0x0DED
B) 0xC0DE
C) 0xDBAD
D) 0xDEDB

Consider a process with 4 pages, numbered 0–3. The page table of the process consists of the following logical page number to physical frame number mappings:

Page No	Frame No
0	11

1	35
2	3
3	1

The process runs on a system with 16 bit virtual addresses and a page size of 256 bytes. The process accesses virtual address 770, which frame number does this virtual address correspond to?
A) Frame 3
B) Frame 0
C) No entry found.
D) Frame 1

35) Consider a virtual address with a page size of 4KB. Two-level paging is used with an equal number of entries in every page table. If the page table entry is 1 byte long, what is the maximum size of the physical address space._____ MB ? **[NAT]**

Consider a computer system with a 32-bit logical address and 4KB page size. The system supports up to 1GB of physical memory. How many entries will be there in an inverted page table?
A) 128K
B) 512K
C) 1M
D) 256K

36) Consider a byte addressable system which uses 32 bits virtual address, 4KB page size with 2-level paging. The page table entry is 4 bytes.
The total size of the outer page table, if it is required to fit the outer table in one frame is _____ KB **[NAT]**

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37) A program has been divided into five modules. Their lengths and base addresses are stored in the segment table, as depicted shown below :

Segment number	Length	Base address
0	200	4100
1	700	1000
2	400	3700
3	900	1800
4	1000	2700

<s,d> represents the segment number and the given offset value of the logical address. Which of the following addresses will not generate a segmentation fault ? **[MSQ]**

A) <3,906>
B) <1,665>
C) <4,770>
D) <0,127>

38) Consider a system with 1KB page size and single-level paging is used. The virtual address space is 36 bits and the physical address space is 32 bits. Calculate the number of frames required to store the entire page table.

move bits to 1B for simplicity

A) 2^18
B) 2^20
C) 2^26
D) 2^28

39) Consider a system with 4KB page size and 3-level paging is used. The virtual address space is 36 bits and the physical address space is 32 bits. The page table entry at every level is 16bytes.The number of frames required to store all the level page tables, if each level uses 8 bits for page table indexing and each page table fits one page-frame_____ **[NAT]**

40) Choose the correct statement(s) among the following: **[MSQ]**

A) Paging eliminates the problem of external fragmentation and therefore the need for compaction.
B) Paging allows sharing of code pages among processes, reducing overall memory requirements.
C) Paging enables processes to run when they are only partially loaded in main memory.
D) Paging reduces the memory access overhead.

41) Suppose that we have a two-level page translation scheme with 4K-byte pages and 4-byte page table entries (includes a valid bit, a couple permission bits, and a pointer to another

page/table entry). What is the format of a 32-bit virtual address

A) Outer Page Table Index : 8 bits, Inner Page Table Index : 14 bits, Offset : 12 bits
B) Outer Page Table Index : 12 bits, Inner Page Table Index : 12 bits, Offset : 12 bits
C) Outer Page Table Index : 10 bits, Inner Page Table Index : 10 bits, Offset : 12 bits
D) Outer Page Table Index : 10 bits, Inner Page Table Index : 12 bits, Offset : 10 bits

42) A multilevel page table is preferred in comparison to a single level page table for translating virtual address to physical address because

(A) it reduces the memory access time to read or write a memory location.
(B) it helps to reduce the size of the page table needed to implement the virtual address space of a process.
(C) it is required by the translation lookaside buffer.
(D) it helps to reduce the number of page faults in page replacement algorithms

43) Consider the following segment table: Which of the following logical addresses (Segment Number, Offset) may generate a TRAP?

Segment	Base	Length
0	219	600
1	2300	14
2	90	100
3	1327	580
4	1952	96

A) 0,430
B) 1,10
C) 2,500
D) 3,400

44) A virtual address ‘a’ in a paging system is equivalent to a pair (p, w), in which ‘p’ is a page number and ‘w’ is a byte number within the page. Let ‘z’ be the number of bytes in a page. The relation between ‘p’, ‘z’, ‘w’ and ‘a’ is
A) p=az + w
B) a=pw + z
C) z=pa + w
D) a=pz + w

45) Consider a page reference string for a process with a working set of M frames, initially all empty. The page reference string is of length P with N distinct page numbers in it. For any page replacement algorithm, lower bound and upper bound on the number of page faults is
A) N, P
B) N, P/2
C) N/2, P
D) N/2, P/2

46) A page table entry provides _____
A) offset
B) limit address
C) base address
D) None

47) Memory mapping through TLB is known as _____
A) associative mapping
B) TLB mapping
C) physical mapping
D) none

48) Rather than having the page table entry for a virtual page, _____ is taken as a page table entry in the inverted page table.

A) Process Id
B) Page table base register (PTBR)
C) Real page frame
D) None

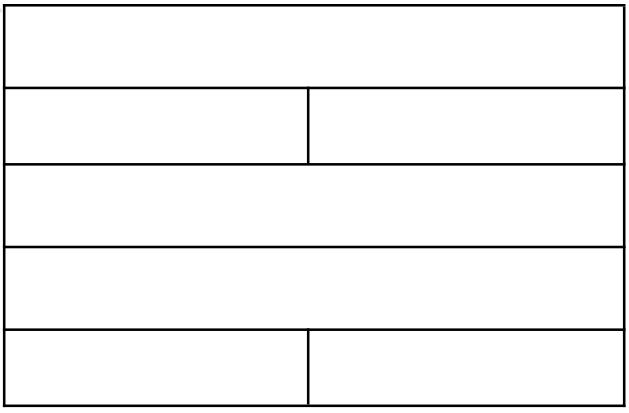
49) In a paging scheme, 16-bit addresses are used with a page size of 512 bytes. If the logical address is **0000010001111101**. What will be the physical address, if the frame address
corresponding to the computed page number is 15.

A) 0001011001101101
B) 0000111001100101
C) 0000111001111101
D) 0001111001111101

:

50) There is a system with 64 pages of 512 bytes page size and a physical memory of 32 frames. How many bits are required in the logical and physical address?

A) 15, 15
B) 15, 14
C) 14, 15
D) 14, 14



51) A program has been divided into five modules. Their lengths and base addresses are stored in the segment table, as depicted shown below :

Segment number	Length	Base address
0	200	4100
1	700	1000
2	400	3700
3	900	1800
4	1000	2700

<s,d> represents the segment number and the offset of the logical address. Which of the following address will generate a segmentation fault ?

A) <3,906>
B) <1,665>
C) <4,770>
D) None

52) A system with 32-bit logical address uses a two-level page table structure. It uses page size of 2^10 bytes . The outer page table is accessed with 8 bits of the address. How many entries are there in the inner page table?

A) 256 entries
B) 8192 entries
C) 16384 entries
D) 4096 entries

53) A computer with a 32-bit address uses a two-level page table. Virtual addresses are split into a 9-bit top-level page table field, an 11-bit second-level page table field, and an offset. How many pages are there in the address space?

A) 2^20
B) 2^12
C) 2^9
D) 2^11

54) A computer with an 8KB page, a 256MB main memory, and a 64GB virtual address space uses an inverted page table to implement its virtual memory. If a hash table is used to map the pages, then what is the number of entries in the hash table?

A) 4M
B) 16K

C) 32K

D) 8M

Page Replacement Algorithms

55) Consider the page reference string given below , assuming 3 page-frames, and all frames are initially empty. Calculate the number of page faults using Optimal algorithm : **[NAT]**

4 , 7, 6, 1, 7, 6, 1, 2, 7, 2

56) Consider the page reference string given below , assuming 4 page-frames, and all frames are initially empty. Calculate the number of page faults using FIFO algorithm : **[NAT]**

4 , 7, 6, 1, 7, 6, 1, 2, 7, 2

57) Consider the page reference string given below , assuming 4 page-frames, and all frames are initially empty. Calculate the number of page faults using LRU algorithm : **[NAT]**

4 , 7, 6, 1, 7, 6, 1, 2, 7, 2

58) A process has 5 logical pages, and accesses them in this order: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Which of the following statements is/are TRUE ? **[MSQ]**

A) The above referenced string suffers from Belady's anomaly when used with FIFO page replacement algorithm.
B) The above referenced string generates 9 page faults with 3 frames, and 10 page faults with 4 frames, using the FIFO page replacement.
C) The above referenced string suffers from Belady's anomaly when used with LRU page replacement algorithm.
D) In LRU, the N most recently used frames are always a subset of N+1 most recently used frames. So if a page fault occurs with N+1 frames, it must have occurred with N frames also.

59) Suppose you know that there will only be 4 processes running at the same time, each with a Resident Set Size (RSS) of 512MB and a working set size of 256KB. Assuming the same system with 32 bit virtual and physical address space with 4KB page size, what is the minimum amount of TLB entries that your system would need to support to be able to map/cache the working set size for one process?

A) 64
B) 128

C) 512
D) 1024

60) Consider a demand paging system with four physical memory frames and the following reference string over seven pages: 1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6
Assuming that memory starts empty, how many page faults will occur and what will be the final contents of memory under the FIFO page replacement policy?

A) 3,7,6,1 in memory and 10 page faults
B) 3,7,6,1 in memory and 11 page faults
C) 3,7,2,1 in memory and 12 page faults
D) 3,7,6,1 in memory and 12 page faults

~~61~~) Consider a simple system running a single process. The size of physical frames and logical pages is 16 bytes. The RAM can hold 3 physical frames. The virtual addresses of the process are 6 bits in size. The program generates the following 20 virtual address references as it runs on the CPU:
0, 1, 20, 2, 20, 21, 32, 31, 0, 60, 0, 0, 16, 1, 17, 18,32, 31, 0, 61
The number of page faults generated by the accesses above, assuming a FIFO page replacement algorithm
A) 6
B) 7
C) 8
D) 9

~~62~~) Consider the following memory reference string :

1,2,3,4,5,3,4,1,6,7,8,7,8,9,7,8,9,5,4,5,4,2

Calculate the average memory access time if memory access time is 100ns and 3000ns page fault service time if on demand Optimal page replacement algorithm is used with a total physical memory of 4 frames.

A) 3000ns
B) 1250ns
C) 1420ns
D) 1550ns

63) A certain page table entry in the page table of a process has both the valid and present bits set, now which of the following is TRUE in the context of TLB and memory access ?
A) A TLB hit occurs, always.

B) A page fault will occur.
C) A TLB hit or miss may occur, cannot say.
D) None of these

64) Consider the following page references, with 3 frames and FIFO page replacement policy is used. Calculate the total number of page faults. **[NAT]**

1, 2, 3, 2, 1, 5, 2, 1, 6, 2, 5, 6, 3, 1, 3, 6, 1, 2, 4, 3

65) Consider the following page references, with 3 frames and OPTIMAL page replacement policy is used. Calculate the total number of page faults. **[NAT]**

1, 2, 3, 2, 1, 5, 2, 1, 6, 2, 5, 6, 3, 1, 3, 6, 1, 2, 4, 3

66) Consider the following page references, with 3 frames and LRU page replacement policy is used. Calculate the total number of page faults. **[NAT]**

1, 2, 3, 2, 1, 5, 2, 1, 6, 2, 5, 6, 3, 1, 3, 6, 1, 2, 4, 3

67) Consider the following code in which the integer is of size 4 bytes and the page size is 4KB, and on demand paging is used with 3 frames initially empty. The number of page faults generated by the code using a FIFO page replacement policy is:_____**[NAT]**

```
int A[4000];

int main()
{
for(i=0;i<4000;i++){ //Row major order access
   A[i] = A[i]+1;
}
return 0;
}
```

68) Consider the following sequence of page accesses:

A, B, D, C, B, A, B, A

If there are three frames of physical memory then the number of page faults using FIFO and

LRU page replacement policies are ..... and ..... respectively.

A. 5,6
B. 6,5
C. 5,5
D. 6,6

69) The recent page references for three processes with a window size of 10 page references is given as follows:

Process	Reference window (Size =10)
P1	0, 1, 2, 0, 2, 4, 5, 1, 3, 4
P2	1, 3, 2, 5, 2, 4, 2, 1, 3, 1
P3	1, 3, 2, 0, 2, 4, 5, 1, 2, 0

Calculate the minimum number of frames required in the main memory to avoid “thrashing”

A) 15
B) 16
C) 17
D) 18

70) Which of the following statements is/are TRUE? **[MSQ]**

A) FIFO page replacement suffers from Belady’s anomaly.
B) LRU page replacement suffers from Belady’s anomaly.
C) Second Chance page replacement suffers from Belady’s anomaly.
D) An algorithm suffers from Belady’s Anomaly if and only if it does not follow stack property.

TLB and Memory Performance Equation

71) Consider a paging system that uses a 3-level page table residing in main memory and a TLB for address translation. Each main memory access takes 150 ns and TLB look up takes

10 ns. Assume that the TLB hit ratio is 90%, the average memory access time in ns (round off to 2 decimal places) is _____. **[NAT]**

72) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. The page fault service takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. TLB update time is negligible.
The average memory access time in ns (round off to 2 decimal places) is _____ .
[NAT]

73) Consider a system with 8-bit virtual and physical addresses, and 16 byte pages. A process in this system has 4 logical pages, which are mapped to 3 physical pages as follows:

Page table

Page	Frame
0	6
1	3
2	11
5	-

TLB

Index	Frame
0	6
2	11

Which of the following is/are TRUE ? **[MSQ]**

A) CPU access to virtual address 7 leads to a TLB hit.
B) CPU access to virtual address 20 leads to a TLB hit.
C) CPU access to virtual address 70 leads to a trap to OS.
D) CPU access to virtual address 80 leads to a page fault.

74) Consider the following combinations and identify which of the following are possible?
[MSQ]

A) TLB: Hit, Page: Hit, Cache: Hit
B) TLB: Hit, Page: Hit, Cache: Miss
C) TLB: Miss, Page: Miss, Cache: Hit
D) TLB: Miss, Page: Miss, Cache: Miss

75) In a paging system with TLB, it takes 30 ns to search the TLB and 90 ns to access the memory. If the TLB hit ratio is 70%, find the effective memory access time (in ns).

A) 110 - 115
B) 145 - 150
C) 150 - 155
D) 55 - 60

76) A computer whose processes have 1024 pages in their address spaces keeps its page tables in memory. The overhead required for reading a word from the page table is 5 nsec. To reduce this overhead, the computer has a TLB, which holds 32 (virtual page, physical page frame) pairs, and can do a lookup in 1 nsec. What hit rate is needed to reduce the mean overhead to 2 nsec?

A)0.75-0.8
B)0.25-0.35
C)0.5 – 0.6
D)0.6-0.65

77) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Assume that the TLB hit ratio is 95%, the average memory access time in ns (round off to 2 decimal places) is _____.

78) Consider a paging system that uses 3-level page table residing in main memory and a TLB for address translation. Each main memory access takes 150 ns and TLB lookup takes 10 ns. Assume that the TLB hit ratio is 90%, the average memory access time in ns (round off to 2 decimal places) is _____.

79) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. TLB update time is negligible. :Here also
The average memory access time in ns (round off to 2 decimal places) is _____ .

80) Consider a paging system that uses 2-level page table residing in main memory and a TLB for address translation. Each main memory access takes 200 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 10000 ns. Assume that the TLB hit ratio is 99%, page fault rate is 1%. TLB update time is negligible. Here service time is given not pfst
The average memory access time in ns (round off to 2 decimal places) is _____ .

81) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk. TLB update time is negligible.
The average memory access time in ns (round off to 2 decimal places) is _____ .

82) Consider a paging system that uses 3-level page table residing in main memory and a TLB for address translation. Each main memory access takes 150 ns and TLB lookup takes 10 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 90%, page fault rate is 10%. Assume that for 15% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk. TLB update time is negligible.
The average memory access time in ns (round off to 2 decimal places) is _____ .

83) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. The page fault service takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. TLB update time is negligible.
The average memory access time in ns (round off to 2 decimal places) is _____ .

84) Consider a paging system that uses 2-level page table residing in main memory and a TLB for address translation. Each main memory access takes 200 ns and TLB lookup takes 20 ns. The page fault service takes 10000 ns. Assume that the TLB hit ratio is 99%, page fault rate is 1%. TLB update time is negligible.
The average memory access time in ns (round off to 2 decimal places) is _____ .

85) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 75 ns, with a cache hit rate of 90%. Assume that the TLB hit ratio is 95%, and the page tables are not cached, the average memory access time in ns (round off to 2 decimal places) is _____.

86) Consider a paging system that uses 2-level page table residing in main memory and a TLB for address translation. Each main memory access takes 150 ns and TLB lookup takes 10 ns. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 125 ns, with a cache hit rate of 95%. Assume that the TLB hit ratio is 90%, and the page tables are not cached, the average memory access time in ns (round offto 2 decimal places) is _____.

87) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. TLB update time is negligible. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 75 ns, with a cache hit rate of 90%, and the page tables are not cached.
The average memory access time in ns (round off to 2 decimal places) is _____ .

88) Consider a paging system that uses 3-level page table residing in main memory and a TLB for address translation. Each main memory access takes 150 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 10000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. TLB update time is negligible. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 125 ns, with a cache hit rate of 95%, and the page tables are not cached. The average memory access time in ns (round off to 2 decimal places) is _____ .

89) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk. TLB update time is negligible. To make the memory access faster, a physical level-1 cache is introduced, with no

write back mechanism. The cache access time is 75 ns, with a cache hit rate of 90%, and the page tables are not cached.
The average memory access time in ns (round off to 2 decimal places) is _____ .

90) Consider a paging system that uses 3-level page table residing in main memory and a TLB for address translation. Each main memory access takes 150 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 10000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk.TLB update time is negligible. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 125 ns, with a cache hit rate of 95%, and the page tables are not cached. The average memory access time in ns (round off to 2 decimal places) is _____ .

91) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. The page fault service takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. TLB update time is negligible. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 75 ns, with a cache hit rate of 90%, and the page tables are not cached.
The average memory access time in ns (round off to 2 decimal places) is _____ .

92) Consider a paging system that uses 2-level page table residing in main memory and a TLB for address translation. Each main memory access takes 200 ns and TLB lookup takes 20 ns. The page fault service takes 10000 ns. Assume that the TLB hit ratio is 99%, page fault rate is 1%. TLB update time is negligible. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 150 ns, with a cache hit rate of 95%, and the page tables are not cached.
The average memory access time in ns (round off to 2 decimal places) is _____ .
176.25

93) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 75 ns, with a cache hit rate of 90%. Assume that the TLB hit ratio is 95%, and the page tables are also physically cached, the average memory access time in ns (round off to 2 decimal places) is _____.

94) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. TLB update time is negligible. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 75 ns, with a cache hit rate of 90%, and the page tables are also physically cached..

The average memory access time in ns (round off to 2 decimal places) is _____ .

95) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk. TLB update time is negligible. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 75 ns, with a cache hit rate of 90%, and the page tables are also physically cached..
The average memory access time in ns (round off to 2 decimal places) is _____ .

96) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. The page fault service takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. TLB update time is negligible. To make the memory access faster, a physical level-1 cache is introduced, with no write back mechanism. The cache access time is 75 ns, with a cache hit rate of 90%, and the page tables are also physically cached.
The average memory access time in ns (round off to 2 decimal places) is _____ .