CS & IT Batch: English

Digital Logic
Combinational Circuit

DPP-04

[MCQ] ★☆☆

1. What are basic gates required to implement a full adder

(a) 1 EX-OR gate, 1 AND gate

(b) 2 EX-OR gate, 1 OR gate

(c) 2 EX-OR gate, 2 AND gate, 1 OR gate

(d) 1 EX-OR gate, 2 AND gate, 2 OR gate

[NAT]

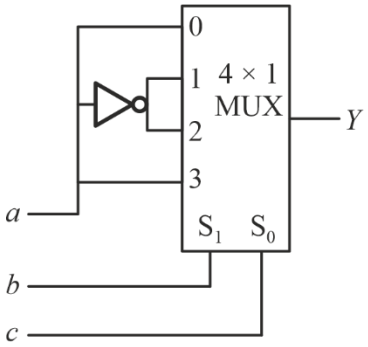
2. How many half adders are required to implement the following expressions.

$D = \bar{A}BC + A\bar{B}C, E = A \oplus B \oplus C$

$F = \bar{A}C + AB\bar{C} + \bar{B}C$

[MCQ] ★★★

3. The following multiplexer circuit is equivalent to _____.



(a) Implementation of sum equation of full adder

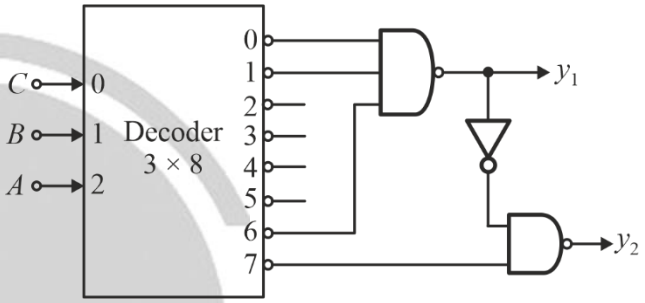
(b) Implementation of carry equation of full adder

(c) Implementation of borrow equation of full subtractor

(d) All the above

[MCQ] ★★☆

4. A 3 line to 8 line decoder with three inputs *A*, *B*, *C* and two outputs y_1 and y_2, is configured as shown below. The minimized expression of outputs will be



(a) $y_1 = \bar{A}\bar{B} + AB\bar{C};\ y_2 = \overline{A \oplus B}$

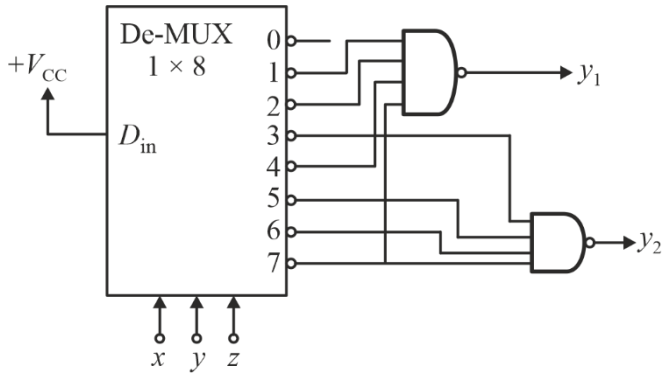
(b) $y_1 = AB + \bar{A}\bar{B}C;\ y_2 = A \oplus B$

(c) $y_1 = \bar{A}B + A\bar{C};\ y_2 = AB + AC$

(d) $y_1 = A\bar{B} + \bar{A}C;\ y_2 = \bar{A}B + \bar{B}C$

[MCQ] ★★★

5. A demultiplexer of size 1 × 8 with active low outputs, is programmed as shown below. The circuit has three inputs *x*, *y*, *z* and generates two outputs y_1, y_2.



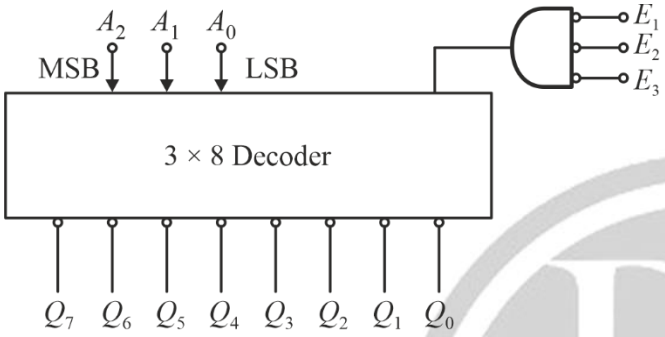
What is this circuit?

(a) Half subtracter (b) Full subtractor

(c) Half adder (d) Full adder

[MCQ] ★★☆

6. The logic diagram of a 3 × 8 decoder with active low outputs is shown below. What is state of outputs Q_7, ….. Q_0 for the set of inputs $E_3 = E_1 = 1$, $E_2 = 0$, $A_2 = A_1 = 1$ and $A_0 = 0$?

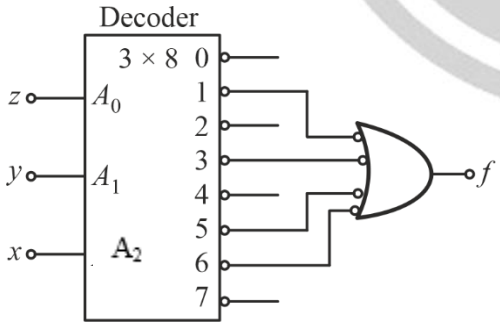


(a) 1111 1111 (b) 1011 1111

(c) 1111 0111 (d) 0000 0000

[MCQ] ★★☆

7. A 3 line to 8 line decoder with active low outputs, is used to realize Boolean function involving three variables x, y and z(x is MSB and z is LSB) as shown below.



The minimized Boolean function $f(x, y, z)$ in POS format, will be

(a) $(\bar{x}+\bar{y}+\bar{z})(x+y+z)(x+\bar{y}+\bar{z})(\bar{x}+y+\bar{z})$

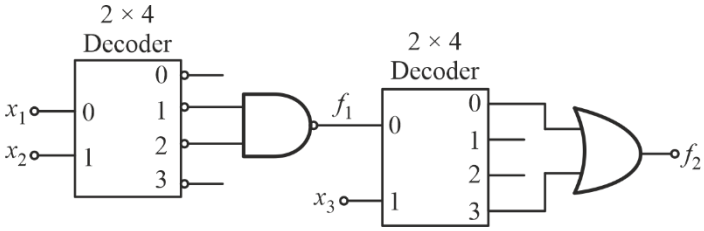
(b) $(\bar{x}+\bar{y}+z)(\bar{x}+y+z)(x+\bar{y}+z)(x+y+\bar{z})$

(c) $(x+z)(y+z)(\bar{x}+\bar{y}+\bar{z})$

(d) $(\bar{x}+\bar{z})(\bar{y}+\bar{z})(x+y+z)$

[MCQ] ★★☆

8. Two 2 × 4 decoders one with active low outputs and another with active high output are interconnected as shown below. The output function $f_2(x_3, x_2, x_1)$ will be



(a) $f_2 = (x_1 \oplus x_2) \odot x_3$

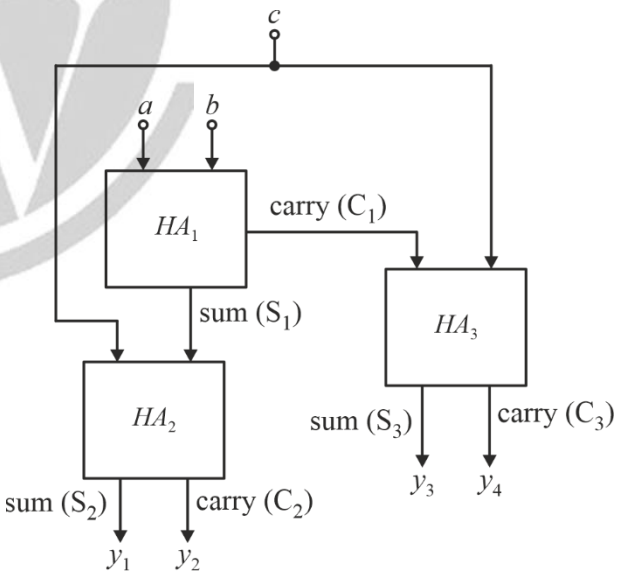
(b) $f_2 = (x_1 \odot x_2) \odot x_3$

(c) $f_2 = (x_1 \oplus x_2) \oplus x_3$

(d) $f_2 = (x_1 \oplus x_2) \oplus x_3$

[MCQ] ★☆☆

9. Three half adders HA_1, HA_2 and HA_3 are inter-coupled as shown below. The four output functions y_1, y_2, y_3 and y_4 are expressed in terms of inputs a, b and c. Which one of the following output expressions, is correct?



(a) $y_1 = (a \oplus b)c$

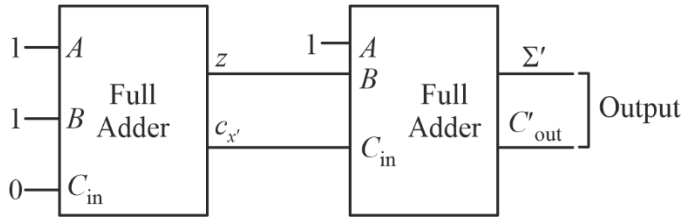
(b) $y_2 = (a \oplus b) \oplus c$

(c) $y_3 = ab \oplus c$

(d) $y_4 = a(b \oplus c)$

[MCQ] ★☆☆

10. Determine the outputs for the circuit shown below.



(a) $\Sigma' = 1, C'_{out} = 1$

(b) $\Sigma' = 0, C'_{out} = 0$

(c) $\Sigma' = 0, C'_{out} = 1$

(d) $\Sigma' = 1, C'_{out} = 0$

[MCQ] ★★☆

11. How many half adders, will be required to add two k bit numbers?

(a) $2k + 1$ (b) $2k - 1$

(c) $2k$ (d) $2(k + 1)$

[NAT] ★★☆

12. Eight 1-bit full adders are cascaded. Each 1-bit full adder generates carry out bit in 10 ns and sum bit in 30 ns. The number of addition performed per second, will be _____ $\times 10^7$.

Answer Key

1. **c**
2. **3**
3. **a**
4. **a**
5. **d**
6. **a**
7. **c**
8. **a**
9. **c**
10. **c**
11. **b**
12. **1**