Block Design for an RFID Integrated Tag in an Open-Access Technology Node.

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***Abstract*—This paper presents a passive fully-integrated RFID tag designed in a 130 nm open-access node using sky130 the process design kit. The RFID tag includes a full-wave rectifier and a voltage limiter to energize the internal blocks, which include a temperature sensor, a ring oscillator, and a switch for modulation. The tag is powered only by the RF signal received from the reader, eliminating the need for an external power source. Simulations were performed to check the operation of the blocks at the schematic and post-layout levels.**

***Index Terms*—Passive RFID tag, SkyWater130, Temperature sensor, CST Studio Suite.**

I. Introduction

The Internet of Things (IoT) Era started in 2017 when the number of IoT devices connected to the Internet surpassed the global population by almost 1 billion [1]. One of the key technologies that have contributed to this growth is Radio Frequency Identification (RFID). RFID is a communication technology that uses electromagnetic waves to transfer data between a reader and a tag for identification, tracking, and data collection without any physical contact [2]. Its small size makes it an imperceptible tool for a wide range of applications, such as tracking inventory in a warehouse or monitoring medical equipment in a hospital [3].

RFID technology has been around for almost 50 years, yet it remains a relevant and important component of the technological revolution that the world is currently experiencing. Since 2008, wireless sensing and positioning have been considered the most demanded functions in IoT devices, and RFID technology has been an important tool in meeting these demands [4]. As a result, there has been a technological breakthrough due to the expansion of devices using integrated technologies. Especially with the reduction of costs due to the massive production of integrated circuits by the miniaturization of electronic components. Still, the design and manufacturing of integrated circuits are reserved for companies or universities that can afford the high prices of the tools and the technology files.

One of the most significant advances in the democratization and easy access for the design of integrated circuits occurred in 2020 with the alliance between three companies: SkyWater Technology Foundry, Google, and Efabless Corporation [5]. This alliance allows the possibility to design and fabricate integrated circuits in a 130-nanometer node with reduced costs. Additionally, Efabless has created the Open multi-project wafer (MPW) program for the free design and fabrication of open-source integrated circuits [6]. This program allows academics, enthusiasts, hobbyists, and people working in the integrated circuit area to submit their designs every two and a half months in the MPW calls. To be part of the calls, the designed project must use SkyWater's open-access available Process Design Kit (PDK) and a standard system-on-chip (SoC) harness with on-chip resources to control and read/write operations from a user-dedicated space called Caravan (for analog projects) [7].

This project is focused on the design of a passive RFID with the sky130 PDK. The RFID is powered through the electromagnetic (EM) coupling between the tag and the reading system. The sections below provide the description of the architecture used in the tag's design, the design methodology, the results obtained, and the conclusions drawn from this work.

II. RFID Architecture Description

Radio Frequency Identification (RFID) is a well-established technology that provides significant benefits by allowing wireless, contactless data reading [8]. In general, RFID technology consists of two main components, as shown in Fig. 1: the reader (highlighted in blue) and the tag (highlighted in red).

The reader is a device that wirelessly communicates with RFID tags through a dissipative medium to capture information stored on them [3]. It emits a radio signal that energizes the tag, allowing it to transmit its data to the reader. The RFID tag can be attached to an object or embedded in a product. It stores information that can be accessed by an RFID reader. The RFID tag comprises an antenna and several circuit blocks that depend on the given purpose of the tag. In addition, to ensure operation at the required frequency, a capacitor is placed in parallel with the coil to achieve resonance and start storing energy to bias the load of the tag.

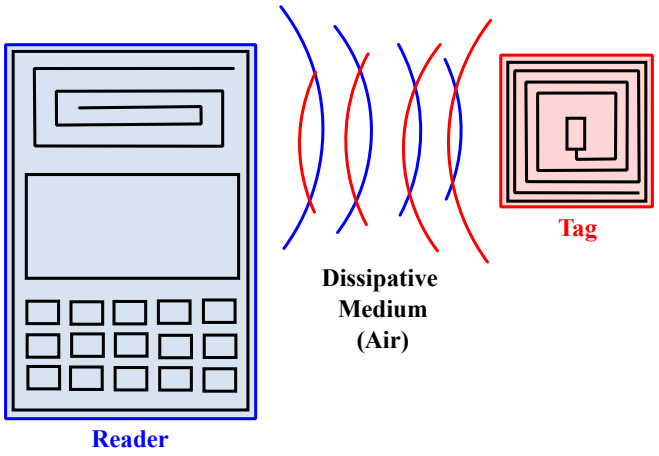

Fig. 1. RFID reader and tag communication. The reader (highlighted in blue) and the tag (highlighted in red) communicate via electromagnetic waves that propagate through the air.

This paper focuses on the design of a fully integrated RFID tag implemented with the open-access PDK sky130. To start the design of the RFID tag, it is necessary to obtain the specifications, such as the operating frequency and the available area.

First of all, we determine the operating frequency of the inductive link. Among the different frequency bands, the industrial, scientific, and medical (ISM) bands are public and commonly used for academic purposes. There are four frequency bands for ISM applications, as Table I presents:

TABLE I
POSSIBLE FREQUENCY ISM BANDS FOR TRANSMITTER AND RECEIVER TUNING.

Band	Frequency Range [MHz]
1	40.66 - 40.7
2	433.05 - 434.79
3	902 - 928
4	2400 - 2500

In this work, a frequency above 900 MHz has been chosen, in accordance with Colombian regulations set by the Agencia Nacional del Espectro (ANE). These regulations specify that the operating frequency for RFID systems must be included in the 915 MHz to 928 MHz frequency range [9]. We select the 922 MHz frequency to develop this work since it is centered in the ISM range mentioned above.

Regarding the layout area, the Open MPW program [6] offers a design area of 10mm^2 (highlighted in green) for the RFID tag, which is the available space for users to develop their designs as Fig. 2 depicts. The area highlighted in gray represents the common test harness mentioned before.

Once both specifications were set, we defined the main blocks that are part of the design of the RFID tag. It is worth mentioning that as stated in the plan presented in 2022, the

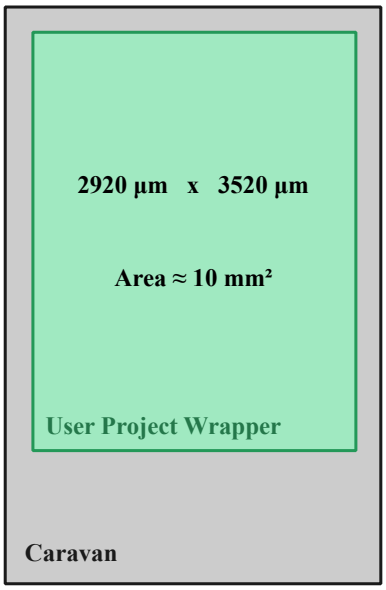

Fig. 2. Area available for the design offered by Efabless Open MPW program

RFID was developed for general purposes, but for this project we chose to focus on temperature measurement applications. Fig. 3 illustrates the block diagram of the designed RFID tag. It is composed of several blocks to transform the incoming electromagnetic wave from a transmitter into a continuous voltage to bias the different blocks, and consequently measure temperature for the latter backscattering transmission. The main blocks are a resonator composed of an inductor and a capacitor, an RF-to-DC circuit, the load, and the backscattering circuit. The general operation of each block will be described as follows.

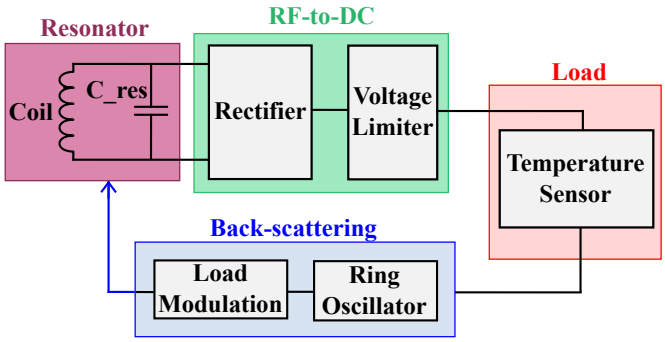

Fig. 3. General architecture of the designed RFID tag.

To start the transmission between the reader and the RFID tag, a variable-in-time current source supplies the reader inductor, producing a magnetic field that varies in space. When the reader is placed close to the tag resonator (highlighted in violet), the magnetic flux flowing across the tag surface induces an electromotive force (emf) in the coil. This emf generates an alternating current that allows the reception of the energy from the reader to the tag [10]. This

energy exchange takes place at a well-defined frequency, 920MHz, as mentioned before.

Once, the incoming energy is in the tag, an RF-to-DC circuit (highlighted in green) composed of a rectifier and a voltage limiter transforms the sinusoidal alternating power into a constant power and protects the load from high voltages that could damage the MOSFET physical structure. A full-wave rectifier is designed to achieve a DC voltage that can properly bias the circuit. Still, a ripple voltage coupled to the rectifier output must be minimized to deliver a bias voltage to the load as constant as possible. We connect a capacitor to the rectifier output to reduce the amplitude of the ripple.

As the amplitude of the rectifier output is dependent on the rectifier input, which, in turn, relies on the distance between the reader and the tag, in some cases the output voltage of the rectifier surpasses the maximum tolerated voltage of the CMOS technology. This presents a risk to the integrity of the transistors that compose the different blocks. With this in mind, a voltage limiter is used at the output of the full-wave rectifier to guarantee an optimal output voltage level for the correct operation of the transistors. The voltage limiter prevents values higher than the maximum tolerated voltage, which is 1.98 V for the sky130 technology.

Once we guarantee that a constant DC voltage supply is provided to the internal components of the tag, the system load (highlighted in red) can be designed. As mentioned before, we defined the load as a temperature measurement sensor.

To transmit the information to the reader, the sensor output is connected to a ring oscillator (RO). The RO transforms the voltage value into its corresponding oscillation frequency for later modulating the gate of a transistor. The information is sent back to the transmitter while using the back-scattering technique (highlighted in blue).

A more extended discussion and description of the circuit and techniques mentioned above will occur in Section III.

III. Design Methodology

This section describes the design methodology used for each block of the RFID tag. The methodology consists of the definition of the topologies used for each block and the implementation of layout techniques to compensate for the PVT variations. These variations impact the performance of the electronic devices caused by differences in process, voltage, and temperature.

A. Antenna

When the integrated coil in the RFID tag is exposed to the electromagnetic field generated in the reader's coil, the tag begins operating. The electromagnetic flux that flows through the receiver antenna induces an AC current, which generates an electromotive force at the terminals of the antenna. This electromotive force sets a bias voltage that enables the operation of the RFID tag. The amount of energy received by the RFID tag depends on the distance between both tags. Thus, there exists a certain threshold distance determined by the dissipative environment, the geometry of the reader and the RFID, and the reader's power, where the transfer of energy stops. In this case, the magnetic field lines no longer pass through the surface of the antenna tag.

In this project, we focus only on the design of the RFID inductor. The inductor was designed considering the available area specified by the Open-MPW project [11]. The inductor layout occupies all the available area provided by the manufacturing company since we desired to maximize the number of magnetic field lines through the RFID tag. After examining various antenna shapes, a rectangular shape was selected as depicted in Fig. 4. The circuits that integrate the tag are placed inside the inductor since we have no available area outside it. This placement would impact negatively the number of magnetic field lines through the inductor because the RFID circuits interfere with the electromagnetic waves. Thus the area of the layouts that compose the RFID block should be minimized.

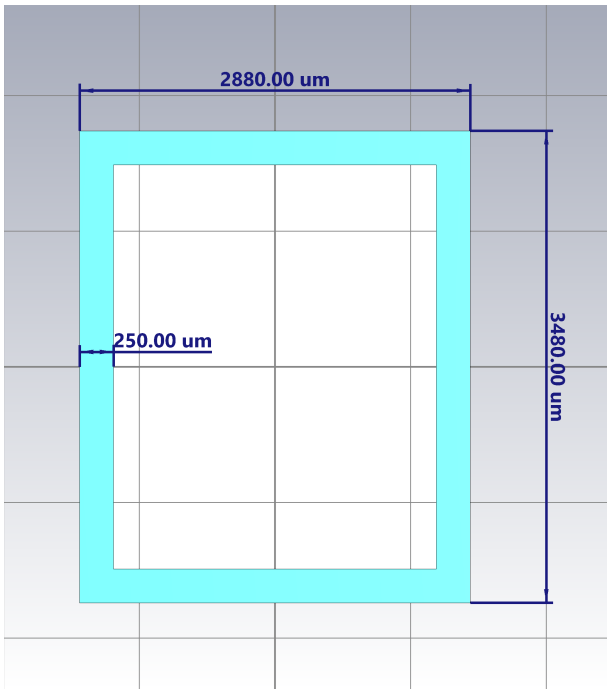

Fig. 4. Antenna design in CST Studio Suite.

Since no schematic, nor Spice model of the desired inductor was present in the PDK library, we modeled the inductor in the CST electromagnetic wave tool. Based on the cross-section of the sky130 technology, we implemented the antenna in the top metal layer of the process stack (Metal 5)

[12], which has a conductivity of 2.74 MS/m. Since Metal 5 is the thickest metal in the sky130 structure, we can achieve the higher quality factor. The main goal of implementing and characterizing the antenna in the CST software, was the generation of an RLC equivalent schematic to consider the effect of the inductor in the system simulation.

Fig. 5 illustrates this model, where L refers to the self-inductance, R refers to the resistance associated with the inductor, and $Cself$ refers to the parasitic capacitance responsible for the self-resonance of the inductor (frequency at which the imaginary part of the impedance is zero).

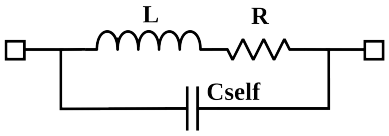

Fig. 5. RLC equivalent schematic of the designed antenna.

Since the self-resonance frequency is above the desired 920MHz ISM oscillation frequency, an additional capacitor $Cres$ is connected in parallel with the inductor, as depicted in Fig. 6.

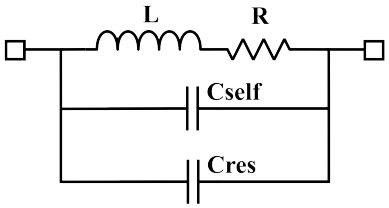

Fig. 6. RLC equivalent schematic of the designed antenna with a resonance capacitor, which sets the coil resonance frequency.

B. Rectifier

To supply power to the blocks that compose the RFID tag, it's necessary to transform the energy captured by the tag's inductor into a DC signal. This is achieved with a full-wave rectifier [10].

Fig. 7 displays the main circuit cell utilized for the full-wave rectifier, composed of two NMOS transistors and two PMOS transistors. The pins of the resonator are connected to the input terminals VIN_P and VIN_N. Assuming that the incoming voltage is a differential signal and that its amplitude value is sufficient to activate all of the transistors in the cell, follows a description of the operation at each cycle of the full-wave rectifier cell.

When a positive voltage value is in VIN_P (negative voltage value in VIN_N), transistors $M2$ and $M3$ turn on, while transistors $M1$ and $M4$ remain deactivated. At this point, a current flows from VIN_P to OUT_H through $M3$.

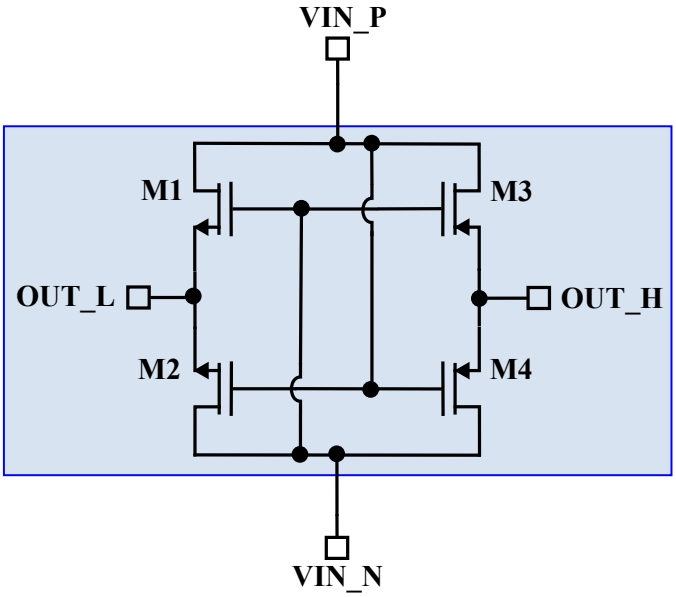

Fig. 7. Schematic of a rectifier cell. The cell is composed of four MOSFET switches which turn on and off in order to generate a DC signal.

Simultaneously, a current flows through $M2$ from OUT_L to VIN_N, creating a differential rectified voltage whose value is (OUT_H - OUT_L). This value is equivalent to $2 * VIN$, where VIN represents the amplitude of the input signal.

In the opposite cycle, when the positive voltage value is in VIN_N (negative voltage value is in VIN_P), transistors $M2$ and $M3$ are deactivated while current flows through $M1$ and $M4$. In this scenario, a current flows from OUT_L to VIN_P through transistor $M1$, and another current flows through $M4$ from VIN_N to OUT_H, generating the same differential voltage, which is equivalent to $2 * VIN$.

The DC voltage obtained in each cycle is $2 * VIN$, however, it is important to consider losses across each of the transistors activated in each cycle. These losses correspond to the threshold voltages of the transistors, which results in an output value of $(2 * VIN - |Vthp| - Vthn)$. It is important to clarify that the deactivated transistors have a leakage current, called reverse current, which should be minimized [10].

Low Voltage Threshold (LVT) transistors are used in the full-wave rectifier circuit to reduce the necessary amount of energy to turn on the transistors. Still, leakage across LVT transistors is larger than leakage across Nominal Voltage Threshold (NVT) transistors, which must be considered. Since it is desired to turn on the RFID tag with a small amount of energy, we decided to work with the LVT transistors.

The voltage required at the rectifier output corresponds a priori to the nominal voltage of the MOSFETs. According to Skywater's PDK, this value is 1.8 V. Characterization of one rectifier cell results in a DC output voltage of 420 mV.

Therefore, it is necessary to cascade more cells to reach the desired rectifier output voltage.

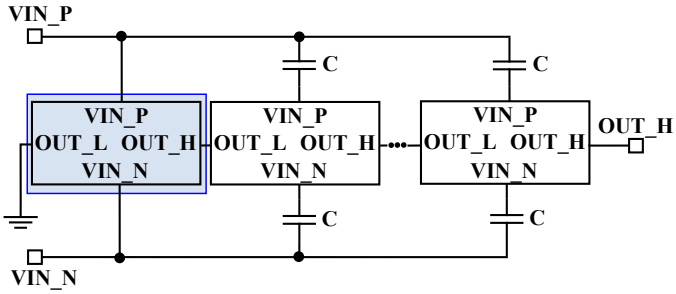

Fig. 8. Rectifier Schematic with N cells.

The cell previously explained can be cascaded N times to achieve the desired value, as depicted in Fig. 8. For this project, N is equal to six. To accumulate voltage between cells and reach the required value, capacitors are connected to the VIN_P and VIN_N inputs of the different cells. Equation (1) provides a theoretical value for the final output voltage [10].

$$OUT_H = N \cdot (2 \cdot VIN - V_{thp} - V_{thn}) \tag{1}$$

We use the minimum transistor length to reduce the parasitic capacitances associated with each transistor to decrease the time that the full-wave rectifier needs to achieve the 1.8V value. For the sky130 technology, the minimum channel length for LVT transistors is 180nm and 350 nm for NMOS and PMOS transistors, respectively.

Designing a rectifier involves an important trade-off between direct current losses and reverse conduction losses. Direct current losses occur when a MOSFET conducts in the forward direction, resulting in power loss due to heat dissipation. The MOSFET's finite resistance during conduction causes this loss. On the other hand, reverse conduction losses occur when the MOSFET is in its off state, but still conducts a small amount of current in the reverse direction. The parasitic diode in the device allows current to flow in the reverse direction, causing power to be dissipated as heat.

To balance direct current losses and reverse conduction losses, the Width-to-Length W/L ratio of transistors must be adjusted when designing a rectifier. Increasing the W/L ratio can improve direct current losses and rectifier performance by decreasing both Roff and Ron. However, decreasing Roff also increases reverse conduction losses. Additionally, a larger W/L ratio increases the total area of the rectifier block, so the dimension trade-off must be balanced. Equations for Ron and $Roff$ are shown in (2) and (3), respectively.

$$R_{on} = \frac{1}{(\mu n \cdot C_{OX} \cdot (W/L)) \cdot (V_G - V_{TH})} \tag{2}$$

$$R_{off} = \frac{1}{\lambda * (W/L) * V_{ds}} \tag{3}$$

Reverse conduction losses can be ignored assuming that $Roff$ is sufficiently large. Furthermore, Ron must also be small without significantly increasing the total area. Based on characterization results, we set $\frac{W}{L} = 150$ for both transistors.

The dimensions of the devices that compose the rectifier are shown in Tables II and III.

TABLE II
FULL-WAVE RECTIFIER TRANSISTORS' DIMENSIONS.

MOSFET	Width	Length	Multiplicity	Fingers
M1	5 µm	0.18 µm	6	1
M2	5 µm	0.18 µm	6	1
M3	10 µm	0.35 µm	3	2
M4	10 µm	0.35 µm	3	2

TABLE III
FULL-WAVE RECTIFIER RESISTANCES' DIMENSIONS.

Device	Width	Length	Multiplicity	Value
C	30 µm	30 µm	1	1.823 pF

Additionally, a capacitance of 3.65 pF is placed on the output of the last rectifier cell to reduce the ripple generated by the rectifier.

C. Voltage Limiter

The voltage limiter is designed to protect the transistors from high voltages and prevent oxide breakdown or damage to the physical structure. During the design phase, we considered that the rectifier output voltage could overcome the 1.8 V nominal value. Thus, a circuit based on a stacked voltage diode was implemented [13]. The voltage limiter maintains the nominal supply voltage of 1.8 V for the load circuits. Fig. 9 presents the schematic implemented for the Voltage Limiter.

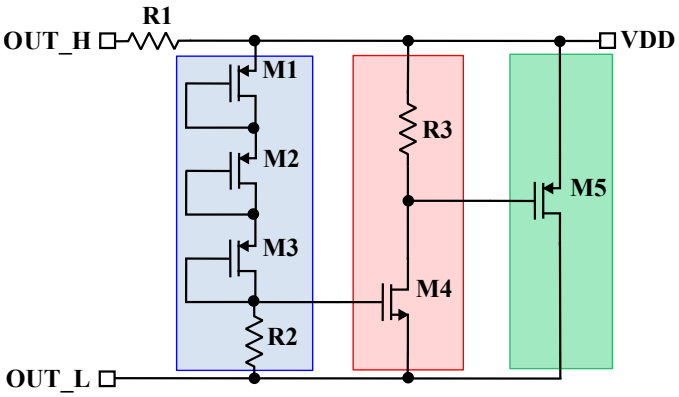

Fig. 9. Voltage Limiter Schematic implemented based on a stacked voltage diode circuit.

The output of the voltage limiter is given by:

$$VDD = 3 \cdot V_{gs} + I_d \cdot R_2 \tag{4}$$

Where Vgs corresponds to:

$$V_{sg} = |V_{thp}| + \sqrt{\frac{2 \cdot I_d}{\mu_P C_{OX} \cdot \frac{W}{L}}} \quad (5)$$

$\mu_P C_{OX}$ and $Vthp$ represent the transconductance parameter and the PMOS transistor threshold voltage, respectively. With a large aspect ratio of the PMOS transistors, the voltage limiter expression is modified to:

$$VDD = 3 \cdot |V_{thp}| + I_d \cdot R_2 \quad (6)$$

Transistors $M1$ - $M3$ are designed to set the value of VDD equal to 1.8 V. When the input voltage is higher than 1.8 V, a voltage drop across resistor R2 turns on transistor $M4$. In turn, transistor $M4$ sets a current through $R3$ that defines a voltage in the gate of transistor $M5$, turning the green branch on. When the $M4$ and $M5$ branches are active, they work as current sinks to maintain the output of the voltage limiter at the required value.

The dimensions of the devices used are given in Table IV and Table V.

TABLE IV
VOLTAGE LIMITER TRANSISTORS' DIMENSIONS.

MOSFET	Width	Length	Multiplicity	Fingers
M1	4 µm	0.35 µm	2	1
M2	4 µm	0.35 µm	2	1
M3	4 µm	0.35 µm	2	1
M4	2 µm	0.7 µm	1	1
M5	16 µm	0.35 µm	1	4

TABLE V
VOLTAGE LIMITER RESISTANCES' DIMENSIONS.

Device	Width	Length	Multiplicity	Value
R1	1 µm	2 µm	1	174.5Ω
R2	1 µm	40 µm	1	80 kΩ
R3	1 µm	60 µm	1	120 kΩ

D. Temperature Sensor

The architecture selected for temperature sensor is depicted in Fig. 10. It consists of three main parts: a bias circuit (highlighted in blue), a PTAT voltage generator (highlighted in red), and a differential amplifier (highlighted in green).

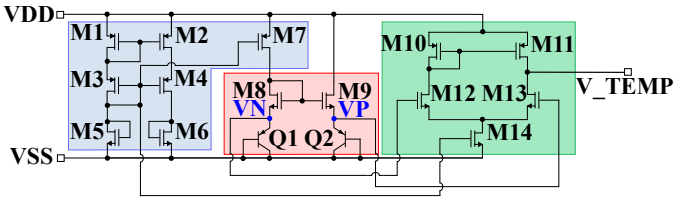

Fig. 10. Temperature Sensor Schematic based on PTAT voltage generator.

The operation of the temperature sensor is based on the correlation between temperature and voltage in the PTAT configuration [14]. This correlation relies on the difference between the two currents across the two BJTs, $Q1$ and $Q2$. The voltage difference between $Q1$ and $Q2$ emitters is proportional to the absolute temperature, which allows a linear behavior across the 0°C to 100°C temperatures range [15].

To design the PTAT voltage generator, a cascode current mirror sets the current through $M8$ to reduce the voltage variations in the nodes VN and VP. This current will be mirrored ten times to the branch connected to $M9$, generating a non-zero differential voltage in VN and VP. Regarding the sensitivity of the temperature sensor, characterization results demonstrated that a small channel length for M8 and M9 impacts negatively the sensitivity. Thus, we define the channel transistor length to 2 µm.

Although the differential voltage between the emitters of the BJT is linear and proportional to temperature, the output voltage of the temperature sensor is small. Therefore we designed an amplification stage to achieve a larger output range [14].

A differential input to a single-ended output amplifier with an active load (highlighted in green) was used amplify the difference between the two BJTs mentioned above. This amplifier uses an unbalanced differential pair composed of $M12$ and $M13$ to compensate for the asymmetry in the PTAT generator currents.

The dimensions of the devices implemented in the design of the Temperature Sensor are shown in Table VI.

TABLE VI
TEMPERATURE SENSOR TRANSISTORS' DIMENSIONS.

MOSFET	Width	Length	Multiplicity	Fingers
M1	2 µm	2 µm	1	1
M2	2 µm	2 µm	1	1
M3	2 µm	2 µm	1	1
M4	2 µm	2 µm	1	1
M5	0.5 µm	2 µm	1	1
M6	0.5 µm	2 µm	1	1
M7	2 µm	2 µm	1	1
M8	4 µm	2 µm	1	1
M9	4 µm	2 µm	10	1
M10	5 µm	2 µm	4	1
M11	5 µm	2 µm	4	1
M12	1 µm	2 µm	4	1
M13	1 µm	0.5 µm	4	1
M14	5 µm	2 µm	4	1
Q1	-	-	1	-
Q2	-	-	1	-

E. Ring Oscillator

A ring oscillator is a circuit that generates a periodic oscillation signal by connecting an odd number of inverters along a chain with positive feedback.

The oscillation frequency is determined by the delay of each inverter in the ring, which is influenced by the sizes of the transistors, the bias voltage, and the capacitive load at the output of each inverter. For this project, the oscillator frequency was set to 100 MHz.

To guarantee that the rise and fall times are closer, a relationship between transistor widths and carrier mobilities in NMOS and PMOS transistors is used. This relationship is shown in equation (7).

$$\frac{W_p}{W_n} = \frac{2.81\mu m}{0.88\mu m} = 3.193 \tag{7}$$

The architecture used in this work is present in Fig. 11 and it is composed of three inverters and three varactors. The varactors are used in this design since they are capacitors that change their values with voltage (highlighted in red). We use the incoming voltage of the amplifier associated with the temperature sensor, V_TEMP, to modify the varactor value, and consequently the oscillation frequency. The linear increase in V_TEMP results in a range of frequencies that increase at a linear rate.

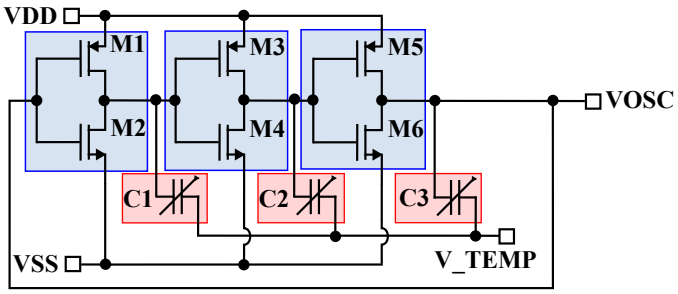

Fig. 11. Ring Oscillator Schematic using varactors.

The dimensions of the devices used in the ring oscillator are shown in Tables VII and VIII.

TABLE VII
RING OSCILLATOR TRANSISTOR DIMENSIONS.

MOSFET	Width	Length	Multiplicity	Fingers
M1	12 µm	2 µm	1	1
M2	4 µm	2 µm	1	1
M3	12 µm	2 µm	1	1
M4	4 µm	2 µm	1	1
M5	12 µm	2 µm	1	1
M6	4 µm	2 µm	1	1

TABLE VIII
DIMENSIONS OF ANOTHER DEVICES IN RING OSCILLATOR.

Device	Width	Length	Multiplicity	Value
C1	5 µm	5 µm	1	190 fF
C2	5 µm	5 µm	1	190 fF
C3	5 µm	5 µm	1	190 fF

F. Switch for Load Modulation

The switch for load modulation is a transistor that turns on and off and enables FSK modulation. Fig. 12 depicts the transistor and its connections.

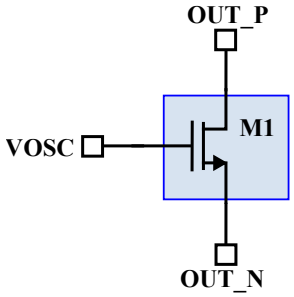

Fig. 12. Switch Schematic for Load Modulation.

To minimize the transistor on-resistance we use the minimum length of the technology. The dimensions of the transistor are shown in Table IX.

TABLE IX
SWITCH FOR LOAD MODULATION DIMENSIONS.

MOSFET	Width	Length	Multiplicity	Value
M1	5 µm	0.18 µm	1	1

IV. RESULTS AND DISCUSSION

This section presents the results obtained for each of the blocks that compose the RFID tag.

First of all, it is important to mention that we followed a design flow that is compatible with the sky130 PDK to test the different blocks. This flow is composed of several open-source tools, that can be installed by anyone. Follows a description of the different stages required to design and test the different circuits that integrate the RFID.

First, the user interface where all the different schematics and test benches associated with each one of the blocks designed are implemented using the Xschem tool [16]. Then, we proceeded to simulate the test benches with Ngspice [17], which is the Spice simulation engine. In the sky130 PDK, it is possible to consider the different process variations (corners) of SkyWater130 technology that affect the design. The nomenclature used for the different corners is presented in Table X.

In the case of the SS, FF, SF, and FS corners, the first letter denotes the NMOS transistor, while the second letter denotes the PMOS transistor. The letter ”S” indicates ”Slow,” and ”F” indicates ”Fast.” This implies that there may be variations in the manufacturing process with respect to the geometries of different elements involved in constructing a transistor. These variations are subject to the machines and processes used during chip production [18].

TABLE X
SKYWATER130 TECHNOLOGY NODE: CORNERS

Corner	NMOS-PMOS	Resistance	Capacitance
TT	Typical-Typical	Typical	Typical
FF	Fast-Fast	Typical	Typical
SS	Slow-Slow	Typical	Typical
FS	Fast-Slow	Typical	Typical
SF	Slow-Fast	Typical	Typical
LL	Typical-Typical	Low	Low
HH	Typical-Typical	High	High
LH	Typical-Typical	Low	High
HL	Typical-Typical	High	Low

In the LL, HH, HL, and LH corners, the letter "L" refers to "Low" variation in resistance and capacitance dimensions compared to typical values for the device. Conversely, the letter "H" refers to the "Higher" variation.

Once we achieve the different specifications for the different blocks, we create the layouts, which correspond to the physical implementations of the blocks, using the Magic tool [19]. To obtain a successful layout, we run and guarantee that the Design Rule Checking (DRC) option respects the manufacturer's design rules. We also performed the Layout versus Schematic (LVS) verification process with Netgen [20] to confirm that the physical design netlist was consistent with the schematic design netlist. Finally, parasitic capacitances and resistances extraction were considered and the results were compared with the schematic results.

A. Antenna

Two solvers of CST Studio Suite were used to model the antenna. The first one, LF Frequency Domain Solver, was used to find the inductance and resistance of the RLC model. To accomplish this, a rectangular shape was drawn and transformed into a coil considering the different parameters associated with the sky130 technology, such as material conductivity, thickness, and dimensions available for antenna construction. We run frequency simulations standing out of the frequency range of around 922MHz.

We used the Frequency Domain Solver as the second solver, which allowed us to determine the self-resonance frequency of the antenna with Z parameters. This frequency occurs when the parasitic capacitance of the inductor resonates with the ideal inductance of the coil, resulting in an extremely high impedance resulting in an impedance completely real, since the imaginary parts cancel each other, as shown in Fig. 13 and Fig. 14.

It is worth mentioning that two simulations run for the chosen antenna to examine how the RLC model changes with the inclusion or exclusion of the cross-section material information. The first simulation was performed on the highest metal layer of the SkyWater130 technology. The second simulation considers the cross-section of the SkyWater130 technology, represented by a substrate of Lossy Silicon material.

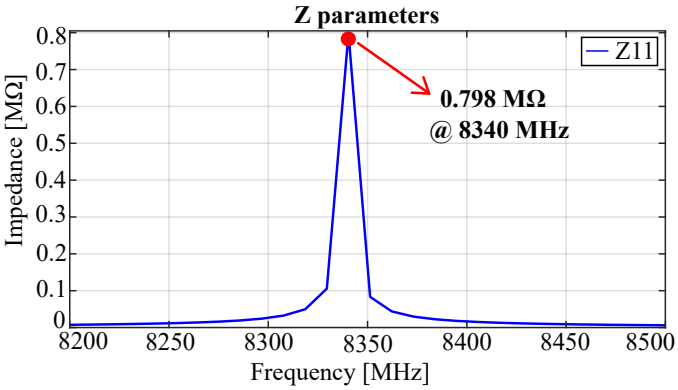

Fig. 13. Z parameters simulation results for the antenna without the lossy substrate using the Frequency Domain Solver.

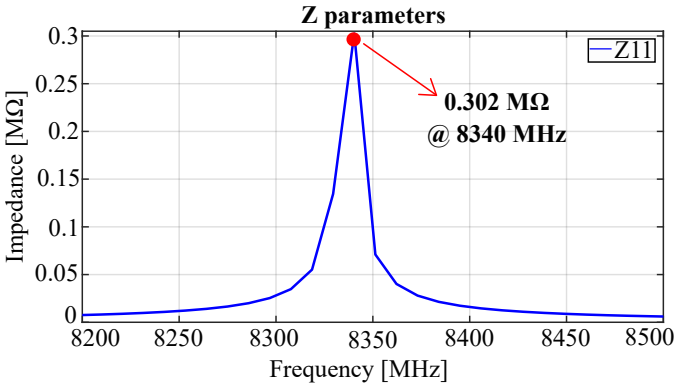

Fig. 14. Z parameters simulation results for the antenna and the lossy substrate using the Frequency Domain Solver.

In addition, Fig. 15 illustrates the reflection coefficient (S11) of the designed antenna without substrate, while Fig. 16 shows the result considering the parameters of the sky130 cross-section.

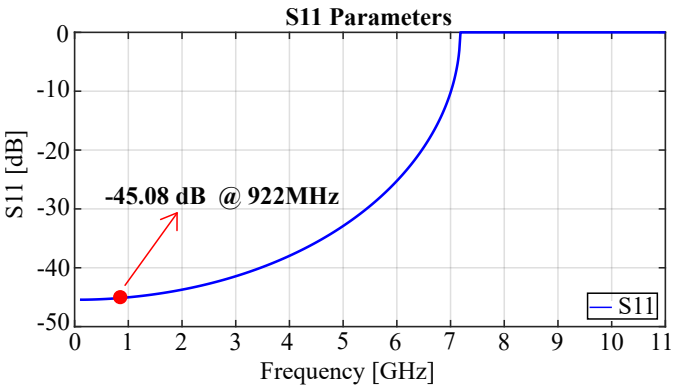

Fig. 15. S11 parameters simulation results for the antenna without the lossy substrate using Frequency Domain Solver.

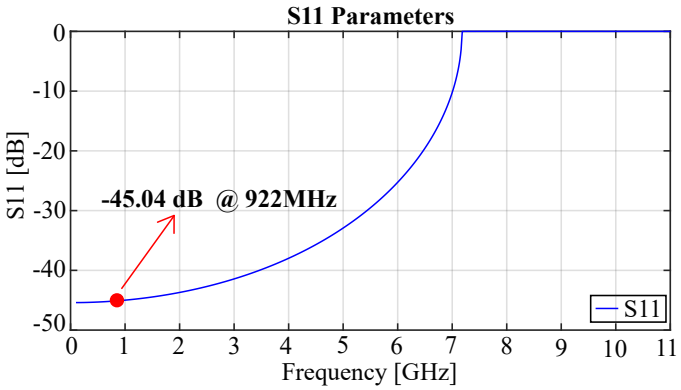

Fig. 16. S11 parameters simulation results for the antenna and the lossy substrate using the Frequency Domain Solver.

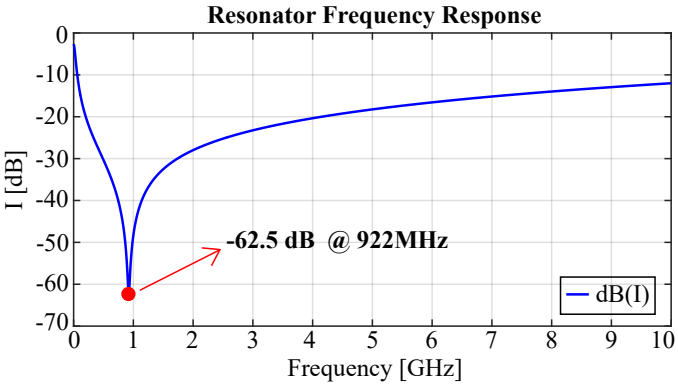

Fig. 19. SPICE simulation Results of the RLC model with the resonance capacitor.

Based on the results mentioned above, we can calculate the self-resonance capacitor as shown in equation (8).

$$C_{self} = \frac{1}{(w)^2 * L} = 49.35fF \tag{8}$$

We can use the same RLC model, as illustrated in Fig. 17 for both simulated antennas since they have the same resonance frequency.

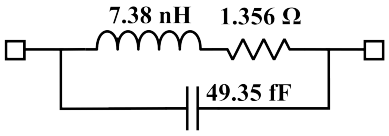

Fig. 17. RLC model of the designed antenna.

After obtaining the results mentioned above, the RLC model of the antenna was simulated in an Xschem test bench with the resonance capacitor. A theoretical value for the resonance capacitor was calculated as shown in equation (9).

$$C_{res} = \frac{1}{(2 * \pi)^2 * Fo^2 * L} = 4.055pF \tag{9}$$

SPICE simulations were run to determine the capacitance value required to achieve a resonance frequency at 922MHz. Once, the resonance capacitance was achieved, we determine the antenna quality factor as shown in Fig. 19.

Finally, the simulated RLC model is presented in Fig. 18.

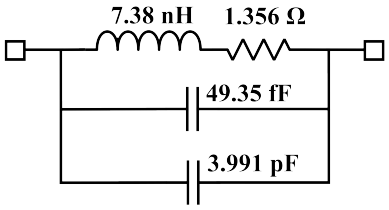

Fig. 18. Final RLC model with Sky130 resonance capacitor.

From the simulation results presented in Figure 19, the quality factor can be calculated with equation (10). Here, f_0 refers to the resonance frequency, and Δf refers to the bandwidth.

$$Q_{factor} = \frac{f_0}{\Delta f} = \frac{922.541MHz}{935.75MHz - 906.61MHz} = 31.55 \tag{10}$$

Fig. 20 shows the layout of the resonator (antenna and resonance capacitor) implemented with Magic. The resonance capacitor consists of C1, C2 and C3, which are in parallel.

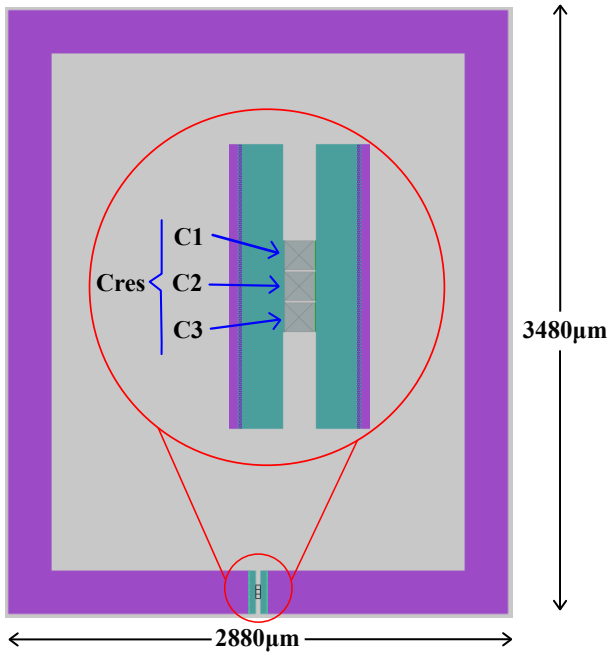

Fig. 20. Layout of the Resonator using Magic.

B. Rectifier

To guarantee the proper operation of the full-wave rectifier, a transient simulation was run with the inductive link modeled by a 0.45 V sinusoidal source. It is worth mentioning that there exist some limitations associated with the components provided by the PDK. For instance, there is no block that represents the coupling factor between two inductors. Thus,

there are some additional works to do by the open-source tools designers to provide complementary tools that enhance robustness and accuracy during the design of integrated circuits. The rectifier physical implementation uses interdigitation as a layout technique to reduce the PVT effects. This technique involves the overlapping of two sets of conductive materials to create a more compact and efficient layout. Fig. 21 shows the layout of the Full-wave Rectifier, with an area of 19360 μm^2.

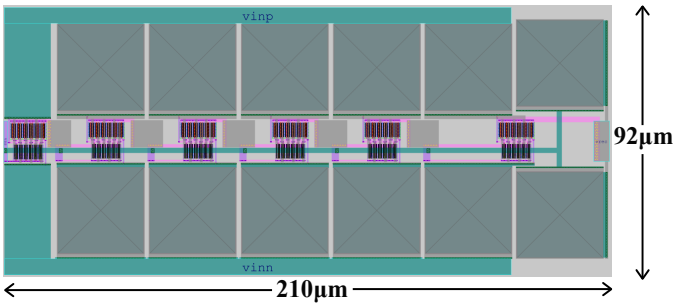

Fig. 21. Full-wave rectifier layout using Magic.

Fig. 22 displays the simulation results for the full-wave rectifier using the TT, best, and worst corners for both schematic and post-layout (parasitic elements).

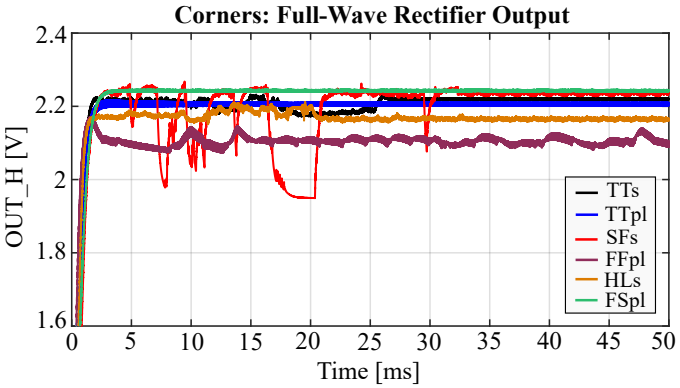

Fig. 22. Corner simulation results for both schematic and post-layout netlists.

In the case of the nominal and the best corners (TTs, TTpl, HLs, SFpl) there is a more stable behavior for the voltage in the post layout simulation, checking in both cases with a stable rectified voltage at the output of the circuit, otherwise when examining the results of the least favorable corners (SFs and FFpl) for both the schematic and layout, we observe an unstable voltage and excessive ripple, respectively.

Despite the results obtained in the SFs and FFpl corners, which suggest that the rectifier block could be improved in some cases, it can be stated that in most cases it fulfills its design purpose.

To improve the performance of the block in the most unfavorable corners, alternatives could be explored, such as increasing the capacitance at the output of the rectifier to decrease the ripple present in the voltage. However, this decision increases the final area of the block, which could interfere with the energy received by the antenna.

C. Voltage Limiter

Fig. 23 depicts the layout of the voltage limiter. We used interdigitation and serpentine resistors as layout techniques. The layout occupies an area of 1570 μm^2.

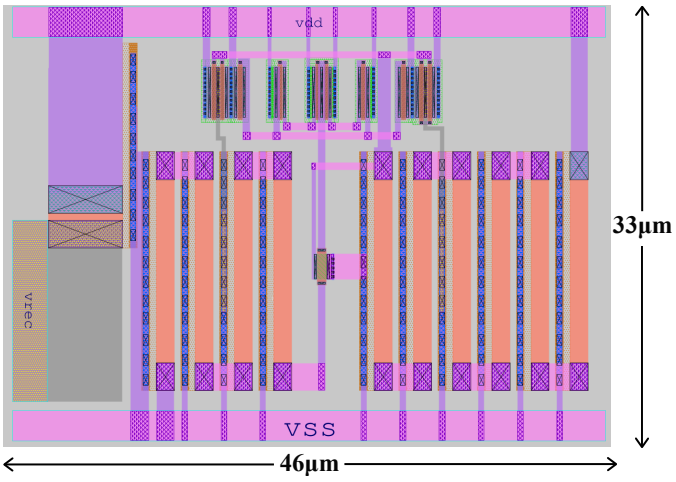

Fig. 23. Voltage Limiter layout using Magic.

A DC-sweep simulation from 0 V to 3 V was used to verify the performance of the Voltage Limiter. The simulation results for both the schematic and the post-layout netlists use TT, best, and worst corners, as presented in Fig. 29.

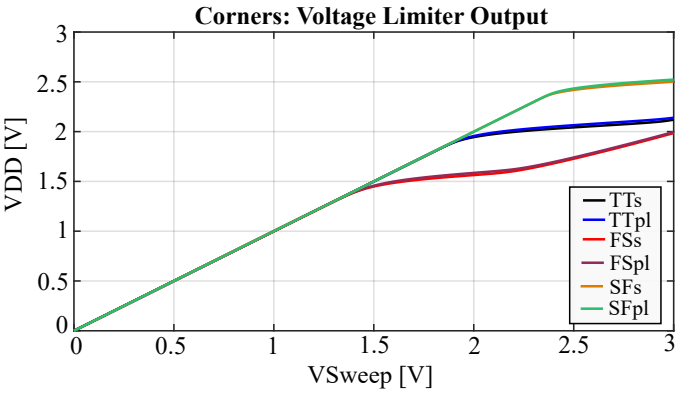

Fig. 24. Corner simulation results of the Voltage Limiter for both schematic and post-layout netlists.

The results indicate that the desired behavior is achieved for corner TT (both schematic and layout), with the voltage achieving the value of 1.8 V. However, this same behavior is not observed for the FS and SF corners. In future work, a calibration for this block could be developed to ensure that all corners perform as expected.

D. Temperature Sensor

For the layout of the Temperature Sensor, we implement the interdigitation technique. The layout is shown in Fig. 25, and occupies an area of 1480 µm^2.

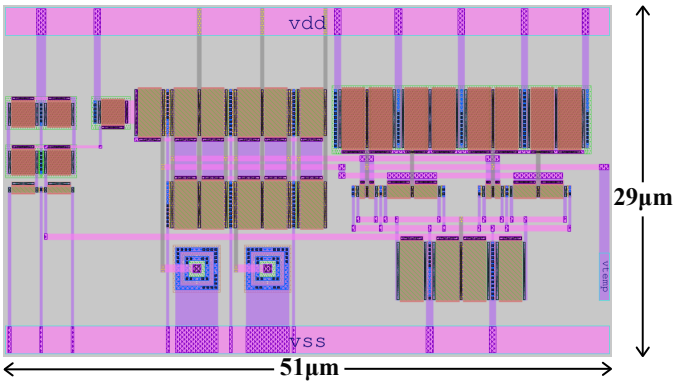

Fig. 25. Temperature Sensor layout using Magic.

A DC simulation of the temperature was implemented from 0°C to 100°C to verify the performance of the Temperature Sensor. Fig. 29 presents the results of the simulation for both the schematic and post-layout netlists using the TT, best and worst corners.

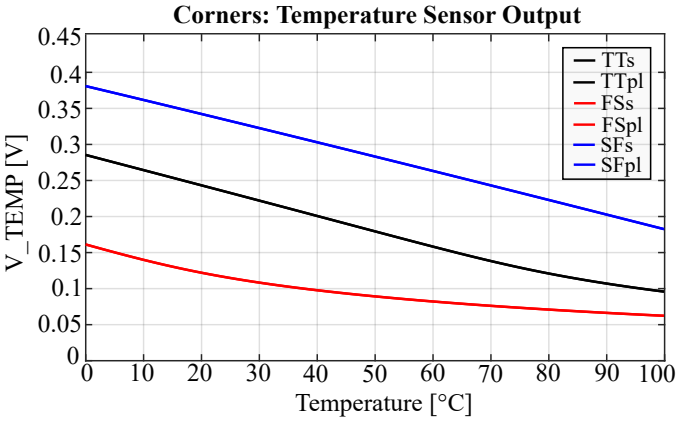

Fig. 26. Corner simulation results of the Temperature Sensor for both schematic and post-layout netlists.

Based on the results obtained, it can be concluded that the temperature sensor performs as expected, with a linear response observed in all corners.

E. Ring Oscillator

Fig. 27 depicts the Ring Oscillator layout. During the implementation phase of the layout, it was important to ensure that the distance of the connections between the inputs and outputs of the different inverters is the same to achieve similar propagation times. The layout has an area of 773 µm^2.

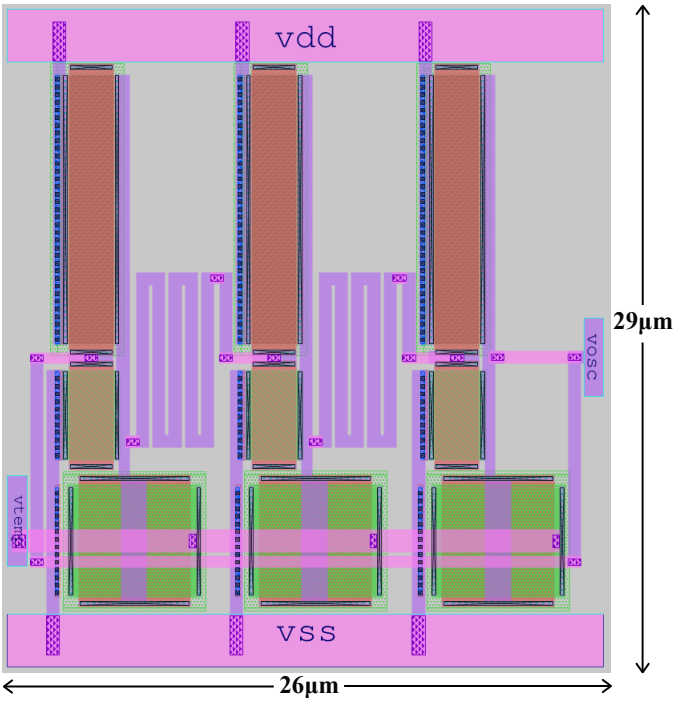

Fig. 27. Ring Oscillator layout using Magic.

To characterize and verify the performance of the ring oscillator, we run a DC simulation that presented the oscillation frequency as a function of the control voltage V_TEMP. With this DC simulation, we identified the frequency range covered by the output voltage of the Temperature Sensor. The simulation results for both the schematic and the post-layout netlists using TT, best, and worst corners are presented in Fig. 29.

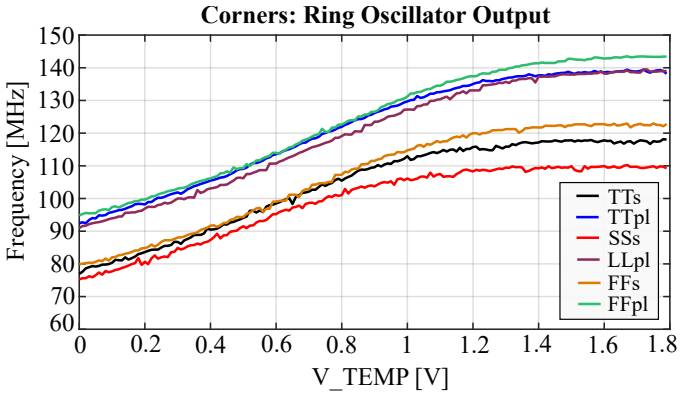

Fig. 28. Corners of Voltage Limiter: Schematic and post-layout results.

Finally, the frequency range of the Ring oscillator for the schematic is 7.5 MHz [81.3882 MHz, 85 MHz], whereas for post-layout results the range is 6.484 MHz [97.29 MHz, 97.29 MHz].

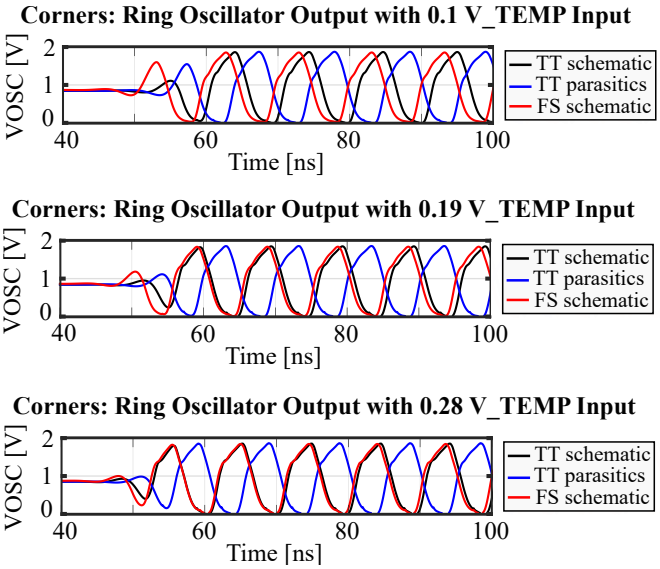

Fig. 29. Corners of Voltage Limiter: Schematic and post-layout netlists.

F. Switch for Load Modulation

Regarding the performance behavior, it was not possible to verify its operation due to the lack of pdk components that facilitate the simulation of an inductive link. Still, we believe that the switch will correctly connect and disconnect the pins of the resonator to backscatter the information at the ring oscillator frequency. Fig. 30 presents the layout area, which is 66 μm^2.

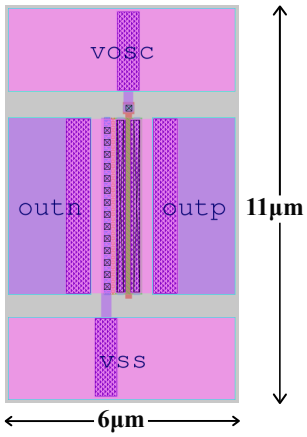

Fig. 30. Load Modulation layout using Magic.

G. RFID Tag

Regarding the performance of the entire system, a transient simulation with a 0.45 V sinusoidal source connected to the input of the rectifier to emulate the inductive link was defined. Simulation results of the rectifier output are illustrated in Fig. 31. The response was as expected for most of the corners, except for the SF corner, where the mobility of the NMOS transistors is lower than the typical resulting in the worst performance for the block.

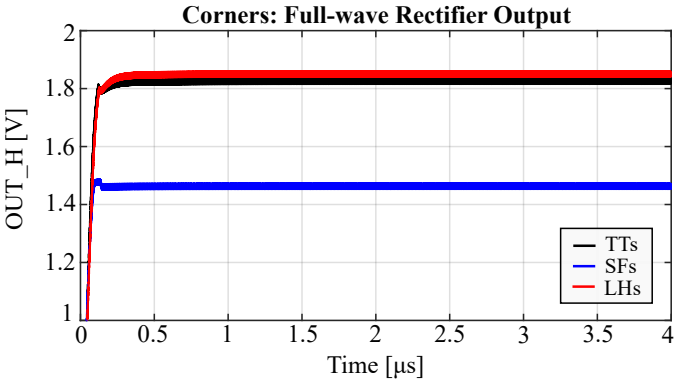

Fig. 31. Simulation of Full-wave rectifier corners in the complete system.

The results from the Voltage Limiter output are displayed in Fig. 32. During the entire operation, the voltage remains steady and close to 1.8 V, with no significant ripple for the majority of the corner cases. However, similar to the rectifier, the SF corner does not reach the expected voltage, which is a consequence of the output voltage at the rectifier stage.

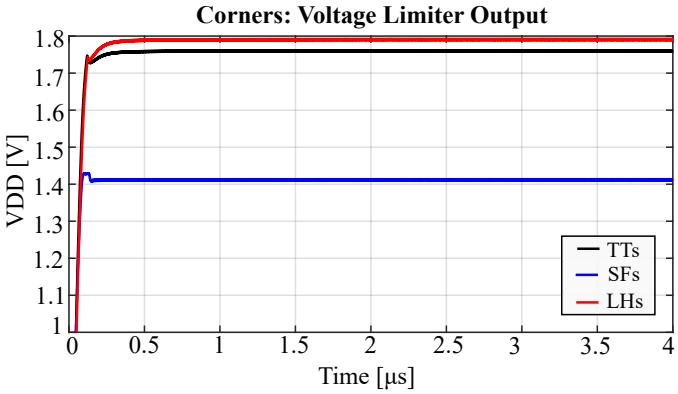

Fig. 32. Simulation of Voltage Limiter corners in the complete system.

To simulate the load, a test bench was implemented with a temperature sweep from 0°C to 100°C. The results of the temperature sensor are shown in Fig. 33. The temperature sensor exhibits the expected linear behavior and a desired linear voltage range. Nonetheless, it is worth mentioning that the FS corner has the least voltage range and consequently the worst performance among the different corners.

The ring oscillator was simulated by performing a frequency simulation versus the control voltage V_TEMP. Fig. 34 displays the results, which show a desirable response. In the TT corner, a frequency differentiation of 6 MHz was achieved, which is very similar to the result in the SS corner. However, the FF corner has a reduced frequency range of 5 MHz.

Finally, the RFID tag layout is shown in Fig. 35. It has an area of approximately 10 mm^2.

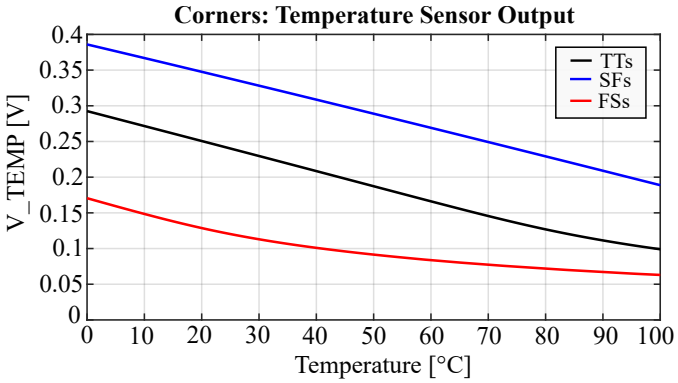

Fig. 33. Simulation of Temperature Sensor corners in the complete system.

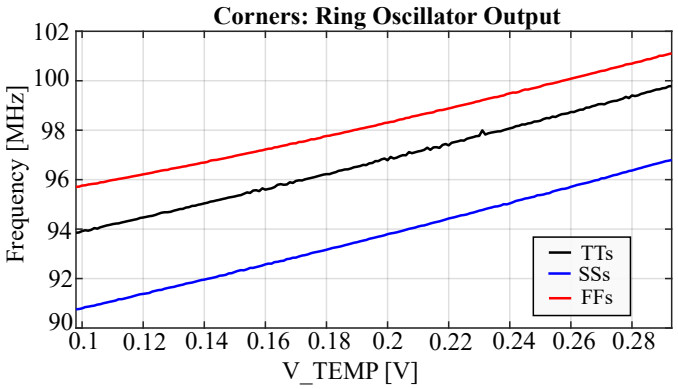

Fig. 34. Simulation of Ring Oscillator corners in the complete system.

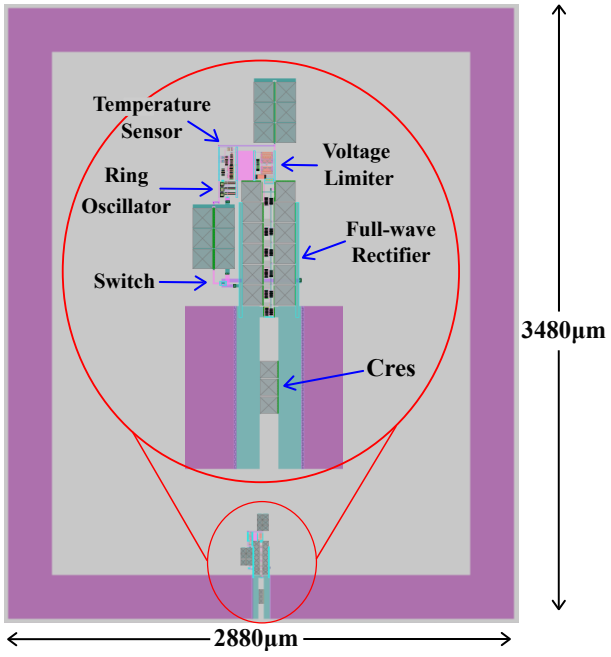

Fig. 35. RFID Tag Layout performed in Magic.

V. Conclusions

This project presents a block design for a fully-integrated RFID tag with the SkyWater130 open-access technology node. The tag includes an integrated antenna and a temperature sensor with a measurement range of 0°C to 100°C. It operates in a frequency range from 905 MHz to 935 MHz, making it suitable to be used according to Colombian regulations. The compact design of the tag could be implemented in several applications since the entire chip measures only 3.2 x 5.3 mm. This research project represents an important step in the development of RFID tags using open-access technology such as SkyWater130. The resulting device is now available to the community.

While the expected results were achieved in all blocks, future work may involve calibration of circuits where to compensate for the corner that does not achieve the desired specification.

Acknowledgment

We would like to express our sincerest gratitude to all the individuals who have contributed to the development of this research. As Isaac Newton once said, "If I have seen further, it is by standing on the shoulders of giants." Indeed, the giants to whom he referred are closer to us than we may imagine. They are our families, professors, OnChip Research Group, and friends, who inspire us day in and day out. They encourage us to pursue our passions, challenge us to think critically, and lift us up when we falter. Without their guidance, advice, and support, this work would not have been possible. We are truly grateful for their mentorship and inspiration, which have helped us to see further and strive for excellence in our research.

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