Electrical Rules Check Report

Class	Document	Message
Warning	Main.SchDoc	Unconnected Port Analog0 at 2800mil,7200mil
Warning	Main.SchDoc	Unconnected Port Analog1 at 2800mil,7100mil
Warning	Main.SchDoc	Unconnected Port Analog2 at 2800mil,7000mil
Warning	Main.SchDoc	Unconnected Port Analog3 at 2800mil,6900mil
Warning	Main.SchDoc	Unconnected Port Boot0 at 2300mil,5800mil
Warning	Main.SchDoc	Unconnected Port GP15 at 6700mil,6900mil
Warning	Main.SchDoc	Unconnected Port I2C_SCL at 6700mil,6400mil
Warning	Main.SchDoc	Unconnected Port I2C_SDA at 6700mil,6300mil
Warning	Main.SchDoc	Unconnected Port SPI-CLK at 2800mil,6700mil
Warning	Main.SchDoc	Unconnected Port SPI-CS1 at 2800mil,6800mil
Warning	Main.SchDoc	Unconnected Port SPI-CS2 at 6700mil,7200mil
Warning	Main.SchDoc	Unconnected Port SPI-CS3 at 6700mil,7100mil
Warning	Main.SchDoc	Unconnected Port SPI-CS4 at 6700mil,7000mil
Warning	Main.SchDoc	Unconnected Port SPI-MISO at 2800mil,6500mil
Warning	Main.SchDoc	Unconnected Port SPI-MOSI at 2800mil,6600mil
Warning	Main.SchDoc	Unconnected Port SWCLK at 2900mil,5800mil
Warning	Main.SchDoc	Unconnected Port SWDIO at 2900mil,5900mil

Design Rules Verification Report

Filename : D:\GoogleDrive\Entwicklung\Circuitstudio_Workspace\E-Rubin_G1_Board\erb-

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.15mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.15mm) (Max=1mm) (Preferred=0.3mm) (All)	0
Width Constraint (Min=0.27mm) (Max=0.35mm) (Preferred=0.35mm) (InNetClass('SD_CARD'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=50mm) (Conductor Width=2mm) (Air Gap=0.2mm) (Entries=4)	0
Minimum Annular Ring (Minimum=0.15mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=6mm) (All)	0
Hole To Hole Clearance (Gap=0.2mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=500mm) (Prefered=12.7mm) (All)	0
Total	0