Electrical Rules Check Report

Class	Document	Message
		Successful Compile for G-Base-1.PrjPcb

Design Rules Verification Report

Filename : D:\GoogleDrive\Entwicklung\Circuitstudio_Workspace\E-Rubin_G1_Board_Bas

Warnings 0
Rule Violations 2

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.15mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.14mm) (Max=1mm) (Preferred=0.2mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=6mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	1
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	1
Board Clearance Constraint (Gap=0mm) (OnLayer('Top Overlay'))	0
Board Clearance Constraint (Gap=0mm) (IsText)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Component Clearance Constraint (Horizontal Gap = 0mm, Vertical Gap = 0mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=100mm) (Prefered=12.7mm) (All)	0
Total	2

Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.081mm < 0.1mm) Between Pad C5-2(88.9mm,42.55mm) on Top Layer And Pad VR1-3(90.3mm,41.8mm)

Net Antennae (Tolerance=0mm) (All)
Net Antennae: Track (91.519mm,21.481mm)(92.257mm,20.743mm) on Mid-Layer 2