CS 341 Assignment 3

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Contents

1 5 Stage, without forwarding or hazard detection

Code

```
.text

main:
    addi s0 zero 5
    add s1 s0 zero
```

Behaviour

Expectation: At the end of the program, we expect registers `s0` and `s1` to have value 5.
Reality: At the end of the program, only register `s0` has value 5. (`s1` is default to 0)

Explanation

The incorrect value is due to data hazard.
To be more specific, we face a **read-before-write (RAW) data hazard**.
`addi s0 zero 5` writes to register `s0` in WB stage during 4th cycle.
`add s1 s0 zero` reads from register `s0` in ID stage during 2nd cycle.
The value read here is not updated yet causing the incorrect computation.

Screenshots

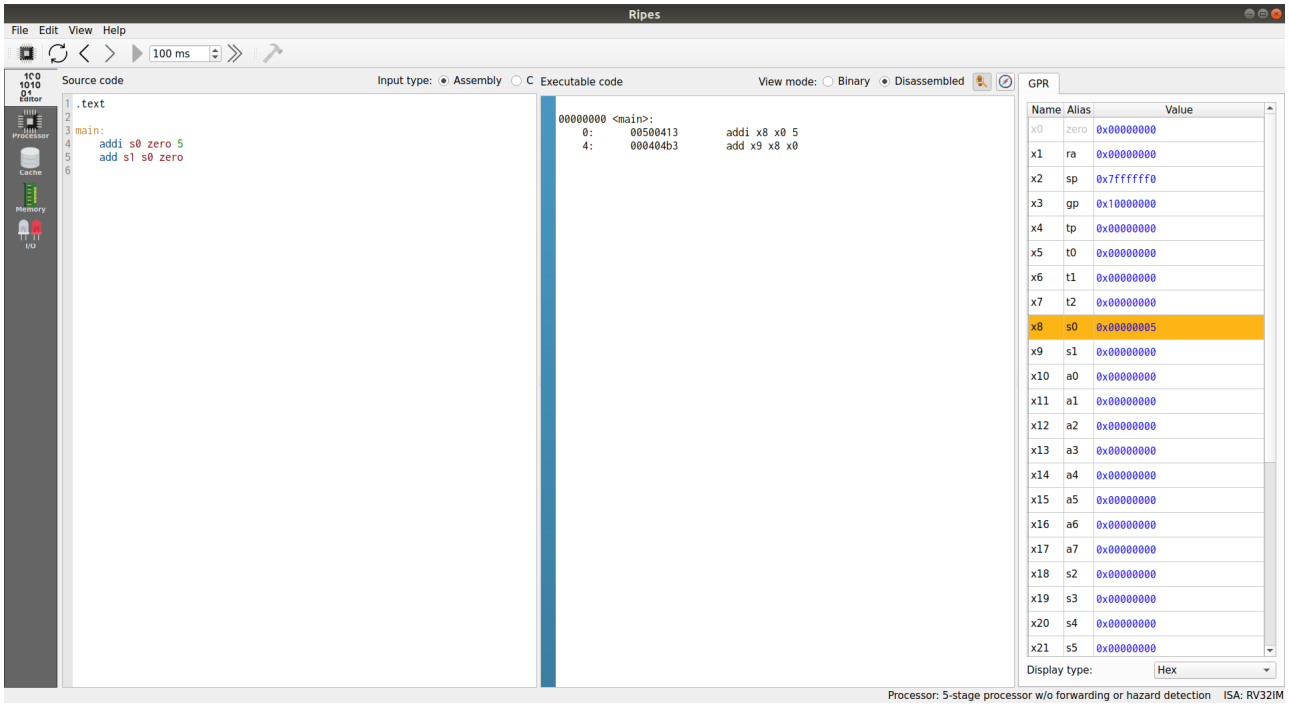

Figure 1: Without hazard detection; Without forwarding;

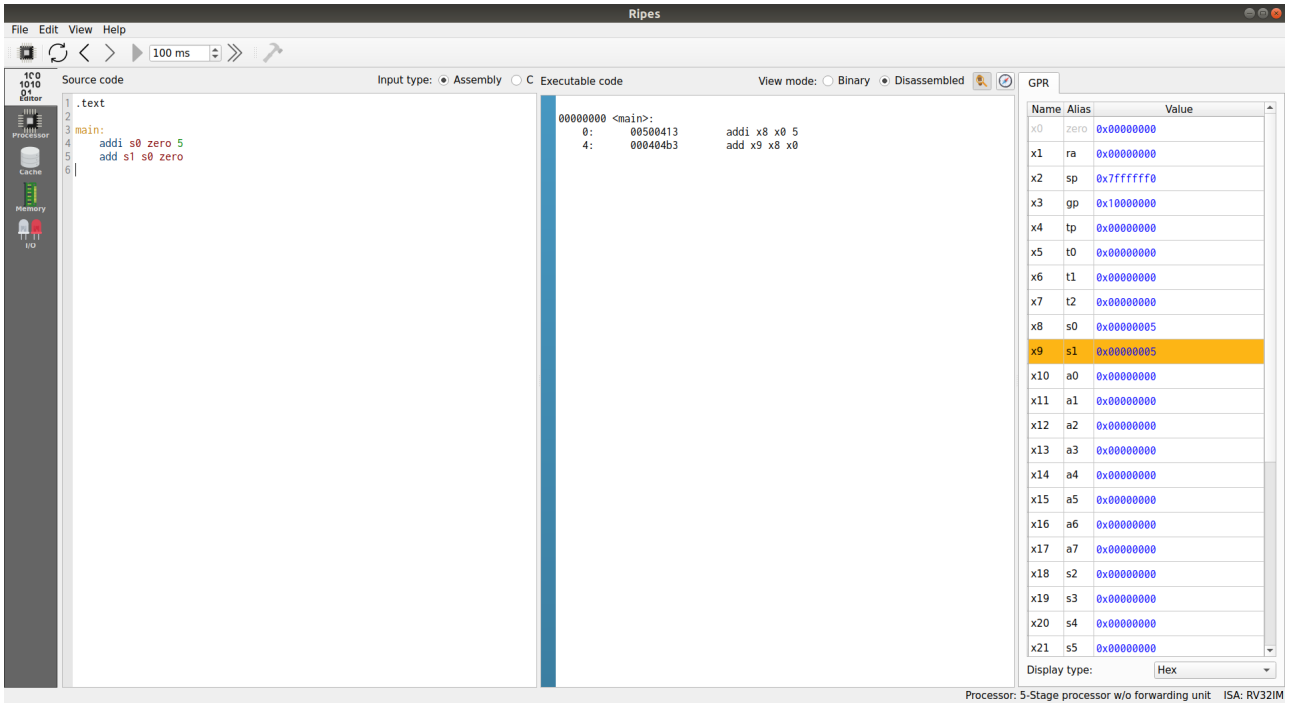

Figure 2: With hazard detection; Without forwarding;

2 5 Stage, without forwarding, with hazard detection

a.

Code

```
.text

main:
    addi s0 zero 5
    add s1 s0 zero
```

Behaviour

At the end of the program, we expect registers `s0` and `s1` to have value 5.
Without forwarding, we observe that ID for second instruction takes 3 cycles (2 stalls).
There are no stalls with forwarding.

Screenshots

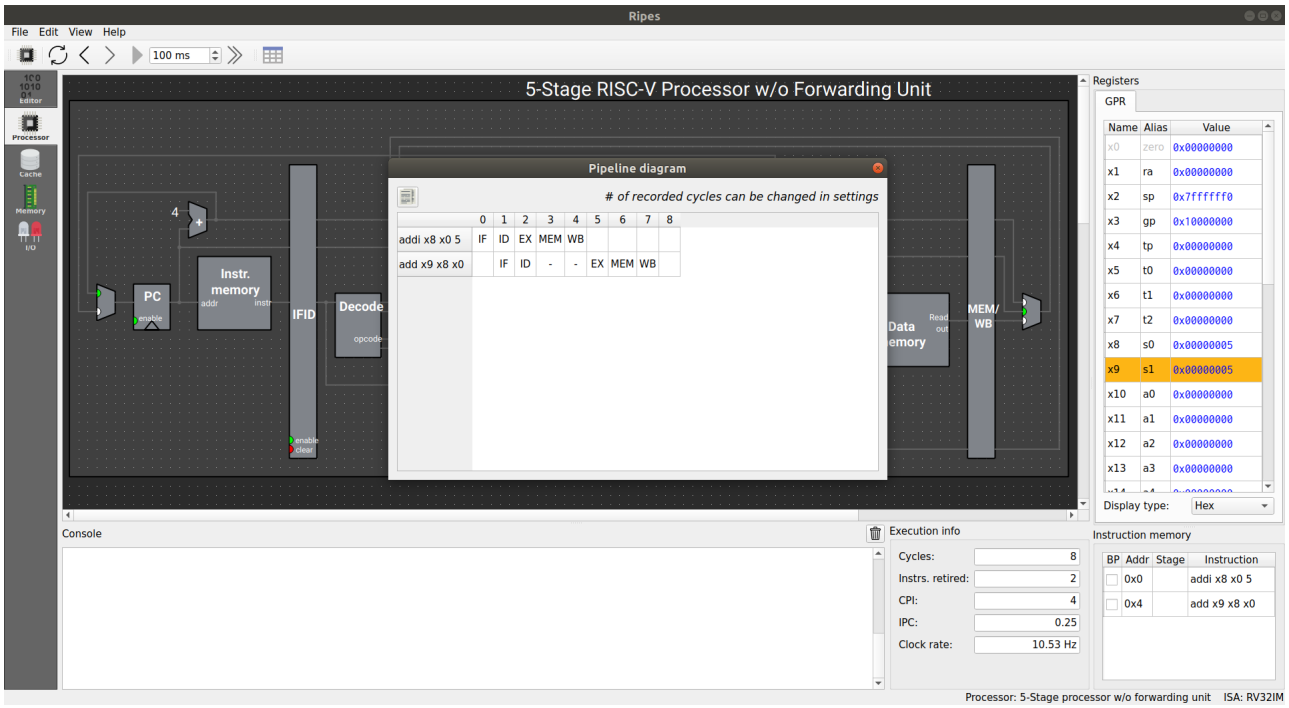

Figure 3: With hazard detection; Without forwarding;

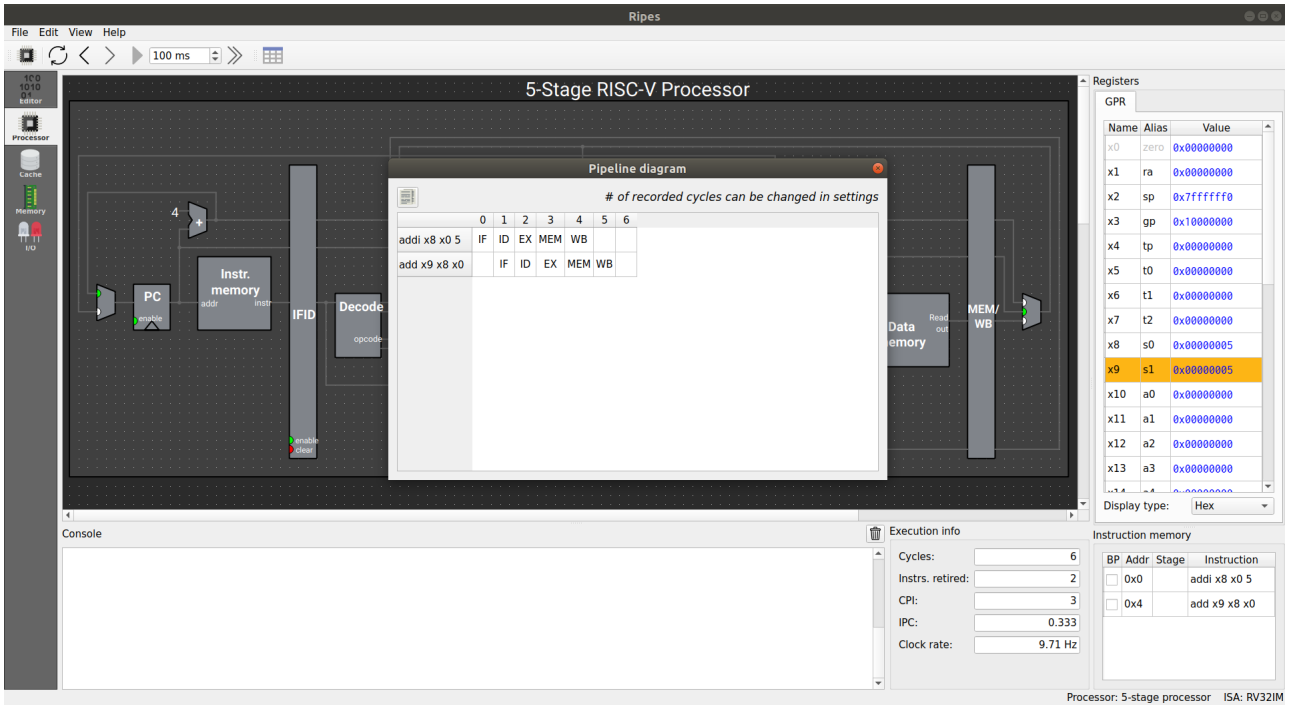

Figure 4: With hazard detection; With forwarding;

b.

Initial Code

```
.text

main:
    addi s0 zero 5
    add s1 s0 zero
    addi s2 zero 6
    addi s3 zero 7
```

Optimized Code

```
.text

main:
    addi s0 zero 5
    addi s2 zero 6
    addi s3 zero 7
    add s1 s0 zero
```

Behaviour

At the end of both the program, we expect registers `s0` and `s1` to have value 5, register `s2` to have value 6 and, register `s3` to have value 7.

Screenshots

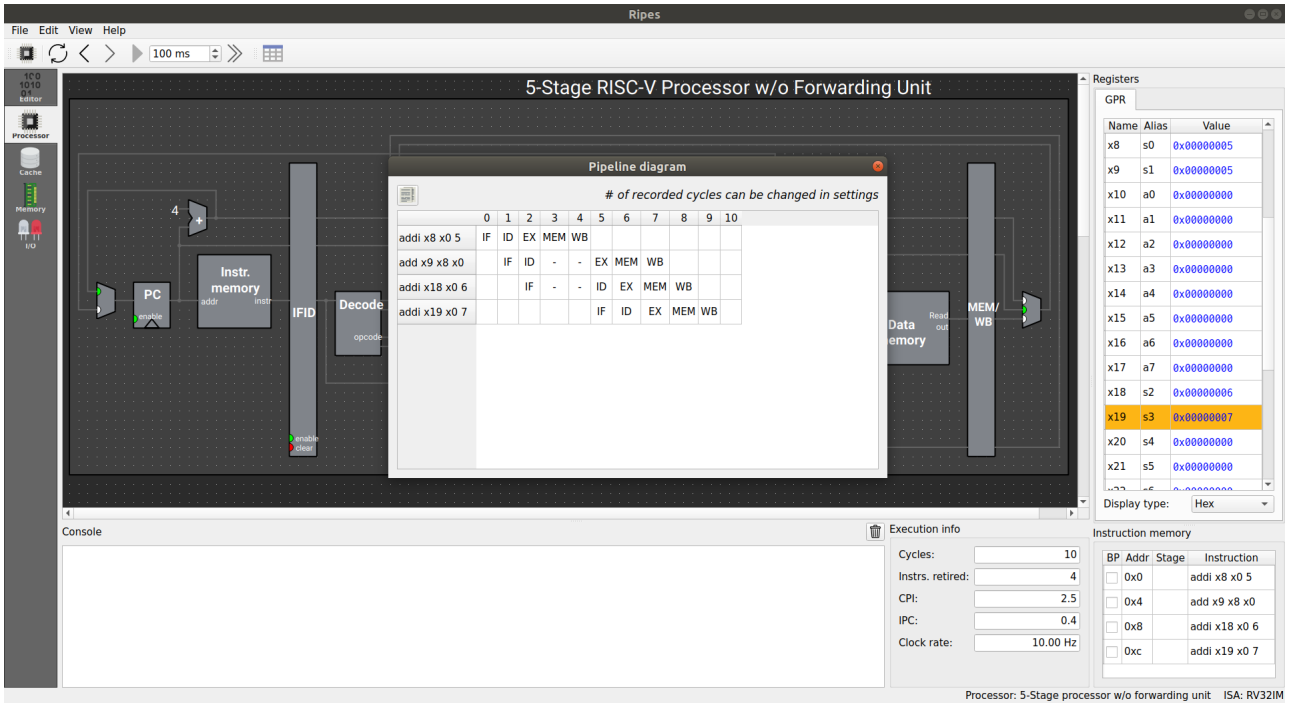

Figure 5: With hazard detection; Without forwarding; Initial code

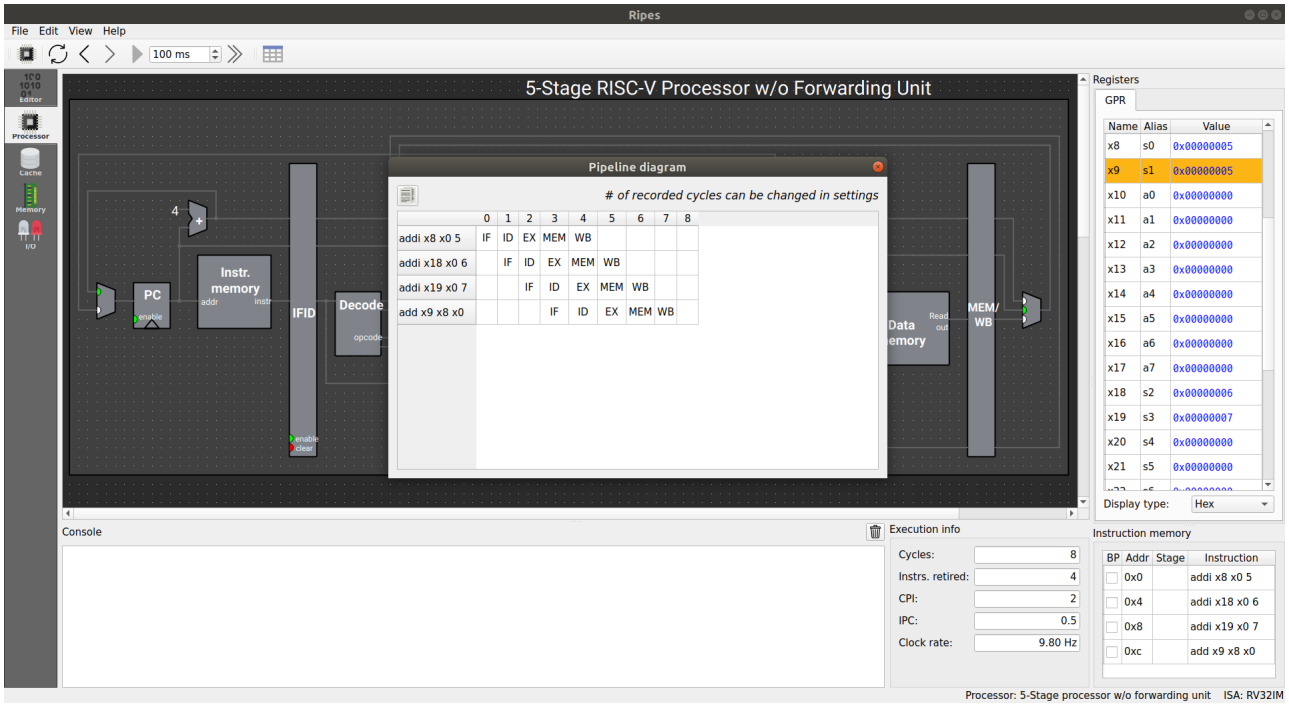

Figure 6: With hazard detection; With forwarding; Optimized code

3 Stalls and Forwarding

a.

Address input of data memory and EX/MEM pipeline after 4th cycle is `0x0000000a`.

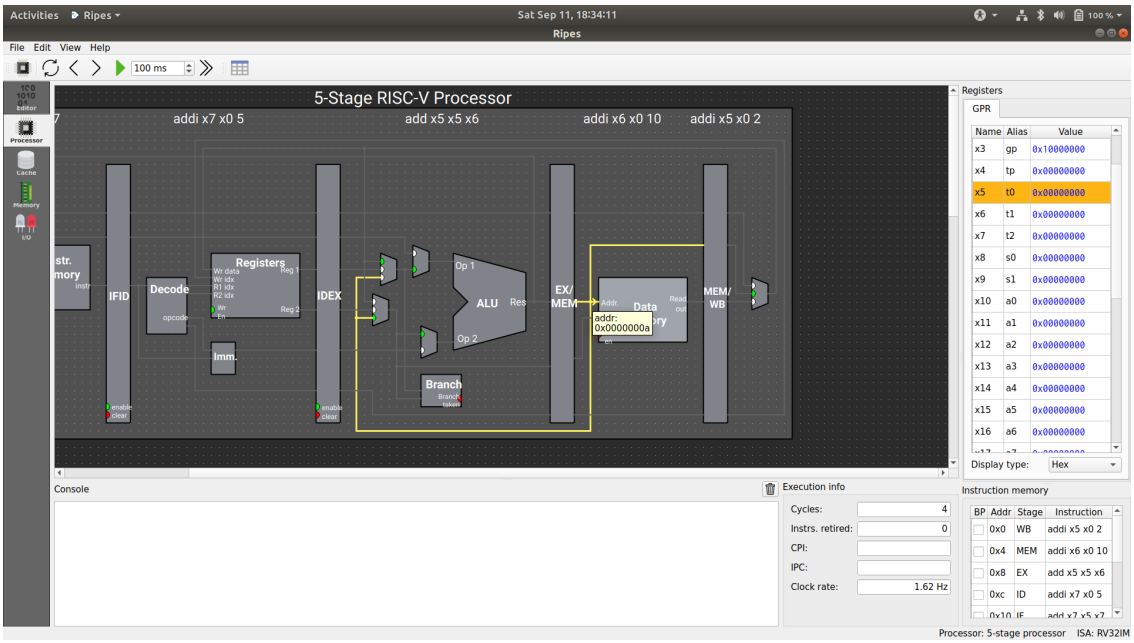

Figure 7: With hazard detection; With forwarding;

b.

R2 idx input of registers block and decoder after 10th cycle is `0x01`.

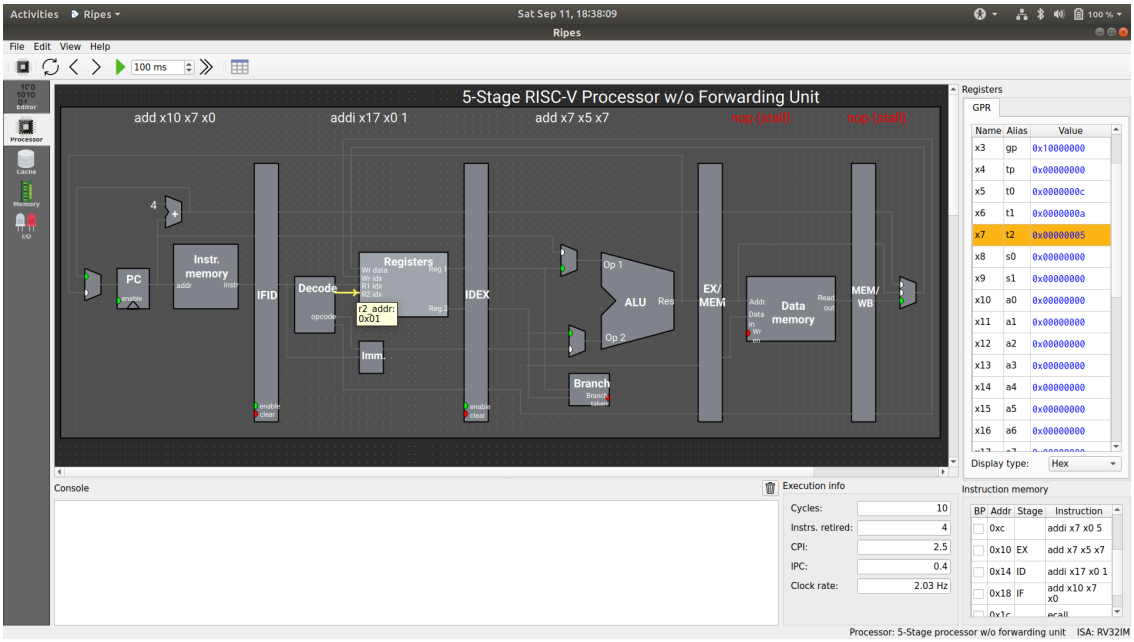

Figure 8: With hazard detection; Without forwarding;

c.

The value stored in `opcode_exec_out` datapath after 4 cycles is `0x13`.

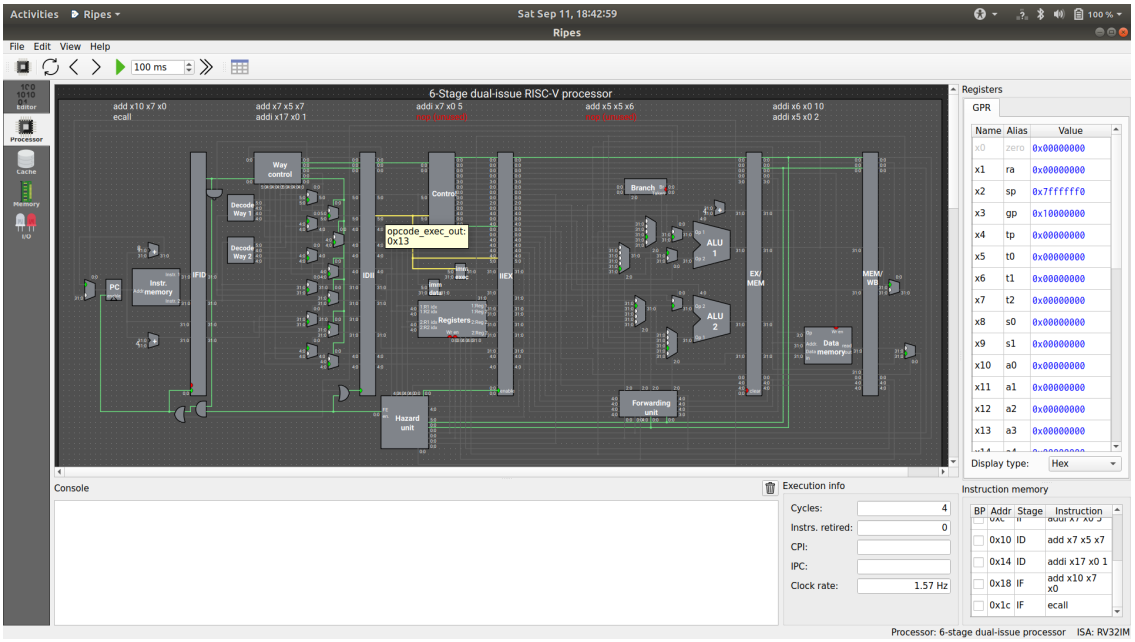

Figure 9: 6-stage dual-issue processor

d.

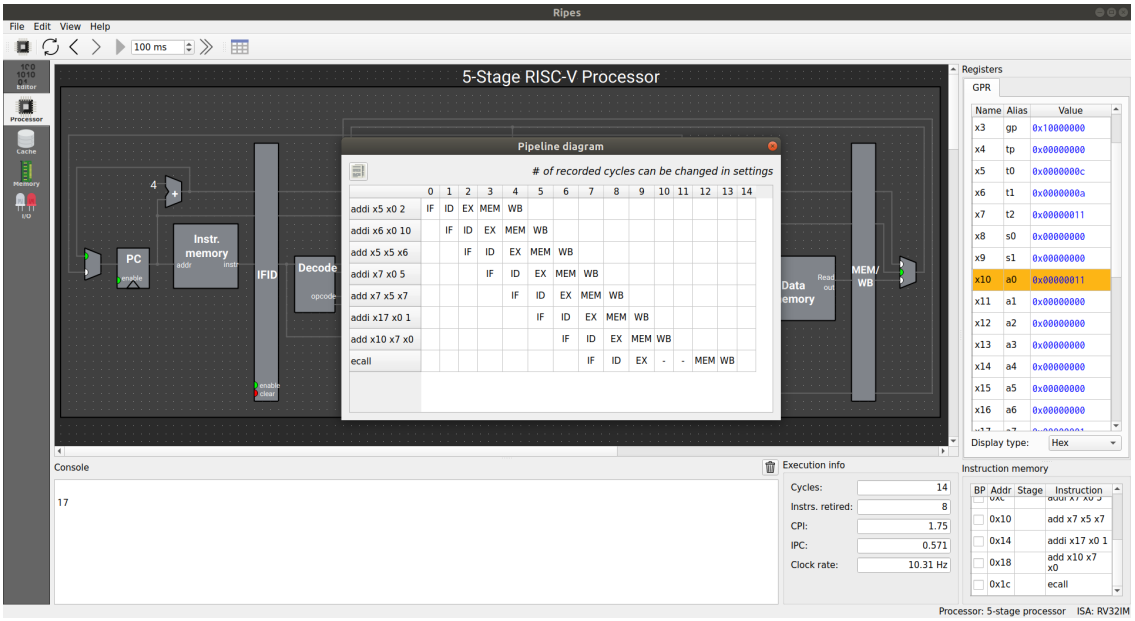

Figure 10: With hazard detection; With forwarding; **Takes 14 cycles**

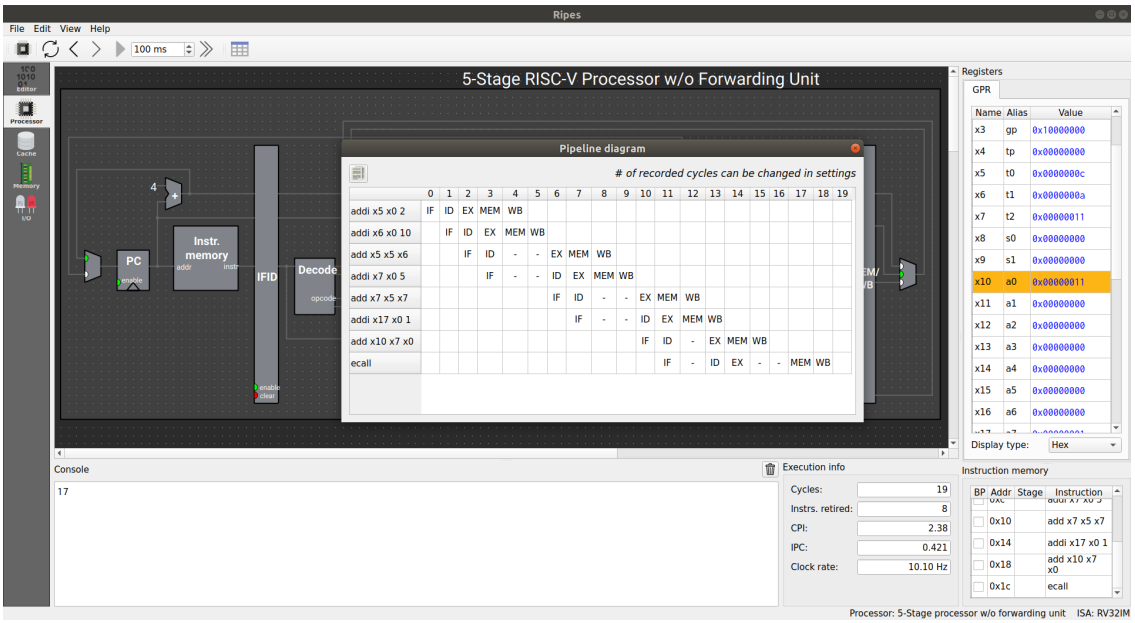

Figure 11: With hazard detection; Without forwarding; **Takes 19 cycles**

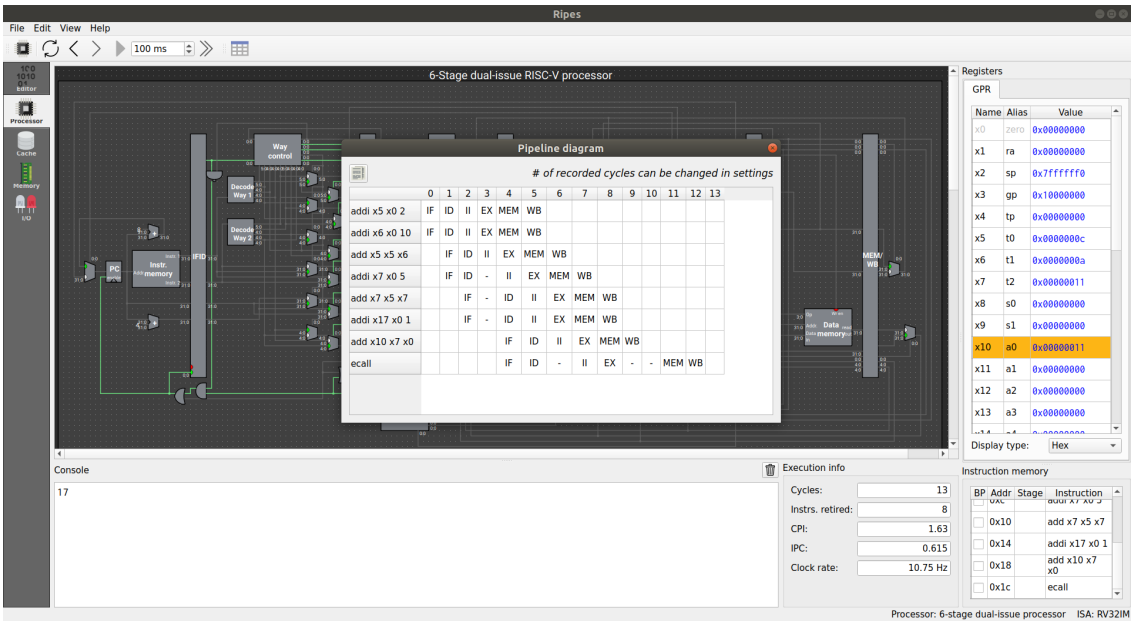

Figure 12: 6-stage dual-issue processor; **Takes 13 cycles**