Implementation of Dual Active Bridge Converter with Single Phase Shift

Devarsh Bhandari 220102032

Department of Electrical Engineering, IIT Guwahati

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Abstract

This report presents the implementation of a Dual Active Bridge converter using given parameters, focusing on controlling power flow in the desired direction with the help of pulses. This report focuses on the simplest case—Single Phase Shift (SPS)—to control power flow.

1 Introduction

1.1 What is the Dual Active Bridge Converter?

A Dual Active Bridge (DAB) converter is a DC-DC voltage converter capable of bidirectional power flow, meaning power can flow from either side depending on the nature of the pulses provided by the control circuit. The conversion process involves transforming DC to AC using an H-bridge, then converting AC to AC through a high-frequency transformer, and finally converting it back to DC using another H-bridge. One of the common applications of the DAB converter is in electric vehicle (EV) charging systems.

1.2 What is Single Phase Shift?

There are various degrees of freedom in the given set-up:

1. The phase shift between the two individual legs of the H-bridge.
2. The phase shift between the pulse trains of the primary-side H-bridge and the secondary-side H-bridge.

In Single Phase Shift (SPS) control, the first degree of freedom is restricted, which means the opposite legs operate in a complementary fashion with a duty ratio of 50%. The control strategy focuses on the second parameter to manage the power transfer through the transformer.

1.3 Advantages

1. **Bidirectional Power Flow**
   The DAB converter supports power flow in both directions, making it ideal for charging and discharging applications such as battery energy storage systems and charging of electric vehicles.

2. **Electrical Isolation**
   The control circuit and the main power circuit are electrically isolated from each other. This ensures that even if a fault or short circuit occurs in the main power circuit, the control circuit remains unaffected, preserving the integrity of typically more expensive control components.

2 Theory

2.1 Basic Functioning of Power Flow

The Dual Active Bridge (DAB) converter operates on the principle of transferring power between two DC sources using a high-frequency AC link formed through transformer isolation. The converter uses two H-bridge inverters—one on the primary side and one on the secondary side—connected through a high-frequency transformer and a leakage inductance.

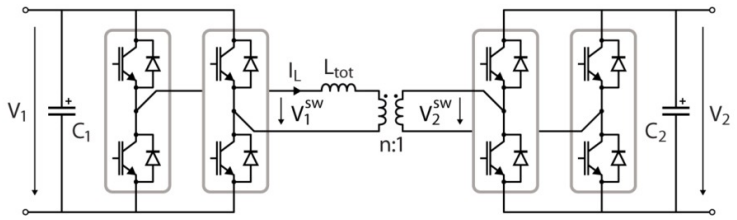


Figure 1: Dual Active Bridge Converter

The key control mechanism for power flow in the DAB is the phase shift between the voltage waveforms generated by the two H-bridges. By introducing a phase shift ϕ, a voltage difference is created across the leakage inductance, which drives current from one side to the other, allowing bidirectional power transfer. The direction and magnitude of power flow are determined by the polarity and extent of this phase shift.

2.2 Functioning of H Bridge

2.2.1 Components

Each H-bridge typically includes:

- Four MOSFETs (or IGBTs for higher power applications)
- Gate driver circuits for each switch (Optocoupler)
- Snubber circuits across switches to reduce voltage spikes
- A heatsink for thermal management

- Isolated DC-DC converter
- Inputs for DC voltage
- Inputs for Power supply for DC to DC converter
- Capacitors

1. **N-MOSFET (IXFH96N20P)**: This MOSFET can block voltages up to 200V and conduct currents up to 96A with an on-state resistance of 18 mΩ, making it suitable for our circuit. According to the datasheet, the gate-source voltage V_{gs} required to turn the MOSFET on lies between 15V and 18V. In power electronics, MOSFETs mostly function as switches, operating in the cutoff and saturation regions.

2. **Gate Driver – Optocoupler (HCPL-3120-000E)**: The controller circuit (FPGA) cannot supply gate pulses of 15V, as it outputs signals at 0–3.3V levels. This requirement is fulfilled by using an optocoupler-based gate driver. Internally, the optocoupler contains an LED that emits light when current flows, which activates a phototransistor or driver circuit on the output side, enabling the gate drive signal.

   This arrangement provides electrical isolation between the control circuit and the main power circuit, protecting the FPGA from high voltage damage. The diode inside the optocoupler requires a forward voltage drop of 1.6V–1.8V and a current of 10–12 mA. Given the FPGA output of 3.3V, an external resistor is used to achieve the required current:
   $$R = \frac{3.3\,\mathrm{V} - 1.6\,\mathrm{V}}{10\,\mathrm{mA}} = 180\,\Omega$$

3. **Snubber Circuit**: A snubber circuit (usually a diode or RC network) is employed to prevent high current spikes during switching. During the deadtime interval—when both legs of the H-bridge are off to avoid shoot-through—no path is available for the inductor current. This causes a rapid voltage rise across the inductor, possibly leading to component damage.

   Snubber circuits provide an alternate path for the inductor current, allowing it to decay gradually and preventing large voltage spikes. Although modern MOSFETs generally include internal body diodes to manage reverse currents, an external snubber is still recommended for added protection.

4. **Heat Sink**: High currents through the MOSFETs generate significant heat. To prevent thermal damage, heat sinks are attached to dissipate the excess heat effectively.

5. **Isolated DC-DC Converter (MGJ2D121509SC)**: MOSFET requires gate pulses of +15V referenced to its source terminal, which often floats and cannot be grounded directly. The isolated DC-DC converter solves this by generating $V_{CC} = +15\,\mathrm{V}$ and $V_{EE} = -8\,\mathrm{V}$ with respect to the floating source. These voltages are supplied to the optocoupler gate driver, applying V_{CC} during the ON state and V_{EE} during the OFF state.

6. **DC Input Voltage**: This is the input supply provided during the experiment. The permissible voltage is limited by:

- Voltage rating of the inductor: $V_{in} + V_{out}$
- Voltage rating of the transformer: V_{out}
- Voltage rating of the MOSFETs: V_{in}

The minimum of these three values determines the safe input voltage.

7. **Power Supply**: The isolated DC-DC converters require a dedicated power supply, which is provided as a 12V input in our case.

8. **Capacitors**: To filter out voltage ripples from the DC input and power supply lines, capacitors of suitable ratings are added to stabilize the voltage and ensure smooth operation.

2.2.2 Working

Let's denote the MOSFETs in one H-bridge as A, B, C, D, where A and B belong to the same leg, and C and D form the diagonal counterparts. At any given time, current can flow through the H-bridge only via diagonally placed MOSFETs. If both MOSFETs from the same leg (e.g., A and B) are turned on simultaneously, it would short the circuit and potentially cause damage.

When A and C are turned on, current flows from A through the load and returns via C. Alternatively, when D and B are on, current flows in the reverse direction—through D to the load and back via B.

This alternating switching action continuously changes the polarity across the inductor and transformer, effectively converting the DC input into an AC waveform.

A similar switching process occurs at the secondary-side H-bridge, with MOSFETs labeled A', B', C', D'. However, the key difference is that the gate pulses on the secondary side are phase-shifted by a certain amount of time. This phase shift ensures that the output current flows predominantly in a single direction, thereby converting the AC waveform back into DC on the secondary side.

2.3 Leakage Inductance

The leakage inductance, typically denoted as L, plays a crucial role in energy transfer and power control in a Dual Active Bridge (DAB) converter. The inductor stores energy and helps maintain the voltage difference that may arise due to mismatches in voltage, thereby safeguarding the circuit against potential faults or transients.

This inductance can either be the intrinsic leakage inductance of the transformer or an external inductor deliberately added in series. However, it is generally recommended to introduce a separate inductor, as the intrinsic leakage inductance is often too low to provide adequate control over the power flow.

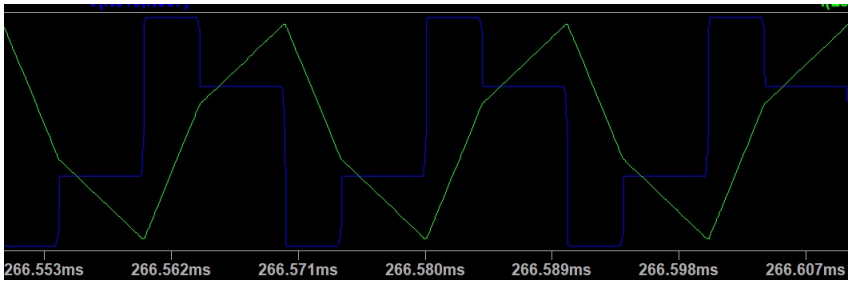


Figure 2: Current(green) and Voltage(blue) waveform

Over a short time span, the relationship between current and time is linear for a constant voltage, which results in the observed waveform.

2.4 Transformer

The transformer in the DAB converter serves two primary purposes: voltage level matching and galvanic isolation. Operating at high frequency, the transformer facilitates voltage transfer based on the turns ratio relation:

$$\frac{N_1}{N_2} = \frac{V_1}{V_2}$$

We have used a transformer with specifications of 0–100V on both primary and secondary sides, a current rating of 8A, and a power rating of 800W. The core material used is ferrite.

In the ideal design, the turns ratio n is derived from the equation:

$$n = \frac{V_{\text{in}}}{V_{\text{out}}}$$

This ratio is optimal for minimizing core losses due to current. However, such a design can also result in higher current spikes in the event of any design inaccuracies. To avoid these potential issues, we were advised to use a transformer with a 1:1 turns ratio.

2.5 Output R and C

At the output of the secondary H-bridge, a resistive load R (rheostat) and a capacitor C are connected. In the practical application, a DC voltage is connected to the other side as well. However, a resistive load is sufficient to show the power flow in one direction successfully , while the capacitor is used to smooth out the voltage ripple caused by the switching operation.

- The resistor R is calculated based on desired output power and voltage using the relation $R = \frac{V_{\text{out}}^2}{P}$.
- The capacitor C is selected to minimize output ripple. In our case, $C = 1\,\text{mF}$ is sufficient for maintaining a stable DC output.

2.6 Controller Circuit for Pulses (FPGA)

The generation of gate signals for the H-bridges is handled by a control circuit implemented on an FPGA (Field Programmable Gate Array). The FPGA is programmed to produce complementary pulse signals with a specific switching frequency (50 kHz in our case) and a programmable phase shift.

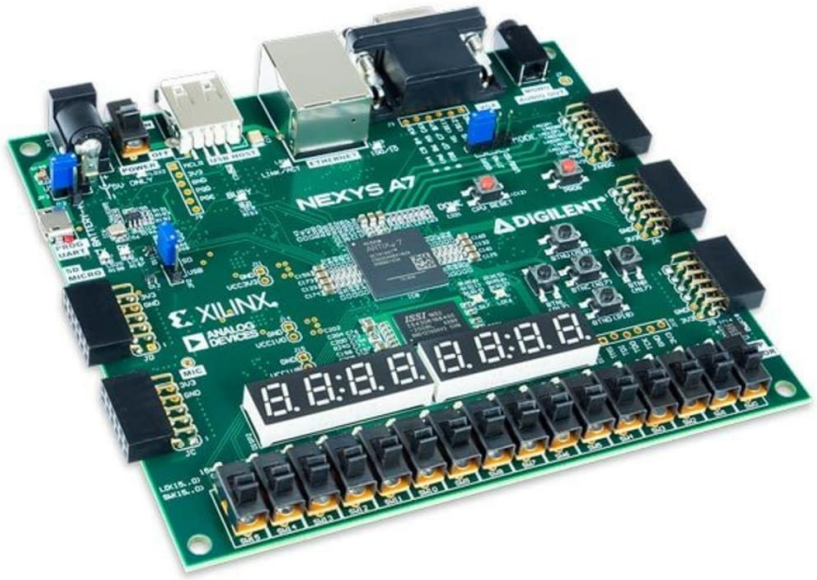


Figure 3: Nexys A7 100T

This phase shift determines the power flow direction and magnitude. Additionally, the FPGA provides precise timing control, including the insertion of dead time ($k = 0.25\,\mu$s) to prevent shoot-through in the H-bridge switches. In a closed-loop system, the FPGA may also take feedback from the output voltage to adjust the phase shift dynamically for regulation.

This FPGA provides a timing precision of up to 10 ns, which is sufficient for our application. The I/O ports of the FPGA operate at 3.3V and are programmable. Below is a sample design written in Verilog, implemented using Xilinx Vivado:

```
module pwm_3(
    input clk, rst,
    output led1, led3,
    output led2, led4,
    output leda, ledc,
    output ledb, ledd
);

localparam deadtime = 974, onduty = 999, startanother = 399;

reg [30:0] counter, counter2, st_counter;
reg led1_next, led2_next, led3_next, led4_next;
reg leda_next, ledb_next, ledc_next, ledd_next;
reg flip, flip2;
reg nexth;

always @(posedge clk) begin
```

```
18      if (rst) begin
19          led1_next <= 0;
20          led2_next <= 0;
21          led3_next <= 0;
22          led4_next <= 0;
23          leda_next <= 0;
24          ledb_next <= 0;
25          ledc_next <= 0;
26          ledd_next <= 0;
27          counter <= 0;
28          counter2 <= 0;
29          st_counter <= 0;
30          flip <= 0;
31          flip2 <= 0;
32          nexth <= 0;
33      end else begin
34          if (nexth == 0) begin
35              st_counter <= st_counter + 1;
36              if (st_counter == startanother)
37                  nexth <= 1;
38          end
39
40          if (counter == onduty) begin
41              counter <= 0;
42              flip <= ~flip;
43          end else begin
44              counter <= counter + 1;
45              if (counter >= deadtime && counter <= onduty) begin
46                  led1_next <= 0;
47                  led3_next <= 0;
48                  led2_next <= 0;
49                  led4_next <= 0;
50              end else begin
51                  if (flip == 0) begin
52                      led1_next <= 1;
53                      led3_next <= 1;
54                      led2_next <= 0;
55                      led4_next <= 0;
56                  end else begin
57                      led1_next <= 0;
58                      led3_next <= 0;
59                      led2_next <= 1;
60                      led4_next <= 1;
61                  end
62              end
63          end
64
65          if (nexth == 1) begin
66              if (counter2 == onduty) begin
67                  counter2 <= 0;
68                  flip2 <= ~flip2;
69              end else begin
70                  counter2 <= counter2 + 1;
71                  if (counter2 >= deadtime && counter2 <= onduty) begin
72                      leda_next <= 0;
73                      ledc_next <= 0;
74                      ledb_next <= 0;
75                      ledd_next <= 0;
```

```
                end else begin
                    if (flip2 == 0) begin
                        leda_next <= 1;
                        ledc_next <= 1;
                        ledb_next <= 0;
                        ledd_next <= 0;
                    end else begin
                        leda_next <= 0;
                        ledc_next <= 0;
                        ledb_next <= 1;
                        ledd_next <= 1;
                    end
                end
            end
        end
    end
end

assign led1 = led1_next;
assign led2 = led2_next;
assign led3 = led3_next;
assign led4 = led4_next;
assign leda = leda_next;
assign ledb = ledb_next;
assign ledc = ledc_next;
assign ledd = ledd_next;

endmodule
```

Listing 1: Verilog module for generating PWM signals with deadtime

3 Practical Calculations

3.1 Parameters and design specifications

We design our Dual Active Bridge (DAB) converter for a voltage step-down from 10V to 5V. This configuration can be generalized for any input and output voltage where the relationship satisfies $V_{\text{in}} = 2 \times V_{\text{out}}$.

- $V_{\text{in}} = 10\,\text{V}$ (Input Voltage)
- $V_{\text{out}} = 5\,\text{V}$ (Output Voltage)
- $L = 500\,\mu\text{H}$ (Leakage Inductance, specified in the laboratory)
- $f_s = 50\,\text{kHz}$ (Switching Frequency provided by FPGA)
- $n = 1$ (Transformer Turn Ratio)

To control power transfer, we define the phase shift duty ratio D, which is expressed as:

$$D = \frac{\phi}{T/2}$$

where ϕ is the phase shift between the pulses of the primary and secondary H-bridges, and T is the time period of the switching pulses.

Maximum power transfer occurs when $D = 0.5$. However, in a closed-loop system where the controller receives feedback from the output, the duty ratio may need to be increased under certain conditions. If the system already operates at $D = 0.5$, there is no margin for further increase. Hence, we choose $D = 0.4$, which allows room for control adjustments. With this setting, the corresponding phase shift becomes:

$$\phi = 4\,\mu\text{s}$$

3.2 Equation of Power and Calculation of R

From the theoretical analysis, the output power is given by:

$$P = \frac{V_{\text{in}} \cdot V_{\text{out}} \cdot D \cdot (1 - D)}{2 \cdot n \cdot f_s \cdot L}$$

Substituting the known values:

$$P = 240\,\text{mW}$$

We place a resistor on the secondary side of the transformer to observe the voltage drop across it. Assuming ideal power transfer (i.e., all input power is delivered to the load):

$$P = P_{\text{out}} = \frac{V_{\text{out}}^2}{R}$$

Solving for R:

$$R = \frac{V_{\text{out}}^2}{P} = \frac{5^2}{0.24} = 100\,\Omega$$

We can safely choose the output capacitor $C = 1\,\text{mF}$ to effectively control the output voltage ripple.

3.3 Dead Time

The dead time k is set to $0.25\,\mu\text{s}$. This value is determined based on the characteristics of the MOSFETs, such as their rise and fall times, and the RC time constant of the snubber circuit.

4 Simulation and Comparison with Results

4.1 Output for H Bridge

Here are the simulation and results of the output pules for driving the MOSFETs. The pulses from the FPGA gets amplified with the help of optocoupler.

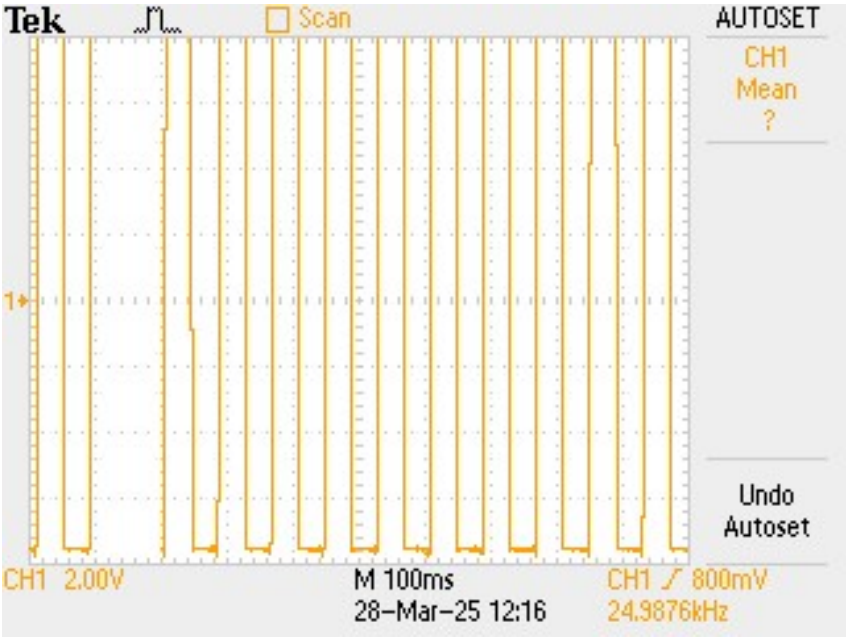


Figure 4: Gate pulses generated for the H-bridge MOSFETs

For a single leg of the H-bridge, the two gate signals are complementary to each other. The figure below shows the output of these complementary pulses generated by the FPGA to drive one leg of the H-bridge.

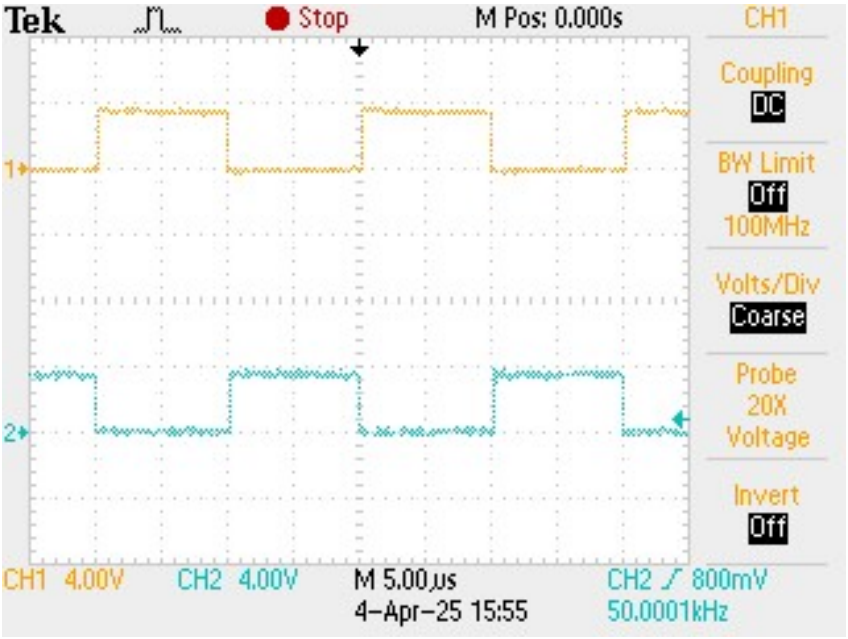
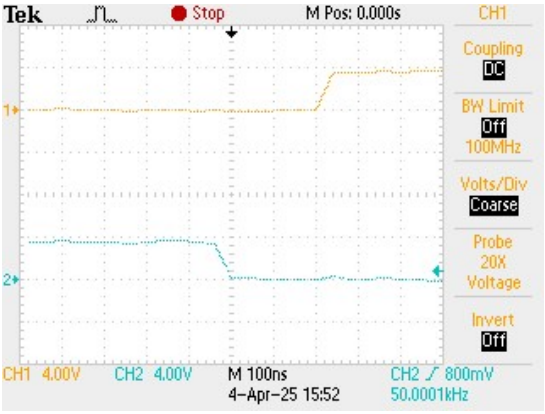
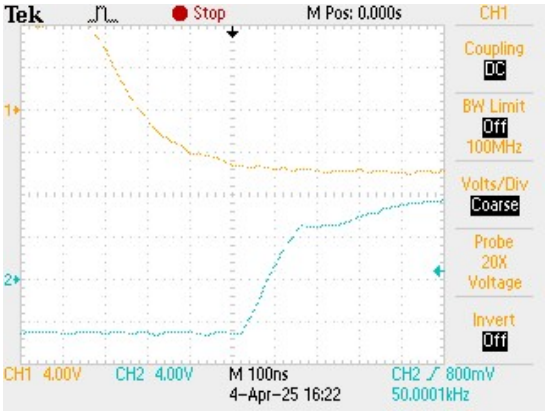


Figure 5: Complimentary Gate pulses generated for the one leg of H-bridge

To avoid potential short circuits or shoot-through conditions in the circuit, a dead time was introduced and precisely controlled through the FPGA.



(a) Deadtime-1



(b) Deadtime-2

Figure 6: Combined figure caption for both images

After assembling all the components of the H-bridge for both legs, the final output waveform of the H-bridge is obtained as shown below.

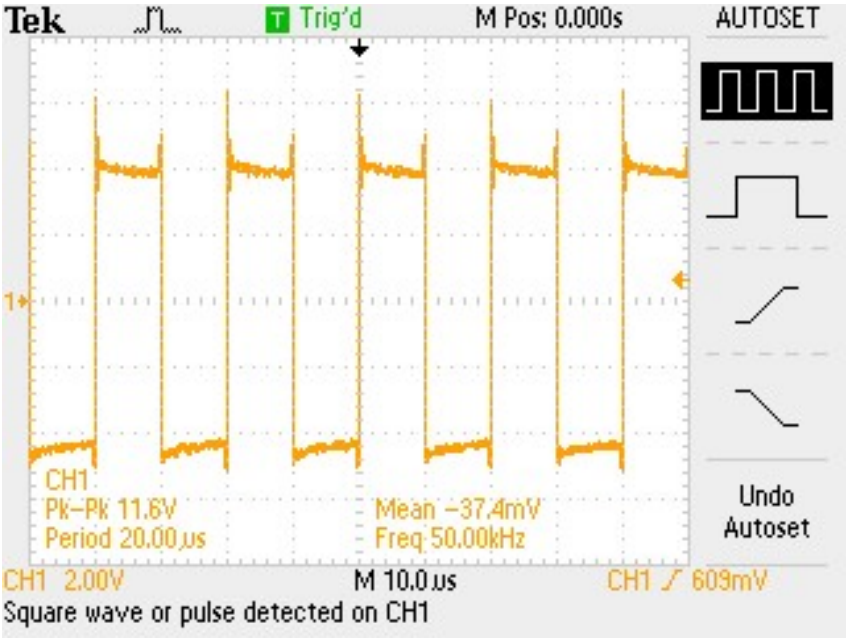


Figure 7: Voltage waveform across H bridge

4.2 Connecting R-L Load to H Bridge

Before implementing the final DAB, it is advised to perform basic circuit output to check possible issues. Therefore, we first applied R-L load to the one H-bridge.

Here is the output across inductor.

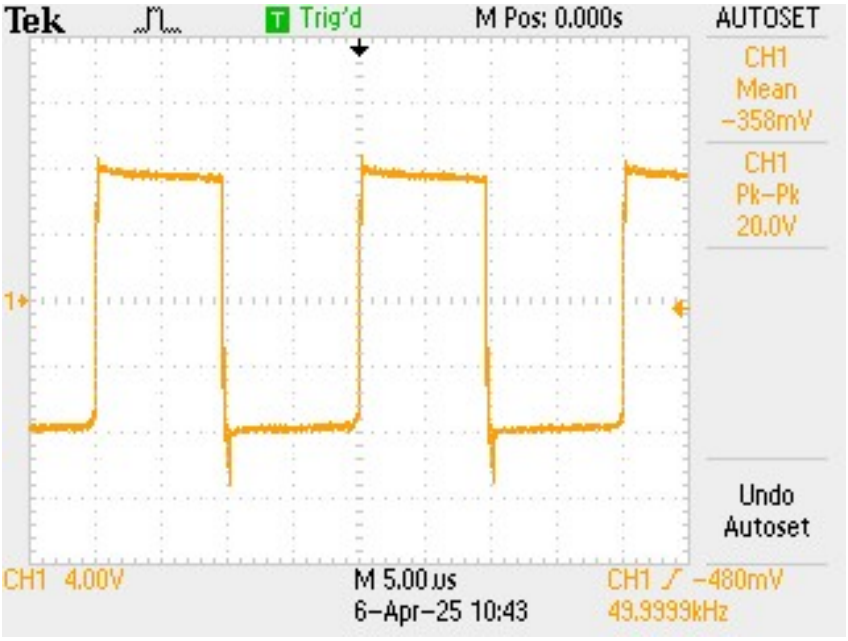


Figure 8: Voltage waveform across inductor for H-bridge for low load

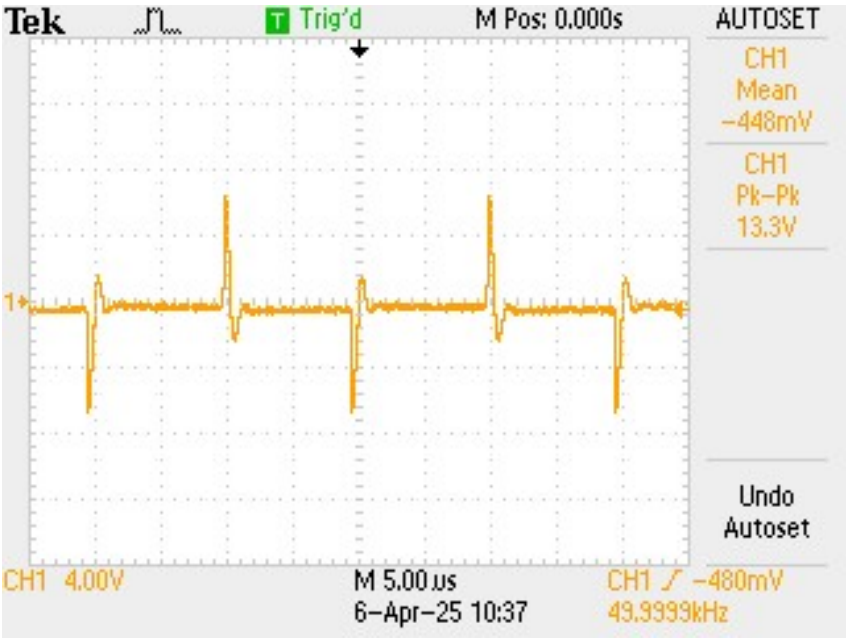


Figure 9: Voltage waveform across inductor for H-bridge for high load

Thus, we can conclude that the inductor is exhibiting the desired behavior.

4.3 Connecting Transformer to H Bridge

To ensure the connection across the transformer and the output for the open circuit, we applied transformer as a load to the H bridge, for which we got desired beahviour.

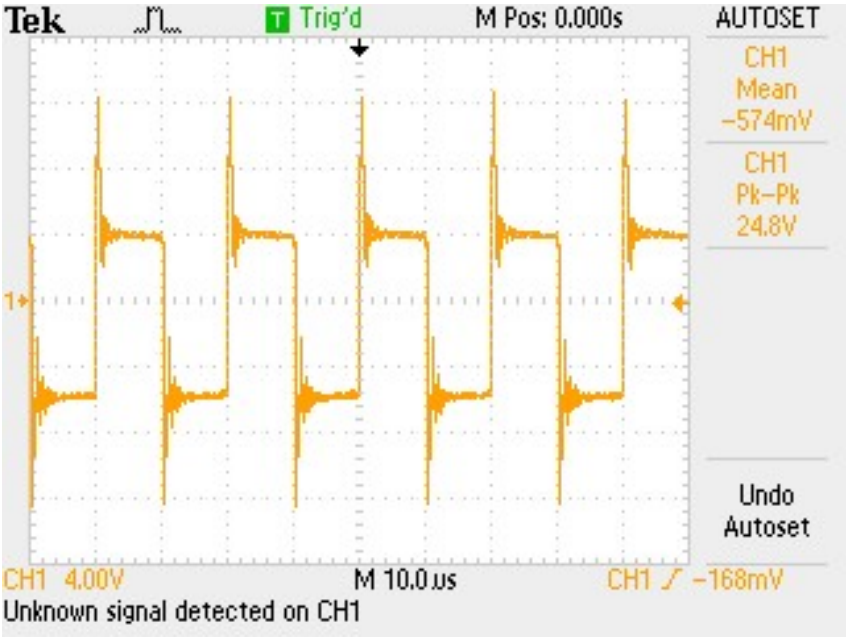


Figure 10: Voltage waveform across secondary side of the transformer

Hence, we are ready for the final implementation of the DAB.

4.4 Final Implementation of DAB and Output

Figure 11 shows the final setup of the Dual Active Bridge (DAB) circuit simulated in LTspice.

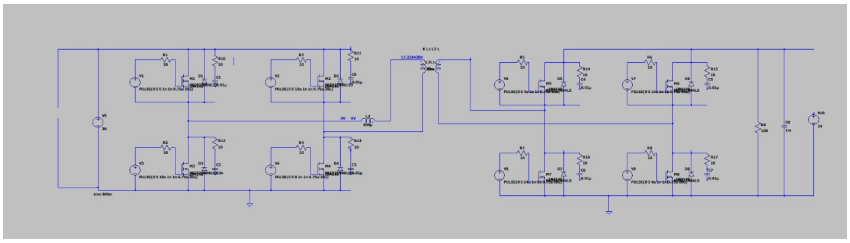


Figure 11: LTspice setup for DAB

Figure 12 shows the practical implementation of the DAB circuit in the laboratory.

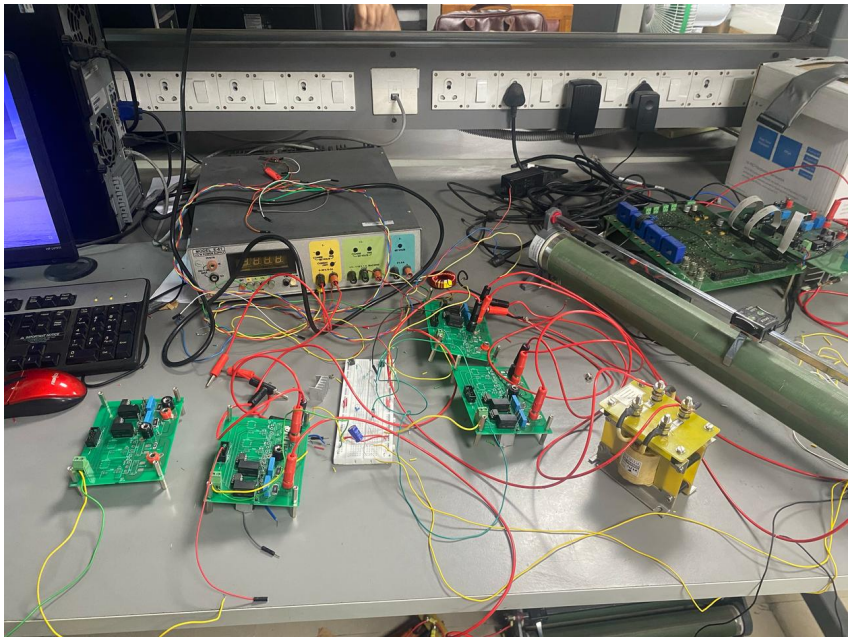


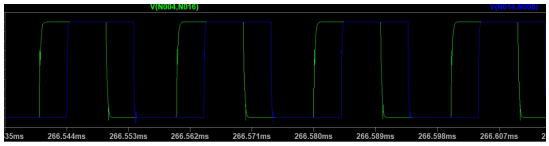
Figure 12: LTspice setup for DAB

We obtained a nearly constant DC output across the rheostat. While the output voltage is not exactly half the input voltage, this deviation is expected due to the non-idealities and losses present in the practical setup. Our earlier calculations assumed ideal conditions with perfect power transfer.

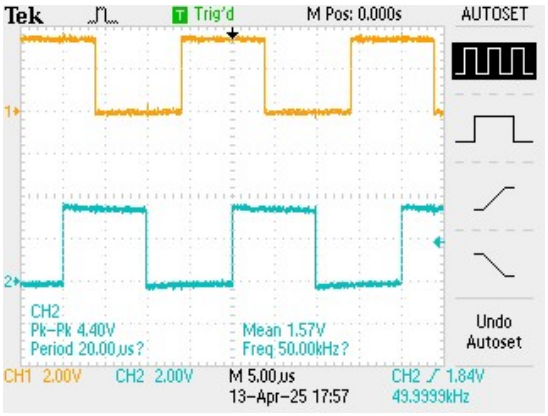
For an input voltage $V_{\text{in}} = 10\,\text{V}$, we measured an output voltage of $V_{\text{out}} = 4.45\,\text{V}$, demonstrating the expected step-down behavior, although with losses.

4.5 Phase shifted pulses

Below are the LTspice simulation and corresponding practical gate pulses waveforms for the MOSFETs, they have phase shift.



(a) LTspice simulation: Gate Pulses phase shifted

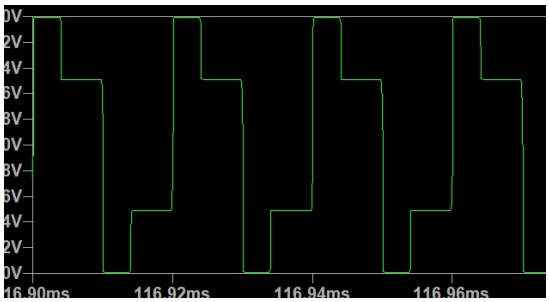


(b) Practical output: Gate pulses phase shifted

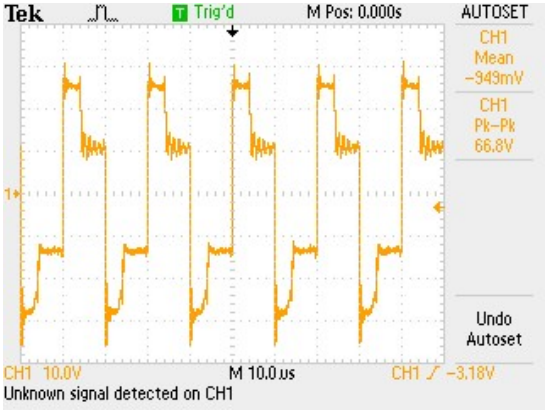
Figure 13: Voltage across the inductor in simulation and practical setup

4.6 Inductor Voltage Waveform

Below are the LTspice simulation and corresponding practical output waveforms for the voltage across the inductor.



(a) LTspice simulation: Inductor voltage waveform

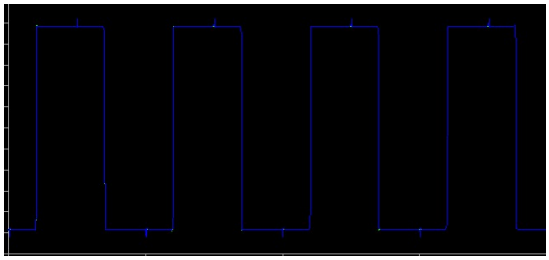


(b) Practical output: Inductor voltage waveform

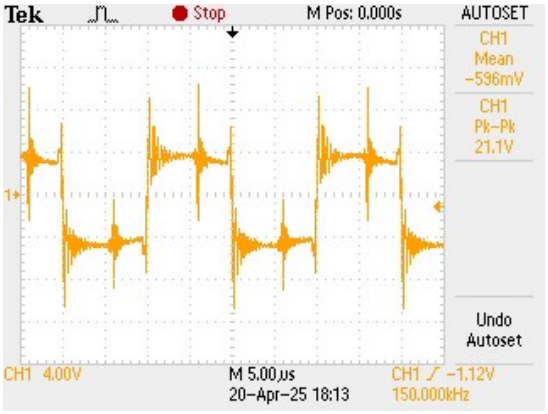
Figure 14: Voltage across the inductor in simulation and practical setup

4.7 Transformer Voltage Waveform

Similarly, the following figures show the LTspice simulation and the practical waveform of voltage across the transformer.



(a) LTspice simulation: Transformer voltage waveform



(b) Practical output: Transformer voltage waveform

Figure 15: Voltage across the transformer in simulation and practical setup

4.8 Aftermath

Here is the final implementation of the DAB using SPS. Due to the limitations of Single Phase Shift control, it is not possible to control every variable in our favor—such as power, voltage, I_{rms}, and reactive power. Hence, although it is the simplest form of DAB, it does not offer sufficient flexibility.

Precautions during the experiment:

1. **Conducting heat sinks:** One mistake we made was using conducting heat sinks on the MOSFETs, which resulted in the failure of a MOSFET. The surface and legs made unintended contact at undesired points, eventually causing the component to blow.

2. **Long wires for connections:** Long wires between the H-bridge, transformer, and inductor introduced a high value of parasitic inductance. This is undesirable, as the closed-loop circuit—after switching off one leg—can resonate, introducing current spikes and potentially damaging the circuit.