fpga_power
fpga_power.sch

IMU
imu.sch

imagers
imagers.sch

jetson_power
jetson_power.sch

fpga_config
fpga_config.sch

power
power.sch

mcu
mcu.sch

jetson_pcie
jetson_pcie.sch

jetson_enet
jetson_enet.sch

fpga_pcie
fpga_pcie.sch

fpga_bank_3b
fpga_bank_3b.sch

fpga_bank_4a
fpga_bank_4a.sch

fpga_bank_5a
fpga_bank_5a.sch

fpga_bank_5b
fpga_bank_5b.sch

fpga_bank_7a
fpga_bank_7a.sch

fpga_bank_8a
fpga_bank_8a.sch

jetson_hdmi
jetson_hdmi.sch

jetson_usb
jetson_usb.sch

jetson_jtag
jetson_jtag.sch

jetson_sata
jetson_sata.sch

jetson_sdcard
jetson_sdcard.sch

jetson_uarts
jetson_uarts.sch

THIS DESIGN IS PROVIDED AS-IS, UNDER THE TERMS OF THE APACHE 2.0 LICENSE. THERE IS ABSOLUTELY NO WARRANTY. THIS DESIGN IS FOR RESEARCH AND DEVELOPMENT. IT MUST NOT BE OPERATED BY UNTRAINED PERSONNEL OUTSIDE OF LABORATORY CONDITIONS. IT MUST NOT BE OPERATED UNATTENDED! AT TIME OF WRITING, NO FORMAL TESTING OR CERTIFICATION HAS BEEN PERFORMED.

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Sheet: /
File: ovc.sch

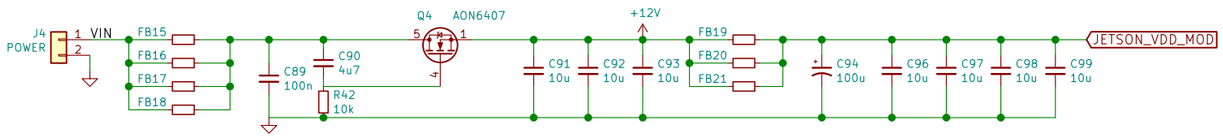
Title:

Size: A4 | Date: | **Rev:**
KiCad E.D.A. kicad 5.0.0-rc2-dev-unknown-d906acc62ubuntu16.04.1 | Id: 1/23

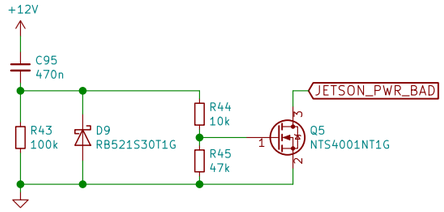
input: 12v DC nominal

TODO: fuse + crowbar

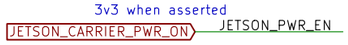
reverse polarity protection
and soft-charge the input caps



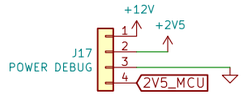
hold PWR_BAD low for +/-50 ms after power is first applied



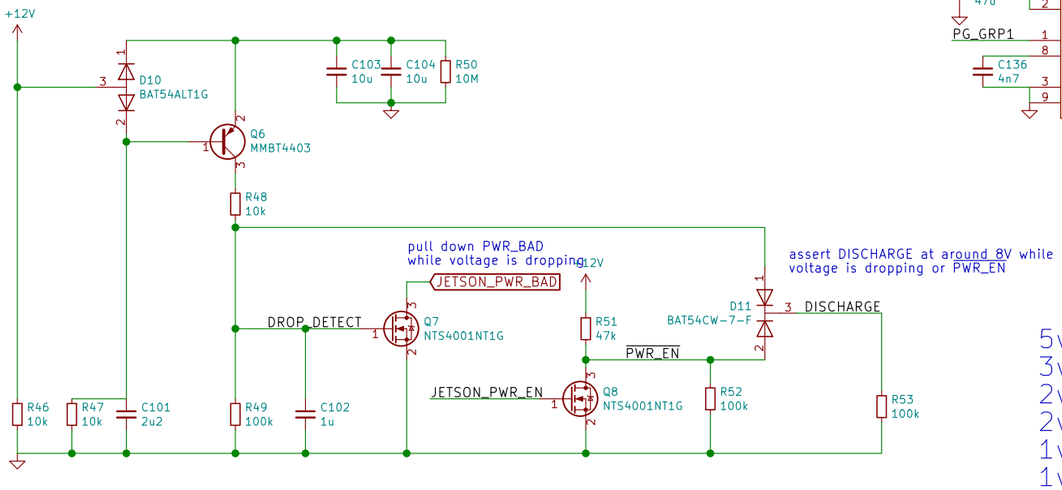
3v3 when asserted



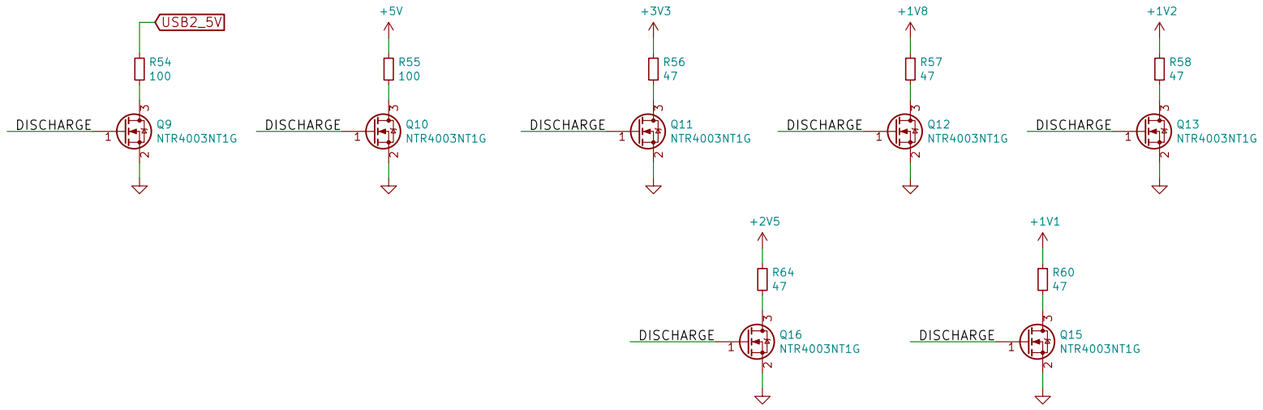
This will hold the Tegra in reset until 1v8 is alive
pullup provided in Jetson



analog voltage-drop detector



active discharge of all rails except 2V5_MCU

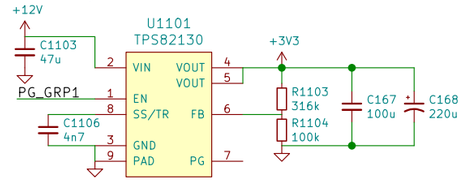


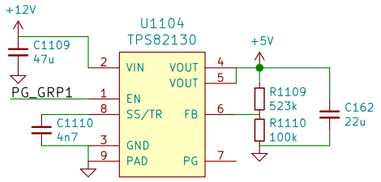
5v: USB (two ports)
3v3: imager analog and LVDS
2v5 always-on: MCU
2v5: FPGA LVDS and I/O
1v8: imager cores and Jetson I/O
1v2: FPGA transceivers
1v1: FPGA core

VOUT = FB * (1 + R1/R2), VFB = 0.8, R2 = 100k

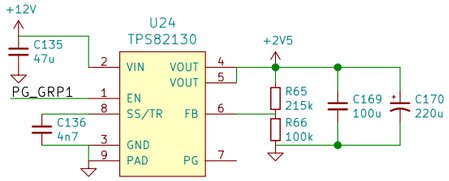
TODO: Replace with beefy LDO:
VOUT = 1.2V => R1 = 50k => closest value: 49.9k => Resulting Vout= 1.200V
VOUT = 1.8V => R1 = 125k => closest value: 124k => Resulting Vout= 1.792V
VOUT = 2.5V => R1 = 212.5k => closest value: 215k => Resulting Vout= 2.520V
VOUT = 3.3V => R1 = 312.5k => closest value: 316k => Resulting Vout= 3.296V
VOUT = 5V => R1 = 525k => closest value: 523k => Resulting Vout= 4.984V

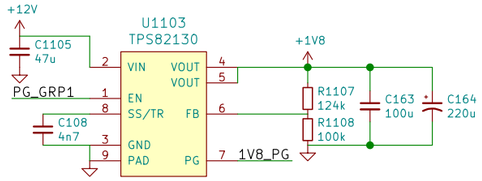
What is the target startup time here ? 4.7nF leads to 2.3ms if I used the right formula (8.2.1.2.4 from datasheet)

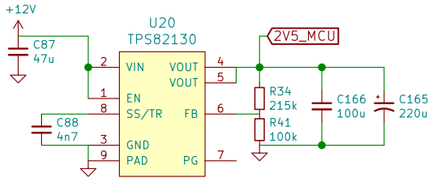


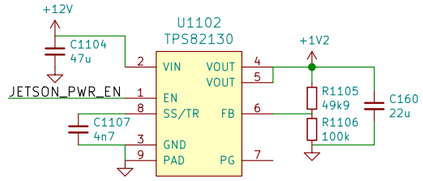


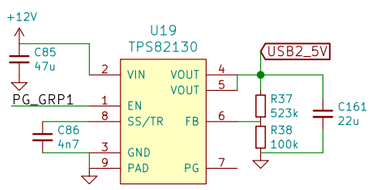
REV.A ERROR: U20 EN PIN MUST BE TIED TO 12V FOR ALWAYS-ON!

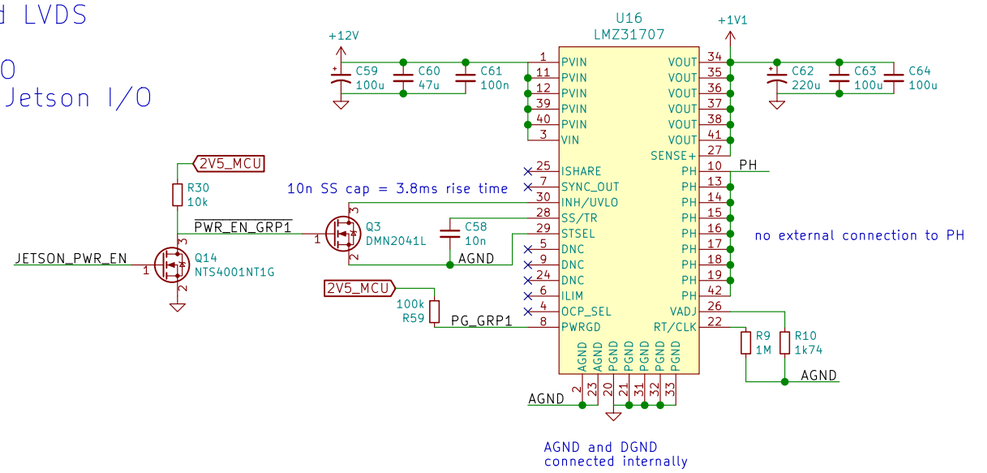












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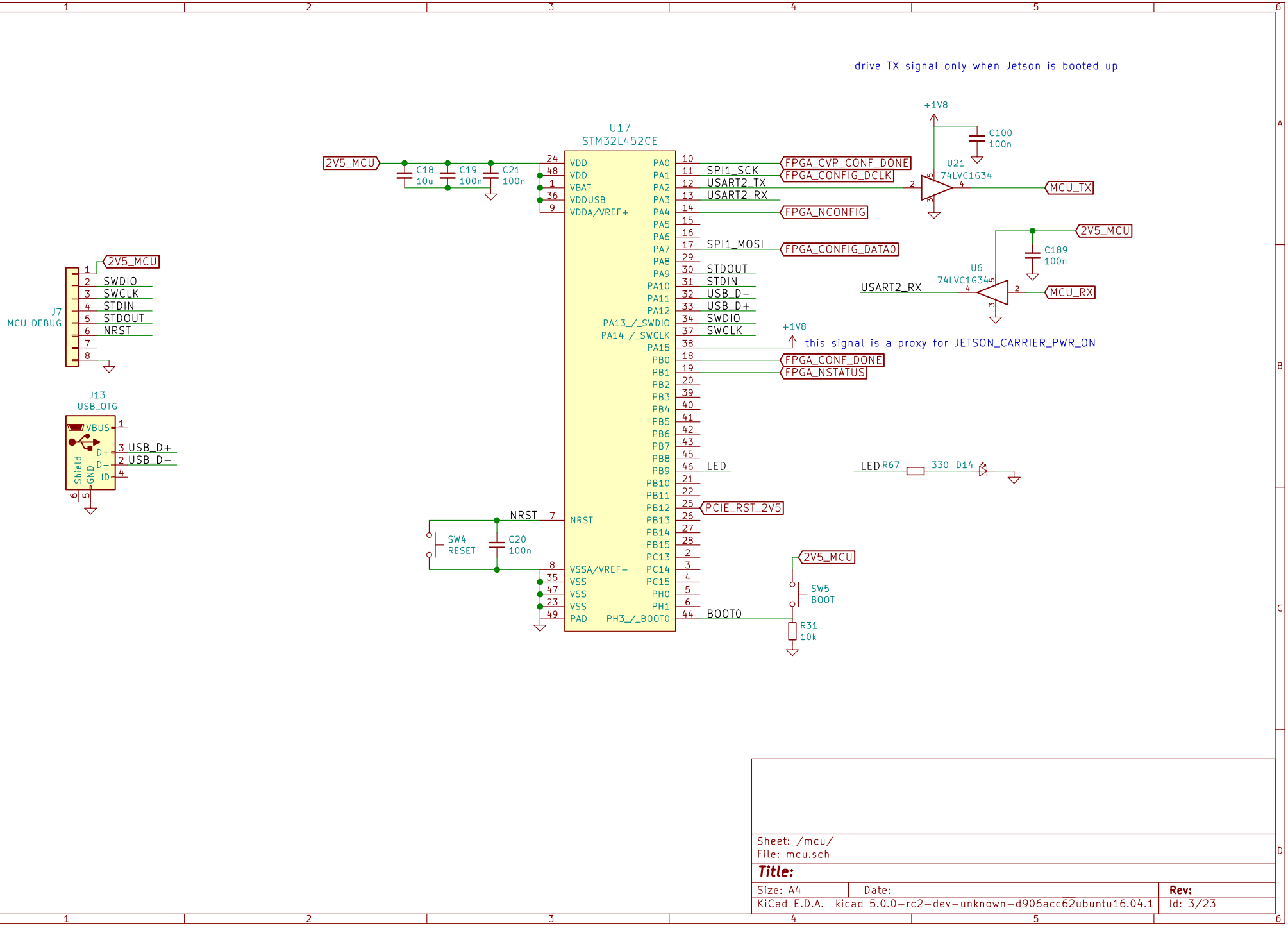
KiCad E.D.A. kicad 5.0.0-rc2-dev-unknown-d906acc62ubuntu16.04.1		Id: 2/23



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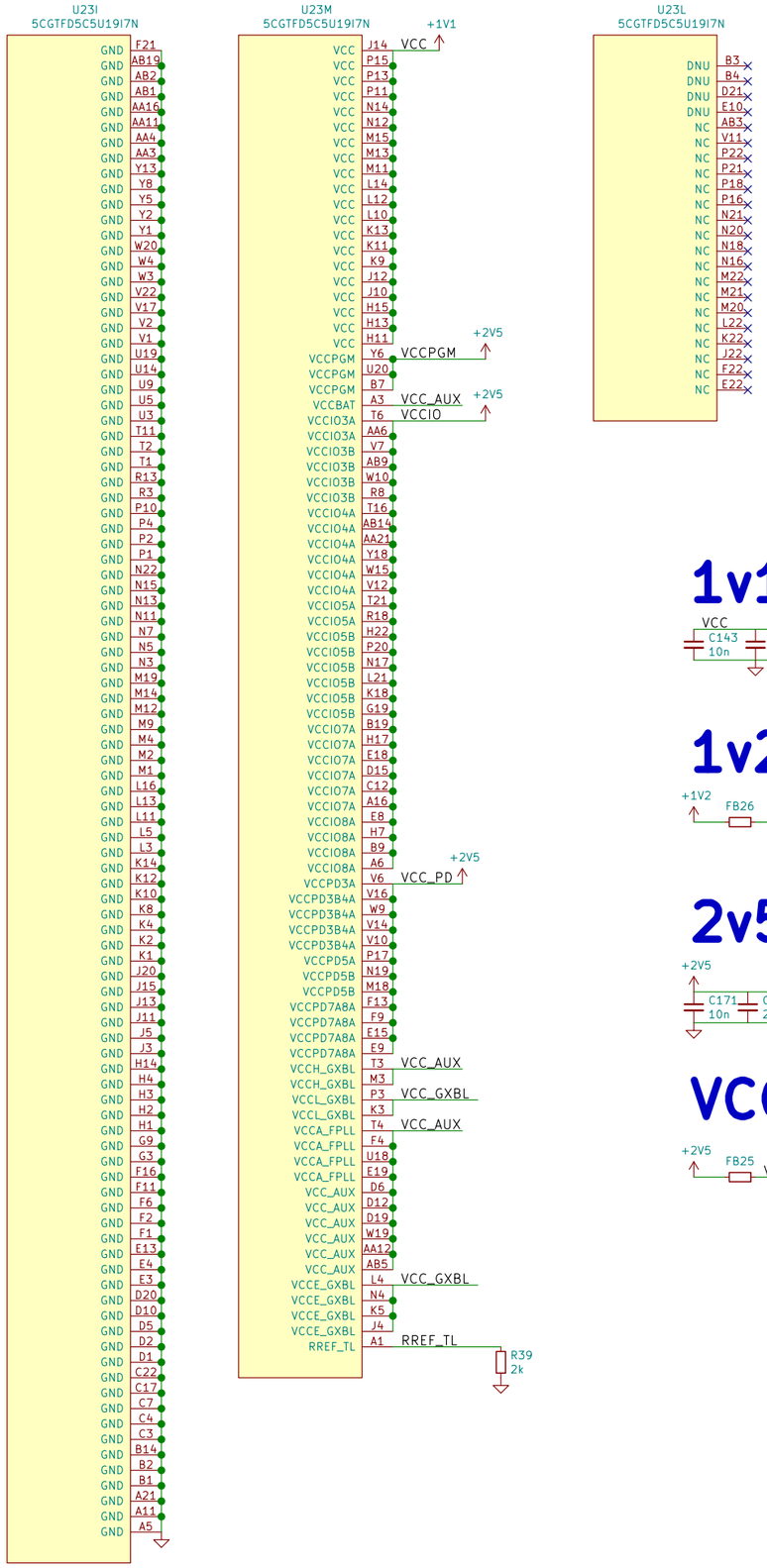
KiCad E.D.A. kicad 5.0.0−rc2−dev−unknown−d906acc62ubuntu16.04.1		Id: 3/23



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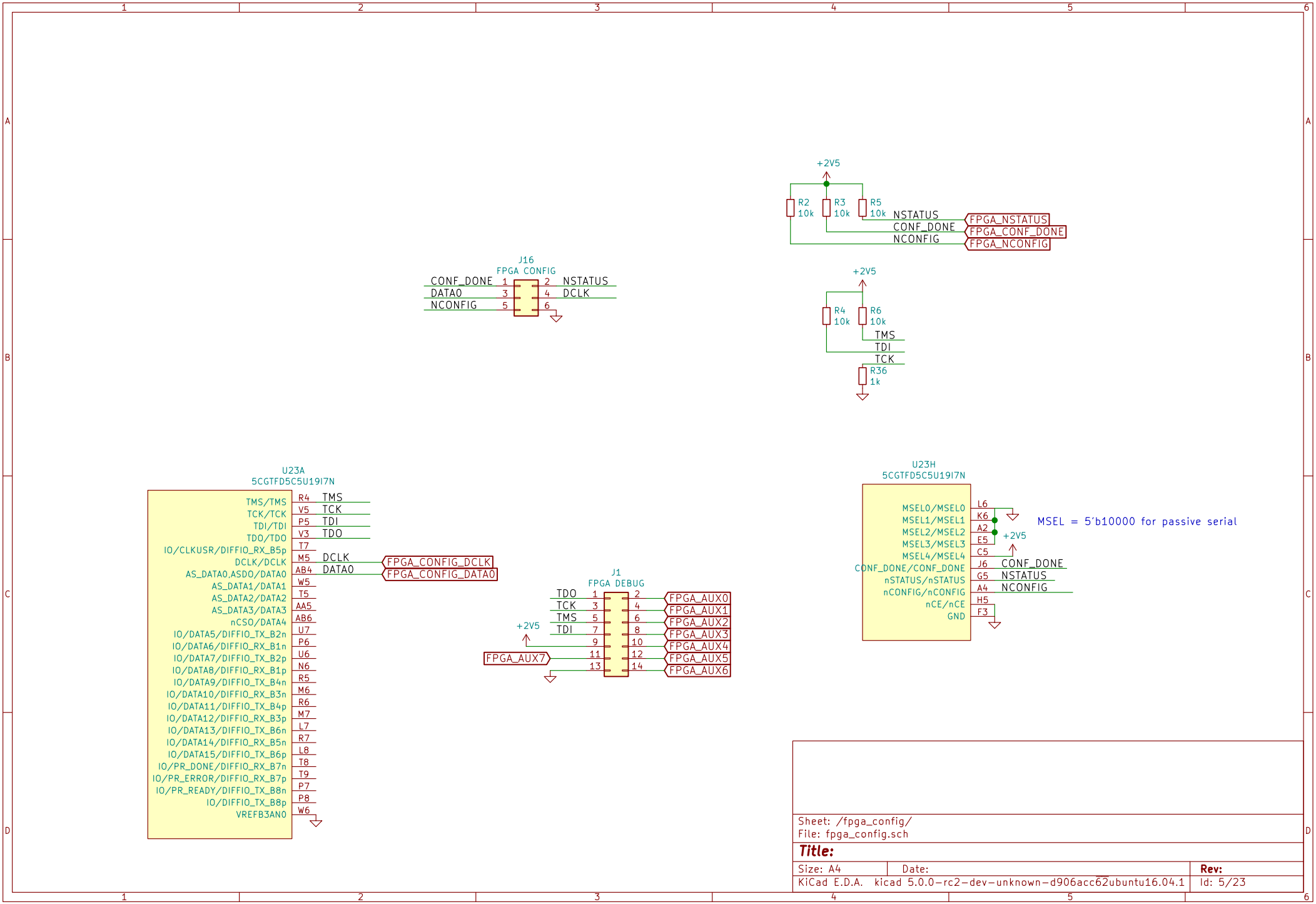
+2V5
R2
10k
R3
10k
R5
10k
NSTATUS
CONF_DONE
NCONFIG
FPGA_NSTATUS
FPGA_CONF_DONE
FPGA_NCONFIG
J16
FPGA CONFIG
CONF_DONE 1
DATA0 3
NCONFIG 5
2 NSTATUS
4 DCLK
6
+2V5
R4
10k
R6
10k
TMS
TDI
TCK
R36
1k
U23A
5CGTFD5C5U19I7N
TMS/TMS R4 TMS
TCK/TCK V5 TCK
TDI/TDI P5 TDI
TDO/TDO V3 TDO
IO/CLKUSR/DIFFIO_RX_B5p T7
DCLK/DCLK M5 DCLK
AS_DATA0,ASDO/DATA0 AB4 DATA0
AS_DATA1/DATA1 W5
AS_DATA2/DATA2 T5
AS_DATA3/DATA3 AA5
nCSO/DATA4 AB6
IO/DATA5/DIFFIO_TX_B2n U7
IO/DATA6/DIFFIO_RX_B1n P6
IO/DATA7/DIFFIO_TX_B2p U6
IO/DATA8/DIFFIO_RX_B1p N6
IO/DATA9/DIFFIO_TX_B4n R5
IO/DATA10/DIFFIO_RX_B3n M6
IO/DATA11/DIFFIO_TX_B4p R6
IO/DATA12/DIFFIO_RX_B3p M7
IO/DATA13/DIFFIO_TX_B6n L7
IO/DATA14/DIFFIO_RX_B5n R7
IO/DATA15/DIFFIO_TX_B6p L8
IO/PR_DONE/DIFFIO_RX_B7n T8
IO/PR_ERROR/DIFFIO_RX_B7p T9
IO/PR_READY/DIFFIO_TX_B8n P7
IO/DIFFIO_TX_B8p P8
VREFB3AN0 W6
FPGA_CONFIG_DCLK
FPGA_CONFIG_DATA0
J1
FPGA DEBUG
TDO 1
TCK 3
TMS 5
TDI 7
9
11
13
+2V5
FPGA_AUX7
2 FPGA_AUX0
4 FPGA_AUX1
6 FPGA_AUX2
8 FPGA_AUX3
10 FPGA_AUX4
12 FPGA_AUX5
14 FPGA_AUX6
U23H
5CGTFD5C5U19I7N
MSEL0/MSEL0 L6
MSEL1/MSEL1 K6
MSEL2/MSEL2 A2
MSEL3/MSEL3 E5
MSEL4/MSEL4 C5
CONF_DONE/CONF_DONE J6 CONF_DONE
nSTATUS/nSTATUS G5 NSTATUS
nCONFIG/nCONFIG A4 NCONFIG
nCE/nCE H5
GND F3
+2V5
MSEL = 5'b10000 for passive serial
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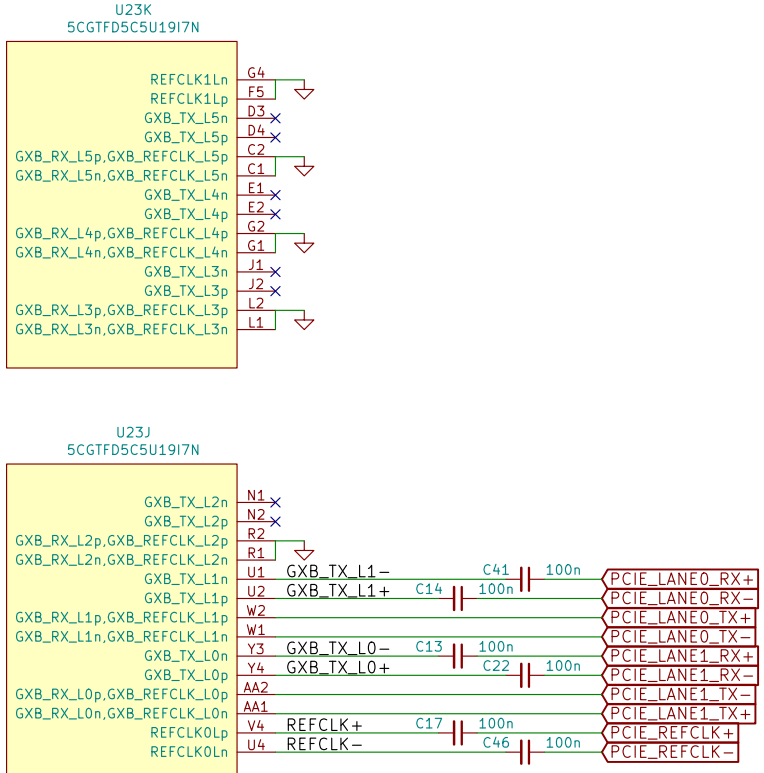
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.0.0-rc2-dev-unknown-d906acc62ubuntu16.04.1
Id: 5/23



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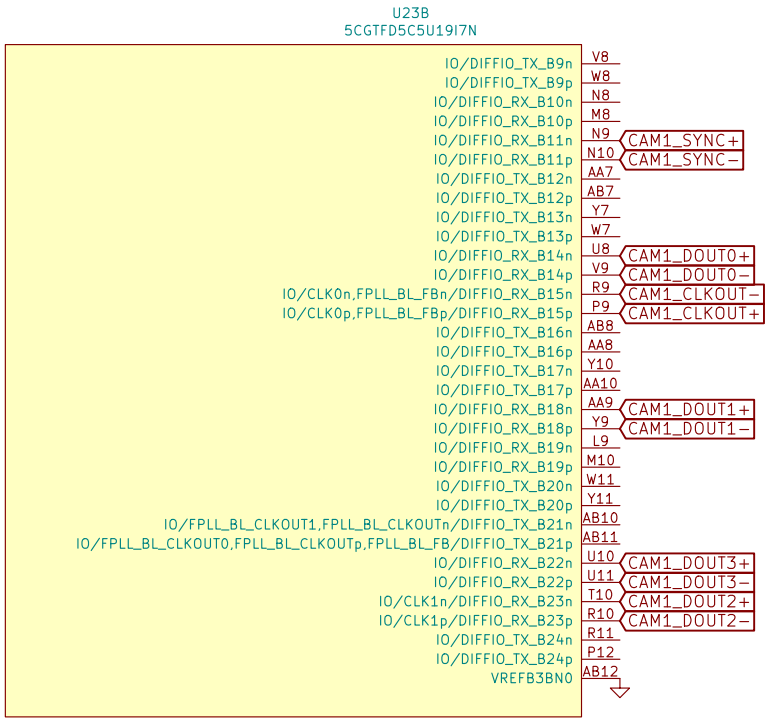

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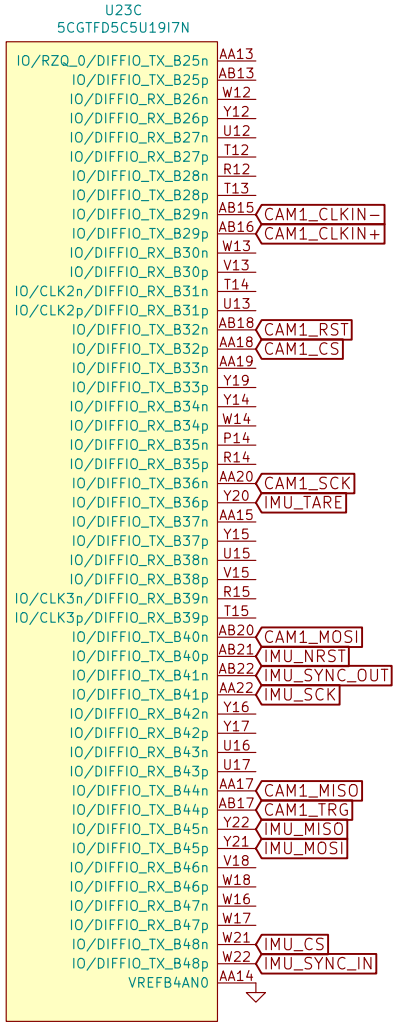

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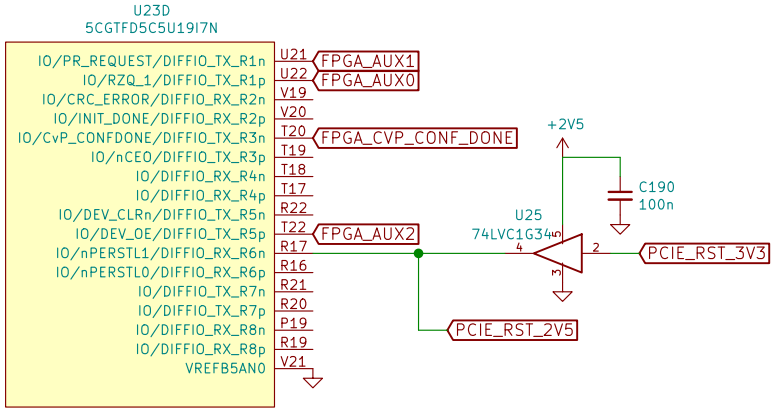

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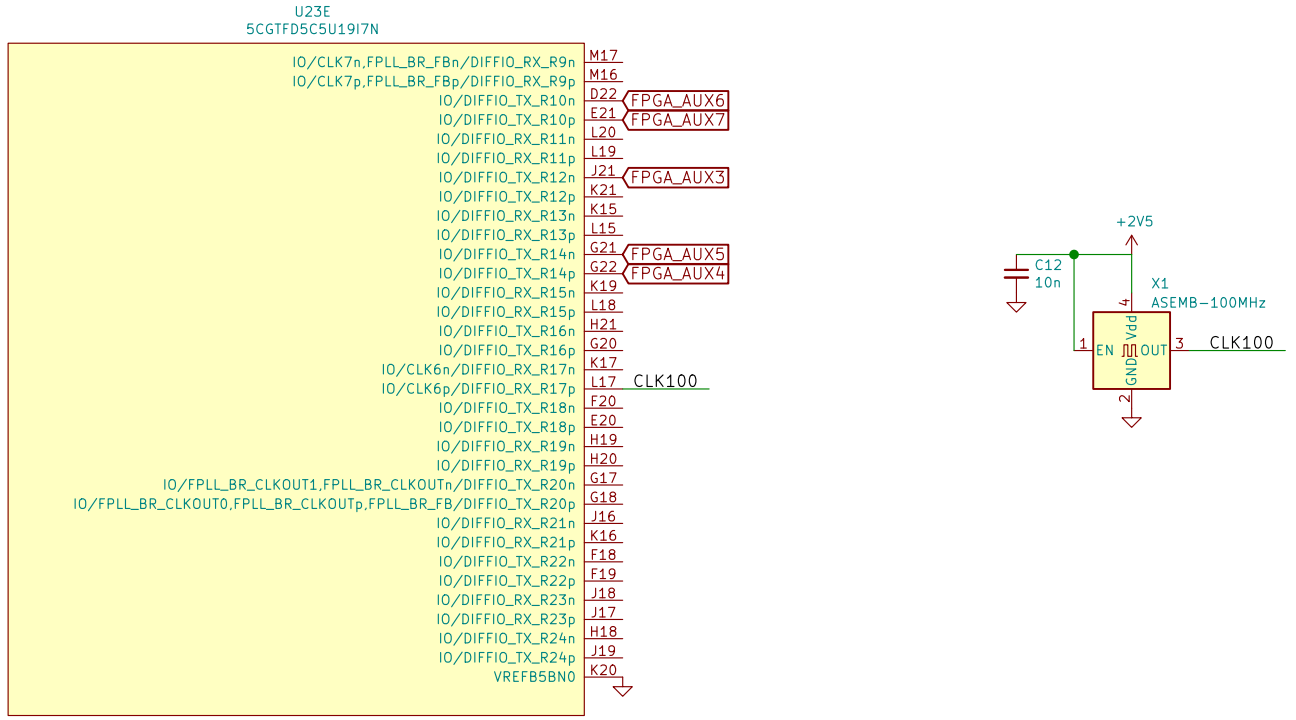

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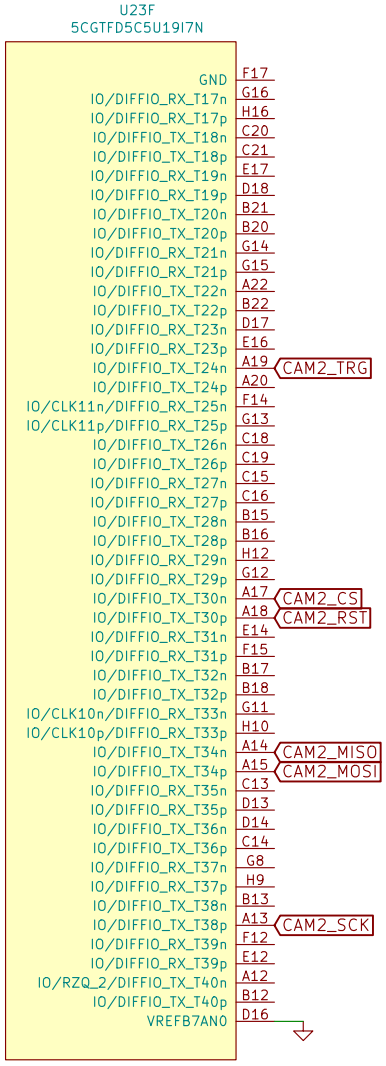

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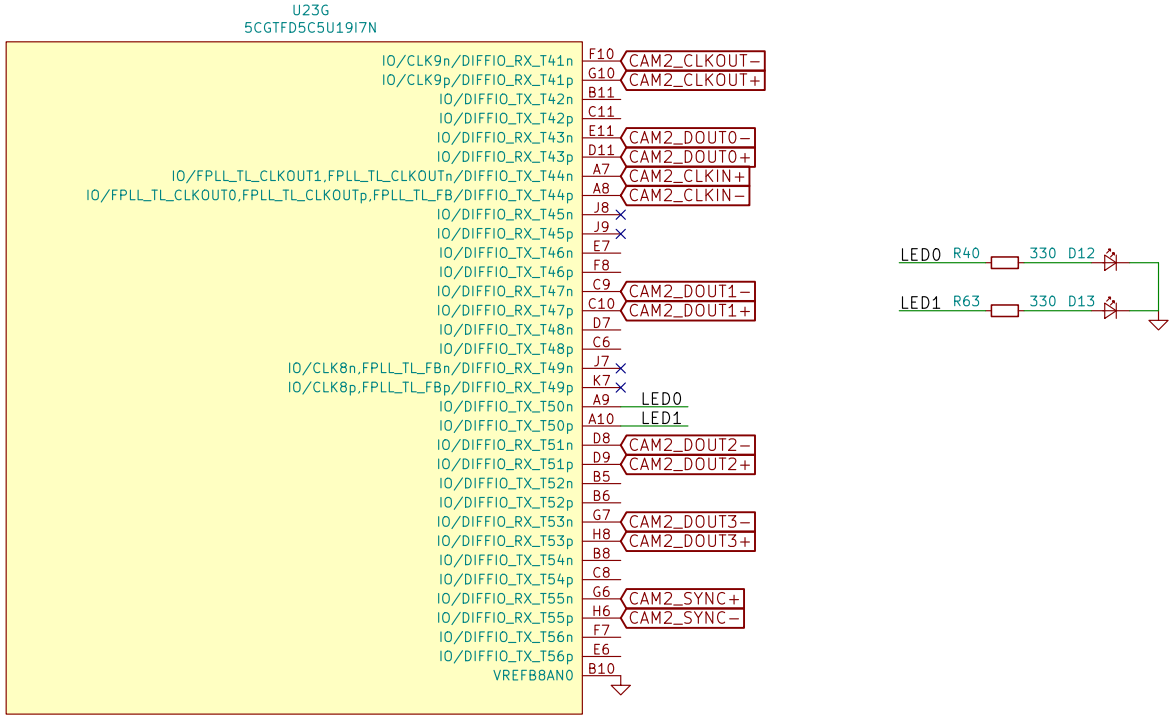

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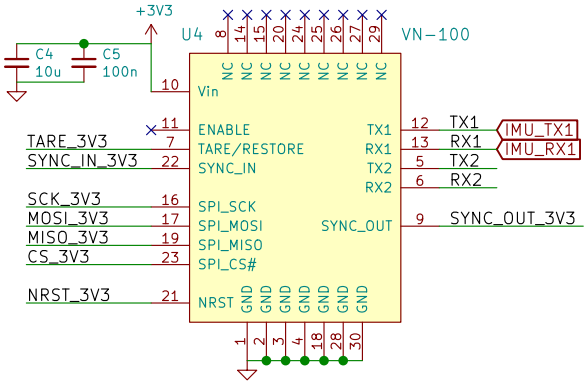

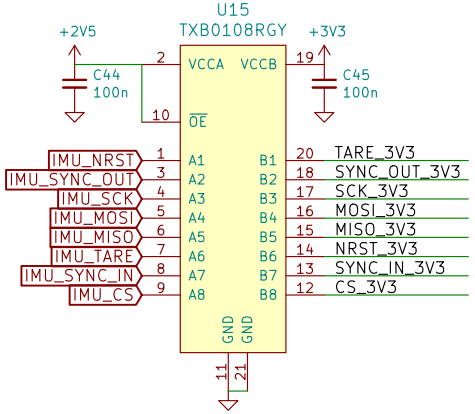

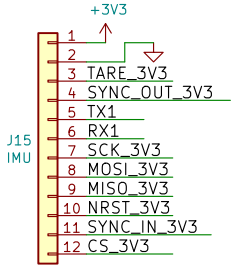

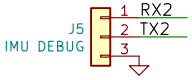

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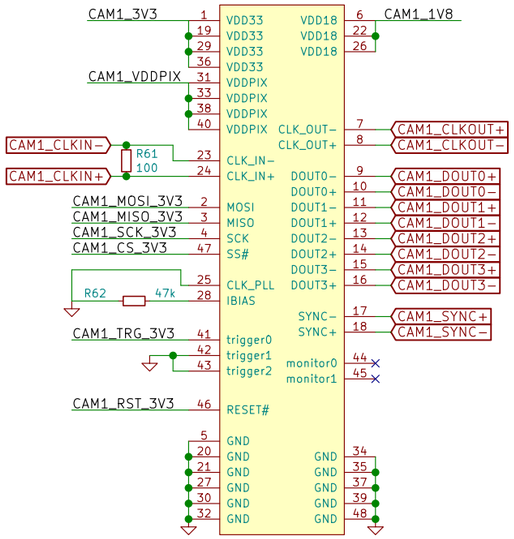
CAMERA

U1



NOIP1SN1300A−QDI

CAM2

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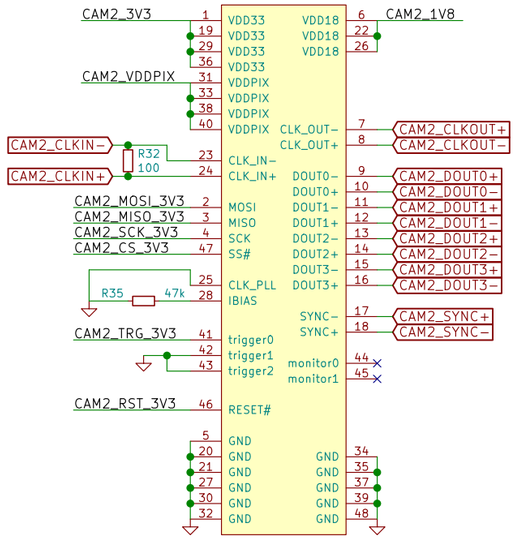

NOIP1SN1300A−QDI

CAM2_CLKIN−
CAM2_CLKIN+
CAM2_CLKOUT+
CAM2_CLKOUT−
CAM2_DOUT0+
CAM2_DOUT0−
CAM2_DOUT1+
CAM2_DOUT1−
CAM2_DOUT2+
CAM2_DOUT2−
CAM2_DOUT3+
CAM2_DOUT3−
CAM2_SYNC+
CAM2_SYNC−
CAM2_RST
CAM2_TRG
CAM2_MOSI
CAM2_MISO
CAM2_SCK
CAM2_CS

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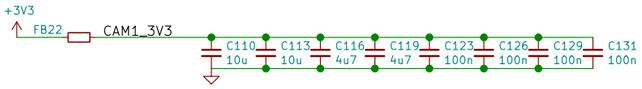

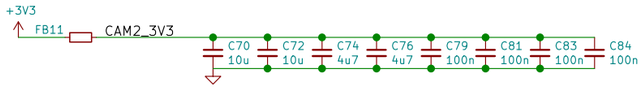

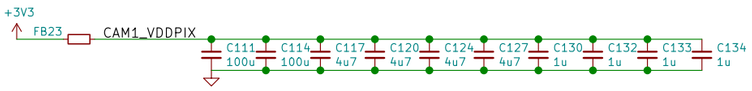

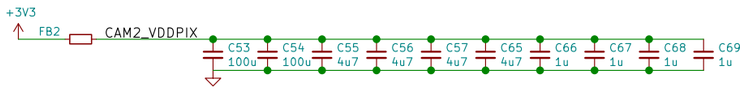

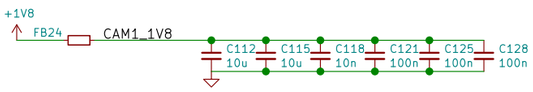

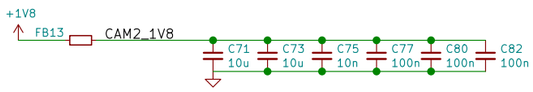

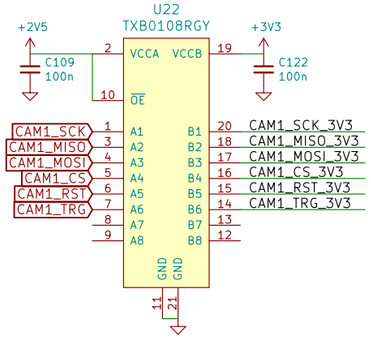

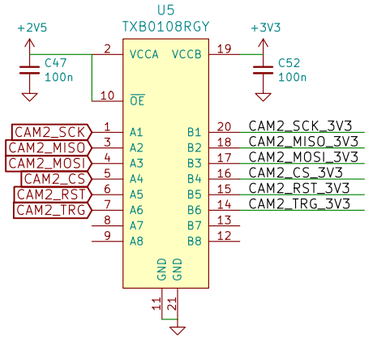

J8 LENS_HOLDER

J9 LENS_HOLDER

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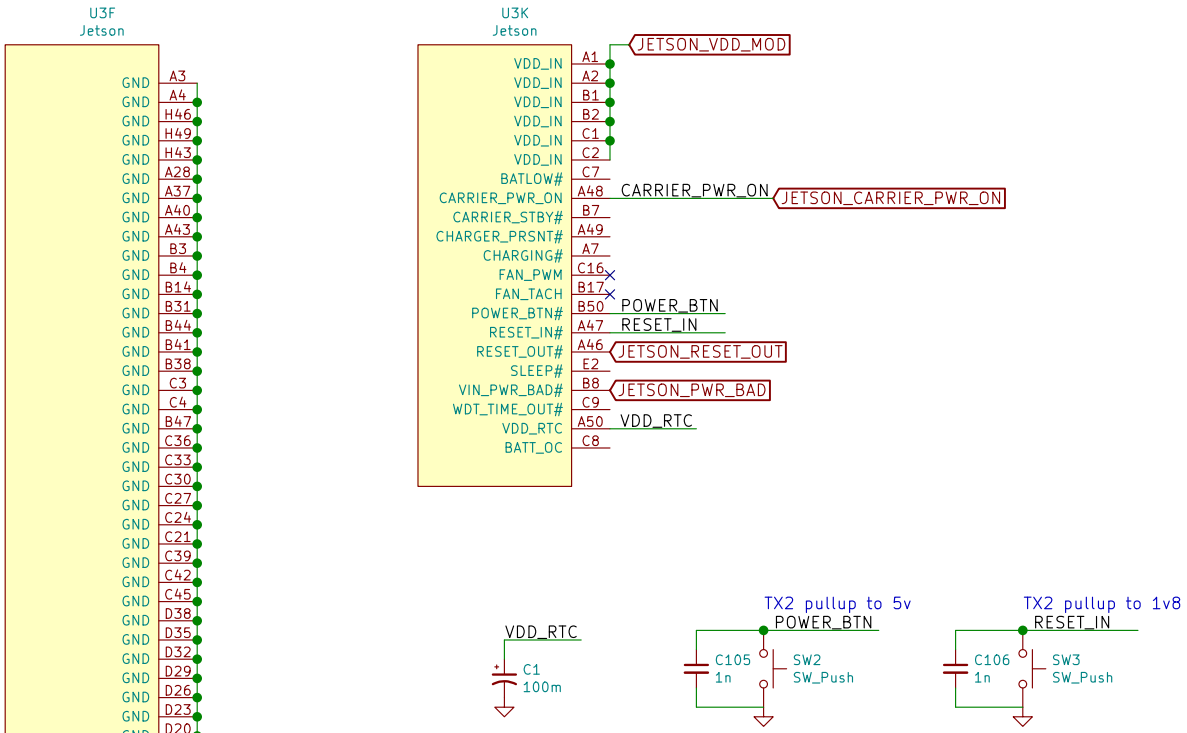

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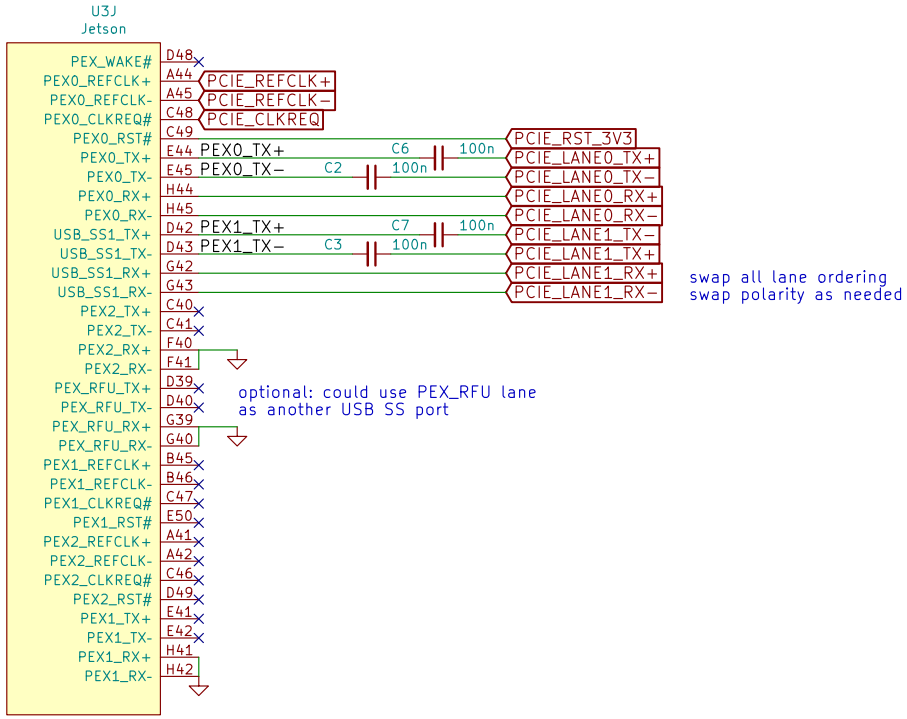

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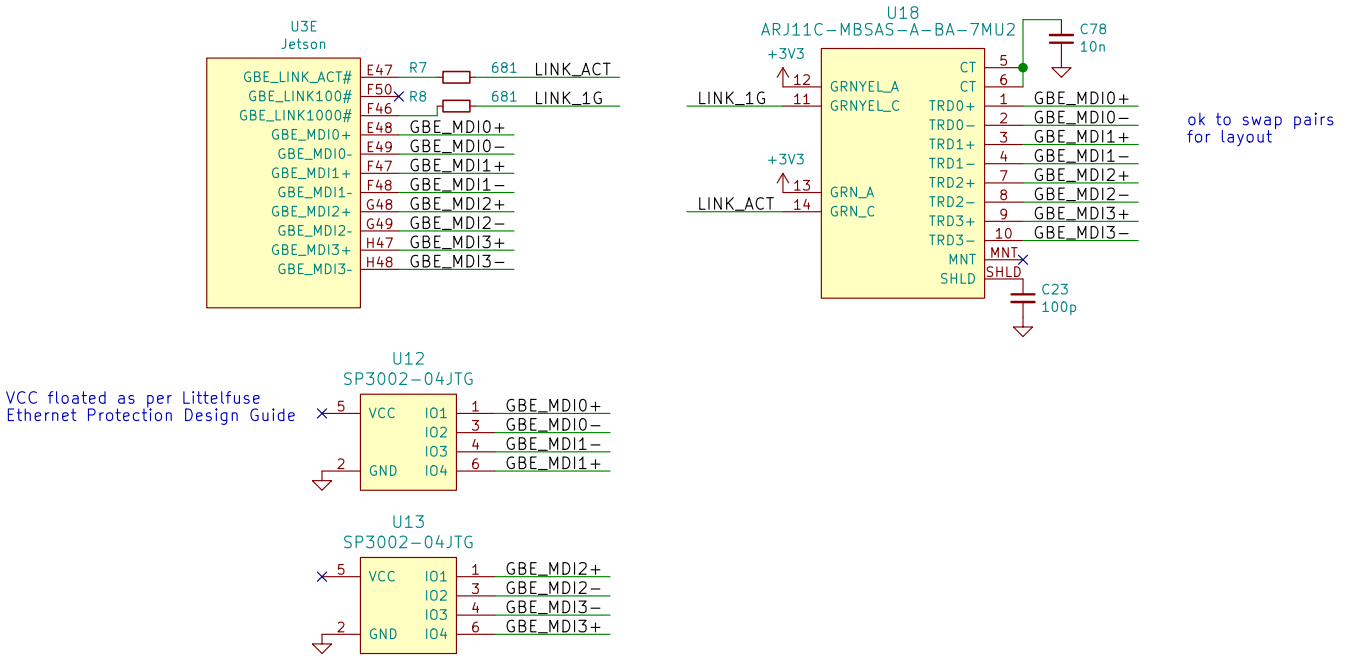

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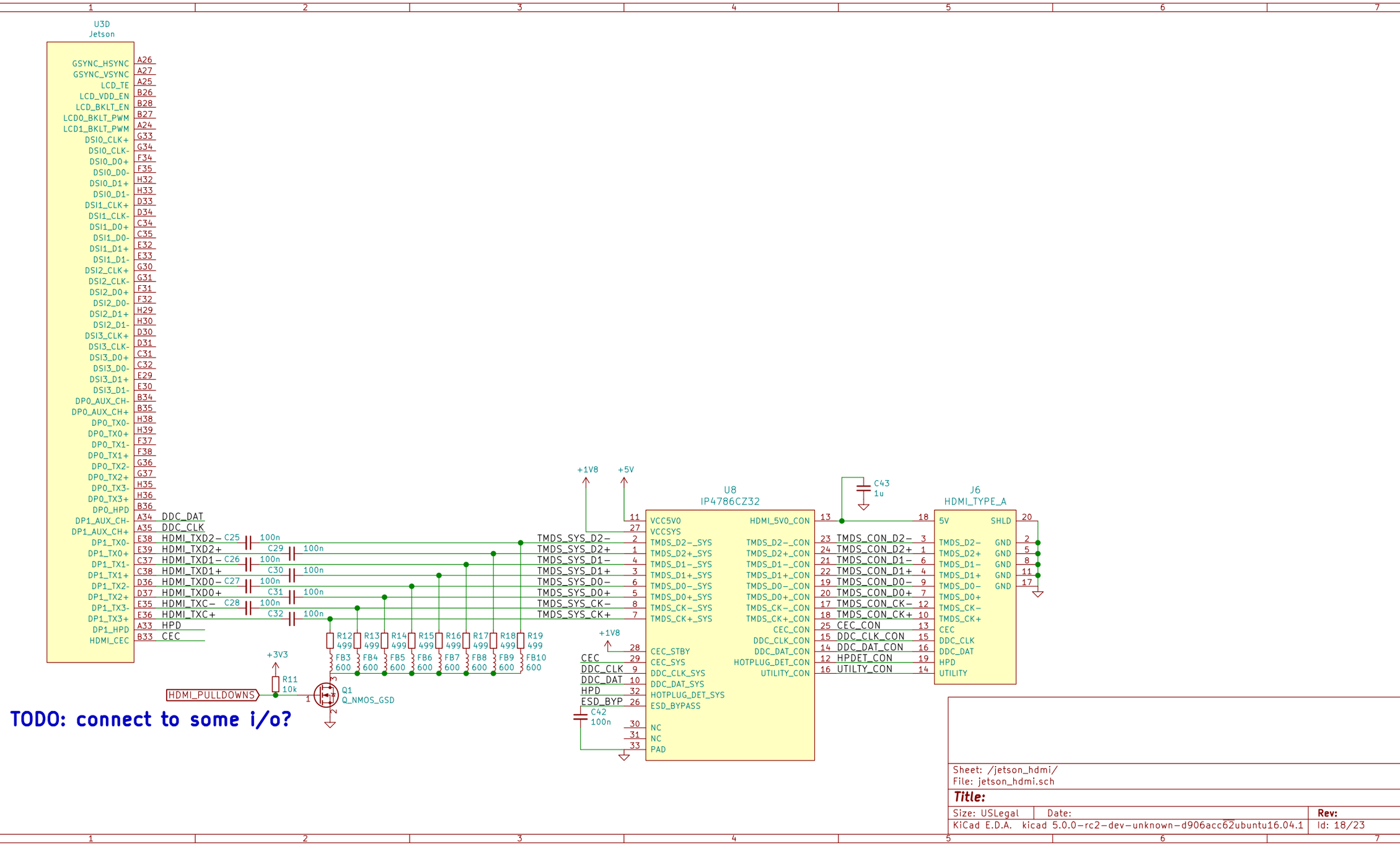
U3D
Jetson
GSYNC_HSYNC A26
GSYNC_VSYNC A27
LCD_TE A25
LCD_VDD_EN B26
LCD_BKLT_EN B28
LCD0_BKLT_PWM B27
LCD1_BKLT_PWM A24
DSI0_CLK+ G33
DSI0_CLK- G34
DSI0_D0+ F34
DSI0_D0- F35
DSI0_D1+ H32
DSI0_D1- H33
DSI1_CLK+ D33
DSI1_CLK- D34
DSI1_D0+ C34
DSI1_D0- C35
DSI1_D1+ E32
DSI1_D1- E33
DSI2_CLK+ G30
DSI2_CLK- G31
DSI2_D0+ F31
DSI2_D0- F32
DSI2_D1+ H29
DSI2_D1- H30
DSI3_CLK+ D30
DSI3_CLK- D31
DSI3_D0+ C31
DSI3_D0- C32
DSI3_D1+ E29
DSI3_D1- E30
DP0_AUX_CH- B34
DP0_AUX_CH+ B35
DP0_TX0- H38
DP0_TX0+ H39
DP0_TX1- F37
DP0_TX1+ F38
DP0_TX2- G36
DP0_TX2+ G37
DP0_TX3- H35
DP0_TX3+ H36
DP0_HPD B36
DP1_AUX_CH- A34 DDC_DAT
DP1_AUX_CH+ A35 DDC_CLK
DP1_TX0- E38 HDMI_TXD2-
DP1_TX0+ E39 HDMI_TXD2+
DP1_TX1- C37 HDMI_TXD1-
DP1_TX1+ C38 HDMI_TXD1+
DP1_TX2- D36 HDMI_TXD0-
DP1_TX2+ D37 HDMI_TXD0+
DP1_TX3- E35 HDMI_TXC-
DP1_TX3+ E36 HDMI_TXC+
DP1_HPD A33 HPD
HDMI_CEC B33 CEC
C25 100n
C29 100n
C26 100n
C30 100n
C27 100n
C31 100n
C28 100n
C32 100n
R12 499
R13 499
R14 499
R15 499
R16 499
R17 499
R18 499
R19 499
FB3 600
FB4 600
FB5 600
FB6 600
FB7 600
FB8 600
FB9 600
FB10 600
+3V3
R11
10k
HDMI_PULLDOWNS
Q1
Q_NMOS_GSD
TODO: connect to some i/o?
+1V8
+5V
U8
IP4786CZ32
VCC5V0 11
VCCSYS 27
TMDS_D2-_SYS
TMDS_D2+_SYS
TMDS_D1-_SYS
TMDS_D1+_SYS
TMDS_D0-_SYS
TMDS_D0+_SYS
TMDS_CK-_SYS
TMDS_CK+_SYS
CEC_STBY 28
CEC_SYS 29
DDC_CLK_SYS 9
DDC_DAT_SYS 10
HOTPLUG_DET_SYS 32
ESD_BYPASS 26
NC 30
NC 31
PAD 33
TMDS_SYS_D2- 2
TMDS_SYS_D2+ 1
TMDS_SYS_D1- 4
TMDS_SYS_D1+ 3
TMDS_SYS_D0- 6
TMDS_SYS_D0+ 5
TMDS_SYS_CK- 8
TMDS_SYS_CK+ 7
HDMI_5V0_CON 13
TMDS_D2-_CON
TMDS_D2+_CON
TMDS_D1-_CON
TMDS_D1+_CON
TMDS_D0-_CON
TMDS_D0+_CON
TMDS_CK-_CON
TMDS_CK+_CON
CEC_CON
DDC_CLK_CON
DDC_DAT_CON
HOTPLUG_DET_CON
UTILITY_CON
C43
1u
C42
100n
J6
HDMI_TYPE_A
5V 18
SHLD 20
TMDS_D2- 23 TMDS_CON_D2- 3
TMDS_D2+ 24 TMDS_CON_D2+ 1
TMDS_D1- 21 TMDS_CON_D1- 6
TMDS_D1+ 22 TMDS_CON_D1+ 4
TMDS_D0- 19 TMDS_CON_D0- 9
TMDS_D0+ 20 TMDS_CON_D0+ 7
TMDS_CK- 17 TMDS_CON_CK- 12
TMDS_CK+ 18 TMDS_CON_CK+ 10
CEC 25 CEC_CON 13
DDC_CLK 15 DDC_CLK_CON 15
DDC_DAT 14 DDC_DAT_CON 16
HPD 12 HPDET_CON 19
UTILITY 16 UTILTY_CON 14
GND 2
GND 5
GND 8
GND 11
GND 17
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Rev:
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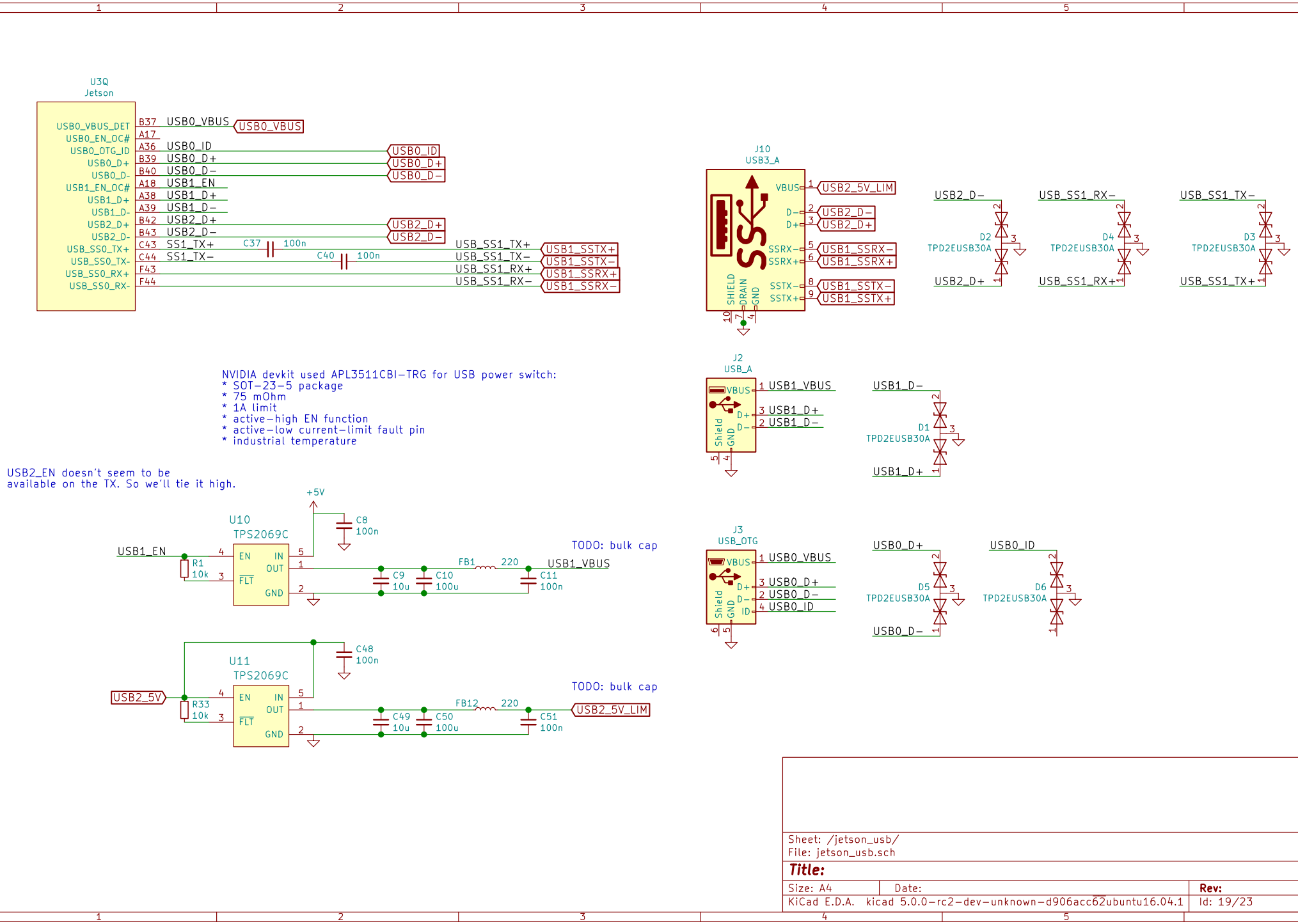
Id: 18/23


U3Q
Jetson
USB0_VBUS_DET
USB0_EN_OC#
USB0_OTG_ID
USB0_D+
USB0_D-
USB1_EN_OC#
USB1_D+
USB1_D-
USB2_D+
USB2_D-
USB_SS0_TX+
USB_SS0_TX-
USB_SS0_RX+
USB_SS0_RX-
B37 USB0_VBUS
A17
A36 USB0_ID
B39 USB0_D+
B40 USB0_D−
A18 USB1_EN
A38 USB1_D+
A39 USB1_D−
B42 USB2_D+
B43 USB2_D−
C43 SS1_TX+
C44 SS1_TX−
F43
F44
C37 100n
C40 100n
USB_SS1_TX+
USB_SS1_TX−
USB_SS1_RX+
USB_SS1_RX−
USB0_VBUS
USB0_ID
USB0_D+
USB0_D−
USB2_D+
USB2_D−
USB1_SSTX+
USB1_SSTX−
USB1_SSRX+
USB1_SSRX−
J10
USB3_A
VBUS
D−
D+
SSRX−
SSRX+
SSTX−
SSTX+
SHIELD
DRAIN
GND
USB2_5V_LIM
USB2_D−
USB2_D+
USB1_SSRX−
USB1_SSRX+
USB1_SSTX−
USB1_SSTX+
D2
TPD2EUSB30A
D4
TPD2EUSB30A
D3
TPD2EUSB30A
USB2_D−
USB2_D+
USB_SS1_RX−
USB_SS1_RX+
USB_SS1_TX−
USB_SS1_TX+
NVIDIA devkit used APL3511CBI−TRG for USB power switch:
* SOT−23−5 package
* 75 mOhm
* 1A limit
* active−high EN function
* active−low current−limit fault pin
* industrial temperature
J2
USB_A
VBUS
D+
D−
Shield
GND
USB1_VBUS
USB1_D+
USB1_D−
D1
TPD2EUSB30A
USB1_D−
USB1_D+
USB2_EN doesn't seem to be
available on the TX. So we'll tie it high.
+5V
U10
TPS2069C
EN
IN
OUT
FLT
GND
USB1_EN
R1
10k
C8
100n
C9
10u
C10
100u
FB1
220
C11
100n
USB1_VBUS
TODO: bulk cap
J3
USB_OTG
VBUS
D+
D−
ID
Shield
GND
USB0_VBUS
USB0_D+
USB0_D−
USB0_ID
USB0_D+
USB0_ID
D5
TPD2EUSB30A
D6
TPD2EUSB30A
USB0_D−
U11
TPS2069C
USB2_5V
R33
10k
C48
100n
C49
10u
C50
100u
FB12
220
C51
100n
USB2_5V_LIM
TODO: bulk cap
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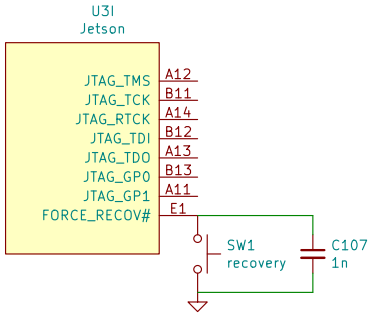
Rev:
KiCad E.D.A. kicad 5.0.0−rc2−dev−unknown−d906acc62ubuntu16.04.1
Id: 19/23



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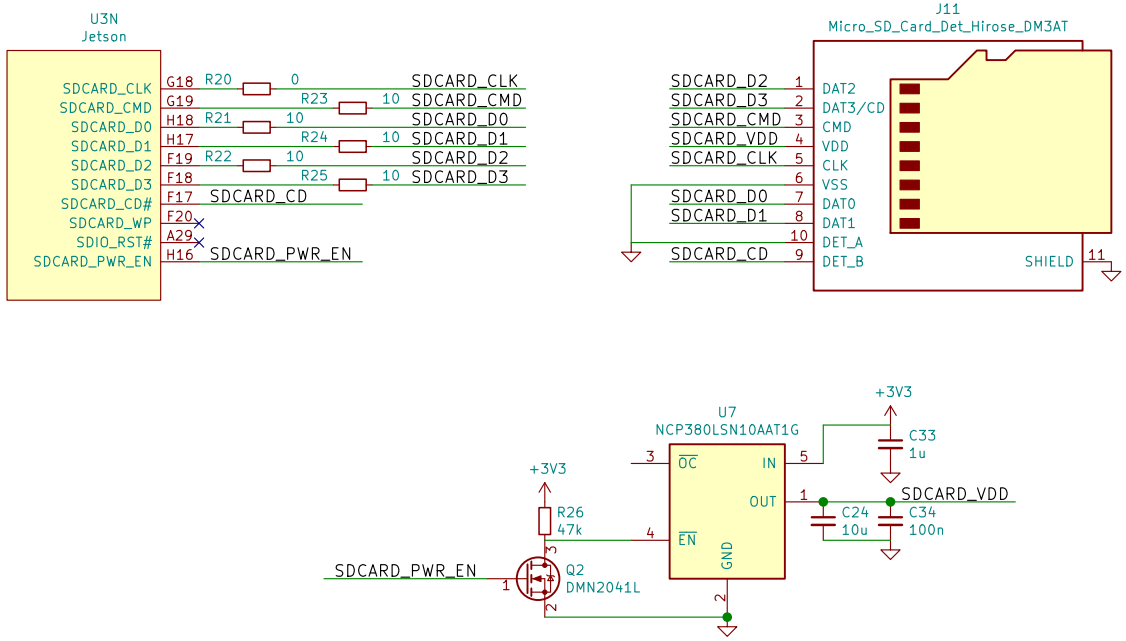

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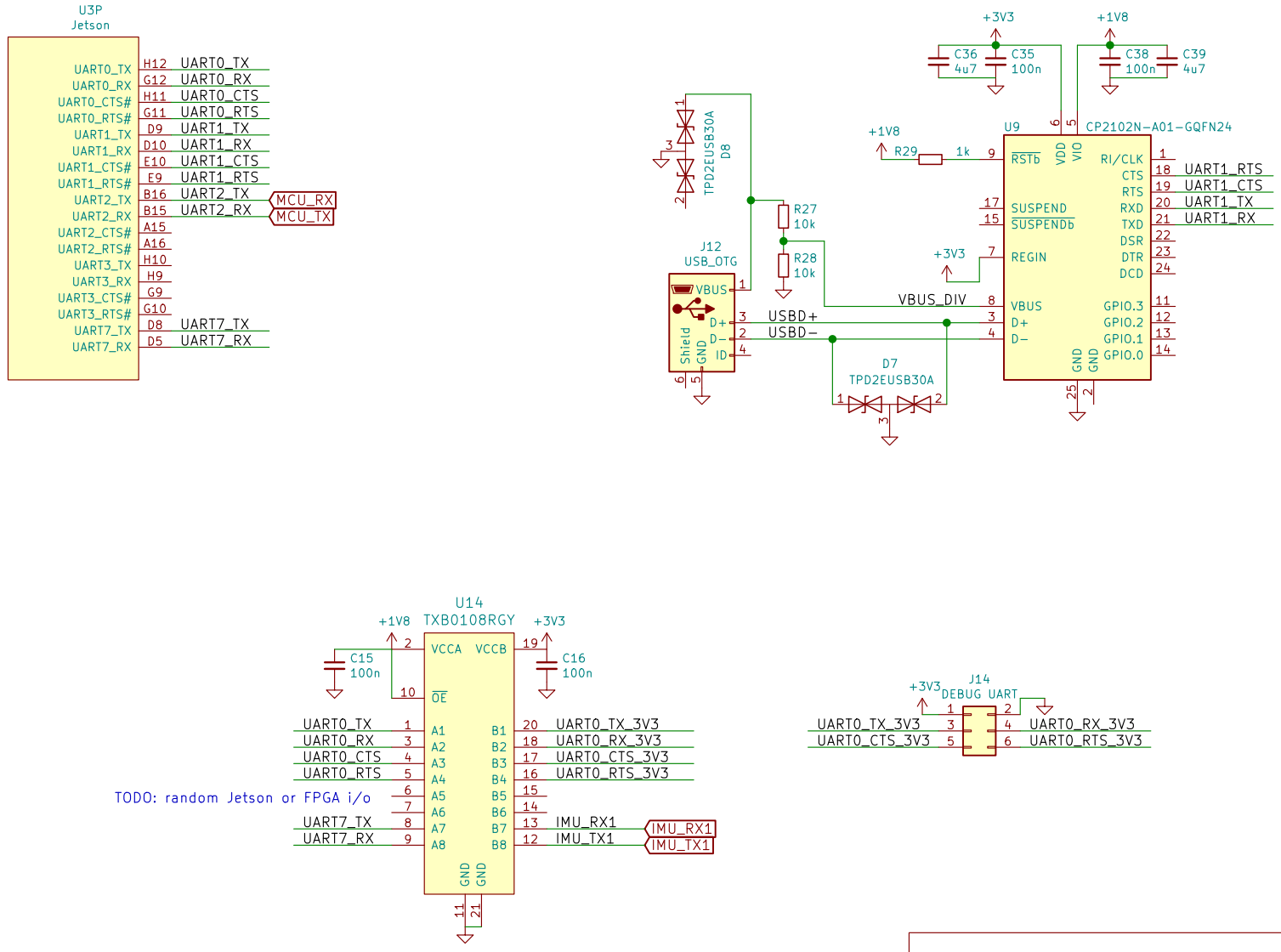

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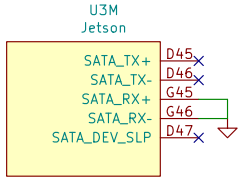

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