

## 1. Description

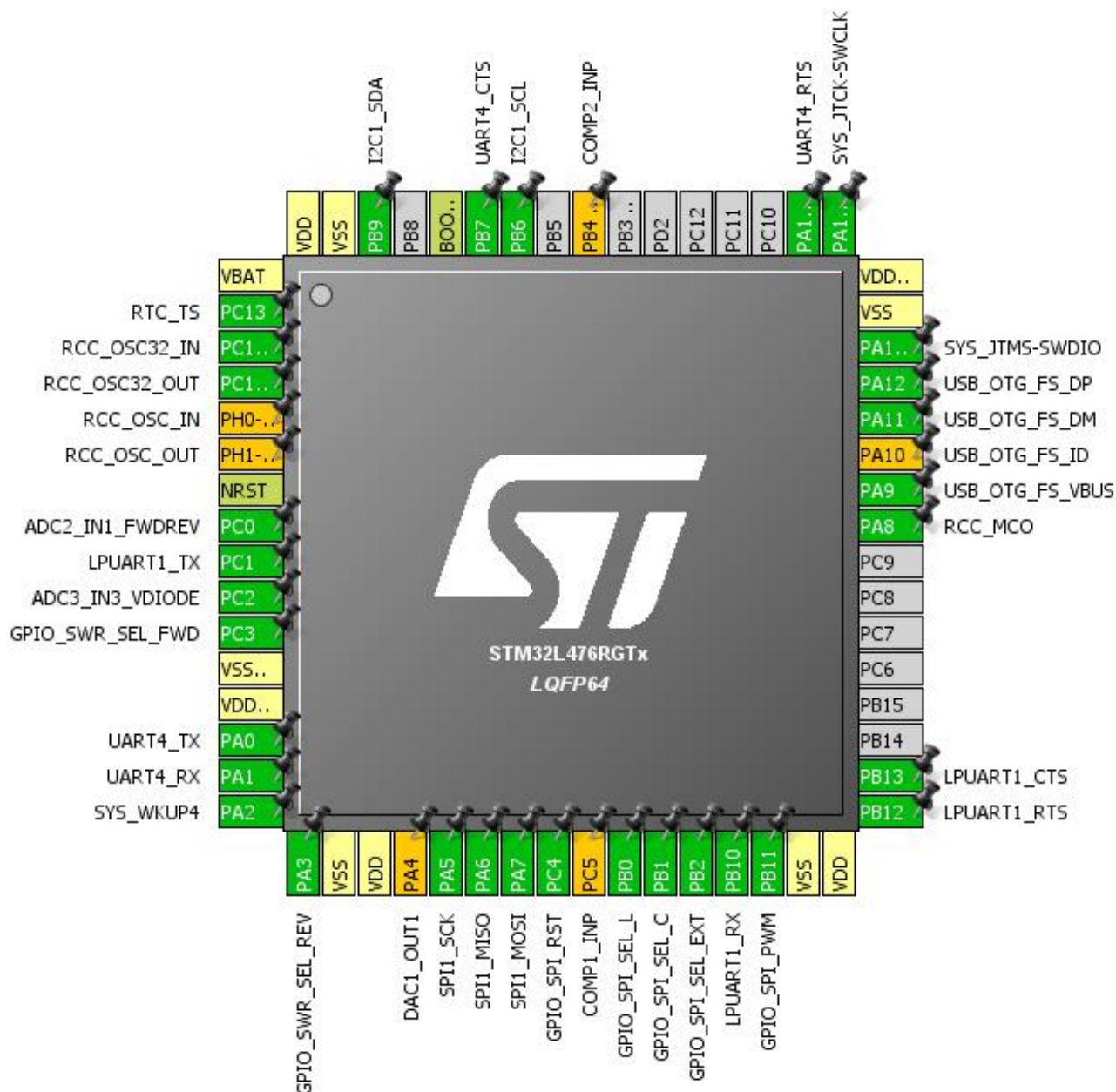
### 1.1. Project

Project Name	DL0WH_BiTuner
Board Name	custom
Generated with:	STM32CubeMX 4.27.0
Date	04/10/2019

### 1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476RGTx
MCU Package	LQFP64
MCU Pin number	64

## 2. Pinout Configuration



### 3. Pins Configuration

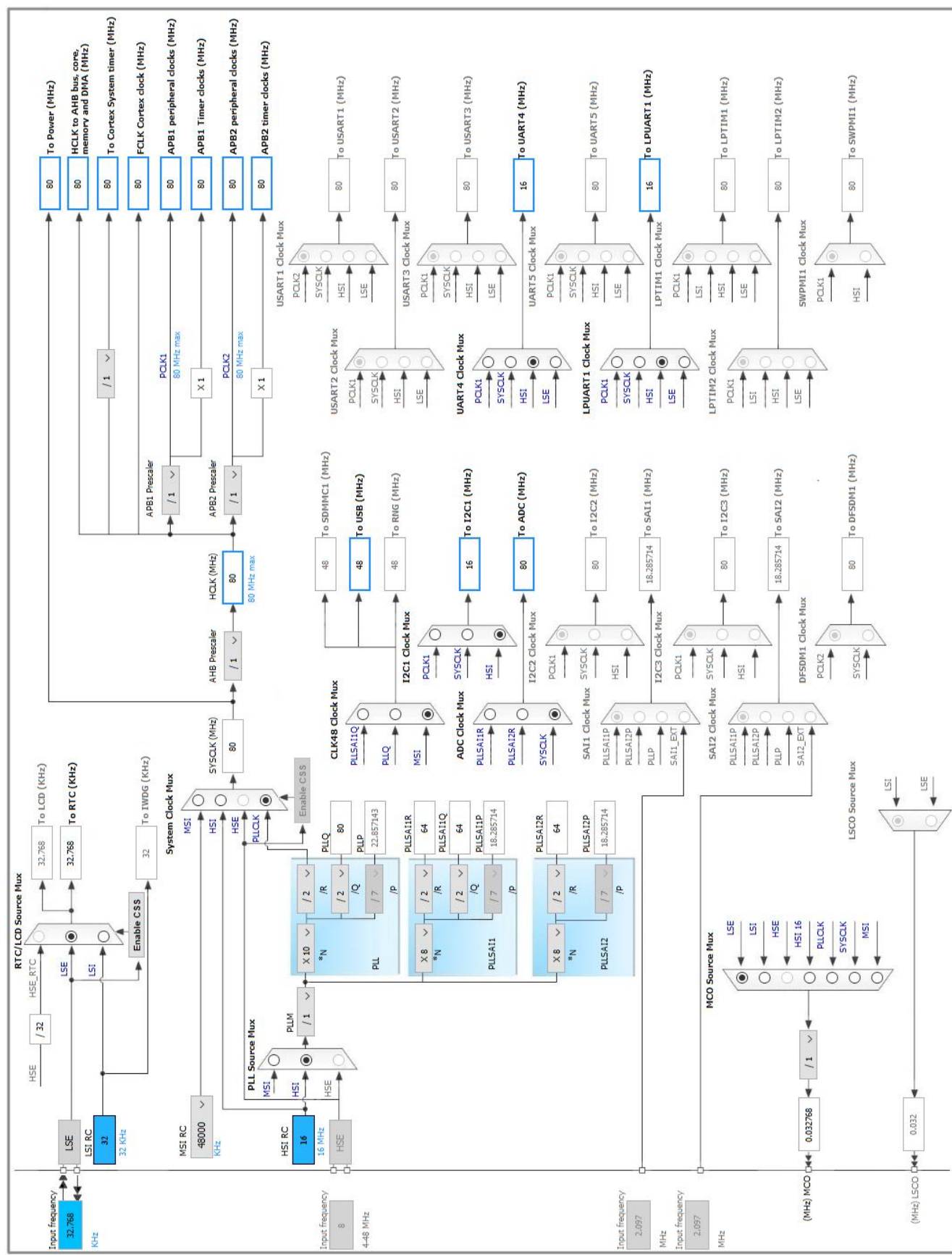
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	RTC_TS	
3	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN (PH0) *	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT (PH1) *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN1, ADC2_IN1	ADC2_IN1_FWDREV
9	PC1	I/O	LPUART1_TX	
10	PC2	I/O	ADC2_IN3, ADC3_IN3	ADC3_IN3_VDIODE
11	PC3 **	I/O	GPIO_Output	GPIO_SWR_SEL_FWD
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0	I/O	UART4_TX	
15	PA1	I/O	UART4_RX	
16	PA2	I/O	SYS_WKUP4	
17	PA3 **	I/O	GPIO_Output	GPIO_SWR_SEL_REV
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	DAC1_OUT1	
21	PA5	I/O	SPI1_SCK	
22	PA6	I/O	SPI1_MISO	
23	PA7	I/O	SPI1_MOSI	
24	PC4 **	I/O	GPIO_Output	GPIO_SPI_RST
25	PC5 *	I/O	COMP1_INP	
26	PB0 **	I/O	GPIO_Output	GPIO_SPI_SEL_L
27	PB1 **	I/O	GPIO_Output	GPIO_SPI_SEL_C
28	PB2 **	I/O	GPIO_Output	GPIO_SPI_SEL_EXT
29	PB10	I/O	LPUART1_RX	
30	PB11 **	I/O	GPIO_Output	GPIO_SPI_PWM
31	VSS	Power		
32	VDD	Power		
33	PB12	I/O	LPUART1_RTS	
34	PB13	I/O	LPUART1_CTS	
41	PA8	I/O	RCC_MCO	
42	PA9	I/O	USB_OTG_FS_VBUS	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
43	PA10 *	I/O	USB_OTG_FS_ID	
44	PA11	I/O	USB_OTG_FS_DM	
45	PA12	I/O	USB_OTG_FS_DP	
46	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDDUSB	Power		
49	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	
50	PA15 (JTDI)	I/O	UART4_RTS	
56	PB4 (NJTRST) *	I/O	COMP2_INP	
58	PB6	I/O	I2C1_SCL	
59	PB7	I/O	UART4_CTS	
60	BOOT0	Boot		
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

\*\* The pin is affected with an I/O function

\* The pin is affected with a peripheral function but no peripheral mode is activated

## 4. Clock Tree Configuration



## 5. IPs and Middleware Configuration

### 5.1. ADC1

**mode: Temperature Sensor Channel**

**mode: Vbat Channel**

**mode: Vrefint Channel**

#### 5.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour **Overrun data overwritten \***

Low Power Auto Wait Disabled

##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling **Enable \***

Oversampling Right Shift No bit shift for oversampling

Oversampling Ratio **Oversampling ratio 16x \***

Regular Oversampling Mode Oversampling Continued Mode

Triggered Regular Oversampling Single trigger for all oversampled conversions

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel **Channel Vrefint \***

Sampling Time **47.5 Cycles \***

Offset Number No offset

##### ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

##### Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

##### Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

#### Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

## 5.2. ADC2

### IN1: IN1 Single-ended

#### 5.2.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling **Enable \***

Oversampling Right Shift **4 bit shift for oversampling \***

Oversampling Ratio **Oversampling ratio 256x \***

Regular Oversampling Mode Oversampling Continued Mode

Triggered Regular Oversampling Single trigger for all oversampled conversions

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 1

Sampling Time **12.5 Cycles \***

Offset Number No offset

##### ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

#### Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

#### Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

#### Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

### 5.3. ADC3

#### IN3: IN3 Single-ended

##### 5.3.1. Parameter Settings:

#### ADC\_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	<b>Overrun data overwritten *</b>
Low Power Auto Wait	Disabled

#### ADC\_Regular\_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	<b>Enable *</b>
Oversampling Right Shift	No bit shift for oversampling
Oversampling Ratio	<b>Oversampling ratio 16x *</b>
Regular Oversampling Mode	Oversampling Continued Mode
Triggered Regular Oversampling	Single trigger for all oversampled conversions
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 3
Sampling Time	<b>47.5 Cycles *</b>
Offset Number	No offset

#### ADC\_Injected\_ConversionMode:

Enable Injected Conversions	Disable
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#### Analog Watchdog 1:

Enable Analog WatchDog1 Mode false



#### Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

#### Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

## 5.4. I2C1

### I2C: I2C

#### 5.4.1. Parameter Settings:

##### Timing configuration:

I2C Speed Mode	<b>Fast Mode *</b>
I2C Speed Frequency (KHz)	400
Rise Time (ns)	<b>50 *</b>
Fall Time (ns)	<b>20 *</b>
Coefficient of Digital Filter	<b>3 *</b>
Analog Filter	Enabled
Timing	<b>0x00200316 *</b>

##### Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

## 5.5. LPUART1

### Mode: Asynchronous

### Hardware Flow Control (RS232): CTS/RTS

#### 5.5.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	<b>9600 *</b>
Word Length	<b>8 Bits (including Parity) *</b>
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable

**Advanced Features:**

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 5.6. RCC

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator  
mode: Master Clock Output**

### 5.6.1. Parameter Settings:

**System Parameters:**

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	<b>Enabled *</b>
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

**RCC Parameters:**

HSI Calibration Value	0x10
MSI Calibration Value	<b>0xfe *</b>
MSI Auto Calibration	Enabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
LSE Drive Capability	<b>LSE oscillator medium low drive capability *</b>

**Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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## 5.7. RTC

**mode: Activate Clock Source**

**mode: Activate Calendar**

**Alarm A: Internal Alarm A**  
**WakeUp: Internal WakeUp**  
**mode: Timestamp**  
**5.7.1. Parameter Settings:**

**General:**

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

**Calendar Time:**

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

**Calendar Date:**

Week Day	Monday
Month	<b>February *</b>
Date	<b>4 *</b>
Year	<b>19 *</b>

**Alarm A:**

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

**Wake UP:**

Wake Up Clock	RTCCLK / 16
Wake Up Counter	0

**Time Stamp:**

Time Stamp Pin Edge	Time Stamp occurs on the Rising edge
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## 5.8. SPI1

**Mode: Full-Duplex Master**

### 5.8.1. Parameter Settings:

#### Basic Parameters:

Frame Format	Motorola
Data Size	<b>8 Bits *</b>
First Bit	MSB First

#### Clock Parameters:

Prescaler (for Baud Rate)	<b>16 *</b>
Baud Rate	<b>5.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	<b>2 Edge *</b>

#### Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

## 5.9. SYS

**Debug: Serial Wire**

**mode: System Wake-Up 4**

**Power Voltage Detector In: Power Voltage Detector In (Internal analog voltage)**

**Timebase Source: TIM2**

### 5.9.1. Parameter Settings:

#### Programmable\_Voltage\_Detector\_Settings:

PVD detection Level	<b>PWR PVD LEVEL 3 (2.5 V) *</b>
PWR PVD Mode	basic mode is used

## 5.10. TIM5

**mode: Clock Source**

### 5.10.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	<b>79999999 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	<b>Enable *</b>

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

## 5.11. UART4

**Mode: Asynchronous**

**Hardware Flow Control (RS232): CTS/RTS**

### 5.11.1. Parameter Settings:

#### Basic Parameters:

Baud Rate	<b>9600 *</b>
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

#### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 5.12. USB\_OTG\_FS

**Mode: Device\_Only**

**Activate\_VBUS: VBUS sensing**

### 5.12.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	<b>Enabled *</b>
Low power	Disabled
Battery charging	<b>Disabled *</b>
Link Power Management	<b>Enabled *</b>
VBUS sensing	Enabled
Signal start of frame	Disabled

## 5.13. FREERTOS

mode: **Enabled**

### 5.13.1. Config parameters:

#### Versions:

FreeRTOS version	10.0.1
CMSIS-RTOS version	1.02

#### Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	<b>256 *</b>
MAX_TASK_NAME_LEN	<b>32 *</b>
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	<b>Enabled *</b>
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	<b>Enabled *</b>
ENABLE_BACKWARD_COMPATIBILITY	<b>Disabled *</b>
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	<b>Enabled *</b>

#### Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	<b>32768 *</b>
Memory Management scheme	heap_4

#### Hook function related definitions:

USE_IDLE_HOOK	<b>Enabled *</b>
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	<b>Enabled *</b>
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	<b>Option1 *</b>

#### Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	<b>Enabled *</b>
USE_TRACE_FACILITY	<b>Enabled *</b>
USE_STATS_FORMATTING_FUNCTIONS	<b>Enabled *</b>

#### Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

#### Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	512

#### Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

### 5.13.2. Include parameters:

#### Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	<b>Enabled *</b>
vTaskSuspend	Enabled
vTaskDelayUntil	<b>Enabled *</b>
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	<b>Enabled *</b>
xSemaphoreGetMutexHolder	<b>Enabled *</b>

pcTaskGetTaskName	Enabled *
uxTaskGetStackHighWaterMark	Enabled *
xTaskGetCurrentTaskHandle	Enabled *
eTaskGetState	Enabled *
xEventGroupSetBitFromISR	Enabled *
xTimerPendFunctionCall	Enabled *
xTaskAbortDelay	Enabled *
xTaskGetHandle	Enabled *

## 5.14. USB\_DEVICE

### Class For FS IP: Communication Device Class (Virtual Port Com)

#### 5.14.1. Parameter Settings:

##### Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	<b>1: Only User messages are shown *</b>
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

##### Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

#### 5.14.2. Device Descriptor:

##### Device Descriptor:

VID (Vendor Identifier)	0x0483
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

##### Device Descriptor FS:

PID (Product Identifier)	0x5740
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
SERIALNUMBER_STRING (Serial number)	00000000001A
CONFIGURATION_STRING (Configuration Identifier)	CDC Config



INTERFACE\_STRING (Interface Identifier)

CDC Interface

**\* User modified value**

## 6. System Configuration

### 6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN1	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ADC2_IN1_FWDREV
ADC2	PC0	ADC2_IN1	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ADC2_IN1_FWDREV
	PC2	ADC2_IN3	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ADC3_IN3_VDIODE
ADC3	PC2	ADC3_IN3	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ADC3_IN3_VDIODE
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	Very High *	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	Very High *	
LPUART1	PC1	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Medium *	
	PB10	LPUART1_RX	Alternate Function Push Pull	Pull-up *	Medium *	
	PB12	LPUART1_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Medium *	
	PB13	LPUART1_CTS	Alternate Function Push Pull	Pull-up *	Medium *	
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PA8	RCC_MCO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RTC	PC13	RTC_TS	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA6	SPI1_MISO	Alternate Function Push Pull	Pull-down *	Very High *	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA2	SYS_WKUP4	n/a	n/a	n/a	
	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
UART4	PA0	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Medium *	
	PA1	UART4_RX	Alternate Function Push Pull	Pull-up *	Medium *	
	PA15 (JTDI)	UART4_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Medium *	
	PB7	UART4_CTS	Alternate Function Push Pull	Pull-up *	Medium *	
USB_OTG_FS	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
Single Mapped Signals	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PC5	COMP1_INP	Analog mode	No pull-up and no pull-down	n/a	
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB4 (NJTRST)	COMP2_INP	Analog mode	No pull-up and no pull-down	n/a	
GPIO	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_SWR_SEL_FWD
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_SWR_SEL_REV
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_SPI_RST
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High *	GPIO_SPI_SEL_L
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High *	GPIO_SPI_SEL_C
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High *	GPIO_SPI_SEL_EXT
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_SPI_PWM

## 6.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_TX	DMA1_Channel3	Memory To Peripheral	Low
SPI1_RX	DMA1_Channel2	Peripheral To Memory	Low
I2C1_RX	DMA1_Channel7	Peripheral To Memory	Low
I2C1_TX	DMA1_Channel6	Memory To Peripheral	Low
LPUART_RX	DMA2_Channel7	Peripheral To Memory	Low
LPUART_TX	DMA2_Channel6	Memory To Peripheral	Low
UART4_RX	DMA2_Channel5	Peripheral To Memory	Low
UART4_TX	DMA2_Channel3	Memory To Peripheral	Low
ADC2	DMA2_Channel4	Peripheral To Memory	Low
ADC1	DMA1_Channel1	Peripheral To Memory	Low

### SPI1\_TX: DMA1\_Channel3 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### SPI1\_RX: DMA1\_Channel2 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### I2C1\_RX: DMA1\_Channel7 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

I2C1\_TX: DMA1\_Channel6 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

LPUART\_RX: DMA2\_Channel7 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

LPUART\_TX: DMA2\_Channel6 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

UART4\_RX: DMA2\_Channel5 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

UART4\_TX: DMA2\_Channel3 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

*ADC2: DMA2\_Channel4 DMA request Settings:*

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Half Word  
Memory Data Width: Half Word

*ADC1: DMA1\_Channel1 DMA request Settings:*

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Half Word  
Memory Data Width: Half Word

### 6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
RTC wake-up interrupt through EXTI line 20	true	5	0
DMA1 channel1 global interrupt	true	5	0
DMA1 channel2 global interrupt	true	5	0
DMA1 channel3 global interrupt	true	5	0
DMA1 channel6 global interrupt	true	5	0
DMA1 channel7 global interrupt	true	5	0
ADC1 and ADC2 interrupts	true	5	0
TIM2 global interrupt	true	0	0
I2C1 event interrupt	true	5	0
I2C1 error interrupt	true	5	0
SPI1 global interrupt	true	5	0
RTC alarm interrupt through EXTI line 18	true	5	0
ADC3 global interrupt	true	5	0
TIM5 global interrupt	true	5	0
UART4 global interrupt	true	5	0
DMA2 channel3 global interrupt	true	5	0
DMA2 channel4 global interrupt	true	5	0
DMA2 channel5 global interrupt	true	5	0
USB OTG FS global interrupt	true	5	0
DMA2 channel6 global interrupt	true	5	0
DMA2 channel7 global interrupt	true	5	0
LPUART1 global interrupt	true	5	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
RTC tamper and time stamp, CSS on LSE interrupts through EXTI line 19	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FPU global interrupt	unused		

**\* User modified value**



## 7. Power Consumption Calculator report

### 7.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476RGTx
Datasheet	025976_Rev4

### 7.2. Parameter Selection

Temperature	25
Vdd	3.6

### 7.3. Sequence

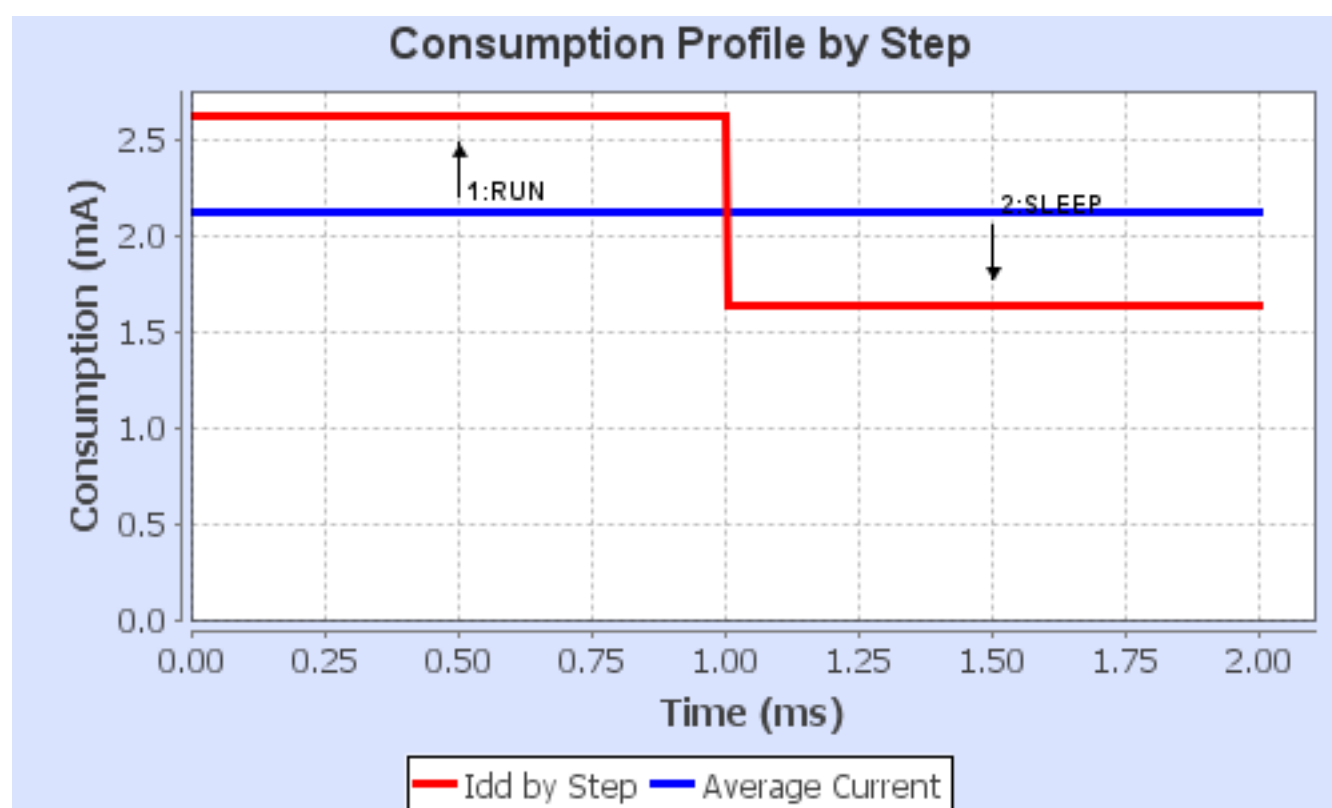
<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	SLEEP
<b>Vdd</b>	3.6	3.6
<b>Voltage Source</b>	Battery	Vbus
<b>Range</b>	Range2-Medium	Range2-Medium
<b>Fetch Type</b>	FLASH/ART/Cache	ON
<b>Clock Configuration</b>	HSE	HSE
<b>Clock Source Frequency</b>	16 MHz	16 MHz
<b>CPU Frequency</b>	16 MHz	16 MHz
<b>Peripherals</b>	ADC1:fs_10_ksp ADC2:fs_10_ksp ADC3:fs_10_ksp AHB_APB1_Bridge AHB_APB2_Bridge CRC DAC1:OUT1-Buffer_OFF- Middle_code GPIOA GPIOB GPIOC GPIOD GPIOH I2C1 LPTIM1 PVD/BOR RNG RTC SPI1 TIM5 UART4 USB_OTG_FS	ADC1:fs_10_ksp ADC2:fs_10_ksp ADC3:fs_10_ksp AHB_APB1_Bridge AHB_APB2_Bridge Bus- Matrix CRC FLASH FW GPIOA GPIOB GPIOC GPIOD GPIOH I2C1 IWDG LPUART1 PVD/BOR PWR RNG RTC SPI1 SRAM1 SRAM2 TIM2 TIM5 UART4 USB OTG FS
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	2.62 mA	1.63 mA

<b>Duration</b>	1 ms	1 ms
<b>DMIPS</b>	0.0	0.0
<b>Ta Max</b>	104.58	104.74
<b>Category</b>	In DS Table	In DS Table

#### 7.4. RESULTS

Sequence Time	2 ms	Average Current	2.12 mA
Battery Life	0	Average DMIPS	20.0 DMIPS

#### 7.5. Chart



## 8. Software Project

### 8.1. Project Settings

Name	Value
Project Name	DL0WH_BiTuner
Project Folder	C:\Users\lespero\git\DL0WH_BiTuner\SW\DL0WH_BiTuner
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_L4 V1.13.0

### 8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

## ***9. Software Pack Report***