33.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 33-1. Port A - alternate functions.

PORT A	PIN #	INTERRUPT	ADCA POS/ GAINPOS	ADCB POS	ADCA NEG	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REFA
GND	60									
AVCC	61									
PA0	62	SYNC	ADC0	ADC8	ADC0		AC0	AC0		AREF
PA1	63	SYNC	ADC1	ADC9	ADC1		AC1	AC1		
PA2	64	SYNC/ASYNC	ADC2	ADC10	ADC2		AC2			
PA3	1	SYNC	ADC3	ADC11	ADC3		AC3	AC3		
PA4	2	SYNC	ADC4	ADC12		ADC4	AC4			
PA5	3	SYNC	ADC5	ADC13		ADC5	AC5	AC5		
PA6	4	SYNC	ADC6	ADC14		ADC6	AC6		AC1OUT	
PA7	5	SYNC	ADC7	ADC15		ADC7		AC7	AC0OUT	

Table 33-2. Port B - alternate functions.

PORT B	PIN #	INTERRUPT	ADCA POS	ADCB POS/ GAINPOS	ADCB NEG	ADCB GAINNEG	ACB POS	ACB NEG	ACB OUT	DACB	REFB	JTAG
PB0	6	SYNC	ADC8	ADC0	ADC0		AC0	AC0			AREF	
PB1	7	SYNC	ADC9	ADC1	ADC1		AC1	AC1				
PB2	8	SYNC/ASYNC	ADC10	ADC2	ADC2		AC2			DAC0		
PB3	9	SYNC	ADC11	ADC3	ADC3		AC3	AC3		DAC1		
PB4	10	SYNC	ADC12	ADC4		ADC4	AC4					TMS
PB5	11	SYNC	ADC13	ADC5		ADC5	AC5	AC5				TDI
PB6	12	SYNC	ADC14	ADC6		ADC6	AC6		AC1OUT			TCK
PB7	13	SYNC	ADC15	ADC7		ADC7		AC7	AC0OUT			TDO
GND	14											
VCC	15											

Table 33-3. Port C - alternate functions.

PORT C	PIN #	INTERRUPT	TCC0 (1)(2)	AWEXC	TCC1	USARTC0 (3)	USARTC1	SPIC (4)	TWIC	CLOCKOUT (5)	EVENTOUT (6)
PC0	16	SYNC	OC0A	$\overline{\text{OC0ALS}}$					SDA		
PC1	17	SYNC	OC0B	OC0AHS		XCK0			SCL		
PC2	18	SYNC/ASYNC	OC0C	$\overline{\text{OC0BLS}}$		RXD0					
PC3	19	SYNC	OC0D	OC0BHS		TXD0					
PC4	20	SYNC		$\overline{\text{OC0CLS}}$	OC1A			$\overline{\text{SS}}$			
PC5	21	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PC6	22	SYNC		$\overline{\text{OC0DLS}}$			RXD1	MISO		clk_{RTC}	
PC7	23	SYNC		OC0DHS			TXD1	SCK		clk_{PER}	EVOUT
GND	24										
VCC	25										

Notes:
1. Pin mapping of all TC0 can optionally be moved to high nibble of port.
2. If TC0 is configured as TC2 all eight pins can be used for PWM output.
3. Pin mapping of all USART0 can optionally be moved to high nibble of port.
4. Pins MOSI and SCK for all SPI can optionally be swapped.
5. CLKOUT can optionally be moved between port C, D and E and between pin 4 and 7.
6. EVOUT can optionally be moved between port C, D and E and between pin 4 and 7.

Table 33-4. Port D - alternate functions.

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USBD	USARTD0	USARTD1	SPID	CLOCKOUT	EVENTOUT
PD0	26	SYNC	OC0A							
PD1	27	SYNC	OC0B			XCK0				
PD2	28	SYNC/ASYNC	OC0C			RXD0				
PD3	29	SYNC	OC0D			TXD0				
PD4	30	SYNC		OC1A				$\overline{\text{SS}}$		
PD5	31	SYNC		OC1B			XCK1	MOSI		
PD6	32	SYNC			D-		RXD1	MISO		
PD7	33	SYNC			D+		TXD1	SCK	clk_{PER}	EVOUT
GND	34									
VCC	35									

Table 33-5. Port E - alternate functions.

PORT E	PIN #	INTERRUPT	TCE0	TCE1	USARTE0	TWIE
PE0	36	SYNC	OC0A			SDA
PE1	37	SYNC	OC0B		XCK0	SCL
PE2	38	SYNC/ASYNC	OC0C		RXD0	
PE3	39	SYNC	OC0D		TXD0	
PE4	40	SYNC		OC1A		
PE5	41	SYNC		OC1B		
TOSC2	42					
TOSC1	43					
GND	44					
VCC	45					

Table 33-6. Port F - alternate functions.

PORT F	PIN #	INTERRUPT	TCF0	USARTF0
PF0	46	SYNC	OC0A	
PF1	47	SYNC	OC0B	XCK0
PF2	48	SYNC/ASYNC	OC0C	RXD0
PF3	49	SYNC	OC0D	TXD0
PF4	50	SYNC		
VBAT	51			
GND	52	SYNC		
VCC	53	SYNC		
PF6	54			
PF7	55			

Table 33-7. Port R - alternate functions.

PORT R	PIN #	INTERRUPT	PDI	XTAL
PDI	56		PDI_DATA	
$\overline{\text{RESET}}$	57		PDI_CLOCK	
PR0	58	SYNC		XTAL2
PR1	59	SYNC		XTAL1