1. Description

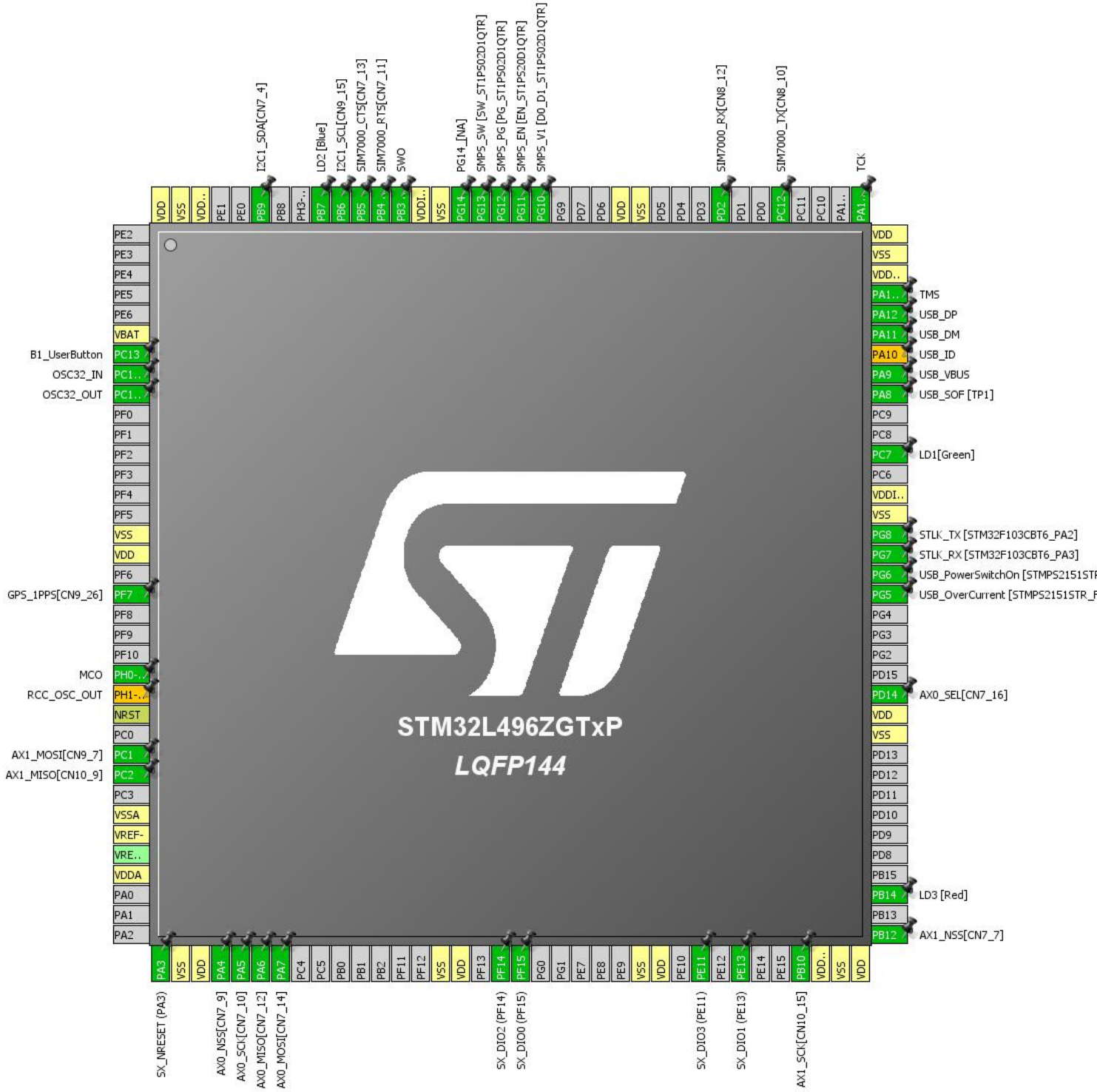
1.1. Project

Project Name	FindMeSAT_V2
Board Name	NUCLEO-L496ZG-P
Generated with:	STM32CubeMX 4.25.0
Date	05/07/2018

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L496ZGTxP
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	B1_UserButton
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	OSC32_IN
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	OSC32_OUT
16	VSS	Power		
17	VDD	Power		
19	PF7	I/O	TIM5_CH2	GPS_1PPS[CN9_26]
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	MCO
24	PH1-OSC_OUT (PH1) *	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	SPI2_MOSI	AX1_MOSI[CN9_7]
28	PC2	I/O	SPI2_MISO	AX1_MISO[CN10_9]
30	VSSA	Power		
31	VREF-	Power		
33	VDDA	Power		
37	PA3 **	I/O	GPIO_Output	SX_NRESET (PA3)
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	SPI1_NSS	AX0_NSS[CN7_9]
41	PA5	I/O	SPI1_SCK	AX0_SCK[CN7_10]
42	PA6	I/O	SPI1_MISO	AX0_MISO[CN7_12]
43	PA7	I/O	SPI1_MOSI	AX0_MOSI[CN7_14]
51	VSS	Power		
52	VDD	Power		
54	PF14 **	I/O	GPIO_Input	SX_DIO2 (PF14)
55	PF15 **	I/O	GPIO_Input	SX_DIO0 (PF15)
61	VSS	Power		
62	VDD	Power		
64	PE11 **	I/O	GPIO_Input	SX_DIO3 (PE11)
66	PE13 **	I/O	GPIO_Input	SX_DIO1 (PE13)
69	PB10	I/O	SPI2_SCK	AX1_SCK[CN10_15]
70	VDD12	Power		
71	VSS	Power		
72	VDD	Power		
73	PB12	I/O	SPI2_NSS	AX1_NSS[CN7_7]
75	PB14 **	I/O	GPIO_Output	LD3 [Red]

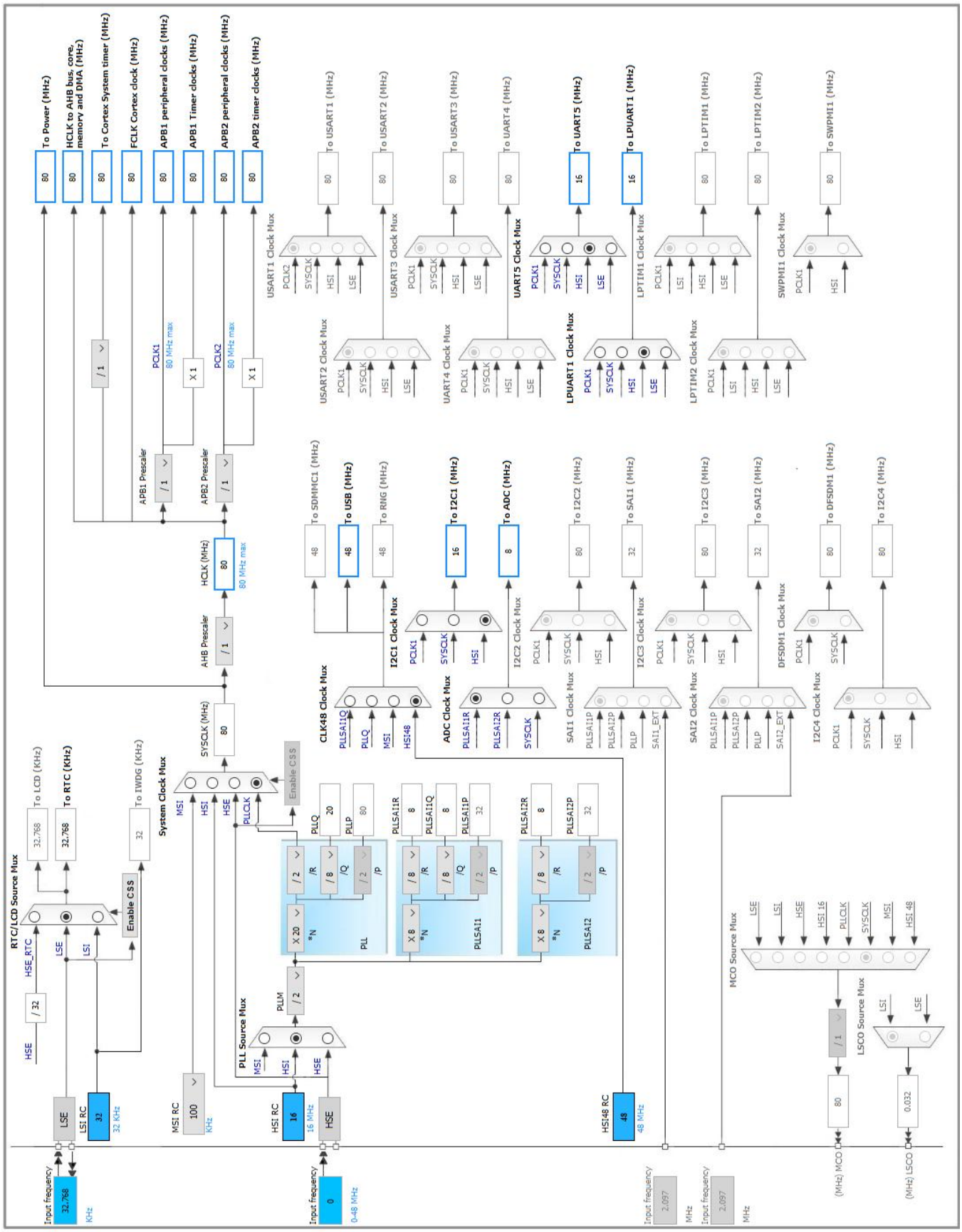
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
83	VSS	Power		
84	VDD	Power		
85	PD14 **	I/O	GPIO_Output	AX0_SEL[CN7_16]
90	PG5 **	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
91	PG6 **	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7	I/O	LPUART1_TX	STLK_RX [STM32F103CBT6_PA3]
93	PG8	I/O	LPUART1_RX	STLK_TX [STM32F103CBT6_PA2]
94	VSS	Power		
95	VDDIO2	Power		
97	PC7 **	I/O	GPIO_Output	LD1[Green]
100	PA8	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 *	I/O	USB_OTG_FS_ID	USB_ID
103	PA11	I/O	USB_OTG_FS_DM	USB_DM
104	PA12	I/O	USB_OTG_FS_DP	USB_DP
105	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
113	PC12	I/O	UART5_TX	SIM7000_TX[CN8_10]
116	PD2	I/O	UART5_RX	SIM7000_RX[CN8_12]
120	VSS	Power		
121	VDD	Power		
125	PG10 **	I/O	GPIO_Output	SMPS_V1 [D0_D1_ST1PS02D1QTR]
126	PG11 **	I/O	GPIO_Output	SMPS_EN [EN_ST1PS20D1QTR]
127	PG12 **	I/O	GPIO_Input	SMPS_PG [PG_ST1PS02D1QTR]
128	PG13 **	I/O	GPIO_Output	SMPS_SW [SW_ST1PS02D1QTR]
129	PG14 **	I/O	GPIO_Analog	PG14_[NA]
130	VSS	Power		
131	VDDIO2	Power		
132	PB3 (JTDO/TRACESWO)	I/O	SYS_JTDO-SWO	SWO
133	PB4 (NJTRST)	I/O	UART5_RTS	SIM7000_RTS[CN7_11]

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
134	PB5	I/O	UART5_CTS	SIM7000_CTS[CN7_13]
135	PB6	I/O	I2C1_SCL	I2C1_SCL[CN9_15]
136	PB7 **	I/O	GPIO_Output	LD2 [Blue]
139	PB9	I/O	I2C1_SDA	I2C1_SDA[CN7_4]
142	VDD12	Power		
143	VSS	Power		
144	VDD	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: Temperature Sensor Channel
mode: Vbat Channel
mode: Vrefint Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	**Overrun data overwritten ***
Low Power Auto Wait	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Enable Regular Oversampling	**Enable ***
Oversampling Right Shift	**4 bit shift for oversampling ***
Oversampling Ratio	**Oversampling ratio 256x ***
Regular Oversampling Mode	Oversampling Continued Mode
Triggered Regular Oversampling	Single trigger for all oversampled conversions
Number Of Conversion	**3 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel Vrefint ***
Sampling Time	**92.5 Cycles ***
Offset Number	No offset
Rank	**2 ***

Channel	**Channel Vbat ***
Sampling Time	**92.5 Cycles ***
Offset Number	No offset
Rank	**3 ***
Channel	Channel Temperature Sensor
Sampling Time	**92.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. I2C1

I2C: I2C

5.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x0010061A ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.3. LPUART1

Mode: Asynchronous

5.3.1. Parameter Settings:

Basic Parameters:

Baud Rate	209700
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable

Advanced Features:

Auto Baudrate Mode	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.4. RCC

High Speed Clock (HSE): BYPASS Clock Source
Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	64

MSI Calibration Value	0
MSI Auto Calibration	**Enabled ***
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

5.5. RTC

mode: Activate Clock Source
mode: Activate Calendar
Alarm A: Internal Alarm A
WakeUp: Internal WakeUp

5.5.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	**Binary data format ***
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	**18 ***

Alarm A:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable

Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

Wake UP:

Wake Up Clock	RTCCLK / 16
Wake Up Counter	0

5.6. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.6.1. Parameter Settings:

Basic Parameters:

Frame Format	**TI ***
Data Size	**8 Bits ***

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**40.0 MBits/s ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

5.7. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.7.1. Parameter Settings:

Basic Parameters:

Frame Format	**TI ***
Data Size	**8 Bits ***

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**40.0 MBits/s ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

5.8. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM2

5.9. TIM5

Clock Source : Internal Clock

Channel2: Input Capture direct mode

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1200000000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.10. UART5

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

5.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**19200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.11. USB_OTG_FS

Mode: Device_Only
Activate_VBUS: VBUS sensing
mode: Activate_SOF

5.11.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	**Disabled ***
Link Power Management	**Enabled ***
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Enabled
Signal start of frame	Enabled

5.12. FREERTOS

mode: Enabled

5.12.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	**Enabled ***
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	**Enabled ***
ENABLE_BACKWARD_COMPATIBILITY	**Disabled ***
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	**8192 ***
Memory Management scheme	**heap_5 ***

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	**Enabled ***
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	**Option2 ***

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	**Enabled ***
USE_TRACE_FACILITY	**Enabled ***
USE_STATS_FORMATTING_FUNCTIONS	**Enabled ***

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	**8 ***
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.12.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	**Enabled ***
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	**Enabled ***
xSemaphoreGetMutexHolder	**Enabled ***
pcTaskGetTaskName	**Enabled ***
uxTaskGetStackHighWaterMark	**Enabled ***
xTaskGetCurrentTaskHandle	**Enabled ***
eTaskGetState	**Enabled ***
xEventGroupSetBitFromISR	**Enabled ***
xTimerPendFunctionCall	**Enabled ***
xTaskAbortDelay	**Enabled ***
xTaskGetHandle	**Enabled ***

5.13. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

5.13.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	**Disabled ***
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

5.13.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	**DF4IAH Solutions ***

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	**FindMeSAT V2 ***
SERIALNUMBER_STRING (Serial number)	00000000001A
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	I2C1_SCL[CN9_15]
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	I2C1_SDA[CN7_4]
LPUART1	PG7	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_RX [STM32F103CBT6_PA3]
	PG8	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_TX [STM32F103CBT6_PA2]
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	OSC32_IN
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	OSC32_OUT
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	MCO
SPI1	PA4	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	AX0_NSS[CN7_9]
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	AX0_SCK[CN7_10]
	PA6	SPI1_MISO	Alternate Function Push Pull	**Pull-up ***	**Very High ***	AX0_MISO[CN7_12]
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	AX0_MOSI[CN7_14]
SPI2	PC1	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	AX1_MOSI[CN9_7]
	PC2	SPI2_MISO	Alternate Function Push Pull	**Pull-up ***	**Very High ***	AX1_MISO[CN10_9]
	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	AX1_SCK[CN10_15]
	PB12	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	AX1_NSS[CN7_7]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PB3 (JTDO/TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
TIM5	PF7	TIM5_CH2	Alternate Function Push Pull	**Pull-up ***	Low	GPS_1PPS[CN9_26]
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	SIM7000_TX[CN8_10]
	PD2	UART5_RX	Alternate Function Push Pull	**Pull-up ***	**Medium ***	SIM7000_RX[CN8_12]
	PB4 (NJTRST)	UART5_RTS	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	SIM7000_RTS[CN7_11]
	PB5	UART5_CTS	Alternate Function Push Pull	**Pull-up ***	**Medium ***	SIM7000_CTS[CN7_13]
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_SOF [TP1]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	USB_VBUS
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DP
Single Mapped Signals	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_ID
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B1_UserButton
	PA3	GPIO_Output	Output Push Pull	**Pull-up ***	Low	SX_NRESET (PA3)
	PF14	GPIO_Input	Input mode	**Pull-down ***	n/a	SX_DIO2 (PF14)
	PF15	GPIO_Input	Input mode	**Pull-down ***	n/a	SX_DIO0 (PF15)
	PE11	GPIO_Input	Input mode	**Pull-down ***	n/a	SX_DIO3 (PE11)
	PE13	GPIO_Input	Input mode	**Pull-down ***	n/a	SX_DIO1 (PE13)
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	AX0_SEL[CN7_16]
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	USB_OverCurrent [STMPS2151STR_FAULT]
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1[Green]
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SMPS_V1 [D0_D1_ST1PS02D1QTR]
	PG11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SMPS_EN [EN_ST1PS20D1QTR]
	PG12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SMPS_PG [PG_ST1PS02D1QTR]
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SMPS_SW [SW_ST1PS02D1QTR]
	PG14	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	PG14_[NA]
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
SPI1_TX	DMA1_Channel3	Memory To Peripheral	Low
SPI1_RX	DMA1_Channel2	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SPI1_TX: DMA1_Channel3 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI1_RX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
RTC wake-up interrupt through EXTI line 20	true	0	0
RCC global interrupt	true	5	0
DMA1 channel1 global interrupt	true	5	0
DMA1 channel2 global interrupt	true	5	0
DMA1 channel3 global interrupt	true	5	0
ADC1 and ADC2 interrupts	true	5	0
TIM2 global interrupt	true	0	0
I2C1 event interrupt	true	5	0
I2C1 error interrupt	true	5	0
SPI1 global interrupt	true	5	0
SPI2 global interrupt	true	5	0
RTC alarm interrupt through EXTI line 18	true	0	0
TIM5 global interrupt	true	5	0
UART5 global interrupt	true	5	0
USB OTG FS global interrupt	true	5	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
EXTI line[15:10] interrupts	unused		
LPUART1 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L496ZGTxP
Datasheet	029173_Rev2

7.2. Parameter Selection

Temperature	25
Vdd	3.0

7.3. SMPS Selection

SMPS	SMPS1_User
Vin	3.3 V
Vout	1.2 V
OffCurrent	250.0 nA
QCurrent	500.0 nA
Efficiency	85 %

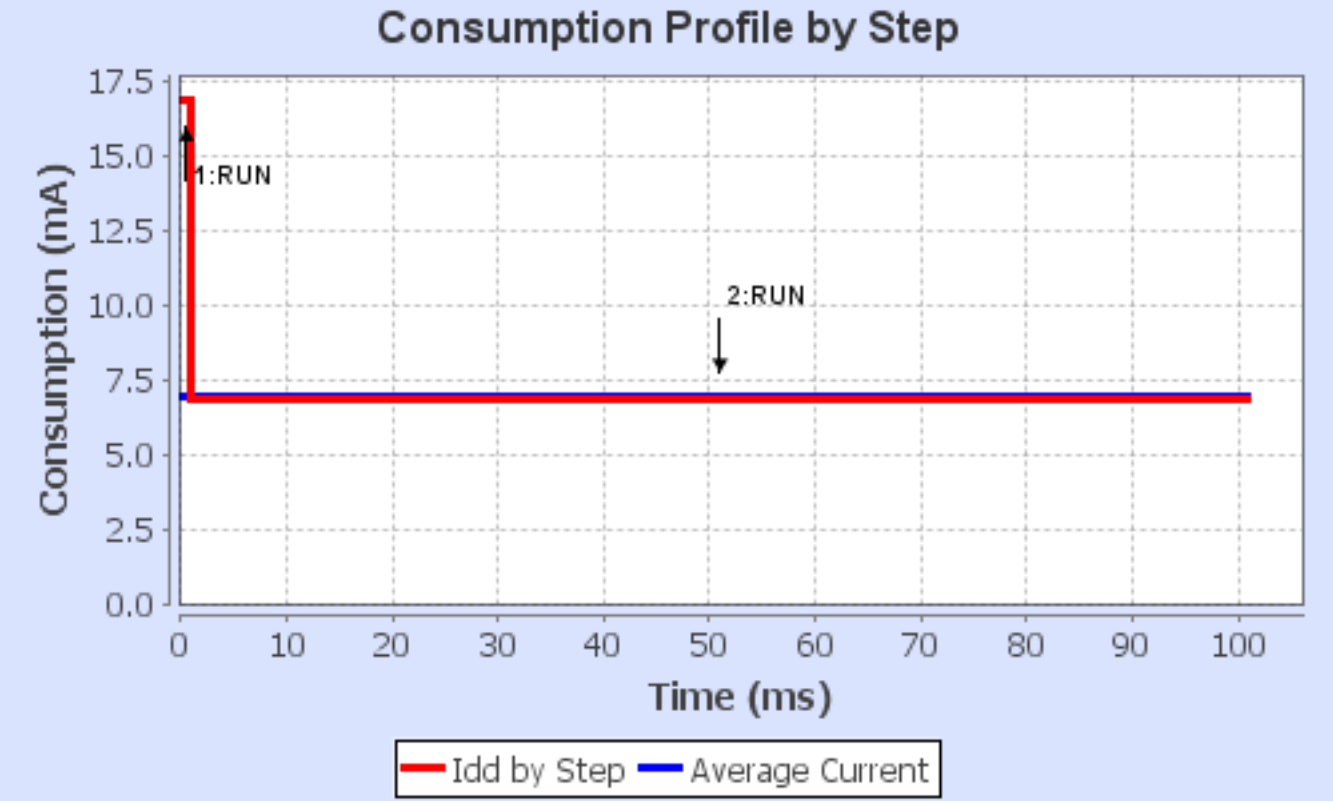
7.4. Sequence

Step	Step1	Step2
Mode	RUN	RUN
SMPS	DISCONNECTED	CONNECTED
Vdd	3.0	3.0
Voltage Source	Vbus	Vbus
Range	Range1-High	Range1-High
Fetch Type	FLASH	FLASH
Clock Configuration	HSE BYP PLL Flash-ON	HSE BYP PLL Flash-ON
Clock Source Frequency	4 MHz	4 MHz
CPU Frequency	80 MHz	80 MHz
Peripherals	GPIOA GPIOB GPIOC GPIOD GPIOE GPIOF GPIOG GPIOH I2C1 LPTIM1 LPUART1 PWR RTC SPI1 SPI2 SPI3 TIM2 TIM5 UART5 USB_OTG_FS	GPIOA GPIOB GPIOC GPIOD GPIOE GPIOF GPIOG GPIOH I2C1 LPUART1 TIM2 TIM5 UART5 USB_OTG_FS
Additional Cons.	0 mA	0 mA
Average Current	16.81 mA	6.85 mA
Duration	1 ms	100 ms
DMIPS	0.0	0.0
Ta Max	103.39	104.34
Category	In DS Table	In DS Table

7.5. RESULTS

Sequence Time	101 ms	Average Current	6.95 mA
Battery Life	0	Average DMIPS	100.0 DMIPS

7.6. Chart


Consumption Profile by Step
Consumption (mA)
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0
1:RUN
2:RUN
0
10
20
30
40
50
60
70
80
90
100
Time (ms)
Idd by Step
Average Current

8. Software Project

8.1. Project Settings

Name	Value
Project Name	FindMeSAT_V2
Project Folder	Z:\nfs_ds_nfs\git\FindMeSAT__SW\FindMeSAT_V2_SW\TrueSTUDIO
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_L4 V1.11.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

9. Software Pack Report